Received 19 May 2024; revised 3 July 2024; accepted 18 July 2024. Date of publication 25 July 2024; date of current version 15 August 2024. The review of this article was arranged by Associate Editor Min Chen.

Digital Object Identifier 10.1109/OJPEL.2024.3433605

Influence of Output Terminations on Common-Mode Conducted Emissions Evaluation of Interface Converters

CHRISTOPHER D. NEW^[D] (Member, IEEE), ANDREW N. LEMMON^[D] (Senior Member, IEEE), AND AARON D. BROVONT^[D] (Member, IEEE)

¹Department of Electrical and Computer Engineering, The University of Alabama, Tuscaloosa, AL 35487 USA ²The Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906 USA

CORRESPONDING AUTHOR: CHRISTOPHER D. NEW (e-mail: christopher.d.new@ieee.org).

This work was supported by the U.S. Office of Naval Research under Award Number N00014-18-1-2156 and was approved for public release under DCN# 43-10131-22.

ABSTRACT Current conducted emissions standards provide considerable flexibility in the handling of interface converters, which are of increasing importance for the design and implementation of microgrids. Of particular interest herein is the approach selected for terminating the output ports of such converters during conducted emissions qualification testing. This article provides a theoretical treatment of an interface converter consisting of a SiC-based single-phase inverter in a custom-built testbed for evaluating conducted emissions. The accompanying analysis demonstrates that the selection of output terminations plays a significant role in determining the resulting emissions, with a difference of up to 40 dB observed in the relevant emissions metrics. These predictions are validated with a set of empirical studies. The dependence on output termination selection is emphasized further in deployed systems, which are not influenced by the presence of compliance measurement equipment. In this configuration, the common-mode resonance of the system is shown to elevate peak emissions due to reduced damping. Overall, this paper highlights an opportunity to improve emissions standards with respect to interface converters by standardizing output terminations, particularly in view of the increased high-frequency emissions produced by systems implemented with wide band-gap technology.

INDEX TERMS EMI, EMC, wide-bandgap semiconductors, qualification, conducted emissions.

NOMENCLATURE

α	Output termination scaling factor.
C_{ag}	A-to-baseplate capacitance.
C_{bp}	Total baseplate capacitance.
C_{lg}	L-to-baseplate capacitance.
C_{li}	Inboard LISN capacitance.
C_{lo}	Outboard LISN capacitance.
C_o	Output termination capacitance.
C_{ug}	U-to-baseplate capacitance.
i_{Q1}	Q_1 switch current.
i_{Q2}	Q_2 switch current.
Lchoke	CM choke inductance.

- L_{choke} CM choke inducta L_l LISN inductance.
- L_l LISN inductance.
- L_o Output termination inductance.
- R_{sweep} Output termination resistance.

Heatsink resistance. R_h R_{li} Inboard LISN resistance. Outboard LISN resistance. R_{lo} $\begin{array}{c} v_{AN}^{\rm cm} \\ v_{bp}^{\rm cm} \end{array}$ A-to-N CM voltage source. Baseplate CM voltage source. Q_1 switch voltage. v_{Q1} Q_2 switch voltage. v_{Q2} v_{UL}^{cm} U-to-L CM voltage source. Zlisn Single LISN impedance. Z_{out}^{cm} Output termination CM impedance. Z_h Heatsink impedance.

I. INTRODUCTION

Accelerating demand for improvements in efficiency and power density in power electronic systems are driving new

© 2024 The Authors. This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 License. For more information, see

https://creativecommons.org/licenses/by-nc-nd/4.0/



implementations toward adoption of wide-bandgap (WBG) semiconductors [1], [2], [3], [4], erosion of electrical and thermal design margins, and densification of packaging solutions [5], [6], [7]. Additionally, categories of applications such as electric vehicles [8], [9], rail transportation [10], and naval vessels [11], [12] are projected to move steadily to higher dc-link voltages in the coming years. This trend is motivated in part by the reduction in ampacity requirements associated with elevated system voltages, and the corresponding size and weight reduction that accrues from the use of smaller power distribution cables. Total cable weight has a measurable impact on overall performance for high-power transportation systems, as these cables contribute to the overhead weight that must be carried about [13], [14].

Overall, these trends are increasing the challenges associated with managing electromagnetic interference (EMI) and ensuring electromagnetic compatibility (EMC) for such systems [15]. For example, the adoption of WBG semiconductors has been linked to an increase in overall emissions due to the high-frequency spectral content associated with the fastswitching transitions of these devices [16], [17]. Densification of system components likewise increases the opportunity for harmful interference, because potential victim receivers within the system are positioned closer to the sources of emissions, which reduces path loss and increases coupling [18]. Finally, the increase of system dc-link voltages and the transition to medium-voltage (MV) scale also increases the burden on EMI management components [19]. Recent studies have demonstrated a linear relationship between dc bus voltage and the conducted emissions in single-phase inverters [20]. The analysis of [20] is general in nature, and this voltage-scaling trend is believed to apply generally to hard-switched power electronic converters.

Additionally, to achieve economies of scale and reduce maintenance costs and system downtime, there is a strong drive to build complex systems from line-replaceable units (LRUs) or basic "building block" converters. The emergence of the Power Electronics Building Block (PEBB) is a prominent example of this concept [21], [22], [23], [24]. In large systems designed around this concept, many of the building blocks will be used as interface converters. Interface converters provide power conditioning for downstream systems and are not designed to directly power end-use loads. In this scenario, it is impractical to qualify the entire system (sources, converters, and loads) in its entirety, and therefore qualification will likely occur at the building-block level. This introduces some challenges with respect to emissions compliance, because today's emissions standards are generally written from the perspective of evaluating end-use equipment. The applicability of these standards to the evaluation of interface converters is not clear due to the ambiguous guidance of applying output terminations.

The contributions of this work are as follows. First, this article analyzes the ambiguity in the handling of interface converters within contemporary emissions standards. This is accomplished by applying the common-mode (CM) equivalent modeling technique reported in [25], [26], [27] to an interface converter with an unknown load. A preliminary form of this analysis was presented in [28]. This work focuses on the conducted EMI emissions, though many of the trends are expected to be similar when considering radiated emissions. Second, this article provides a systematic analysis of the influence of converter input and output terminations on measured emissions. For example, this analysis reveals that the influence of output terminations is more significant in deployed systems compared to compliance measurements under certain conditions. Third, this article identifies and demonstrates techniques to reduce emissions from a deployed interface converter by leveraging its CM equivalent model (CEM). The provided example illustrates a surprising increase in emissions due to the inclusion of a CM choke. This behavior is subsequently explained and remedied through analysis of the CEM.

The organization of this article is as follows. Section II provides a brief introduction to the treatment of interface converters within contemporary emissions standards. Section III provides a derivation of a CEM for an example interface converter with scaled output terminations. Section IV provides a simulation study to demonstrate the influence of output terminations in the context of this example. Section V presents empirical validation of the model predictions included in the previous section. Section VI compares the emissions produced during qualification measurements and field deployment. Additionally, the CEM is employed to identify targeted mitigation strategies to suppress emissions in the deployed configuration.

II. APPLICATION OF CONDUCTED EMISSIONS STANDARDS TO INTERFACE CONVERTERS

This paper evaluates the emissions of interface converters with respect to MIL-STD-461, which is required for qualification of equipment for U.S. military applications [29]. Commercial standards (e.g., CISPR 32 [30], EN 55032 [31], 47 CFR Part 15 [32], etc.) differ from MIL-STD-461 in terms of implementation details but are similar in concept and structure. Thus, while the particular requirements of MIL-STD-461 are referenced throughout this paper, the discussion, analysis, and conclusions herein largely apply to commercial standards as well.

The hardware setup prescribed by MIL-STD-461 to evaluate conducted emissions of systems under sub-part CE-102 is shown in Fig. 1. The Line Impedance Stabilization Network (LISN) components shown therein are of particular interest. All modern conducted emissions standards call for the use of LISNs (or equivalent structures) between the Equipment Under Test (EUT) and the utility power supply. LISNs provide a standard reference impedance for emissions measurements. Conducted emissions compliance in the kHz to MHz band is generally accomplished by evaluating voltage measurements from current-viewing resistors within the LISNs. These voltage measurements are compared to a limit line specified by the standard in order to determine whether the EUT passes



FIGURE 1. Evaluation setup from MIL-STD-461 [29].

compliance. The use of a standard reference impedance for these measurements is necessary to ensure that compliance standards can be consistently applied across different EUTs, and at different test facilities, and with different measurement equipment, etc.

It is important to note that Fig. 1 does not depict the EUT as offering output power terminals. In other words, the EUT in Fig. 1 is an end-use device, which directly consumes the power supplied by the input power terminals. This is the paradigm shared by most modern compliance standards. One known exception is IEC 62040-2 which is specific to uninterruptable power supplies (UPSs) and thus includes provisions for loading the system output [33]. However, these provisions focus exclusively on the differential mode (DM) load attached between the output terminals. In contrast to the treatment of the input terminals, the standard does not specify a defined reference impedance between the output terminals and the system ground plane. This load configuration does not account for common-mode (CM) current flowing through the system output, which is a significant concern for interface converters. Other than IEC 62040-2, to the best of the authors' knowledge, the hardware setup shown in Fig. 1 can be applied unambiguously only for end-use equipment. It is noted that for the evaluation of power electronic converters, this model corresponds to point-of-load (POL) converters that are physically integrated with end-use equipment. The applicability of this model to two-port, intermediate conversion devices that are not integrated with end-use equipment is not clear.

In the case of a two-port interface converter without a dedicated load, there may be no obvious or logical method to terminate the output of the EUT for a conducted emissions qualification. The EUT may not be intended for a single, specific end use, or the end use may not be known to the designers. The guidance in the standard for handling EUTs with output power leads is quite limited. The only reference to this scenario in MIL-STD-461 is found in Appendix A of the standard ("Application Guide"), which is not a mandatory part of the standard [29]:

However, there are several reasons that this guidance may be difficult to apply in the qualification of interface converters. For example, this guidance presupposes that the system designer or compliance engineer knows the output termination scheme that would produce "worst-case emission and susceptibility characteristics." More fundamentally, this guidance presupposes that such a configuration objectively exists for all EUTs. In practice, the fact that this guidance is not mandatory provides broad latitude for system designers and compliance engineers to select an output termination scheme of their own choosing. In general, voluntary selection of "worst-case" conditions by system designers during compliance evaluation is not considered likely, particularly when the method for identifying such conditions is not clear. Instead, in the face of limited and ambiguous guidance, the selection of an output termination scheme is most likely to be determined by convenience.

Several authors provide context for investigating the sensitivities of current compliance measurement setups. In [34], Crebier et al. demonstrated that LISN measurements are susceptible to line side impedance which can be mitigated by applying correction factors to the measurements. In [35], de Beer et al. used high-bandwidth current probes to perform emissions measurements with and without LISNs present in the system. The results demonstrated different EMI spectra when the LISNs are removed from the system and analysis is provided to explain the observed discrepancies. In [36], Ananda et al. used LISNs with different shielding levels to investigate the influence of the ground connection on LISN measurements. The suggestion from the analysis is to adopt a LISN with a shield for improved emissions measurements. In [37], Ziadé et al. discussed the significant influence of LISN input impedance on conducted EMI measurements and proposed methods for determining the uncertainty. In [38] and [39], Ales et al. and Amjadifard et al. proposed multistage LISNs to reduce the susceptibility of LISNs to the impedance of the input power line. In [40], Khilnani et al. identified a limitation with LISNs for performing low-frequency measurements and suggest modifying standard LISNs to overcome this limitation. In [41], Didat et al. demonstrated that significant CM current can flow through the EMI receiver during compliance measurements and influence the measured emissions. These studies all demonstrate the influences of the various aspects of the metrology required during conducted emissions compliance measurements. However, to the authors' knowledge, the impact of the output terminations adopted during compliance measurements has not been evaluated.

In this paper, the impact of the output termination scheme, including the impedance of the load to the testbed ground, will be systematically analyzed as a means of determining the conditions that might constitute a worst-case scenario. It will be shown that the output termination scheme is indeed a critical factor—even the dominant factor—affecting the qualification measurement at the LISNs. Moreover, it will be shown that the termination of convenience (i.e., a floating load) provides a poor representation of the conducted emissions in the final, deployed application.

Output power leads should be terminated with appropriate electrical loading that produces potentially worst-case emission and susceptibility characteristics.



FIGURE 2. Architecture of EMI characterization testbed for two-port devices.



FIGURE 3. EMI characterization testbed in half-bridge configuration with scaled LISNs employed as output terminations.

III. THEORETICAL ANALYSIS OF OUTPUT TERMINATIONS

To begin the analysis of the impact of the output termination scheme, it is helpful to provide further definition of the test system. The EUT in the testbed of Fig. 2 is specified to be a half-bridge inverter since it is flexible and useful yet simple. The detailed system for analysis is represented in Fig. 3. It can be shown that the conducted emissions of this system are dominated by its CM behavior. As such, this test setup has been extensively characterized and investigated to determine the most critical elements to include within a high-frequency CM model. The development and validation of this model is detailed in [27]. It is noted that the parasitic baseplate capacitances of the half-bridge module are included as they represent an important leakage path affecting the EMI qualification measurement at the LISNs. The distribution of parasitic capacitance between the half-bridge terminals is assumed to be asymmetric as described in [26], [27]. Furthermore, it is instructive for sake of analysis, to assume that the output terminations are scaled copies of the LISNs:

$$Z_{\rm out} = \frac{Z_{\rm lisn}}{\alpha} \tag{1}$$

where Z_{lisn} is the impedance of a single LISN as measured from the EUT-side terminal to the testbed ground and $\alpha \in [0, \infty)$.

The focus of the present work is understanding the influence of the output termination scheme on the emissions



FIGURE 4. CEM of the half-bridge testbed shown in Fig. 3. The CEM was developed using the procedure described in [25].

characteristics of this example system, with particular emphasis on CM behavior. To this end, the system model is reduced to its CEM shown in Fig. 4 in accordance with the methodology demonstrated in [27], where

$$v_{UL}^{\rm cm} = \frac{1}{2}(v_{Q1} - v_{Q2}) \tag{2}$$

$$v_{AN}^{\rm cm} \approx \frac{1}{4} (v_{Q1} - v_{Q2})$$
 (3)

$$v_{bp}^{\rm cm} = \frac{C_{ug} + C_{lg}}{C_{bp}} \frac{v_{Q1} - v_{Q2}}{2}.$$
 (4)

Valuable insight as to the impact of the output termination scheme can be gained by splitting the LISN current into the two component loop currents depicted in Fig. 4: the baseplate loop current $i_{\text{lisn},bp}$ and the output loop current $i_{\text{lisn},ol}$. The baseplate loop current is intrinsic to the qualification setup for a given EUT. For standard LISN specifications, it will be shown that this current is largely independent of the choice of output termination. In contrast, the output loop current is formed by the output terminations and is therefore heavily dependent on the selection thereof. This section will analyze these dependencies in order to systematically determine the choice of output terminations that meets the letter and/or spirit of the standard.

The baseplate and output loop components of the total CM current flowing through the LISNs can be determined through an unconventional implementation of superposition. Specifically, the loop currents in Fig. 4 are defined implicitly by the relationship

$$i_{\text{lisn}}^{\text{cm}} = i_{\text{lisn},ol} + i_{\text{lisn},bp} \,. \tag{5}$$

Expressions for the loop contributions are derived in the following paragraphs. First, the total baseplate current is solved for by the standard method of simplifying the circuit to a Thévenin equivalent with respect to the baseplate path. The "baseplate loop" portion of this current—the part that flows through the inboard LISN legs at the input—is determined using current division. Second, the output loop contribution is determined by forcing the baseplate current to be zero by definition (i.e., removing the baseplate path from the circuit) and employing voltage division.



FIGURE 5. Thévenin equivalent form of the testbed CEM with respect to the baseplate.

A. BASEPLATE CURRENT LOOP

By applying source transformations to v_{UL}^{cm} and v_{AN}^{cm} and combining parallel branches, the system model can be reduced to Thévenin form with respect to the leakage path through the baseplate as shown in Fig. 5. The equivalent voltage source driving current through the baseplate is given by

$$v_{bp,eq} = \frac{1}{2} \left(\frac{C_{ug} + C_{lg}}{C_{bp}} - \frac{2 + \alpha}{2(1 + \alpha)} \right) (v_{Q1} - v_{Q2}).$$
(6)

Commonly in multi-chip power modules, C_{ug} and C_{ag} are roughly equal due to similar direct-bond-copper (DBC) substrate size requirements to fit equal number of die on both DBCs. In contrast, C_{lg} does not require die attach, and thus is generally significantly smaller than the other two capacitances [27]. This geometric convention is observed in practice by several authors [27], [42], [43], [44], [45]. In this analysis, if it is assumed that C_{lg} is small and that C_{ug} and C_{ag} are roughly equal then the equivalent voltage source in (6) is approximately

$$v_{bp,eq} \approx -\frac{v_{Q1} - v_{Q2}}{4(1+\alpha)}.$$
 (7)

The total current through the baseplate can be expressed in the Laplace domain as

$$I_{bp}(s) = \frac{V_{bp,eq}(s)}{Z_p + Z_{\text{lisn}}^{\text{cm}}}$$
(8)

where Z_p is the series combination of the total baseplate capacitance and heat sink impedance, and $Z_{\text{lisn}}^{\text{cm}}$ is the parallel combination of all of the input and output terminating impedances (i.e., LISNs and scaled LISNs, respectively):

$$Z_{\rm lisn}^{\rm cm} = \frac{Z_{\rm lisn}}{2(1+\alpha)}.$$
(9)

The portion of the total baseplate current that flows through the inboard legs of the LISNs is readily determined from the model of Fig. 4 using current division. Specifically, the total CM current circulating between the baseplate and LISNs is

$$I_{\rm in}(s) = \frac{Y_{\rm in}}{Y_{\rm in} + Y_{\rm out}} I_{bp}(s)$$
$$= \frac{1}{1 + \alpha} I_{bp}(s) \tag{10}$$

and the fraction of this current flowing through the currentviewing resistors in the measurement legs is

$$I_{\text{lisn},bp} = G_i(s)I_{\text{in}}(s) \tag{11}$$



FIGURE 6. The testbed CEM with the leakage path neglected in order to isolate emissions due to currents circulating through the output.

where

$$G_{i}(s) = \frac{L_{l}C_{lo}s^{2} + R_{lo}C_{lo}s + 1}{L_{l}C_{lo}s^{2} + (R_{li} + R_{lo})C_{lo}s + 1 + \frac{C_{lo}}{C_{li}}}.$$
 (12)

It is noted that the primary effect of $G_i(s)$ for nominal LISN parameters is to reduce the magnitude of current components below 100 kHz. Above 100 kHz, $G_i(s)$ is approximately unity.

In summary, the voltage drop across the LISN resistors due to the baseplate current can be expressed as

$$V_{\text{lisn},bp} = \frac{R_{li}G_i(s)}{8(1+\alpha)^2} \frac{\left(V_{Q1}(s) - V_{Q2}(s)\right)}{Z_p + Z_{\text{lisn}}^{\text{cm}}}.$$
 (13)

Equation (13) indicates that the contribution of the baseplate loop is greatest with α near zero. The case $\alpha = 0$ corresponds to the output being open-circuited with respect to the CM. Although this case does not yield the maximum baseplate current, all of the baseplate current is forced to return through the LISNs, thereby maximizing its contribution to the LISN voltage.

For the purposes of this analysis, the key feature of (13) is the term $(1 + \alpha)^2$ in the denominator of the coefficient. Recalling (9), if $|Z_{\text{lisn}}^{\text{cm}}| \gg |Z_p|$, then the baseplate loop contribution to the LISN voltage is inversely proportional to α . Alternatively, if $|Z_p| \gg |Z_{\text{lisn}}^{\text{cm}}|$, then $V_{\text{lisn},bp}$ is inversely proportional to α^2 . Regardless, (13) shows that $V_{\text{lisn},bp}$ decreases as α increases.

B. OUTPUT LOOP CURRENT

The contribution of the output loop current, $i_{\text{lisn},ol}$, to the LISN voltage may be isolated by simply eliminating the leakage path through the baseplate from the model of Fig. 4 as shown in Fig. 6. The voltage induced across the inboard LISN resistors by the output loop is then readily determined by voltage division for the CM sources given in (2) and (3):

$$V_{\text{lisn},ol} = \frac{\alpha}{(1+\alpha)} \frac{R_{li}}{R_{li} + \frac{1}{C_{li}s}} \frac{V_{Q1}(s) - V_{Q2}(s)}{4}.$$
 (14)

Equation (14) indicates that the LISN voltage associated with $i_{\text{lisn},ol}$ increases asymptotically to a finite maximum as α approaches infinity. The case $\alpha \rightarrow \infty$ corresponds to shorting the output directly to the testbed ground, thereby minimizing the loop impedance. Thus, it is observed that the contribution of the output loop to the LISN voltage, $V_{\text{lisn},ol}$, increases as





FIGURE 7. EMI characterization testbed in half-bridge configuration with practical output terminations.

 α increases, and this stands in direct contrast to $V_{\text{lisn},bp}$ —cf., (13). The opposing trends revealed by this analysis of $V_{\text{lisn},ol}$ and $V_{\text{lisn},bp}$ with respect to α are explored in greater detail in the following sections.

IV. SIMULATION STUDY

A. OUTPUT TERMINATION SCHEME

The analysis of the previous section provides insight into the impact of varying the output terminations of the EUT within the context of a standard compliance setup. However, the scaling of the output terminations considered therein was selected for convenience of analysis rather than for convenience of implementation or experimental verification. In this section, an alternative configuration of the output terminations that is more amenable to realization in a physical testbed is considered. This analysis is first introduced in the form of a simulation study, which is empirically validated in the following section of this paper.

An alternative configuration of the output terminations is presented in Fig. 7. It is noted that this configuration is identical to the configuration analyzed in the previous section for the special case of $R_{li} = \infty$. However, the configuration of Fig. 7 represents a more practical topology than the scaled impedance of the previous section for two reasons. First, this configuration makes it straightforward to vary the value of the output CM impedance in a physical testbed by changing the value of R_{sweep} while retaining a fixed value for C_o . Since the termination of an interface converter is often unknown to a designer, the addition of the R_{sweep} variable introduces a degree of freedom for systematically varying the output termination. R_{sweep} , which does not directly represent a component in a deployed system, provides a frequency-independent method for isolating the influence of the termination method on an interface converter. The output CM impedance is defined for the balanced output terminations shown in Fig. 7 as

$$Z_{\text{out}}^{\text{cm}}(s) \triangleq \frac{1}{2} \left(L_o s + \frac{1}{C_o s} + R_{\text{sweep}} \right).$$
(15)

TABLE 1. Testbed Parameters

Parameter	Description	Value	Units		
	EUT				
V _{dc}	dc voltage	600	V		
f_{sw}	switching frequency	100	kHz		
d	duty cycle	50.09	%		
t_{dt}	dead time	400	ns		
$C_{ m dc}$	dc-link capacitor	400	μF		
C_n	neutral-forming capacitor	100	μF		
C_{ug}	U-to-baseplate capacitance	191	pF		
C_{ag}	A-to-baseplate capacitance	255.7	pF		
C_{lg}	L-to-baseplate capacitance	102.6	pF		
C_{bp}	total baseplate capacitance	549.3	pF		
R_h	heat sink resistance	0	Ω		
R_g	external gate resistance	2	Ω		
	LISNs				
L_l	input inductor	51.7	μH		
C_{li}	inboard capacitor	0.22	μF		
C_{lo}	outboard capacitor	8	μF		
R_{li}	inboard resistor	50	Ω		
R_{lo}	outboard resistor	5	Ω		
	Output Terminations				
Lo	output inductance	52.2	μH		
C_o	output capacitance	0.1	μF		
R _{sweep}	output resistor	1-10,000	Ω		

Second, this configuration mimics the topology of primary interest in this paper—namely, that of an interface converter feeding downstream systems. In this scenario, L_o represents the inductance of the feeder cables attached to the downstream system, and C_o represents the stray ground capacitance of the feeder cables as well as the capacitive contribution of the downstream system EMI filter.

B. SIMULATION STUDY

The system considered in the simulation study is the testbed of Fig. 7 and the component values shown in Table 1. The influence of varying R_{sweep} between 1 Ω and 10 k Ω for this configuration is presented in Fig. 8. It is noted that values of R_{sweep} outside this range were also evaluated as part of this study. However, these configurations were observed to conform to the behavior of the bounding cases demonstrated in Fig. 8 and are therefore not presented here. Fig. 8 demonstrates the influence of R_{sweep} on the CM LISN voltage, V_{lisn}^{cm} . The primary influence of Z_{out}^{cm} is associated with the switching frequency and low-order harmonics. For low values of Z_{out}^{cm} , as represented by $R_{\text{sweep}} = 1 \ \Omega$, emissions in this band are increased by as much as 40 dB compared to the high Z_{out}^{cm} case, as represented by $R_{\text{sweep}} = 10 \text{ k}\Omega$. On the other hand, emissions in the frequency range between 1-3 MHz are reduced by as much as 20 dB for low values of R_{sweep} . Finally, emissions above 3 MHz are minimally affected by the value of R_{sweep} .

Additional insight into the system behavior can be obtained by evaluating the individual contributions of the baseplate and output loops to the total CM LISN voltage profiles demonstrated in Fig. 8. These individual contributions are presented in Fig. 9, along with the total spectrum of $V_{\text{lisn}}^{\text{cm}}$, for the two



FIGURE 8. Simulated emissions in qualification configuration with output terminating resistance swept from 1 Ω to 10 k Ω . The bounding cases of $R_{\text{sweep}} = 1 \Omega$ and $R_{\text{sweep}} = 10 \text{ k}\Omega$ capture the same behavior as a short and open load, respectively.



FIGURE 9. Contributions of output and baseplate current loops to total emissions in qualification configuration for (a) high-impedance output termination and (b) low-impedance output termination.

bounding cases considered in this study: $R_{sweep} = 1 \Omega$ and $R_{sweep} = 10 \ k\Omega$. For the high- Z_{out}^{cm} ($R_{sweep} = 10 \ k\Omega$) case shown in Fig. 9(a), total emissions are influenced by both the output loop and the baseplate loop. However, the baseplate loop is more influential than the output loop across the entire frequency range shown. For the low- Z_{out}^{cm} ($R_{sweep} = 1 \ \Omega$) case shown in Fig. 9(b), the influence is strongly frequency-dependent. For example, emissions in the range of the switching frequency are dominated by the output loop, while the emissions at frequencies above 3 MHz are mainly determined by the baseplate loop.

C. NET EFFECT OF OUTPUT TERMINATIONS

The simulation study presented in this section demonstrates that the CM impedance of the output terminations dramatically influences the conducted emissions of an interface



FIGURE 10. Notional contribution of output loop current and baseplate loop current to the CM LISN voltage based on simulation analysis.

converter in the conventional qualification setup. The measured LISN voltage, which is used to determine compliance, is dominated by the contribution of CM currents flowing through the power module baseplate and the output terminations. However, the relative significance of these two loops is frequency dependent. These relationships are summarized in the notional emissions envelopes plotted in Fig. 10. When the coupling of the converter output to the reference plane is strong $(Z_{out}^{cm} \rightarrow 0)$, the emissions profile is dominated by the contribution of the output loop, and peak emissions occur at the switching frequency. On the other hand, when the coupling of the converter output to the reference plane is weak $(Z_{out}^{cm} \rightarrow \infty)$, the emissions profile is dominated by the contribution of the baseplate loop. Peak emissions in this case are strongly dependent on the parasitic characteristics of the EUT.

Overall, this analysis demonstrates that the method selected for terminating the output port of an interface converter has a significant impact on the resulting conducted emissions profile. Since this influence is frequency-dependent, no single configuration of the output terminations can be unequivocally identified as the "worst-case" scenario for emissions and susceptibility across all frequency bands. On the other hand, it is possible to identify one configuration of the output terminations that increases emissions at the switching frequency and a different configuration that increases emissions in the MHz band. However, neither of these configurations can be claimed to answer the guidance provided in the standard for "worst case emission and susceptibility characteristics". This being the case, this guidance leads to a conundrum in which practitioners have no objective criteria by which to select output terminations for qualification testing. Anecdotal evidence suggests that this selection is often determined by convenience, in which case terminations with high CM impedance to the reference plane are likely to be used $(Z_{out}^{cm} \rightarrow \infty)$. This could lead to a scenario in which an interface converter passes qualification but causes electromagnetic compatibility problems when deployed. This possibility is evaluated in the application example included in Section VI.



FIGURE 11. Realized experimental testbed modified from [27].

V. EMPIRICAL VALIDATION

To validate the predictions presented in the previous section, the same conditions used in the simulation study were also evaluated empirically using an adaptation of the laboratory testbed described and characterized in [27]. The testbed, shown in Fig. 11, is based on MIL-STD-461, CE-102 [29] and features an isolated copper reference plane and custom LISNs designed for evaluating WBG semiconductors. The original configuration of this testbed as described in [27] is consistent with the schematic shown in Fig. 3 for $\alpha = 1$. However, for this study, the testbed was modified to employ the L-C-R output termination scheme shown in Fig. 7. The modified output terminations employ air-core 50 μ H inductors which were characterized in a previous effort by the authors [27]. Each of the output capacitance elements, C_o , was set to 0.1 μ F and implemented using high-quality film capacitors [46]. All components used to implement the output termination resistance, R_{sweep} , were selected from the same Ohmite TGH series of power resistors to minimize parasitic differences between the various values considered [47]. Finally, the single-phase, half-bridge inverter was implemented with a commercially available 1.2 kV, 120 A SiC half-bridge power module from Wolfspeed [48]. The half-bridge inverter was operated with a dc input bus of 600 V utilizing fixed-duty-ratio PWM and a switching frequency of 100 kHz. The circuit parameter values match the values used in the simulation study presented in Table 1, with the inclusion of the parasitic parameters shown

TABLE 2.	Characterized	LISN Component,	Output	Termination	Component,
and Lead	Parasitic Valu	es [27]			

	Value				
Parameter	L	U	Α	Ν	Units
L_t	307.0	362.0	339.0	203.5	nH
C_t	16.67	15.00	13.57	14.59	pF
C_{pi}	52.77	47.50	42.96	46.19	pF
$\dot{C_{po}}$	15.56	14.00	20.16	21.12	pF



FIGURE 12. (a) LISN model with interconnect parasitics included. (b) Output termination model with interconnect parasitics included [27].

in Table 2. As described in [27], the most important parasitics of this system with respect to CM behavior are the baseplate capacitances of the power module and the parastics of the LISNs and output terminations. The same parasitic model from [27], shown in Fig. 12(a), was adopted in this paper for the LISNs. The model of the output terminations used in this paper is shown in Fig. 12(b). This model is updated with respect to that discussed in [27] due to the modified output terminations employed in this paper. Additional provisions were made in the testbed to limit the influence of other parasitic factors. These steps included elevating the PCB, dc-link capacitors, and neutral-forming capacitors from the chassis to reduce capacitive coupling; fitting a 9.8 mH CM choke at the testbed input to minimize the influence of CM currents from the input power supply; employing a large CM choke on the power input of the gate drivers; adopting a low-capacitive isolation transformer within the gate driver design [49]; and using fiber-optic isolation for the gate driver input signals [50]. The LISN voltages and the switch voltages were simultaneously monitored with high-bandwidth differential probes [51] and a suitable eight-channel oscilloscope [52]. These voltage measurements were performed with differential probes rather than a conventional EMI receiver to eliminate the direct Earth-ground connection which would otherwise be introduced by the instrument. This connection has been demonstrated to exacerbate the flow of circulating CM currents in this type of qualification setup [41]. In order to validate the isolated voltage measurement technique, frequency-domain measurements were also performed with this setup using a 3-GHz spectrum analyzer [53]. The isolated voltage probe measurements were compared with the spectrum analyzer measurements in the frequency domain, and strong agreement was observed across the range of frequencies considered in this study.

Fig. 13 presents a comparison of the predicted and measured LISN voltages for the five output termination configurations considered in the previous simulation study. Similar to [27], the simulation predictions were obtained by solving the CEM in MATLAB for integer harmonics of the switching frequency, ranging from 100 kHz to 10 MHz. The measured results were obtained by converting the time-domain isolated voltage measurements to the frequency domain via FFT using a Hann window. The spectral comparisons for all cases demonstrate good agreement up to 7 MHz, and reasonable agreement is achieved up to 10 MHz. Notably, the experimental results corroborate the predictions presented in the preceding section regarding the influence of the output terminations on the emissions envelope of this system. As predicted by the model, no single output termination configuration produces higher emissions across the entire frequency range considered. The highest emissions observed at the switching frequency (100 kHz) occur with low- Z_{out}^{cm} ($R_{sweep} =$ 1 Ω), while the highest emissions between 0.9 and 2 MHz occur with high- Z_{out}^{cm} ($R_{sweep} = 10 \text{ k}\Omega$).

The edge rates of the simulated switch voltage waveforms were calibrated to the measured system behavior for each experimental case demonstrated in Fig. 13. This calibration is necessary because the switch voltage waveforms are not consistent for these cases. The variation in switch voltage edge rates can be explained by considering the the mixed-mode behavior of this system. For each of the cases considered in Fig. 13, the DM impedance remains constant, while the CM impedance varies considerably due to the changes in R_{sweep} . Consequently, the DM load current remains fixed at approximately 4.2 Arms for all cases considered, but the measured CM load current varies between 0.1 Arms and 6.7 Arms for the same set of conditions. Thus, the overall mixed-mode current through the power module terminals is observed to be heavily dependent on the CM impedance for this system. It is well known that the switching edge rates of unipolar devices such as SiC MOSFETs are strongly influenced by the device drain current [7], [54], [55]. This influence is believed to be the reason that changing the CM impedance of the output terminations also influences the voltage edge rates (dv/dt) of the switching elements in this system.

To confirm this suspected sensitivity, an additional experiment was carried out. A high-bandwidth Rogowski coil [56]



FIGURE 13. Comparison of measured and simulated LISN voltages in the EMI testbed for (a) $R_{sweep} = 10 \text{ k}\Omega$, (b) $R_{sweep} = 1 \text{ k}\Omega$, (c) $R_{sweep} = 250 \Omega$, (d) $R_{sweep} = 50 \Omega$, and (e) $R_{sweep} = 1 \Omega$.



FIGURE 14. (a) Current of the high-side MOSFET (i_{Q1}) and (b) voltage of the high-side MOSFET (v_{Q1}) . Both plots consider converter operation with $R_{\text{sweep}} = 1 \ \Omega$ and $R_{\text{sweep}} = 10 \ \text{k}\Omega$.

was attached to the high-side drain terminal of the power module during operation to measure the mixed-mode switch current. Simultaneously, an isolated voltage probe [51] was employed to measure the drain-to-source voltage of the same switch position. The measured switch position currents and voltages of the $R_{\text{sweep}} = 1 \ \Omega$ and $R_{\text{sweep}} = 10 \ \text{k}\Omega$ cases are compared in Fig. 14. Notably, the peak mixed-mode current magnitude in the $R_{\text{sweep}} = 1 \ \Omega$ case is 70% higher than the $R_{\text{sweep}} = 10 \text{ k}\Omega$ case, and the dv/dt also increases by >80%. This comparison suggests that the increased mixed-mode current is likely the reason for the increased dv/dt observed with low values of Z_{out}^{cm} . This is also believed to be the cause of the subtle changes in high-frequency behavior observed for the different cases in Fig. 13. Although the model calibration in this work focused on adjusting for edge rate differences due to the changing mixed-mode currents, this calibration process could similarly be employed to account for differences in edge rates due to other parameters such as varying the gate resistance.

VI. APPLICATION EXAMPLE DEMONSTRATING DEPLOYED EMISSIONS

A. DEPLOYED CONFIGURATION

The use of LISNs is well established for evaluating conducted emissions during qualification measurements. However, LISNs are not present when a system is deployed. Thus, to evaluate the emissions profile of a converter in its "deployed" configuration, a new figure of merit (FOM) must be adopted. For this study, the input CM current, i_{in}^{cm} , is adopted as a new FOM for assessing the conducted emissions of interface converters in the deployed configuration. As a baseline, the original simulation study shown in Fig. 8, which includes LISNs, was repeated. The new FOM was calculated for this study, and the results are plotted in Fig. 15. Additionally, calibrated edge rates were employed



FIGURE 15. Simulated input CM current emissions in qualification configuration with output terminating resistance swept from 1 Ω to 10 k Ω .

for each configuration to account for the differences in rise and fall times discussed previously. Comparing the trends of Figs. 8 and 15 reveals that the updated FOM results are similar to those obtained with the conventional LISN voltage FOM. Namely, emissions are highest at low-frequency when $R_{\text{sweep}} = 1 \Omega$ and are highest in the 0.9 to 2 MHz range when $R_{\text{sweep}} = 10 \text{ k}\Omega$.

While LISNs are not physically installed alongside deployed converters, the LISN can be adjusted to reflect the properties of a deployed interface converter by making modest changes to its structure. As detailed in [29], the line inductors of the LISN are intended to model the input cabling to the EUT when installed. Similarly, the LISN capacitors are used to represent the capacitive coupling to the common reference plane in a deployed configuration. However, the 50 Ω resistors on the EUT-side of the LISN structure are strictly an artifact of the metrology used to perform qualification measurements and have no relevance to a deployed setup. Additionally, it has been demonstrated that these terminations significantly influence the emissions performance of a converter in a manner that is not consistent with its deployed use [27]. Therefore, replacing these terminations with a high-impedance value is a reasonable starting point for evaluating the conducted emissions characteristics of a converter in the deployed state.

To evaluate the emissions of an interface converter in the deployed configuration, the simulation considered in this work was reconfigured with $R_{li} = 1 \text{ k}\Omega$ rather than $R_{li} =$ 50 Ω . This setup is more representative of a deployed converter with parasitic input coupling, rather than a converter attached to qualification instrumentation. An updated simulation study was performed to evaluate the sensitivity of the deployed system configuration to variations in the output-side coupling, again by varying the R_{sweep} parameter. The results of this study are presented in Fig. 16. Comparing the qualification configuration shown in Fig. 15 with the deployed configuration shown in Fig. 16 reveals the influence of the 50 Ω termination used during qualification measurements. Namely, the system CM resonance at approximately 1.1 MHz



FIGURE 16. Simulated input CM current emissions in deployed configuration with output terminating resistance swept from 1 Ω to 10 k Ω .



FIGURE 17. Empirical input CM current emissions in deployed configuration with output terminating resistance swept from 1 Ω to 10 k Ω .

is prominently reflected in the envelope of i_{in}^{cm} for this configuration with high values of R_{sweep} . The fact that this content is absent from the qualification setup suggests that this resonance is suppressed by the 50 Ω instrument terminators employed in that case.

To validate the results from this simulation study, the physical testbed was also modified to employ $R_{li} = 1 \text{ k}\Omega$. Conditions identical to those of the simulation study were evaluated empirically by varying the value of R_{sweep} . During these procedures, i_{in}^{cm} was measured with a high-bandwidth current probe [57] at the location indicated by the i_{in}^{cm} label in Fig. 7. Both connections between the input LISNs and power electronics were routed through the same current sensor to directly measure the CM current. These results are presented in Fig. 17. For each output configuration, the figure shows both the measured spectra and the envelope of the measured spectral peaks. The empirical results demonstrate strong agreement with the model predictions shown in Fig. 16. Importantly, the elevated emissions predicted by the simulation at the CM resonance are prominently observed in the $R_{\text{sweep}} = 10 \text{ k}\Omega$ experimental results. This study suggests that a system could comply with all qualification requirements and nevertheless demonstrate troublesome emissions when deployed due to the emergence of CM resonances, which were masked during qualification. Furthermore, this study demonstrates that the influence of output terminations can be more impactful in deployed systems compared to qualification measurements.

B. DEPLOYED SYSTEM EMISSIONS MITIGATION

Heretofore, the CEM has been employed as a tool for predicting the emissions of an interface converter across a wide range of system configurations. This analysis has demonstrated the strong predictive capabilities of the model. However, the primary parameter used in the simulation studies, R_{sweep} , was selected as a convenient means to represent the system's parasitic output coupling for the sake of analysis. To make use of the resulting findings, this analysis must be linked to one or more degrees-of-freedom that are generally available to system designers. Accordingly, this section details a targeted two-step approach that leverages the CEM to identify mitigation techniques using system parameters that are available for this purpose. It is noted that this analysis requires a "baseline" emissions envelope to apply the proposed mitigation steps. Generally, the "worst-case" system configuration should be selected for this baseline, if possible. As discussed previously, for some systems there may be no single configuration that can be identified as the "worst-case" at all frequencies. For the subsequent analysis, the R_{sweep} value of 1 Ω was selected for the "baseline" configuration. The baseline emissions profile is shown as $R_{\text{sweep}} = 1 \Omega$ in Fig. 17.

1) SUPPRESSION OF f_{SW} CONTENT

Analysis of the baseline profile reveals high emissions at the switching frequency, f_{sw} . As shown in Fig. 10, the emissions at low-frequencies are dominated by the output loop. To mitigate these low-frequency emissions, the output loop impedance can be increased by introducing a CM choke between the inverter and the output termination. This is a common technique found in the literature for reducing circulating currents between a converter and its attached load [58], [59], [60]. This scheme also represents the attachment of an output termination or load that includes an internal CM choke. In the CEM, this CM choke is expressed as an additional inductance between the EUT and the output termination as shown in Fig. 18.

Using the techniques described in Section III, the testbed can be reduced to Thévenin form with respect to the output loop as shown in Fig. 19. The equivalent voltage source of this circuit is given by

$$v_{ol,eq} \approx \frac{1}{4} (v_{Q1} - v_{Q2}).$$
 (16)

Inspection of the Thévenin equivalent circuit reveals that the CM choke inductance, output inductance, and baseplate capacitance form an anti-resonance in the outer loop (assuming





FIGURE 18. CEM with output CM choke and L-C-R output termination.



FIGURE 19. Thévenin equivalent form of the testbed CEM with respect to the output loop and including CM choke.

TABLE 3. Realized CM Choke Fabrication Details

Description	Value
Cores	Ferroxcube TX42/26.13-3E25
# Cores	8
AWG	18
# Turns	8
L _{choke} (@100 kHz)	4.6 mH

 $C_o \gg C_{bp}$) at frequency

$$f_{\text{term}} \approx \frac{1}{2\pi \sqrt{C_{bp}(L_{\text{choke}} + \frac{L_o}{2})}}$$
 (17)

where L_{choke} is the CM inductance introduced by the CM choke and f_{term} is the anti-resonant frequency of the output loop. In order to achieve maximum attenuation at the switching frequency, L_{choke} may be solved when $f_{term} = f_{sw}$ resulting in

$$L_{\text{choke}, f_{SW}} \approx \frac{1}{(2\pi f_{\text{sw}})^2 C_{bp}} - \frac{L_o}{2} = 4.6 \,\text{mH}$$
 (18)

where $L_{\text{choke}, fsw}$ is the CM choke value required to create an anti-resonance at f_{sw} .

To demonstrate the influence of the proposed mitigation solution, a CM choke with a value of 4.6 mH was introduced into the testbed. The implementation details of the realized CM choke are presented in Table 3. The measured spectra for this configuration are compared with the baseline emissions in Fig. 20. By targeting the anti-resonance at the switching frequency, the CM choke reduces emissions by over 50 dB at 100 kHz. However, as anticipated by the model, the CM



FIGURE 20. Empirical input CM current emissions in deployed configuration with and without an output CM choke ($R_{sweep} = 1 \Omega$).



FIGURE 21. Primary CM resonant contributors to the baseplate current loop ($L_{choke} \gg L_o$ and deployed configuration).

choke also creates a high- Z_{out}^{cm} configuration, resulting in behavior similar to the $R_{sweep} = 10 \text{ k}\Omega$ case studied previously. The influence of the system CM resonance is prominent in the 0.7 MHz to 1.5 MHz frequency range, where emissions increase as much as 20 dB. This outcome would potentially be surprising were it not for the predictions of the CEM provided previously. In the authors' experience, the introduction of a CM choke is usually the first mitigation step attempted when troublesome CM behavior is identified. However, the possibility that inserting a CM choke could lead to the activation of a latent system CM resonance is not widely recognized.

2) SUPPRESS CM RESONANCE

To mitigate the increased emissions introduced by the CM choke, it is necessary to establish the primary contributors to the system CM resonance. Referring to Fig. 18, it is observed that the output termination exerts minimal influence on the CM resonance when $L_{choke} \gg L_o$. This is found to be the case for the proposed value of 4.6 mH, which produces a high- Z_{out}^{cm} configuration of the system. Similarly, in the deployed configuration with a high value of R_{li} , the series C_{li} and R_{li} branch exerts little influence on the CM resonance. The remaining components, which constitute the primary contributors to the system CM resonance, are shown in Fig. 21.



FIGURE 22. Empirical input CM current emissions in deployed configuration with and without R_h damping ($R_{sweep} = 1 \Omega$, $L_{choke} = 4.6$ mH).

Inspection of Fig. 21 reveals a second-order resonant circuit. Though most of the component values are parasitic or intrinsic to the system, the value of Z_h represents a degree-of-freedom that is available to the system designer. Heretofore, this impedance, which represents the connection between the module cold plate and the reference plane, was neglected (i.e., $Z_h = 0$). This corresponds to a configuration with the cold plate directly bonded to the reference plane. However, to damp the CM resonance, a resistance may be introduced in this position (i.e., $Z_h = R_h$). Assuming that $C_{lo} \gg C_{bp}$, the resistance may be selected by solving for the critically damped resistance of the second-order circuit using

$$R_{h,\text{crit}} \approx \sqrt{\frac{2L_l}{C_{bp}}} - \frac{R_{lo}}{2} = 431.3 \,\Omega. \tag{19}$$

The impact of the proposed damping resistance was demonstrated by introducing the closest available value ($R_h =$ 405 Ω) into the realized testbed. The measured emissions profile of this configuration is compared with that of the configuration employing only the CM choke in Fig. 22. As predicted, the introduction of R_h damps the CM resonance which was prominently observed when the CM choke was introduced. At 1.1 MHz, the addition of $R_h = 405 \Omega$ reduces measured emissions by over 10 dB. Notably, introducing R_h provides this damping without diminishing the emissions improvements at low frequencies that are provided by the CM choke.

It is noted that the attachment of the cold plate to the reference plane (i.e., $Z_h = 0$) may be desirable in some systems to maintain the cold plate at a touch-safe potential. For such cases, the CEM can be further employed to determine the maximum R_h value that can be introduced without exceeding a specified touch-safe potential (e.g., 50 V). For the system under consideration, this resistance was determined to be 87.5 Ω . This scenario was also experimentally verified by introducing the closest available value ($R_h = 83 \Omega$) into the realized testbed. The experimental results for this configuration are also presented in Fig. 22. This configuration provides

1194

a measurable reduction in emissions at the CM resonance compared to the un-damped case (>4 dB) while maintaining touch safety. Overall, the examples included in this section demonstrate that a thorough understanding of the sources of CM behavior in a given system can lead to simple and effective EMI mitigation solutions.

VII. CONCLUSION

This article provides an analysis of the conducted emissions characteristics of interface converters, which supply power to downstream systems with unknown properties. Current emissions standards provide limited and ambiguous guidance for the evaluation of interface converters, because they are typically written from the standpoint of qualifying end-use equipment. This article introduces a CEM to evaluate the influence of output terminations on the emissions profile of a representative interface converter. This influence is found to be considerable, with peak emissions varying as much as 40 dB depending on the selected output termination.

Further analysis is included to demonstrate that the effect of output termination on interface converters in deployed systems can be more pronounced than in qualification measurements. This study suggests that a system could comply with all qualification requirements and nevertheless demonstrate troublesome emissions when deployed due to the emergence of CM resonances, which were masked during qualification. The CEM is also leveraged to identify emissions mitigation techniques that target emissions in specific frequency bands. These mitigation techniques are demonstrated to yield emissions reductions of 50 dB at the switching frequency and more than 10 dB at the CM resonant frequency for the system under consideration.

This paper demonstrates the influence of output terminations on conducted emissions, both during qualification measurements and in deployed systems. As demonstrated herein, the influence of these terminations produces a degree of variability in conducted emissions measurements, which is believed to be generally undesirable. To reduce this variability, future conducted emissions standards could introduce standardized output terminations for evaluating the emissions of interface converters. Such a change would be analogous to the introduction of LISNs to provide a reference impedance for leakage currents at the system input. Adopting a similar circuit on the converter output would establish known leakage paths with well-defined impedance profiles, which could improve the consistency of compliance measurements for interface converters. Furthermore, alternative metrology such as current probes or time-domain isolated voltage measurements could be adopted as well. These steps could reduce the sensitivity of compliance measurements to the input characteristics of the measurement equipment and could also reduce the possibility of circulating currents within auxiliary wiring. It is noted that adopting these or similar approaches may introduce other system-level influences that have not been anticipated by the authors. Therefore, such changes would need to be carefully



considered and discussed by subject-matter experts prior to adoption.

Overall, this paper highlights an opportunity to improve emissions standards with respect to interface converters by standardizing output terminations, particularly in view of the increased high-frequency emissions produced by systems implemented with wide band-gap technology.

REFERENCES

- X. She, A. Q. Huang, O. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.
- [2] X. Li et al., "A SiC power MOSFET loss model suitable for high-frequency applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8268–8276, Oct. 2017.
- [3] F. F. Wang and Z. Zhang, "Overview of silicon carbide technology: Device, converter, system, and application," *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 13–32, 2016.
- [4] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.
- [5] Y. Xie, C. Chen, Z. Huang, T. Liu, Y. Kang, and F. Luo, "High frequency conducted EMI investigation on packaging and modulation for a SiC-based high frequency converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1789–1804, Sep. 2019.
- [6] D. Han, J. Noppakunkajorn, and B. Sarlioglu, "Comprehensive efficiency, weight, and volume comparison of SiC- and Si-based bidirectional DC–DC converters for hybrid electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 63, no. 7, pp. 3001–3010, Sep. 2014.
- [7] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance evaluation of high-power SiC MOSFET modules in comparison to Si IGBT modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019.
- [8] L. Gill, T. Ikari, T. Kai, B. Li, K. Ngo, and D. Dong, "Medium voltage dual active bridge using 3.3 kV SiC MOSFETs for EV charging application," in *IEEE 2019 Energy Convers. Congr. Expo.*, pp. 1237–1244.
- [9] S. Srdic, X. Liang, C. Zhang, W. Yu, and S. Lukic, "A SiC-based highperformance medium-voltage fast charger for plug-in electric vehicles," in *IEEE 2016 Energy Convers. Congr. Expo.*, pp. 1–6.
- [10] C. Zhao et al., "Power electronic traction transformer-medium voltage prototype," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3257–3268, Jul. 2014.
- [11] IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships, IEEE Standard 1709-2018 (Revision of IEEE Standard 1709-2010), 2018.
- [12] R. M. Cuzner, "Power electronics packaging challenges for future warship applications," in *IEEE 2015 Int. Workshop Integr. Power Packag.*, pp. 5–8.
- [13] J. Ciezki and R. Ashton, "Selection and stability issues associated with a navy shipboard DC zonal electric distribution system," *IEEE Trans. Power Del.*, vol. 15, no. 2, pp. 665–669, Apr. 2000.
- [14] J. Kuseian, "Naval power systems technology development roadmap," PMS 320, May 2013, Accessed: Oct. 26, 2022. [Online]. Available: https://defenseinnovationmarketplace.dtic.mil/wp-content/uploads/ 2018/02/NavalPowerSystemsTechnologyRoadmap.pdf
- [15] B. Zhang and S. Wang, "A survey of EMI research in power electronics systems with wide-bandgap semiconductor devices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 626–643, Mar. 2020.
- [16] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 5, pp. 2154–2165, Sep./Oct. 2011.
- [17] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, May 2014.
- [18] H. W. Ott, *Electromagnetic Compatibility Engineering*. Hoboken, NJ, USA: Wiley, 2009.

- [19] A. K. Tripathi et al., "Design considerations of a 15-kV SiC IGBTbased medium-voltage high-frequency isolated DC–DC converter," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3284–3294, Jul./Aug. 2015.
- [20] A. D. Brovont, J. Zhao, and A. N. Lemmon, "Modeling and validation of conducted emissions trends in medium-voltage power electronic systems," in *IEEE 2020 Appl. Power Electron. Conf. Expo.*, pp. 1438–1444.
- [21] T. Ericsen, N. Hingorani, and Y. Khersonsky, "PEBB power electronics building blocks from concept to reality," in *IEEE 2006 Rec. Conf. Papers - Ind. Appl. Soc. 53rd Annu. Petroleum Chem. Ind. Conf.*, pp. 1–7.
- [22] A. Monti and F. Ponci, "PEBB standardization for high-level control: A proposal," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3700–3709, Oct. 2012.
- [23] S. Rosado, F. Wang, and D. Boroyevich, "Design of PEBB based power electronics systems," in *IEEE 2006 Power Eng. Soc. Gen. Meeting*, p. 5.
- [24] J. Wang et al., "Power electronics building block (PEBB) design based on 1.7 kV SiC MOSFET modules," in *IEEE 2017 Electric Ship Technol. Symp.*, pp. 612–619.
- [25] A. D. Brovont and S. D. Pekarek, "Derivation and application of equivalent circuits to model common-mode current in microgrids," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 297–308, Mar. 2017.
- [26] A. D. Brovont, A. N. Lemmon, C. New, B. W. Nelson, and B. T. DeBoi, "Analysis and cancellation of leakage current through power module baseplate capacitance," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4678–4688, May 2020.
- [27] A. N. Lemmon, A. D. Brovont, C. D. New, B. W. Nelson, and B. T. DeBoi, "Modeling and validation of common-mode emissions in wide bandgap-based converter structures," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8034–8049, Aug. 2020.
- [28] A. N. Lemmon and A. D. Brovont, "Impact of output terminations on conducted emissions evaluation of interface converters," in *IEEE 2021 Electric Ship Technol. Symp.*, pp. 1–7.
- [29] Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment, MIL-STD-461, Department of Defense Interface Standard, Dec. 2015.
- [30] Electromagnetic Compatibility of Multimedia Equipment–Emission Requirements, CISPR 32:2015: International Electrotechnical Commission, Mar., 2015.
- [31] Electromagnetic Compatibility of Multimedia Equipment–Emission Requirements, EN 55032:2015, European Union, Jul. 2015.
- [32] Code of Federal Regulations, Title 47, Part 15 Radio Frequency Devices, 47 CFR 15, Federal Communications Commission, Oct. 2010.
- [33] Uninterruptible Power Systems (UPS) Part 2: Electromagnetic Compatibility (EMC) Requirements, IEC 62040-2, International Electrotechnical Commission, Geneva, CH, Nov. 2016.
- [34] J. Crebier, J. Roudet, and J. Schanen, "Problems using LISN in EMI characterization of power electronic converters," in *Proc. IEEE 30th Annu. Power Electron. Specialists Conf. Rec. (Cat. No.99CH36321)*, 1999, vol. 1, pp. 307–312.
- [35] A. de Beer, G. N. Wooding, and J. van Wyk, "Problematic aspects when using a LISN for converter EMI characterisation," in *IEEE 2013 Int. Conf. Ind. Technol.*, pp. 633–637.
- [36] W. Ananda, S. A. Cahyadi, I. Inayaturohman, and D. Hamdani, "The effect of the grounding condition of line impedance stabilization network on the measurement validity of conducted emission parameter," in *IEEE 2017 Int. Conf. High Voltage Eng. Power Syst.*, pp. 498–502.
- [37] F. Ziadé et al., "Improvement of LISN measurement accuracy based on calculable adapters," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 2, pp. 365–377, Feb. 2016.
- [38] A. Ales, F. T. Belkacem, and D. Moussaoui, "Laboratory line impedance stabilisation network: Experimental studies," in *IEEE 2011* 10th Int. Conf. Environ. Elect. Eng., 2011, pp. 1–4.
- [39] R. Amjadifard, M. Tavakoli Bina, H. Khaloozadeh, and F. Bagheroskouei, "Proposing an improved DC LISN for measuring conducted EMI noise," *IEEE Trans. Electromagn. Compat.*, vol. 63, no. 3, pp. 752–761, Jun. 2021.
- [40] A. Khilnani, L. Wan, M. Sumner, D. Thomas, A. Hamid, and F. Grassi, "Conducted emissions measurements in DC grids: Issues in applying existing LISN topologies and possible solutions," in *IEEE 2021 15th Int. Conf. Compat., Power Electron. Power Eng.*, pp. 1–6.

- [41] M. Didat, C. D. New, S. Choi, and A. Lemmon, "Improved methodology for conducted EMI assessment of wide band-gap power electronics," *IEEE Open J. Power Electron.*, vol. 3, pp. 731–740, 2022.
- [42] N. Christensen et al., "Common mode current mitigation for medium voltage half bridge SiC modules," in *IEEE 2017 19th Eur. Conf. Power Electron. Appl.*, pp. P.1–P.8.
- [43] A. B. Jørgensen et al., "Reduction of parasitic capacitance in 10 kV SiC MOSFET power modules using 3D FEM," in *IEEE 2017 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.8.
- [44] G. Engelmann, S. Quabeck, J. Gottschlich, and R. W. De Doncker, "Experimental and simulative investigations on stray capacitances and stray inductances of power modules," in *IEEE 2017 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.10.
- [45] H. Chen and D. Divan, "High speed switching issues of high power rated silicon-carbide devices and the mitigation methods," in *IEEE 2015 Energy Convers. Congr. Expo.*, pp. 2254–2260.
- [46] TDK, "Film capacitors: Metallized polypropylene film capacitors (MKP)," B32656S2104J564 datasheet, Dec. 2021. [Online]. Available: https://www.tdk-electronics.tdk.com/inf/20/20/db/fc_2009/ MKP_B32656S.pdf
- [47] Ohmite, "TGH series: 120 and 200 watt SOT227Package thick film power," TGH Series datasheet, Nov. 2021. [Online]. Available: https://www.ohmite.com/assets/docs/res_tgh.pdf
- [48] Wolfspeed, "1200 V, 120 A all-silicon carbide high performance, switching optimized, half-bridge module," CAS120M12BM2 datasheet, Nov. 2020. [Online]. Available: https://www.wolfspeed.com/
- [49] Murata Power Solutions, "MGJ3 series: 5.2kVDC isolated 3 W gate drive SM DC-DC converters," MGJ3T12150505MC datasheet, 2021. [Online]. Available: https://www.murata.com/
- [50] Broadcom, "AFBR-16xxZ and AFBR-26x4Z/25x9Z: DC-50MBd versatile link fiber optic transmitter and receiver for 1 mm POF and 200 μ m PCS," AFBR-2634Z datasheet, Jul. 2016. [Online]. Available: https://www.broadcom.com/

- [51] Tektronix, "High-voltage differential probes," THDP0200 datasheet, Apr. 2021. [Online]. Available: https://www.tek.com/
- [52] Tektronix, "5 series MSO mixed signal oscilloscope datasheet," MSO58 5-BW-1000 datasheet, Jun. 2022. [Online]. Available: https://www.tek. com/
- [53] Keysight Technologies, "CXA X-series signal analyzer N9000 A," N9000A-ATO-79195 datasheet, Apr. 2018. [Online]. Available: https: //www.keysight.com/us/en/assets/7018-02222/data-sheets-archived /5990-4327.pdf
- [54] Z. Chen, D. Boroyevich, R. Burgos, and F. Wang, "Characterization and modeling of 1.2 kV, 20 a SiC MOSFETs," in *IEEE 2009 Energy Convers. Congr. Expo.*, pp. 1480–1487.
- [55] Y. Jiao and M. M. Jovanovic, "Comparative evaluation of static and dynamic performance of 1.2-kV SiC power switches," in *IEEE 2018 Appl. Power Electron. Conf. Expo.*, pp. 2704–2711.
- [56] Tektronix, "Current probes," TRCP0300 datasheet, Jan. 2019. [Online]. Available: https://www.tek.com/
- [57] Tektronix, "30 A AC/DC Current Probe," TCP0030 A datasheet, Aug. 2017. [Online]. Available: https://www.tek.com/
- [58] D. Han, C. T. Morris, W. Lee, and B. Sarlioglu, "Comparison between output cm chokes for SiC drive operating at 20- and 200-kHz switching frequencies," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2178–2188, May/Jun. 2017.
- [59] A. Muetze and C. R. Sullivan, "Simplified design of common-mode chokes for reduction of motor ground currents in inverter drives," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2570–2577, Nov./Dec. 2011.
- [60] C. Mei, J. Balda, W. Waite, and K. Carr, "Minimization and cancellation of common-mode currents, shaft voltages and bearing currents for induction motor drives," in *Proc. IEEE 34th Annu. Conf. Power Electron. Specialist, 2003. PESC '03.*, 2003, vol. 3, pp. 1127–1132.