Zero-Voltage Switching and Natural Voltage Balancing of a 3 kW 1 MHz Input-Series-Output-Parallel GaN LLC Converter

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ABSTRACT Input-Series-Output-Parallel (ISOP) LLC converters have the capability to leverage lower voltage semiconductor devices, thereby enabling applications with higher voltage requirements. The primary advantages lie in enhanced efficiency and power density attributed to improved device performance. Given the utilization of multiple modular LLC converters, the potential impact of component parameter mismatch becomes a significant concern. Specifically, issues related to input voltage sharing (IVS) and device zero voltage switching (ZVS) are critical considerations. This paper develops a precise mathematical model during deadtime to determine ZVS boundaries, taking into account parameter mismatches. Within the developed boundaries, all LLC sub-modules are assured of ZVS operation. To assess IVS performance, a mathematical model is formulated using the first harmonic approximation (FHA) equivalent circuit. To validate the proposed modeling and analysis, a 3 kW 1 MHz GaN-based ISOP LLC is constructed, comprising four modular 750W-LLC units. Experimental results showcase successful ZVS operations and natural voltage balancing of the ISOP LLC converter across a broad range of parameter mismatches.

INDEX TERMS Input-series-output-parallel, input voltage sharing, LLC resonant converter, zero voltage switching, GaN.

I. INTRODUCTION

Datacenter is one of the major electric loads of our digital world and its usage is rapidly increasing. Without major efficiency improvement, its electricity usage, plus other telecommunication device and personal computers, could reach 51% of worldwide electricity demand by 2030 [1], [2]. All of this equipment shares a common power conversion architecture with a power factor correction (PFC) front end and an isolated 400 V to 48 V DC/DC stage which usually adopts the popular LLC topology due to its high-power efficiency characteristic [3], [4], [5], [6]. 600 V power devices such as Si MOSFET or GaN FET must be used on the primary side. A large transformer turns ratio is also needed leading to complicated transformer design and large winding loss. Besides, the high current stress on the LLC secondary side

requires a number of paralleled devices and a complex gate driving loop design. To solve these issues, input-series-output-parallel (ISOP) LLC can be used. By distributing the power to a number of LLC modules, the ISOP LLC reduces the secondary side current stress in each sub-module. Magnetic design also becomes easier due to the reduced turn ratio of the transformer [7], [8]. A four-module ISOP LLC is shown in Fig. 1. To summarize, it has the following advantages [3], [9], [10], [11]: easier device selection due to more available devices at lower voltage ratings; an increase in the efficiency due to improved device figure of merit (FOM) of lower voltage devices compared to 600 V devices; reduced thermal stress in each sub-module and possibility to include a redundant sub-module; flexibility to expand to different input voltages and power levels.
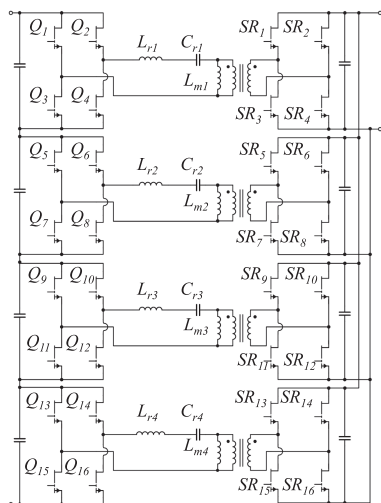
FIGURE 1. Topology of a four-module ISOP LLC.

LLC resonant tank parameter mismatch is inevitable in the ISOP LLC and is a major concern. The mismatch of the magnetizing inductor L_m, the resonant inductor L_r and resonant capacitor C_r between different sub-modules may result in different working conditions for each sub-module. One particular concern is its impact on the zero voltage switching (ZVS). Partially discharged devices not only lower the system efficiency but also increases device thermal stress. A fixed deadtime setting that ensures device ZVS in all sub-modules becomes essential. An LLC equivalent circuit model during the deadtime is a very useful too in understanding and addressing the issue. However, these models are not satisfactory and require major improvements. Some papers treat magnetizing current as a current source charging/discharging the device's output capacitance C_{oss} during the deadtime. A model considering only the primary side device's C_{oss} is applied in [12], [13]. Secondary side device's C_{oss} is neglected in this model due to the large transformer turn ratio. The model is not applicable for ISOP LLC due to the significantly reduced transformer turn ratio in each module. A model taking secondary device's C_{oss} into consideration is proposed in [14], [15]. In the above models, magnetizing current is assumed to be the only part dealing with device C_{oss} during the deadtime. This is not accurate since the device discharging current may not always comes from the magnetizing current alone. Failing to consider this may cause inaccurate deadtime prediction and partial ZVS or hard switching. Improved circuit models are proposed in [16], [17] for a more accurate analysis but only a half-bridge based LLC is analyzed and detailed mathematic analysis is not provided. Therefore, to accurately define the ZVS boundaries of an ISOP LLC, a detailed deadtime circuit model and mathematic analysis are proposed in this paper. With this model, the deadtime and allowable mismatch ranges can be extracted. If a deadtime is within the range, LLC can achieve ZVS in a given parameter mismatch range.

Another concern caused by the parameter mismatch is the input voltage sharing (IVS) among modules. Various papers

investigated this issue but so far the proposed solutions are not optimal. One lossy method is to apply a voltage divider consisting of resistors to each module input [18]. An active voltage divider circuit using operational amplifiers is proposed in [19]. In [20], [21], MOSFET working in linear region is placed in parallel with each ISOP module. These circuits all lead to an extra power loss as well as increased system complexity. Active IVS control is also reported in many literatures. One of the most utilized methods is common duty control [22], [23], which utilizes system natural voltage sharing property. This method requires all modules parameter to be well matched and is hard to achieve in practice. A positive output voltage gradient control is proposed in [8]. The control regulates module output voltage to increase with input voltage and act as positive input impedance. However, system output voltage regulation characteristic is affected. Some papers also proposed IVS close loop control. The controller would sense the input voltage of each module and provides duty ratio adjustment to each module while the main control loop provides the major duty ratio [28]. With sub-module input current as the feedback, IVS based on charge control is proposed in [24]. A current inner loop control is added to the IVS loop in [10], [25] for a better dynamic performance. These methods all require an IVS controller which decreases system reliability and increase the implementation complexity. Sensors are also needed to provide feedback signals. [7] uses an extra Buck converter as a voltage pre-regulator for each LLC module. The two-stage converter not only lowers system efficiency but also increases system cost and volume. To summarize, all reported IVS methods are making the simple and unregulated LLC more complicated. In [9], ISOP LLC natural IVS property is mentioned but no analysis is given. Besides, few methods referenced above are verified in an ISOP LLC. So, another major contribution of this paper is the development of a novel model based on First Harmonic Approximation (FHA) to evaluate the IVS performance of an unregulated ISOP LLC. The voltage sharing performance can be predicted when considering parameter mismatch. Finally, a 3 kW 1 MHz ISOP LLC is developed to verify the ZVS and IVS models. The developed ISOP LLC shows excellent efficiency, power density and natural input voltage balancing property due to its small L_r/L_m ratio and flat voltage gain in a wide frequency range.

The paper is organized as follows. Section II develops the novel circuit model of the LLC during the deadtime. Parameter mismatch range and deadtime boundaries where the designed ISOP LLC achieves ZVS is derived. Section III shows proposed circuit model of a four-module ISOP LLC for IVS evaluation. In Section IV, experimental results are provided to verify the ZVS and IVS performance. Conclusions are included in Section V.

II. PROPOSED DETAILED DEADTIME MODEL AND DESIGN
Simplified waveforms of an LLC converter are given in Fig. 2, with both over-resonant (i.e. switching frequency higher than resonant frequency) and under-resonant (i.e. switching frequency lower than resonant frequency) conditions listed. A
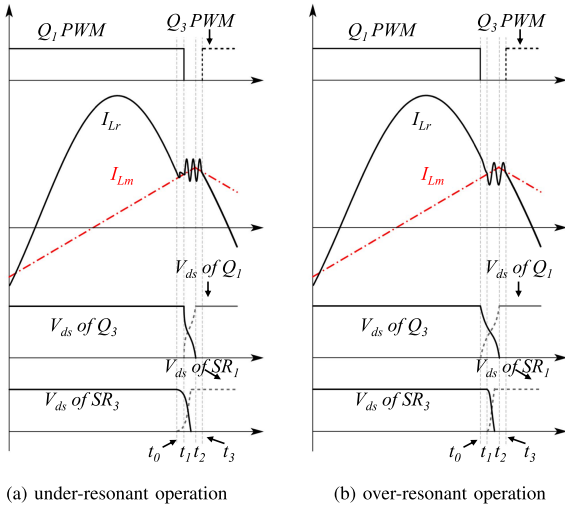
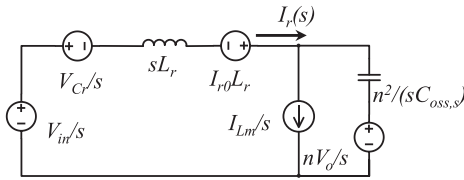FIGURE 2. Simplified waveform of LLC under various conditions.

(a) under-resonant operation (b) over-resonant operation

FIGURE 3. t_0 to t_1 stage LLC under-resonant operation s domain equivalent circuit.
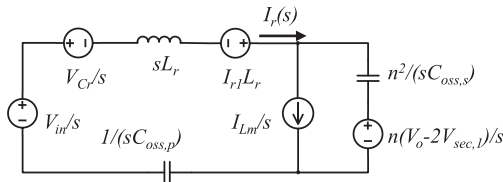

FIGURE 4. t_1 to t_2 stage LLC under-resonant operation s domain equivalent circuit.

pair of primary device gate signal working in complementary with a deadtime is shown together with the resonant current I_{Lr}, magnetizing current I_{Lm} and V_{ds} of primary and secondary devices. During the deadtime, devices are being charged/discharged. The deadtime is further divided into several stages. The models and time duration of each stage are developed. Following assumptions are made in this analysis: 1) Magnetizing current and resonant capacitor voltage remains constant during the deadtime. 2) The C_{oss} of the GaN devices has a constant value. 3) The on-state resistance and reverse conduction voltage drop of the GaN devices are neglected. 4) Other parasitic parameters such as power stage inductance are neglected.

Three s-domain circuit models of the LLC in under-resonant operation condition are developed and given in Figs. 3 to 7.

Stage t_0 to t_1: At t_0, the resonant current equals the magnetizing current and the secondary side current reaches zero.
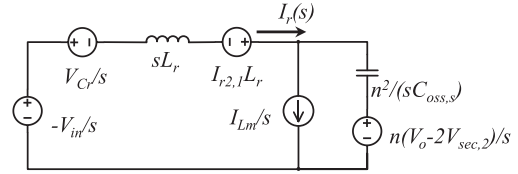

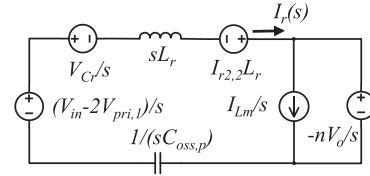FIGURE 5. t_1 to t_2 second stage s domain equivalent circuit, Case 1.

FIGURE 6. t_1 to t_2 second stage s domain equivalent circuit, Case 2.
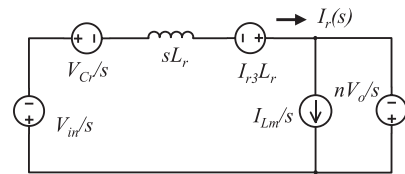

FIGURE 7. t_2 to t_3 stage LLC under-resonant operation s domain equivalent circuit.

Secondary devices are turned off and I_{Lr} starts to oscillate with the resonant tank component and the device C_{oss}. Following equations show the magnetizing current and resonant capacitor voltage value.

$$I_{Lm} = V_{in}/(4L_m f_s) \tag{1}$$

$$V_{Cr} = P_o/(4V_{in}C_r f_s) \tag{2}$$

After solving the model in time domain, the resonant current in this stage is expressed in (3). The time duration of this stage is $\Delta t_1 = (1/f_s - 1/f_r)/2$ [26].

$$I_r(t) = I_{Lm} + \frac{V_{in} - V_{Cr} - nV_o}{n\sqrt{L_r/C_{oss}}} \sin\left(\frac{n}{\sqrt{L_r C_{oss,s}}} t\right) \tag{3}$$

Secondary device V_{ds} is charged to $V_{sec,1}$ at the end of this stage and it can be calculated as:

$$V_{sec,1} = \frac{n}{2C_{oss,s}} \int_0^{\Delta t_1} I_{Lm} - I_r(t)\,dt \tag{4}$$

Stage t_1 to t_2: Primary devices are turned off at t_1. Device C_{oss} will join the resonance with the resonant tank components. Both side device capacitance is charged and discharged at this time. $V_{sec,1}$ becomes the secondary device initial V_{ds} at this stage. I_{r1} is the initial resonant current value and can be figured out by (3). (5) shows the solved time domain resonant current expression.

$$I_r(t) = A_2 + (I_{r1} - A_2)cos(\omega_2 t) + D_2 \sin(\omega_2 t) \tag{5}$$

$$A_2 = \frac{I_{Lm}C_{oss,p}}{C_{oss,p} + n^2 C_{oss,s}} \tag{6}$$

$$D_2 = \frac{V_{in} - V_{Cr} - nV_o + 2nV_{sec,1}}{\omega_2 L_r} \tag{7}$$

$$\omega_2 = 1/\sqrt{L_r \left(C_{oss,p} \parallel n^2 C_{oss,s}\right)} \tag{8}$$

The first part of this stage ends when either primary or secondary devices are fully discharged. As the device discharging speed is effected by various factors like magnetizing inductance, switching frequency, device parameters and system operating conditions, the device that get discharged first various from case to case. The second part of this stage is dived into two cases.

Case 1: The first part of this stage ends at $t_{2,1}$ and primary devices fully discharged prior to secondary devices, with the equivalent circuit given in Fig. 5. The time duration of the first part of this stage can be calculated below and (10) shows the secondary device initial value $V_{sec,2}$ in this case. $I_r(t)$ is expressed in (5).

$$V_{in} = \frac{1}{2C_{oss,p}} \int_0^{t_{2,1}-t_1} I_r(t)\, dt \tag{9}$$

$$V_{sec,2} - V_{sec,1} = \frac{n}{2C_{oss,s}} \int_0^{t_{2,1}-t_1} I_{Lm} - I_r(t)\, dt \tag{10}$$

The time domain equation of the resonant current in this part is given in (11). $I_{r2,1}$ is the resonant current's initial value of Case 1 and it can be calculated using (5).

$$I_r(t) = I_{r2,1} + \frac{-V_{in} - V_{Cr} - nV_o + 2nV_{sec,2}}{\omega_{2,1} L_r} \sin(\omega_{2,1} t) \tag{11}$$

$$\omega_{2,1} = n/\sqrt{L_r C_{oss,s}} \tag{12}$$

This part ends when secondary device is fully discharged. (13) solves the time duration of this situation, where $I_r(t)$ follows expression in (11).

$$V_o - V_{sec,2} = \frac{n}{2C_{oss,s}} \int_0^{t_2-t_{2,1}} I_r(t) - I_{Lm}\, dt \tag{13}$$

Case 2: The first part of this stage ends at $t_{2,2}$ and secondary devices fully discharged first, with the equivalent circuit given in Fig. 6. $V_{pri,1}$ is the primary device partially discharged V_{ds} value. The time duration of first part of this stage can be solved below using the $I_r(t)$ expressed in (5).

$$V_o - V_{sec,1} = \frac{n}{2C_{oss,s}} \int_0^{t_{2,2}-t_1} I_{Lm} - I_r(t)\, dt \tag{14}$$

In this case, secondary device voltage is clamped, and primary device is still being charged and discharged. Time domain equation of the resonant current is given in (15). $I_{r2,2}$ is the resonant current initial value of situation 2 and follows the same calculation method as $I_{r2,1}$.

$$\begin{aligned} I_r(t) = & \ I_{r2,2} \cos(\omega_{2,2} t) \\ & + \frac{V_{in} - 2V_{pri,1} - V_{Cr} + nV_o}{\omega_{2,2} L_r} \sin(\omega_{2,2} t) \end{aligned} \tag{15}$$
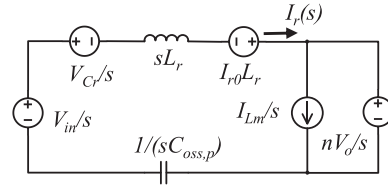

FIGURE 8. t_0 to t_1 stage LLC over-resonant operation s domain equivalent circuit.

$$\omega_{2,2} = 1/\sqrt{L_r C_{oss,p}} \tag{16}$$

This part ends when the primary device is fully discharged. (17) solves the time duration of this situation, where $I_r(t)$ follows expression in (15).

$$V_{in} - V_{pri,1} = \frac{1}{2C_{oss,p}} \int_0^{t_2-t_{2,2}} I_r(t)\, dt \tag{17}$$

Stage t_2 to t_3: Both primary and secondary devices are fully discharged and clamped to the input and output voltages respectively at t_2. Voltage is applied to the resonant inductor. Fig. 7 shows the s domain equivalent circuit model. The stage ends when the resonant current reaches zero, and (18) shows the duration of this stage.

$$t_3 - t_2 = \frac{I_{r3} L_r}{V_{in} + V_{Cr} - nV_o} \tag{18}$$

Circuit models of LLC in over-resonant operation is similar to the under-resonant one. The major difference occurs in the first stage. A simplified description is given.

Stage t_0 to t_1: Fig. 8 shows the s-domain equivalent circuit in this case. Primary devices are turned off at t_0. Since resonant current is still larger than magnetizing current, the secondary devices are conducting at this moment. This current also charges/discharges the primary C_{oss}. The initial resonant current I_{r0} is given in (19), [27].

$$I_{r0} = \frac{-nV_o}{\sqrt{L_r/C_r}} \left(\frac{\pi f_r L_r nV_o}{2 f_s L_M V_{in}} + \left(\frac{nV_o}{V_{in}} - \frac{V_{in}}{nV_o} \right) \tan\left(\frac{\pi f_r}{2 f_s} \right) \right) \tag{19}$$

The time duration of this stage is Δt_1 and it can be solved by (20). The system equations during other stages can follow the same analysis of the under-resonant case.

$$I_{Lm} = I_{r0} \cos(\omega_1 \Delta t_1) + \frac{V_{in} - V_{Cr} - nV_o}{\omega_1 L_r} \sin(\omega_1 \Delta t_1) \tag{20}$$

Stage t_1 to t_2: Unlike under-resonant operation, the primary device is partially discharged at the initial of this stage. The resonant current expression is the same as (5), with D_2 changed to:

$$D_2 = \frac{V_{in} - V_{Cr} - nV_o - 2nV_{pri,1}}{\omega_2 L_r} \tag{21}$$

Like the second stage of under-resonant operation, this stage is also divided into two stages.

Case 1: In this case, primary devices are fully discharged first. The resonant current and frequency formula is the same
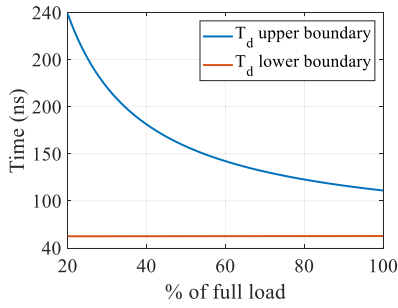
FIGURE 9. Deadtime boundary for an LLC module under various loads @ $L_r = 50$ nH, $L_m = 5\mu$H, $C_r = 500$ nF, $f_s = 1$ MHz.

FIGURE 10. Overlap region of primary deadtime boundaries under ±10% mismatch of L_m, L_r and C_r and various loads.

from (11) to (13). The difference lies in the time duration of the stage and the secondary device initial voltage $V_{sec,2}$.

$$V_{in} - V_{pri,1} = \frac{1}{2C_{oss,p}} \int_0^{t_{2,1}} I_r(t)\, dt \qquad (22)$$

$$V_{sec,2} = \frac{n}{2C_{oss,s}} \int_0^{t_{2,1}} I_{Lm} - I_r(t)\, dt \qquad (23)$$

Case 2: Secondary devices are fully discharged first under this situation. Like in under-resonant operation, this stage ends when both side devices achieves fully discharge. Time duration of first part of this stage is calculated as:

$$V_o = \frac{n}{2C_{oss,s}} \int_0^{t_{2,2}} I_{Lm} - I_r(t)\, dt \qquad (24)$$

Primary device is still being charged and discharged. Time domain equation of the resonant current is similar as (15), where $V_{pri,1}$ to be replaced by $V_{pri,2}$, which can be solved by following equation.

$$V_{pri,2} - V_{pri,1} = \frac{1}{2C_{oss,p}} \int_0^{t_{2,2}} I_r(t)\, dt \qquad (25)$$

Equation to solve the time duration of this stage is given in (26).

$$V_{in} - V_{pri,2} = \frac{1}{2C_{oss,p}} \int_0^{t_2 - t_{2,2}} I_r(t)\, dt \qquad (26)$$

Stage t_2 to t_3: The system operation at over-resonant is the same as the under-resonant one during this stage and share the same equations.

The developed model helps to calculate ZVS deadtime needed under various C_r, L_r and L_m parameter mismatch conditions. The model is applied to the designed 400 V 3 kW ISOP LLC. Since there are 4 LLC modules inside the converter, each individual LLC module is designed with the following nominal parameters: $V_{in} = 100$ V, $V_{out} = 48$ V, $P = 750$ W, $L_r = 50$ nH, $L_m = 5$ μH, $C_r = 500$ nF, $f_s = 1$ MHz, EPC2033 and EPC2029 GaN FET as primary and secondary devices respectively. Fig. 9 shows the solved deadtime boundaries under various load condition. The lower boundary represents the deadtime needed to achieve exact primary device ZVS. The upper boundary is the time for the resonant current to reach zero after full ZVS for all devices.
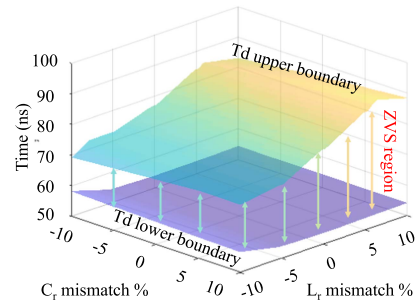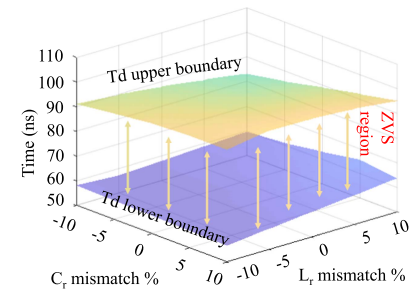

FIGURE 11. Overlap region of secondary deadtime boundaries under ±10% mismatch of L_m, L_r and C_r and various loads.
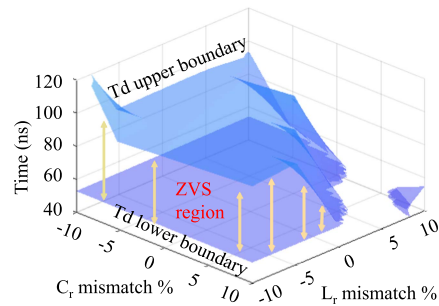

FIGURE 12. Overlap region of primary deadtime boundaries under ±10% mismatch of L_m, L_r and C_r and $L_r = 200$ nH.

Different resonant tank parameter mismatch or load leads to different deadtime boundaries. So the deadtime to guarantee ZVS under all these conditions lies in the overlapped region of the boundaries. To obtain this region, L_m, L_r and C_r mismatches are all taken into consideration during the analysis. It is identified that there is an overlapped deadtime region over the whole load range if the parameter mismatch range is reduced to 10%. Results are summarized in Figs. 10 and 11, with mismatches from L_m, L_r and C_r all taken into consideration. Based on them, the designed ISOP LLC can guarantee ZVS with a single deadtime setting for all modules.

Fig. 12 shows the overlapped primary deadtime region for the designed LLC with an increased L_r value of 200 nH and the same resonant frequency. No deadtime region is found for all devices with 10% parameter mismatch. Here are the explanations. The energy to discharge device C_{oss} comes from
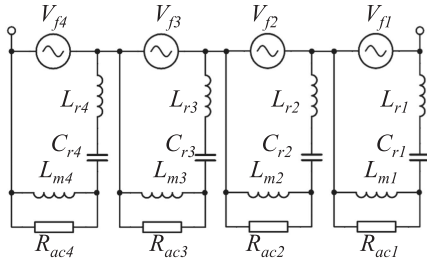
FIGURE 13. FHA equivalent circuit of a four-module ISOP LLC.

FIGURE 14. Voltage difference between module 1 and 2 only considering C_{r2} parameter mismatch.

the energy in system inductor. The energy is dominated by L_m if L_r is small enough. The deadtime for all device ZVS considering parameter mismatch is also easy to find since only L_m provides with ZVS energy. With L_r value increasing, its energy and influence on the circuit during the deadtime becomes ineligible. Device ZVS depends on two energy storage components and their parameter mismatch makes the situation more complex. The deadtime boundaries for all device ZVS may be found with a reduced mismatch range. To ensure all devices to achieve ZVS at a single deadtime and reasonable parameter mismatch, a small L_r value is desirable in the ISOP LLC for a given resonant frequency.

III. MODELLING AND ANALYSIS OF VOLTAGE SHARING PROPERTY OF THE ISOP LLC SYSTEM

The FHA equivalent circuit of a four-module ISOP LLC is given in Fig. 13. Since all LLC sub-modules share the same gate signals, they have the same fundamental frequency (switching frequency). Each LLC module has its own resonant tank parameters L_{rx}, C_{rx} and L_{mx} and their output voltage are the same. The R_{acx} in the figure is the equivalent AC load resistance of the x_{th} module reflected to the primary side. The voltage gain of each LLC module is determined by its own module parameter and has no relationship with their input DC capacitors. Assuming the voltage gain of the x_{th} LLC module is M_x and its input voltage is V_{inx}, following relationship can be derived.

$$\frac{V_{in1}M_1}{n} = \frac{V_{in2}M_2}{n} = \frac{V_{in3}M_3}{n} = \frac{V_{in4}M_4}{n} = V_{out} \quad (27)$$

Based on above equations, the ratio d_{th} of the x_{th} LLC module input voltage over the total system input voltage is given in (28), where x ranges from 1 to 4. The equation means that the LLC sub-module input voltage difference is a result of the LLC modules' voltage gain difference. On the other hand, the voltage gain is affected by the resonant tank parameters.

$$d_x = \frac{\frac{1}{M_x}}{\frac{1}{M_1} + \frac{1}{M_2} + \frac{1}{M_3} + \frac{1}{M_4}} \quad (28)$$

Taking the component value in LLC module 1 as the nominal value, the resonant tank component value of the four
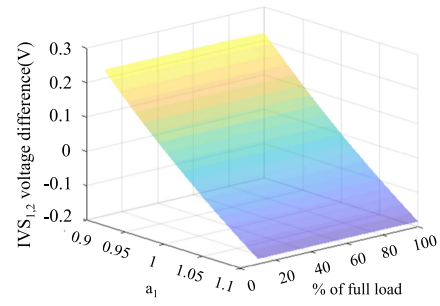
modules are given below.

$$\begin{cases} C_{r1} = C_r, \ C_{r2} = a_1 C_r, \ C_{r3} = a_2 C_r, \ C_{r4} = a_3 C_r, \\ L_{r1} = L_r, \ L_{r2} = b_1 L_r, \ L_{r3} = b_2 L_r, \ L_{r4} = b_3 L_r, \\ L_{m1} = L_m, \ L_{m2} = e_1 L_m, \ L_{m3} = e_2 L_m, \ L_{m4} = e_3 L_m \end{cases} \quad (29)$$

where parameters $a_1 \sim a_3$, $b_1 \sim b_3$ and $e_1 \sim e_3$ represent the variations of each resonant tank component value.

During the steady state operation of the ISOP LLC, the input average current of each module is the same due to the series connection. The average current flowing through the input DC capacitor equals to zero. Therefore, the average current flowing through the resonant tank of each module also equals. Since the modules output are connected in parallel, the output voltage also maintains the same. It is then easy to get the conclusion that the impedance magnitude of L_m and R_{ac} in parallel of each LLC module is the same. Considering the parameter mismatch effect, (30) to (32) can be obtained. The equivalent load of each LLC module can be solved. LLC module voltage gain and the IVS difference between modules can then be obtained.

$$| R_{ac1} // X_{Lm1} | = \cdots = | R_{ac4} // X_{Lm4} | \quad (30)$$

$$R_{acx} = \frac{\omega L_m}{\sqrt{\frac{\omega^2 L_m^2}{R_{ac1}^2} + 1 - \frac{1}{e_x^2}}}, \ (x = 2, 3, 4) \quad (31)$$

$$\frac{1}{R_{ac}} = \frac{1}{R_{ac1}} + \frac{1}{R_{ac2}} + \frac{1}{R_{ac3}} + \frac{1}{R_{ac4}} \quad (32)$$

To illustrate the IVS of the designed four-module ISOP LLC converter considering parameter mismatch, the voltage difference between LLC module 1 and 2 is calculated. Voltage difference between them is shown in Figs. 14 to 16. In the plots, only the parameter mismatch of one component in LLC module 2 is considered. The component value in the tank is also assumed to have a 10% tolerances. The load conditions are shown on the y-axis. The voltage difference between the two LLC modules is given on z-axis. The voltage difference increases with the L_{r2} or C_{r2} deviating from its nominal value, but the difference is very small within the investigated range. The influence of L_m mismatch or load conditions on ISOP
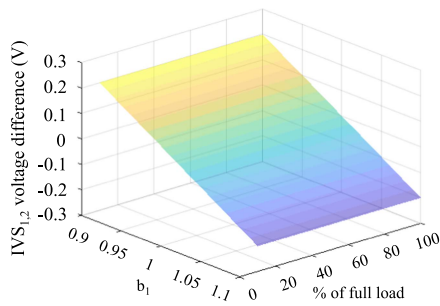
FIGURE 15. Voltage difference between module 1 and 2 only considering L_{r2} parameter mismatch.
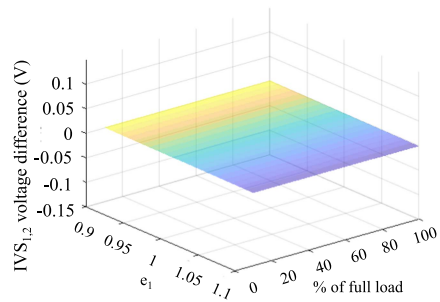

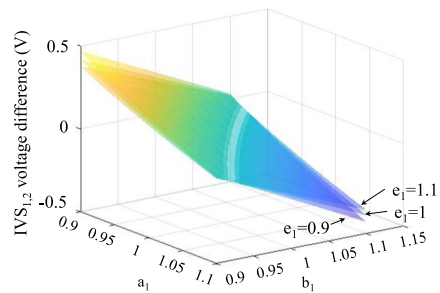**FIGURE 16. Voltage difference between module 1 and 2 only considering L_{m2} parameter mismatch.**

FIGURE 17. Voltage difference between module 1 and 2 under full load and various mismatch conditions.

FIGURE 18. Voltage gain curve of an LLC under various L_r.
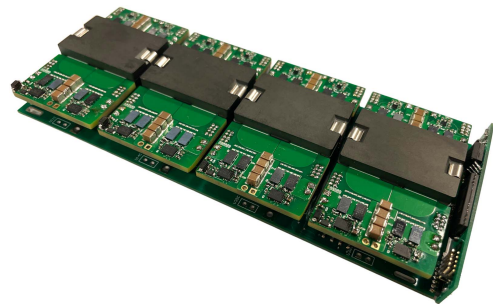
FIGURE 19. Designed four-module ISOP LLC converter.

LLC IVS is negligible in this LLC according to the plots. The IVS difference in two modules caused by parameter mismatch in a third module can also be figured out by above analysis. The conclusion is that the IVS difference between two LLC modules is not affected by parameter mismatch in another module of the ISOP LLC.

The IVS difference caused by parameter mismatch between the two modules under full load is given in Fig. 17. The most positive voltage difference would occur at $a_1 = 0.9$, $b_1 = 0.9$ and $L_m = 0.9$. The most negative voltage difference would occur at $a_1 = 1.1$, $b_1 = 1.1$ and $L_m = 0.9$. The IVS worst case and the corresponding parameter mismatch is derived. The largest voltage sharing difference of the designed ISOP LLC occurs when one LLC module has a $90\%C_r$, $90\%L_r$, $90\%L_m$ and one module has a $110\%C_r$, $110\%L_r$ and $90\%L_m$. From the plot, the maximum IVS difference in the designed LLC is around 1 V or 1% since the nominal value of the input voltage
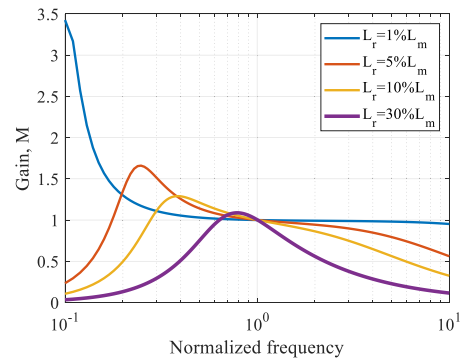
is 100 V. Therefore, the developed ISOP LLC demonstrates excellent natural voltage balancing performance.

The above analysis can also be used to design ISOP LLC for good IVS capability. Once a resonant frequency is determined, the value of L_r or C_r can change. To achieving better IVS, smaller L_r is preferred. Assuming an LLC converter with a resonant frequency of 1 MHz and an L_m of 5 μH, Fig. 18 shows the voltage gain curve of the LLC with varying L_r. A smaller L_r/L_m leads to a flatter voltage gain over a wider frequency range, which would lead to less voltage gain deviation when parameter mismatch exists.

IV. EXPERIMENTAL VERIFICATION

A 3 kW 1 MHz GaN based four-module ISOP LLC converter is designed to verify above analysis and conclusions. The converter prototype is shown in Fig. 19 and its detailed specification is summarized in Table 1. 150V-rating EPC2033 and 80V-rating EPC2029 are used as primary and secondary side devices for each LLC module. The converter achieves a peak efficiency of around 98.8% as Fig. 20 shows, which proves the benefits of applying low voltage-rating GaN devices and ISOP topology to data-center power supply applications. The rated input voltage for each LLC module is 100 V and rate full power for each LLC module is 750 W. A deadtime of 70 *ns* is selected for the ISOP LLC primary side and 70 *ns* is selected for the secondary side.

To evaluate the proposed deadtime model, the LLC module with various parameter mismatch is tested. Due the difficulty

TABLE 1 ISOP LLC System Specification

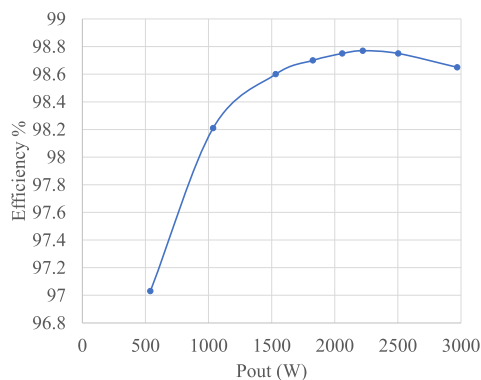| Parameters	Parameter value
Input voltage	400V
Output voltage	48V
L_m	$5\mu H$
L_r	50nH
C_r	500nF
f_s	1MHz
P_{full}	3kW
Primary device	EPC2033
Secondary device	EPC2029

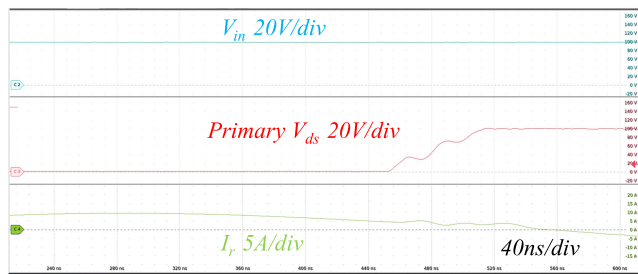**FIGURE 20.** Measured efficiency of the designed converter.

FIGURE 21. LLC deadtime waveform with -10% C_r, $+1\%$ L_r and $+8\%$ L_m mismatch.

of measuring L_r, their values are estimated based on magnetic simulation. Testing waveforms are shown in Figs. 21 and 22. Fig. 23 is the tested device V_{ds} derived from the oscilloscope. And Fig. 24 shows the calculated V_{ds} from the proposed model. The voltage waveform shows excellent match and verifies the accuracy of proposed model.

Using the components value in LLC module 2 as the nominal value, the parameter mismatch for each modules are given in Table 2. With each LLC module set to operate at 1 MHz, the obtained waveform of the ISOP LLC working at different load conditions is given Figs. 25 and 26. The input voltage of each LLC module is measured at each module's input filter capacitor by 200 MHz THDP0200 differential probes from Tektronix. The detailed input voltage value of each LLC is displayed by Tektronix MSO58 oscilloscope. The resonant
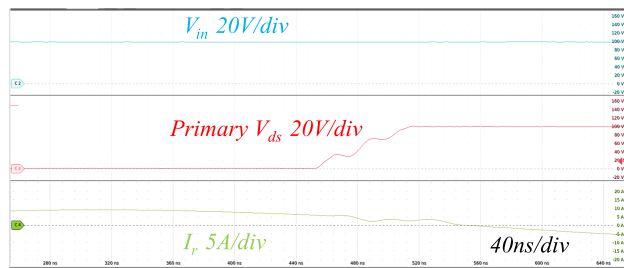
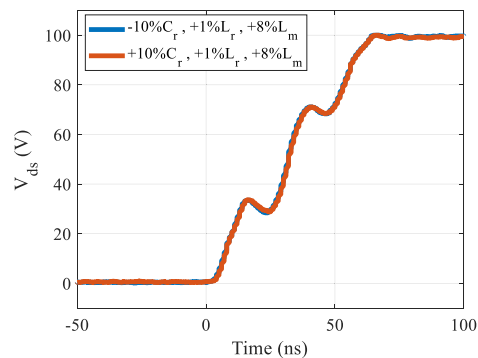**FIGURE 22.** LLC deadtime waveform with $+10\%$ C_r, $+1\%$ L_r and $+8\%$ L_m mismatch.

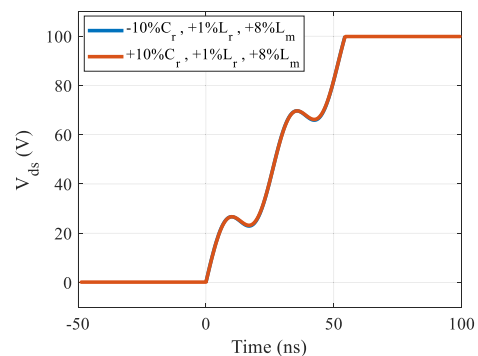**FIGURE 23.** Tested device V_{ds} under various conditions.

FIGURE 24. Modeled device V_{ds} under various conditions.

TABLE 2 Parameter Mismatch of Each LLC Module

LLC Module No.	C_r mismatch	L_r mismatch	L_m mismatch
No.1	-10%	-3%	-10%
No.2	0%	0%	0%
No.3	-3%	$+1\%$	$+4\%$
No.4	$+10\%$	$+2\%$	$+10\%$

current of one module is also given in the figures. The IVS performance matches the expectations from the proposed model and analysis. The IVS change due to load change is quite small and this also matches the analysis very well.

The system waveform during a load transient is given in Figs. 27 and 28. The system output current is plotted when switched between 10 A and 20 A. From the testing waveform,
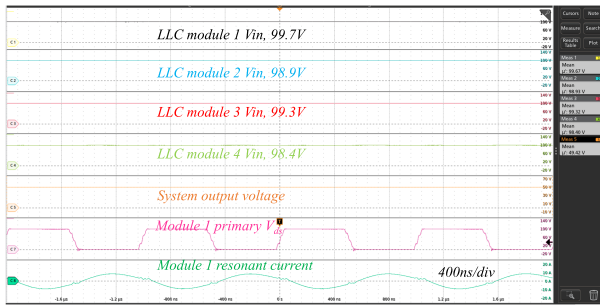
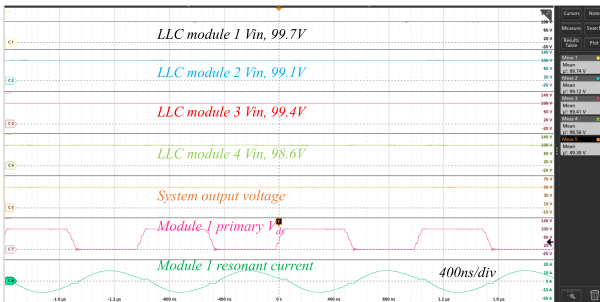**FIGURE 25.** Waveform of the ISOP LLC with 2 kW load.

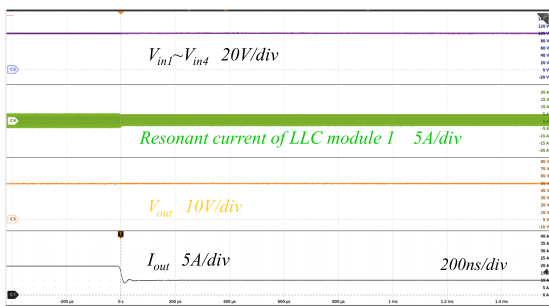**FIGURE 26.** Waveform of the ISOP LLC with 3 kW load.

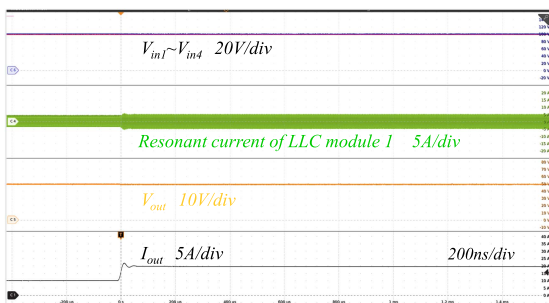**FIGURE 27.** LLC waveform with load change from 20 A to 10 A.

FIGURE 28. LLC waveform with load change from 10 A to 20 A.

one can see that the input voltage of each LLC module does not encounter obvious IVS unbalance. The designed ISOP LLC achieves excellent IVS performance even during the load transient condition. Fig. 29 shows the testing waveform during the ISOP LLC startup process. With the input voltage slowly ramping up to the rated full voltage value, the input voltage of
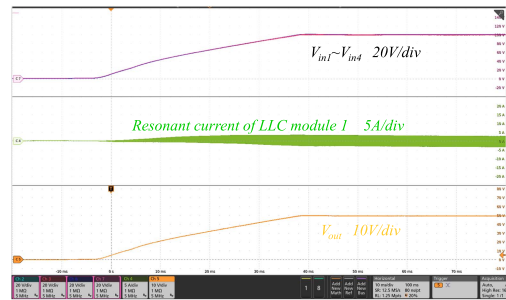

FIGURE 29. Startup waveform of the ISOP LLC.

each individual LLC module also increases. The figure proves that the ISOP LLC also achieves perfect IVS performance during the startup transient condition.

V. CONCLUSION

A comprehensive study of the ZVS and IVS performance of the ISOP LLC with resonant tank parameter mismatch is presented in this paper. An accurate LLC deadtime equivalent circuit model is proposed to analyze the LLC time domain behavior during the deadtime. The model provides an analytical V_{ds} equation. Based on this model, the LLC deadtime boundaries under various load and parameter mismatch conditions can be calculated. Parameter mismatch of less than 10% is needed to guarantee an overlapping boundary hence a fixed deadtime can be used for all ISOP modules. A small value of L_r is also preferred to find this fixed deadtime.

A novel ISOP LLC analytical model based on FHA equivalent circuit is further developed to enable quick and easy input voltage sharing study. The resonant tank parameter mismatch is then investigated. Based on the analysis, large L_r/L_m ratio would cause severe voltage sharing problems and a small L_r/L_m ratio is preferred to achieve good IVS performance. This conclusion can also be verified by LLC gain plot. LLC with small L_r/L_m demonstrates a flatter gain near resonant point and its value does not deviate much from unity considering parameter mismatch. L_m mismatch or load condition has very little effect on the IVS. The worst-case IVS performance due to parameter mismatch is also identified. Finally, the analysis is verified on a 3 kW 1 MHz GaN ISOP LLC. The ISOP LLC achieves very high efficiency of 98.8% with ZVS with an optimal fixed deadtime setting. Excellent natural IVS property is also demonstrated under various operating conditions include load transient. The maximum voltage sharing difference observed is less than 2 V under all conditions.

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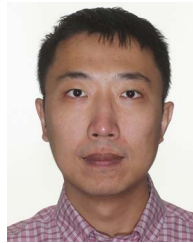
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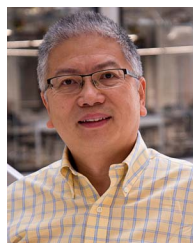
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