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A General Analytical Formulation for LCL Filter Design for Grid-Connected PWM-Driven Cascaded H-Bridge Inverters

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ABSTRACT This paper proposes a general analytical formulation for LCL filter design for grid-connected PWM-driven cascaded H-bridge inverters. The novelty of this work deals with providing some easy-of-use analytical expressions that allow for properly sizing the filter inductances and capacitance values considering the number of voltage levels, the DC-link voltage, the adopted multicarrier pulse width modulation strategy, and the switching frequency. Although multilevel inverters performance strongly depends on the adopted modulation strategy and switching frequency, a general mathematical formulation that allows for properly sizing the LCL filter by considering such parameters simultaneously is currently missing. The proposed approach is generalized for the most adopted multicarrier pulse width modulation strategies. To validate the proposed approach, an extended investigation analysis is performed by hardware-in-the-loop real-time tests. According to international standards EN50160 and IEEE Std 1547–2018, the voltage total harmonic distortion and current total rated distortion are adopted to evaluate the LCL filter performance. Tests are carried out in several working conditions, defined in terms of provided apparent power and power factor values. Finally, the proposed analytical formulation is adopted to formulate an optimized LCL filter design algorithm that allows for matching the standard requirements without oversizing the filter parameters.

INDEX TERMS Cascaded H-bridge multilevel inverter (CHBMI), multilevel inverters, LCL filter, power quality, multi-carrier pulse width modulation (MC-PWM), passive damping.

I. INTRODUCTION

Nowadays renewable energy source plants are a valuable solution to reduce energy production from traditional polluting power plants and contribute to achieving the power system decarbonization goal [1], [2]. Cascaded H-Bridge Multilevel Inverter (CHBMI) represents the preferred Multilevel Inverters (MI) topology in grid-connected applications, due to its modularity, scalability, fault-tolerant capability, and low Electro-Magnetic Interferences (EMIs) [3], [4], [5], [6]. Compared to other MI topologies, CHBMI requires separated DC sources: such a feature can represent a drawback in several applications since a multi-output isolated transformer is required; however CHBMI represents the first choice in applications where isolated DC sources are intrinsically available, such as in photovoltaic applications [7], [8], [9], [10]. MIs performance strongly depends on the adopted modulation strategy [11], [12]. The most employed modulation strategies for MIs are the MultiCarrier Pulse Width Modulations (MC-PWMs). They represent the direct evolution of traditional PWM strategy and share the implementation simplicity and low computational cost. The MC-PWM effect in the frequency domain deals with the subdivision of voltage harmonics in subgroups, centered around specific multiples of the switching frequency, generally, located in the high-frequency range [13], [14], [15], [16]. Thus, to fulfill the voltage and current standards requirements, reported in [17] and [18], and, at the same time, to maintain high-efficiency operation and

reduced power system cost, the adoption of proper switching frequency value and grid-filter sizing assumes a vital role.

The most commonly adopted filter topology in grid-connected applications is the LCL filter since it can provide good filtering performance without oversizing the inductances, compared to the L or LC filter topologies [19]. The third-order LCL filter design requires the adoption of damping methods, to avoid resonance issues. They can be classified as passive and active: the former consists in modifying the filter structure, for example by adding a resistor in series with the capacitor; the latter requires controller parameters or controller structure modifications. Although passive damping methods reduce the overall efficiency due to extra losses related to additional passive components, they are easier to implement. Active damping methods do not have associated losses despite they require additional control solutions such as digital filters [20].

For filter design purposes, the adoption of MIs implies the inclusion of other parameters, in addition to the switching frequency. Such parameters include the number of phase voltage levels and the adopted MC-PWM strategy. As a consequence, the higher number of available parameters makes the design of the LCL filter a challenging task. At the same time, appropriate management of these parameters can lead to meeting several conflicting design goals, i.e., high system efficiency, low voltage and current harmonic content, low filter weight, bulk, and cost.

Several methods for the LCL filter design have been developed into the scientific literature; one of the most commonly adopted is based on current ripple calculation. Authors of [21] propose a resonant-frequency-based LCL filter design for a single-phase H-Bridge Inverter, taking into account the core magnetic permeability and the inductive line impedance. An LCL filter design method for a Power Factor Correction (PFC) application is proposed in [22]. This method relies on inverter current ripple calculation and it is carried out for traditional Two-Level Voltage Source Inverters (2L-VSI). In [23], an LCL filter design method, which includes inductor core and winding design specifically related to aerospace applications, is discussed. In [24], an LCL filter design method is proposed for a three-phase active rectifier and it is based on frequency domain current ripple calculation. This method implies setting constraints on several quantities and it does not provide easy-to-use formulas for LCL filter parameters design.

As can be seen, most of the design methods proposed in the literature deal with traditional 2L-VSIs, and only a few papers consider MIs. In [25], an LCL filter design method for the Neutral Point Clamped (NPC) multilevel inverter topology is proposed and it is based on current ripple calculation and constraints. This work is focused on low switching frequency applications and considers only the asymmetrical regular sampled (ASR) sine-triangle PWM with phase disposition carriers and one-sixth third-harmonic injection. In [26], another LCL filter design method for a three-level NPC is proposed. In detail, only the space vector modulation is considered in the filter design. Moreover, several passive damping solutions are examined. In [27], two LCL filter design methods, based on the allowed current ripple and on an iterative design algorithm for CHBMIs are presented and discussed, respectively. The study is performed in the simulation environment but only PS-PWM modulation is considered for a fixed value of switching frequency. In [28], an LCL filter design method for a single-phase CHBMI topology is proposed: the proposed method takes into account the current ripple, however, it is specifically designed for only one MC-PWM strategy, i.e., the PS-PWM strategy and a generalization for other MC-PWM strategies is missing. Moreover, such a method does not consider the PS-PWM features in the capacitor design of the LCL filter, such as its voltage harmonics shifting over the spectrum, resulting in oversizing the capacitor. An LCL filter optimization design procedure with a mathematical model, based on a heuristic approach, is proposed in [29]. The procedure is valid for any MI topology and any number of voltage levels. In detail, the LCL filter design procedure is synthesized as an optimization problem, and a genetic algorithm is applied to find the best solution in terms of inverter total harmonic distortion and energy losses. The approach has been applied to CHBMIs but only the Phase Disposition (PD) PWM scheme is considered and it is computationally complex. A current control design procedure of a single-phase grid-tied five-level packed Ucell inverter (PUC5) with an LCL output filter is presented and discussed in [30]. The filter performance is evaluated at unity PF operation but, again, only PD modulation is taken into account. In [31], the authors discuss the LCL filter design for a CHBMLI-based Distribution Static Compensator (DSTATCOM) system by considering the switching frequency, modulation index, and filter requirements of a DSTATCOM system. Although the study considers several load conditions, the power quality performance, and the effect of system parameters, it is performed in a simulation environment and considers only the PS-PWM modulation technique.

The literature review shows that only a few papers take into account the CHBMI topology; moreover, almost every discussed work takes into account at most one MC-PWM strategy, and attention is not paid at all in generalizing the design method in terms of adopted MC-PWM strategy, number of inverter voltage levels, and switching frequency. Last but not least, attention must be paid to the coordination between the designed filter and the PI tuning process. Indeed, PI parameters strongly depend both on the previously designed filter, which affects the integral constant, and the adopted MC-PWM strategy, which affects the control action application delay, and the system resonance frequency, leading to stability issues.

This paper aims to provide an LCL filter design general analytical formulation for grid-connected CHBMI controlled with several MC-PWM strategies. The key novelty of this work deals with providing some simple and easy-to-use analytical expressions that allow for considering the number of inverter voltage levels, the DC-link voltage, the commonly

adopted MC-PWM strategy, and the switching frequency all at once. The goal of the proposed analytical formulation is to maximize the system steady-state performance in terms of harmonic distortion without oversizing the filter. Moreover, the paper focuses on the PI-tuning process, providing a generalized procedure that allows for setting the appropriate current control bandwidth as a function of the MC-PWM strategy and switching frequency.

The dependency on the adopted MC-PWM strategy, both for LCL filter design and PI tuning purposes, is explicated through a simple parameter. It allows for updating the filter values and the PI parameters depending on the harmonic shift over the spectrum.

For validation purposes, several tests have been carried out on the Hardware-In-the-Loop (HIL) environment where three-phase Five-level (3P-5L) CHBMI, LCL filter, and grid models were implemented on Typhoon HIL 404, considering different working points in terms of injected apparent power and power factor. The results of voltage and current harmonics have been investigated and compared to voltages and current standards limitations reported in the EN50160 and the IEEE Std 1547–2018, respectively [17], [18]. According to the standards, voltage and current spectra, the voltage Total Harmonic Distortion (THD), and current Total Rated Distortion (TRD) have been adopted as analysis tools. Moreover, a further analysis was carried out to find the set of design parameters that allows to match the standard limitations without oversizing the filter.

It must be underlined that the proposed general analytical formulation depends on DC-link voltage, the adopted MC-PWM strategy, and the switching frequency. However, since MC-PWM strategies can be applied to any MI topology, it follows that the proposed general analytical formulation can be applied to any MI topology, including conventional single DC source (e.g., Neutral Point Clamped (NPC), Flying Capacitor (FC) and Modular Multilevel converter (MMC)) and multiple DC sources (e.g., CHBMI). Moreover, the formulation can also be applied to innovative reduced switch count topologies (e.g., T-type inverters and multilevel modules). Therefore, it is possible to summarize the main scientific advancements presented in this work as follows:

- the proposed analytical design method is generalized for all MC-PWM schemes and any MI topology;
- the generalization considers the number of voltage levels, the switching frequency, the DC-link voltage, and the modulation scheme, thanks to the introduction of the proper coefficient;
- generalization of the PI tuning process considering the impact of the MC-PWM scheme in the bandwidth of the current loop control, allowing for coordination between the designed LCL filter and the PI tuning parameters;
- the proposed approach has been validated considering the voltages and current standards limitations EN50160 and the IEEE Std 1547–2018;
- the proposed approach is optimized to avoid filter oversizing.

This paper is structured as follows: Section II reports a brief review of the adopted MC-PWM strategies; Section III describes the proposed analytical approach for the LCL filter design; Section IV presents some details related to the control strategy, PI tuning, control system stability, and test bench; Section V presents and discusses the HIL results and provides optimal LCL filter design guidelines. Finally, Section VI summarizes the conclusions. The important abbreviations used throughout the paper are listed in Table 1.

II. OVERVIEW OF MULTICARRIER PULSE WIDTH MODULATION

In this section, a brief review of the MC-PWM strategies adopted in this work and a focus on the switching frequency is carried out. Such a review is preliminary to the proposed filter design method.

To clarify the impact of the MC-PWM strategies in the filter design, the virtual switching frequency f_h is defined to support the proposed work. In detail, f_h represents the frequency value where the first group of harmonics is centered in the frequency domain. Indeed, in the following section f_h has been mathematically defined for each MC-PWM scheme. Generally, the number of carriers n_c is related to the number of phase voltage levels n_l according to the following expression (1):

$$n_c = n_l - 1. \tag{1}$$

MC-PWM can be classified in LS and PS depending on the carriers peak-to-peak amplitude, and mutual amplitude and phase shift [32], [33], [34]. It is important to note that LS and PS schemes have different effects on voltage harmonic response and converter efficiency, as discussed in [35].

Concerning the LS-PWM, carriers are characterized by the same peak-to-peak amplitude and they are mutually amplitude-shifted.

According to [14], LS-PWM strategies can be classified into Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition (APOD). They present the same harmonic distribution in the frequency domain, i.e., voltage harmonics are centered around the switching frequency and its integer multiples. The first group of voltage harmonics is centered around the switching frequency f_{sw}, according to the following relation:

$$f_h = f_{sw} \tag{2}$$

It must be underlined that the distribution of harmonics in the frequency domain does not depend on the number of inverter voltage levels. Since all LS-PWM strategies exhibit the same behavior in terms of harmonic shift over the spectrum, it is reasonable to assume that, for fixed switching frequency, all LS-PWM strategies require the same LCL filter. Thus, only PD (Fig. 1(a)) is considered for further discussions, since it guarantees the lowest THD among all LS-PWM strategies, especially with a reduced amplitude modulation index [14].

PS-PWM, shown in Fig. 1(c), is characterized by carriers with the same average value equal to zero, the same peak amplitude, and a mutual phase shift φ_i which depends on the

TABLE 1. List of Important Abbreviations Used Throughout The Paper in Alphabetical Order

Abbreviation	Definition	Abbreviation	Definition
APOD	Alternative Phase Opposition Disposition	POD	Phase Opposition Disposition
CHBMI	Cascaded H-Bridge Multilevel Inverter	PFC	Power Factor Correction
DP	Design Parameter	PS	Phase Shifted
EMI	Electro Magnetic Interference	PWM	Pulse Width Modulation
FPGA	Field Programmable Gate Array	S	Sinusoidal
HIL	Hardware-In-the-Loop	SCA	Suppressed Carrier Arrangement
LS	Level Shifted	SOM	System on Module
MC	Multicarrier	STATCOM	Static Compensator
MI	Multilevel Inverters	THD	Total Harmonic Distortion
NPC	Neutral Point Clamped	TRD	Total Rated Distortion
PED	Power Electronics and Drive	VSI	Voltage Source Inverter
PD	Phase Disposition	VOC	Voltage Oriented Control

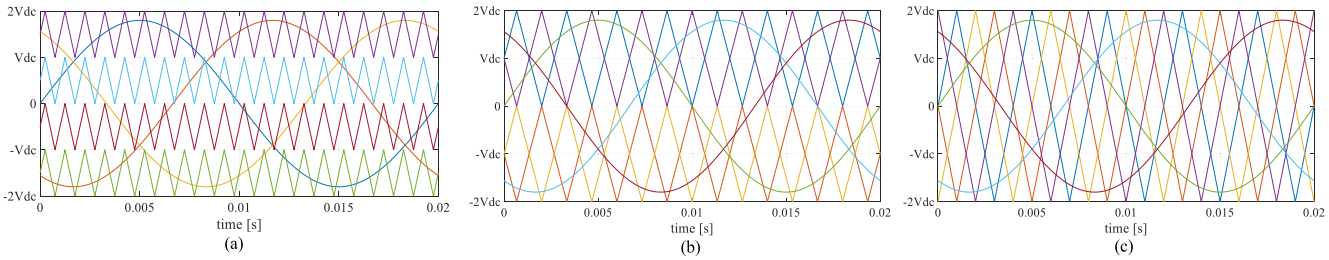

FIGURE 1. MC-PWM schemes: (a) SPD-PWM; (b) SSCA-PWM and (c) SPS-PWM.

number of cascaded H-bridges per phase, according to (3):

$$\varphi_i = \frac{(i-1)\cdot 180}{N} \tag{3}$$

where i is the *ith* H-Bridge module considered. The voltage harmonics are centered around multiples of the switching frequency as a function of the number of the voltage levels n_l. In detail, the first group of voltage harmonics is centered around the virtual frequency f_h according to (4):

$$f_h = (n_l - 1)\cdot f_{sw} \tag{4}$$

Thus, the voltage harmonics, generated by PS-PWM are centered at frequency f_h and its integer multiplies. It should be noted that PS allows for obtaining a shifting effect on the voltage harmonics depending on the number of voltage levels in comparison to LS-PWM strategies.

According to [35], Suppressed Carrier Arrangement (SCA) modulation is a hybrid scheme between LS and PS, as shown in Fig. 1(b). SCA-PWM is characterized by stacked couples of carriers that have the same peak-to-peak amplitude and a mutual phase shift equal to 180°. It determines voltage harmonics centered around multiples of two-time the switching frequency and the first group of harmonics are centered at f_h according to (5):

$$f_h = 2f_{sw} \tag{5}$$

Similarly to the LS-PWM schemes, the harmonics distribution in the frequency domain does not depend on the number of converter levels.

In conclusion, each MC-PWM strategy displaces harmonics over the spectrum differently, depending on the carriers level and phase shift. Such a behavior in the frequency domain is correlated to a different number of the CHBMI state transitions in the time domain, for a fixed carriers switching frequency. Thus, the virtual switching frequency f_h indicates the effective number of CHBMI state transitions and is linked to the switching frequency according to relations (2), (4), and (5).

III. LCL FILTER DESIGN

In this section, the LCL filter design is discussed. The proposed method aims to define a general formulation for evaluating the inductances and capacitance of the LCL filter using an analytical approach in the time domain, specifically designed for multilevel inverters. Indeed, the current ripple and the maximum allowable power factor reduction have been considered to calculate the inductances and capacitance, respectively. The proposed approach is discussed with respect to the 3P-5L CHBMI topology, which is adopted in this work for validation purposes and whose scheme is reported in Fig. 2. However, the proposed method is generalized for any number of voltage levels considering PD-PWM, PS-PWM, and

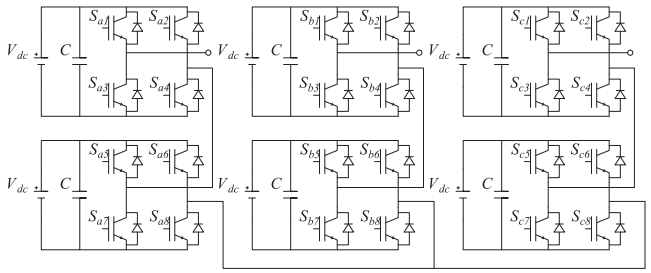

FIGURE 2. 3P-5L CHBMI circuit scheme.

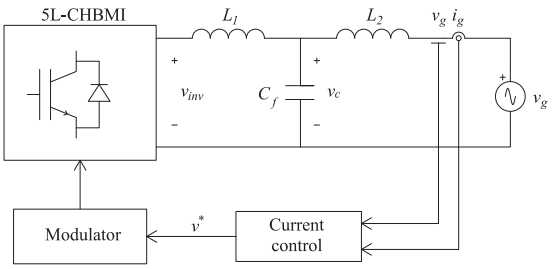

FIGURE 3. Grid-connected inverter scheme.

SCA-PWM schemes with Sinusoidal (S) modulating wave, as shown in Fig. 1. Finally, it must be underlined that the proposed method can be applied to every MI topology. In detail, with regard to the design formulas that will be derived in the following sections, it is sufficient to consider the V_{DC} as the amplitude of one voltage level related to the new MI topology. In the case of CHBMI, V_{DC} is the DC-link voltage of a single H-Bridge module.

A. INDUCTOR DESIGN

The design of the inductances is based on the current ripple evaluation, which, as is well known, depends on the adopted modulation scheme. The proposed approach is based on the following steps:

1) determination of the current increment expressions;
2) evaluation of the time intervals T^+ and T^- for each considered modulation scheme;
3) calculation of the maximum current ripple;
4) determination of the minimum value of the inductances.

Assuming that the grid voltage system is symmetric and the filter is balanced, the expression of the current ripple is determined by considering the single-phase scheme shown in Fig. 3.

It is reasonable to assume that, in the low-frequency range, the capacitor branch impedance is much larger than the longitudinal impedance. The current absorbed by the capacitor can be neglected, resulting in an L-filter with the series inductors L_1 and L_2. Therefore, the voltage across the series of the inductances L_{12} can be expressed as:

$$v_{inv} - v_g = L_{12}\frac{di_g}{dt} \tag{6}$$

where v_{inv} is the inverter phase voltage, v_g is the grid voltage, and i_g is the grid current. Moreover, due to the low value of the voltage drop across the series of the inductances L_{12}, the grid voltage v_g can be approximated to the fundamental component of the inverter output voltage. According to [15], for a 3P-5L CHBMI, it can be expressed as:

$$v_g = 2MV_{DC}\sin(\omega_1 t) \tag{7}$$

where M is the amplitude modulation index, V_{DC} is the DC-link voltage of the single H-Bridge module, according to Fig. 2, and ω_1 is the fundamental frequency. This hypothesis simplifies the current ripple evaluation and is valid for a 5L-CHBMI in the linear modulation region. Fig. 4 shows one carrier period T_{PWM} of each modulation scheme (SPD-PWM, SPS-PWM, and SSCA-PWM) considered in this work. Fig. 4 includes the carriers pattern, a sample of the modulating signal v_m, the inverter output voltage $v_{inv,}$ and the inductor current i_L. For each modulation scheme, two cases that deal with an amplitude modulation index lower (Fig. 4(a), (c), (e)) and higher (Fig. 4(b), (d), (f)) than 0.5, are analyzed, respectively. Such two cases determine phase voltages with three or five voltage levels. The modulating signal sample is considered constant during a switching period since the modulating signal has a frequency much lower than the switching frequency. Looking at the phase voltage, the time intervals T^+ and T^-, where the phase voltage is equal to 0 and V_{DC} respectively, can be identified. It can be assumed that the phase current increases linearly during the interval T^+ and decreases linearly during T^-. The positive and negative current increment expressions Δi^+ and Δi^-, relative to the time intervals T^+ and T^-, can be computed by integrating on their respective intervals and relations (8) and (9) are obtained:

$$\Delta i^+ = \frac{v_{inv} - v_g}{L_{12}}T^+ \tag{8}$$

$$\Delta i^- = \frac{-v_{inv} + v_g}{L_{12}}T^- \tag{9}$$

It should be noted that Δi^+ and Δi^- are influenced by the employed modulation technique through the terms v_{inv}, T^+, and T^-. Taking into account the waveforms shown in Fig. 4, the evaluation of the time intervals T^+ and T^- can be carried out by applying geometrical considerations to the similar triangles, highlighted in orange and light blue, for each considered modulation scheme. By looking at Fig. 4(a), taking into account the half-period symmetry, the analysis can be carried out with respect to the interval 0-$T_{PWM}/2$. Thus, it is possible to express T^+ and T^- as a function of the switching period T_{PWM}, the modulating signal amplitude v_m, and the carrier signal amplitude V_{tri}, as follows:

$$T^+ = 2\frac{v_m}{V_{tri}}T_{PWM} \tag{10}$$

$$T^- = 2T_{PWM}\left(\frac{1}{2} - \frac{v_m}{V_{tri}}\right) \tag{11}$$

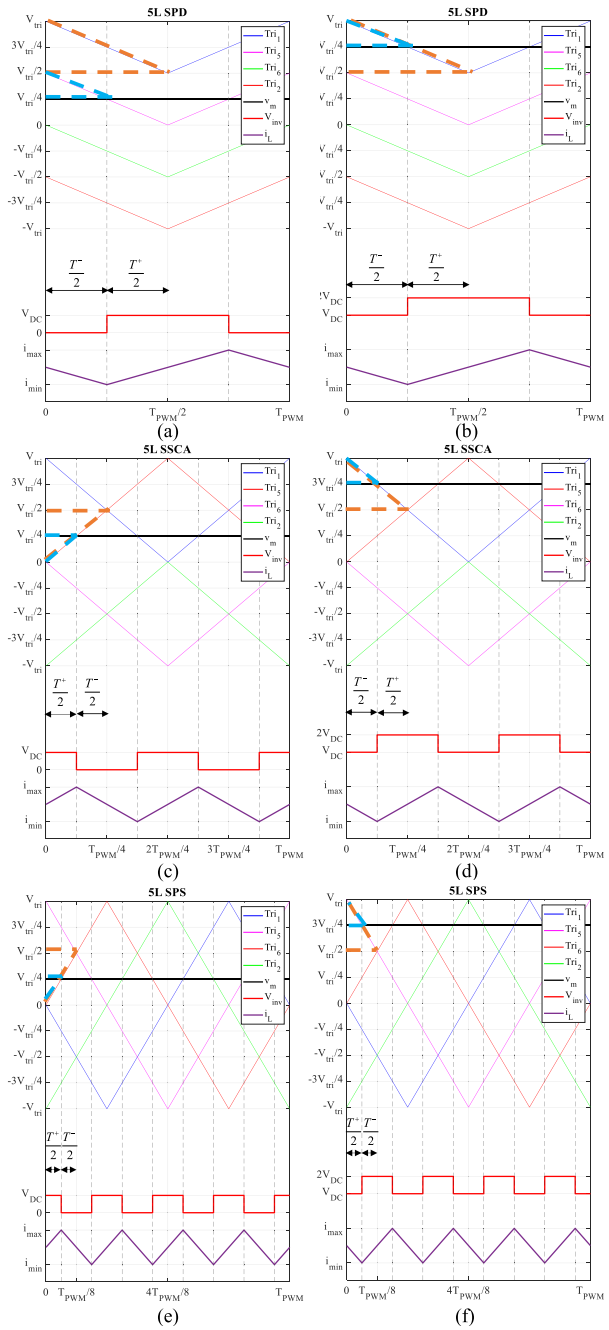

FIGURE 4. Modulation schemes: (a) SPD and inverter output voltage between 0 and V_{DC}; (b) SPD and inverter output voltage between V_{DC} and 2 V_{DC}; (c) SSCA and inverter output voltage between 0 and V_{DC}; (d) SSCA and inverter output voltage between V_{DC} and 2 V_{DC}; (e) SPS and inverter output voltage between 0 and V_{DC}; (f) SPS and inverter output voltage between V_{DC} and 2 V_{DC}.

Furthermore, it can be assumed that:

$$\frac{v_m}{V_{tri}} = M\sin(\omega_1 t) \tag{12}$$

Considering the expressions (10), (11), and (12), the current increments expressions (8) and (9) can be rewritten as follows:

$$\Delta i^{+} = \frac{V_{DC}}{L_{12}} \cdot 2T_{PWM} \cdot [1 - M\sin(\omega_1 t)]\,[2M\sin(\omega_1 t) - 1] \tag{13}$$

$$\Delta i^{-} = \frac{V_{DC}}{L_{12}} \cdot 2T_{PWM} \cdot [1 - M\sin(\omega_1 t)]\,[2M\sin(\omega_1 t) - 1] \tag{14}$$

Hence the two current increment expressions assume the same value demonstrating the correctness of the procedure, thus, it can be assumed that $\Delta i^{+} = \Delta i^{-} = \Delta i$. Consequently, the maximum current ripple across L_{12} can be expressed as (15):

$$\Delta i_{\max} = \frac{V_{DC}}{4 \cdot L_{12}} T_{PWM} \tag{15}$$

It can be demonstrated that, by repeating the previously described procedure with respect to Fig. 4(b), where when the output inverter voltage is between V_{DC} and $2V_{DC}$, the maximum current ripple expression coincides with (15). Thus, it can be stated that the expression (15) is valid over the entire period of the grid-voltage and does not depend on the value of the duty cycle. The same procedure can be carried out also for SSCA and SPS modulations, respectively. In detail, with respect to the Fig. 4(c) and (d), the time intervals T^{+} and T^{-} can be expressed as:

$$T^{+} = \frac{v_m}{V_{tri}} T_{PWM} \tag{16}$$

$$T^{-} = T_{PWM}\left(\frac{1}{2} - \frac{v_m}{V_{tri}}\right) \tag{17}$$

With respect to the Fig. 4(e) and (f), the time intervals T^{+} and T^{-} can be expressed as:

$$T^{+} = \frac{1}{2}\frac{v_m}{V_{tri}} T_{PWM} \tag{18}$$

$$T^{-} = \frac{1}{2} T_{PWM}\left(\frac{1}{2} - \frac{v_m}{V_{tri}}\right) \tag{19}$$

Then, the current ripple calculation can be performed for SSCA and SPS modulations in the same way described for the SPD modulation. For SSCA modulation, by substituting (16) in (8) and (17) in (9), the maximum current ripple can be calculated as:

$$\Delta i_{\max} = \frac{V_{DC}}{8 \cdot L_{12}} T_{PWM} \tag{20}$$

With respect to PS, by substituting (18) in (8) and (19) in (9), the maximum current ripple can be calculated as:

$$\Delta i_{\max} = \frac{V_{DC}}{16 \cdot L_{12}} T_{PWM} \tag{21}$$

Similarly to the discussion reported in [35], (15), (20), and (21) can be generalized taking into account MC-PWM strategies and the number of voltage levels n_l. Considering the ratio

TABLE 2. C_{MC} Coefficient Values

Modulation	C_{MC}
SPD-PWM	1
SSCA-PWM	2
SPS-PWM	n_l-1

between the virtual switching frequency f_h and the switching frequency f_{sw}, it is possible to define an identification coefficient for each considered MC-PWM technique, called C_{MC} [35]:

$$C_{MC} = \frac{f_h}{f_{sw}} \tag{22}$$

In Table 2 the C_{MC} coefficient values are reported.

It should be noted that the C_{MC} value identified in the case of SPD is valid for all LS-PWM strategies. Furthermore, as previously described, the C_{MC} coefficient allows for considering the number of voltage levels, as evidenced by the case of SPS-PWM.

Moreover, it can be easily demonstrated that by performing the whole procedure for a generic 3P-NL CHBMI, the (23) is obtained:

$$\Delta i_{\max} = \frac{V_{DC}}{4 \cdot L_{12} \cdot C_{MC}} T_{PWM}. \tag{23}$$

Thus, the expression (23) of the maximum current ripple takes into account the single H-Bridge DC link voltage, the series of inductances L_{12}, and the term T_{PWM}/C_{MC}. The last term represents the virtual switching period which depends on the number of the voltage levels of the converter according to the discussion in Section II. It allows for a complete generalization of the proposed formulation.

By defining the maximum current ripple coefficient λ_{L12} as:

$$\lambda_{L12} = \frac{\Delta i_{\max}}{I_{1,peak}} \tag{24}$$

where $I_{1,peak}$ is the peak value of rated grid current. Thus, with respect to (23), by isolating the term L_{12}, it follows:

$$L_{12} = \frac{V_{DC}}{4 \cdot \lambda_{L12} \cdot I_{1,peak} \cdot C_{MC}} \cdot T_{PWM} \tag{25}$$

The expression (25) represents the general analytical formula that takes into account the modulation scheme, the switching frequency, the number of voltage levels and the CHBMI rated current.

Since it is proposed a symmetrical filter, the inverter side inductance L_1 and the grid side inductance L_2 can be calculated as follows:

$$L_1 = L_2 = \frac{L_{12}}{2} \tag{26}$$

B. MIDDLE BRANCH DESIGN

The middle branch of the LCL grid filter is composed of a capacitor in series with a damping resistor to filter voltage harmonics and attenuate the resonance peak.

The design of the filter capacitor C_f is based on the maximum allowable power factor reduction. According to the previous discussion reported in Section II, since SPD-PWM is characterized by the coincidence between the switching frequency and the virtual switching frequency, the capacitance design formulas coincide with the case of the 2L-VSI, which is known in the literature. Thus, the capacitance design at first is carried out with respect to the SPD-PWM, and, subsequently, such an approach is generalized for other MC-PWM strategies by taking into account the coefficient C_{MC}.

With respect to the SPD-PWM strategy, the capacitor is designed by assigning the maximum reactive power relative to the inverter rated power, x, according to (27).

$$C_{f,PD} = x \cdot C_b \tag{27}$$

where C_b is the base capacitance defined according to (28):

$$C_b = \frac{1}{\omega_1 \cdot Z_b} \tag{28}$$

and Z_b is the base impedance, defined as (29):

$$Z_b = \frac{V_g^2}{S} \tag{29}$$

where V_g is the grid voltage RMS and S is the inverter-rated apparent power. The reactance of the sized capacitor is expressed as:

$$X_{C_f,PD}(\omega) = \frac{1}{\omega \cdot x \cdot C_b}. \tag{30}$$

With respect to the frequency domain, the adopted design approach determines a very low capacitive reactance at the switching frequency. However, since SSCA and SPS modulation are characterized by a shift of the harmonics over the spectrum, adopting relation (27) implies a filter over-sizing, since there are no harmonics to be filtered at the switching frequency. Thus, the filter capacitance related to SSCA and SPS-PWM is obtained by imposing that the generic capacitive reactance X_{cf} at the virtual switching frequency must have the same value of $X_{cf,PD}$ at the switching frequency, as follows:

$$X_{C_f,PD}(\omega_{sw}) = X_{C_f}(\omega_h) \tag{31}$$

where ω_h is the virtual switching pulsation, which is related to the switching frequency f_{sw} by the following relation:

$$\omega_h = 2\pi f_{sw} \cdot C_{MC} \tag{32}$$

By exploiting relation (31), it follows:

$$\frac{1}{\omega_{sw} \cdot x \cdot C_b} = \frac{1}{\omega_{sw} \cdot C_{MC} \cdot C_f} \tag{33}$$

Then, by isolating C_f in (33), the filter capacitor can be designed as:

$$C_f = \frac{x \cdot C_b}{C_{MC}} \tag{34}$$

Relation (34) represents the generalized formula, which allows to take into account the harmonic displacement over the spectra, which depends on the adopted MC-PWM strategy.

The damping resistor R_d is designed to be equal to one-third of the capacitor reactance at the resonance pulsation, ω_{res}, (35).

$$R_d = \frac{1}{3C_f\omega_{res}} \tag{35}$$

where ω_{res} is the resonance frequency expressed as:

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{36}$$

C. FILTER DESIGN CONSTRAINTS

In this subsection, the LCL filter design constraints are introduced. First, the designed filter has to meet constraints that deal with limiting the voltage drop across the inductances and the oscillations that occur at the resonance frequency due to harmonics. In detail, the voltage drop across the total filter inductance $\Delta V_{\%}$ should be less than 10% to maintain the desired fundamental voltage output. It can be verified by the following expression:

$$\Delta V_{\%} = \frac{S \cdot \omega_1 \cdot L_{12}}{{V_g}^2} \cdot 100 \leq 10\% \tag{37}$$

Moreover, to avoid potential instability due to resonance phenomena, the filter resonance frequency must match the following relation:

$$10 \cdot f_1 \leq f_{res} \leq 0.5 \cdot f_h \tag{38}$$

where f_1 is the fundamental frequency and f_h is the virtual switching frequency. It must be underlined that relation (38) is commonly formulated in the scientific literature by considering the switching frequency f_{sw} [24]. However, in this work, the switching frequency f_{sw} is replaced with the virtual switching frequency f_h to take into account the effective harmonic group displacement over the spectrum, determined by the adopted MC-PWM strategy and by the number of voltage levels. Even in this case, the constraint on the resonance frequency is generalized through the parameter C_{MC}, according to (22). It follows that, for fixed carriers frequency, the deeper the shift in the high-frequency range of the first group of voltage harmonic, the wider the admissible resonance frequency range.

D. CASE STUDY

In this subsection, the proposed LCL filter design method is applied to a case study. The system under test consists of a symmetrical 3P-5L CHBMI, a 3P LCL filter, and the main grid, whose main parameters are summarized in Table 3. These parameters have been chosen considering a real test rig available at the University of Palermo, whose detailed experimental characterization is reported in [35].

With respect to the MC-PWM strategy, the switching frequency is equal to 10 kHz, and the virtual switching frequency is considered in the design process through the parameter C_{MC}. Moreover, two filter design parameters are defined: the maximum current ripple λ_{L12}, expressed in percent of the rated current, and maximum reactive power relative to the inverter rated power x. In this application, $\lambda_{L12} = 20\%$ and $x = 5\%$, which are commonly adopted values in the literature, are chosen, as can be seen as a way of example in [28]. By applying the previously discussed analytical formulations for each considered modulation scheme, the LCL filter design values are reported in Table 4.

TABLE 3. Main Parameters of the System Under Test

Symbol	Quantity	Value
S	Rated apparent power [VA]	1650
Vg	Rated line grid voltage RMS [V]	125
f_g	Rated grid frequency [Hz]	50
V_{DC}	DC voltage input of each H-Bridge [V]	55
f_{sw}	Switching frequency [kHz]	10

TABLE 4. LCL Filter Design Example Values

Symbol	Quantity	Modulation		
		SPD	SSCA	SPS
L_1	Converter-side inductance [μH]	320	160	80
L_2	Grid-side inductance [μH]	320	160	80
C_f	Filter capacitance [μF]	16.8	8.4	4.2
R_1	Inv.-side winding resistance [Ω]	0.01	0.01	0.01
R_2	Grid-side winding resistance [Ω]	0.01	0.01	0.01
R_d	Damping resistance [Ω]	1.028	1.027	1.027
f_{res}	Resonance frequency [kHz]	3.07	6.15	12.3
$\Delta V_{\%}$	Filter voltage drop [%]	2.12	1.06	0.53

Table 4 shows that the obtained inductances and capacitance values vary substantially with each considered modulation strategy. Therefore, the proposed method, which allows for taking into account the adopted MC-PWM strategy, provides filter design values specifically tailored to the used modulation strategy. Moreover, it can be noticed that both constraints (37) and (38) are met for all three modulation strategies.

The designed filter behavior can be easily studied by performing a frequency domain analysis. In detail, according to the state-space model theory [25], the inverter voltage to grid current transfer function, $G_P(s)$, can be expressed as:

$$G_P(s) = \frac{I_g}{V_{inv}} = \frac{\frac{R_d}{L_1 \cdot L_2} \cdot \left[s + \frac{1}{C_f \cdot R_d}\right]}{s^3 + b \cdot s^2 + c \cdot s + d} \tag{39}$$

where the denominator coefficients are:

$$b = \frac{L_2(R_1 + R_d) + L_1(R_2 + R_d)}{L_1 \cdot L_2} \tag{40}$$

$$c = \frac{R_1 R_2 + R_1 R_d + R_2 R_d}{L_1 \cdot L_2} \tag{41}$$

$$d = \frac{R_1 + R_2}{L_1 \cdot L_2 \cdot C_f}. \tag{42}$$

Magnitude and phase bode plots of the transfer function (39) are reported in Fig. 5 for every considered MC-PWM

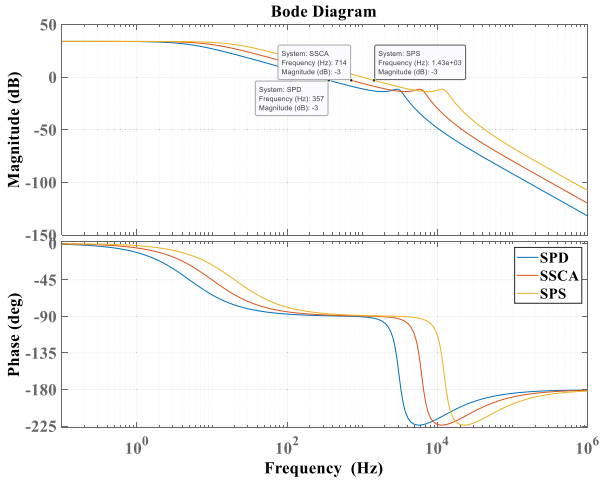

FIGURE 5. Inverter voltage to grid current transfer function bode plots.

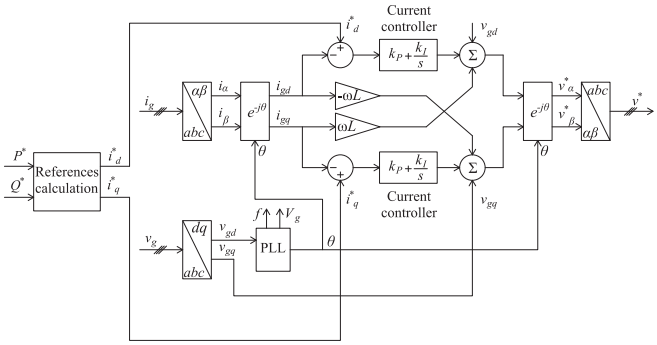

FIGURE 6. Voltage-oriented control scheme.

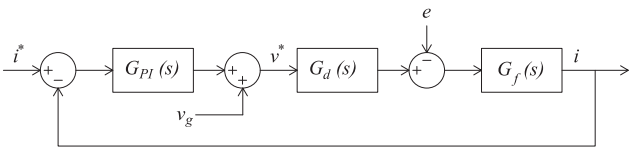

FIGURE 7. Control system scheme.

strategy. It can be detected a very similar behavior of the three designed filters. In detail, concerning the magnitude diagram, they are characterized by different cutoff frequencies, equal to 357 Hz, 715 Hz, and 1430 Hz, and a shift in the resonance frequency which takes place at 3.07 kHz, 6.15 kHz, and 12.3 kHz for SPD, SSCA, and SPS, respectively.

Moreover, it can be noticed that the designed damping resistance properly reduces the resonance peak, allowing for avoiding stability issues. Thus, the frequency response confirms the effectiveness of the proposed general analytical formulation, allowing for the design of LCL filters tailored specifically to each modulation scheme.

IV. CONTROL IMPLEMENTATION AND TEST BENCH

In this section, the adopted control strategy is discussed and the test bench is presented. In detail, efforts are devoted to the control parameter tuning and control system stability analysis. The former is carried out through an analytical approach that allows for taking into account the adopted modulation strategy. The latter is carried out by investigating the open-loop current transfer function gain and phase margins.

A. CONTROL PARAMETERS TUNING

To test the filtering capability, a Voltage Oriented Control (VOC) in the *d-q* domain is adopted [36]. In detail, it allows for controlling the grid-injected currents in terms of magnitude and power factor by adjusting the active and reactive power references. In Fig. 6, the control scheme of the implemented VOC is reported.

According to [36], the current controller tuning is based on the scheme of Fig. 7, where G_{PI} is the PI transfer function, G_d is the transfer function which takes into account the inverter delay, and G_f is the transfer function of the LCL filter neglecting the middle branch.

Transfer functions G_{PI}, G_d, and G_f are defined according to the following relations:

$$G_{PI}(s) = K_P + \frac{K_I}{s} = K_P\left(1 + \frac{1}{T_I s}\right) \tag{43}$$

$$G_d(s) = \frac{1}{1 + T_d s} \tag{44}$$

$$G_f(s) = \frac{1}{R_{12} + L_{12} s} \tag{45}$$

where T_d is the inverter delay, R_{12} is the equivalent resistance related to the filter winding resistances R_1 and R_2, whose values are reported in Table 4, K_P and T_I are the PI regulator proportional gain and integral time constant, respectively.

According to the discussion concerning the MC-PWM strategies in Section II, each carrier's pattern is characterized by a different virtual switching frequency. Therefore, in terms of control action application, each MC-PWM strategy exhibits its own modulation delay T_d. Thus, such delay is particularized for each modulation strategy through the C_{MC} coefficient, according to the following relation:

$$T_d = 1.5\frac{T_{PWM}}{C_{MC}} \tag{46}$$

According to [36], it is possible to perform a zero-pole cancellation in the closed-loop transfer function by imposing the following relation:

$$T_I = \frac{L_{12}}{R_{12}} \tag{47}$$

Since L_{12} and R_{12} values vary with the modulation strategy, according to Table 4, it results that even the integral time constant T_I depends on the modulation strategy. Imposing (47) allows for obtaining a second-order closed-loop transfer

TABLE 5. PI Regulators Tuning Parameters

Symbol	Quantity	Modulation		
		SPD	SSCA	SPS
K_P	Proportional gain	2.1269	2.1269	2.1269
T_I	Integral constant	0.0319	0.0159	0.008
ω_n	Natural pulsation	4714.8	9426.5	18859
ζ	Damping coefficient	0.707	0.707	0.707

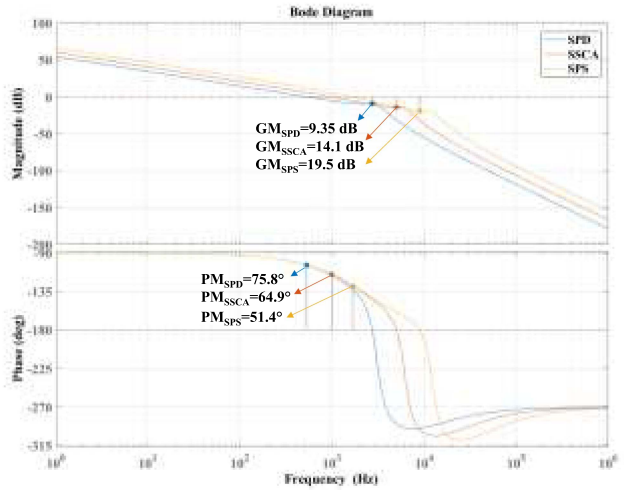

FIGURE 8. Open loop transfer function Bode plots.

function; thus, the proportional gain can be calculated as:

$$K_P = L_{12}\, T_d {\omega_n}^2 = \frac{1.5 L_{12} \omega_n^2 T_{PWM}}{C_{MC}} \tag{48}$$

where ω_n is the natural pulsation that is a function of the desired damping coefficient ζ, according to (49):

$$\omega_n = \frac{1}{2T_d\zeta} = \frac{C_{MC}}{3T_{PWM}\zeta} \tag{49}$$

It should be noted that expressions (48) and (49) allow to generalize the PI regulator tuning process taking into account the MC-PWM strategy through the C_{MC} coefficient. Indeed, K_P can be calculated by combining expressions (48)–(49) and assigning the desired value of the damping coefficient ζ. In detail, it was chosen a damping coefficient equal to 0.707 for all three modulation techniques to achieve good dynamic performance with tolerable overshoot. In Table 5 PI tuning parameters are reported for each modulation strategy.

It is interesting to note that the impact of MC-PWM techniques on the PI tuning procedure has been demonstrated.

Finally, the controlled system stability is proven by investigating the open loop current transfer function magnitude and phase margins. For this purpose, the open loop current transfer function $F(s)$ is defined as follows:

$$F(s) = G_{PI}(s) \cdot G_d(s) \cdot G_P(s) \tag{50}$$

Fig. 8 shows the open loop current transfer function frequency response for each considered MC-PWM, where gain and phase margins are shown.

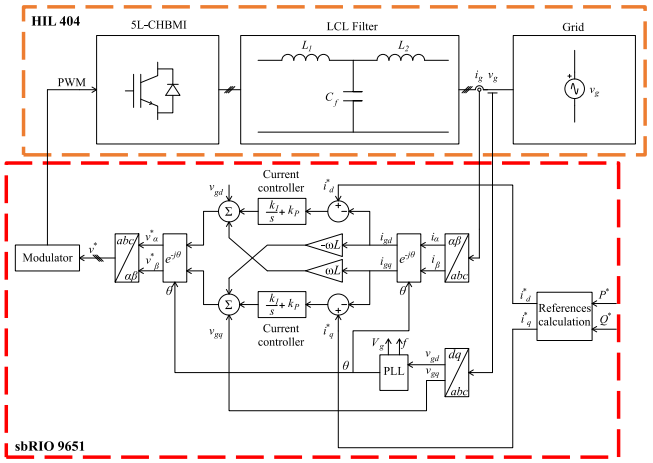

FIGURE 9. Experimental setup block diagram.

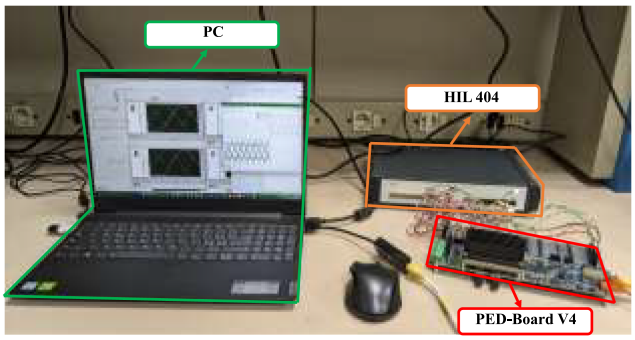

FIGURE 10. Test bench.

Looking at Fig. 8, it can be noted that the Gain Margins (GM) are equal to 9.35 dB, 14.1 dB, and 19.5 dB for SPD, SSCA, and SPS, respectively. Moreover, the Phase Margins (PM) are equal to 75.8°, 64.9°, and 51.4° for SPD, SSCA, and SPS, respectively. Therefore, this analysis proves that the proposed method guarantees robust system stability independently of the adopted MC-PWM strategy.

B. CONTROLLER AND HIL

In Figs. 9 and 12 the experimental setup block diagram and test bench scheme are reported, respectively. As graphically represented, the system under test is subdivided into two main parts: control and hardware.

The adopted controller is the sbRIO 9651 System on Module, by National Instruments, whose technical data are reported in Table 6. It consists of an FPGA and a DSP module, which can be programmed independently.

The adopted controller is installed on the Power Electronics and Drive (PED) Board V4, whose main data are reported in Table 7. The control algorithm was entirely implemented in the LabVIEW environment which is a visual programming language. In detail, the algorithm is composed of two main full-parallel structures. One is a high-frequency cycle

TABLE 6. SoM sbRIO 9651 Technical Data

Quantity	Value
Type	Xilinx Zynq-7000 SoC
Architecture	ARM Cortex A-9
Speed	667 MHz
Cores	2
Logic Cells	85000
Flip-flops	106400
LUTs	53200
DSP slices	220

TABLE 7. PED-Board v4 Characteristics

Hardware	Features
PWM Channels	30x, 0÷15 V or 0÷5V selectable voltage
14 bit-ADC	8 channels, Simultaneous sampling o 1.45 µs conversion time, 8 channels o Differential input o -5V÷5V or 0V÷10V configurable inputs magnetic induction
14-bit-ADC	8 channels, Simultaneous sampling o 1.45 µs conversion time, 8 channels o Differential input o -5V÷5V or 0V÷10V configurable inputs
10 bit-ADC	8 channels, up to 200 kS/s
Digital I/O	46x3.3V standard
Ethernet	programming, debugging and operation

TABLE 8. HIL 404 Characteristics

Hardware	Features
ZU4EG Ultrascale+Zync SoC	up to 4 processing cores
Analog inputs (AI)	16x, up to 1MSPS, ± 10V
Analog Outputs (AO)	16x, up to 5MSPS, ± 10V
Digital inputs (DI)	32x, ± 15V
Digital outputs (DO)	32x, 0:5V
Ethernet	2x RJ45; up to 1000 Mbps

in which the modulator is implemented so it includes carrier, dead-time, and PWM generation. The other is a structure in which the acquisition, control and modulating signals generation operations are carried out. It's triggered to synchronize the data sampling and the control action application with the carrier's maximum and minimum values. Thus, the sampling frequency is equal to the virtual switching frequency for each type of modulation technique. Once compiled in the FPGA the algorithm can be controlled with a Real Time control panel.

The power system is emulated by Typhoon Hardware-in-the-loop (HIL) 404 whose main features are reported in Table 8. The model built in the Typhoon HIL 404 consists of a three-phase five-level CHBMI connected to a stiff grid by an LCL filter. To run the real-time simulation on HIL 404, the power system has been split among the available four cores. Since each core can run at most two power converters, the 3P-5L CHBMI model has been split into three single-phase CHBMI, which run in parallel on three separate cores. The remaining core is devoted to the three-phase LCL filter and grid models. In detail, the grid is modeled by three sinewave voltage sources.

TABLE 9. Working Points

$cos\varphi$ [-] - S [%]	25	50	75	100
1	WP4	WP3	WP2	WP1
0.9	WP8	WP7	WP6	WP5
0.8	WP12	WP11	WP10	WP9
0.7	WP16	WP15	WP14	WP13

V. HARDWARE-IN-THE-LOOP RESULTS

In this section, the proposed LCL filter design method is validated by HIL real-time results. In detail, each considered MC-PWM strategy has been adopted to control the system under several working conditions, defined as a function of the injected apparent power, expressed in percentage of the rated apparent power reported in Table 3, and the imposed power factor. The working points (WPs) are summarized in Table 9. The standards considered for validation purposes are the EN50160 for voltages and the IEEE Std 1547–2018 for currents.

According to these standards, the LCL filter performance are evaluated by taking into account the voltage THD and the current TRD, which give information about the overall harmonic behavior, and the voltage and current spectra. According to the standards, the voltage THD and current TRD are defined as follows:

$$THD_{\%} = \frac{\sqrt{\sum_{h=2}^{40} {V_h}^2}}{V_1} \cdot 100 \tag{51}$$

$$TRD_{\%} = \frac{\sqrt{{I^2}_{RMS} - {I^2}_1}}{I_{rated}} \cdot 100 \tag{52}$$

where V_h is the voltage harmonic, V_1 is the voltage fundamental harmonic, I_{RMS} is the current RMS value, I_1 is the current fundamental harmonic, and I_{rated} is the RMS value of the rated current. Standards indicate the limits in terms of THD and TRD previously defined. Moreover, a specified single harmonics limit is provided for voltage and current quantities up to the 25th and 50th harmonic, respectively. In detail, standards specify a maximum voltage THD of 8% and a maximum current TRD of 5%. Standards require these limits to be met only under the rated operating conditions. However, since the grid working conditions can change over time, standards requirements have been considered over the entire defined working range. Per each working point, voltage and current trends are sampled on HIL 404 with a sampling frequency of 4MHz and a sampling window of 0.2 s, i.e., 10 voltage and current periods are sampled, according to IEEE standard 519.

A. LCL FILTER DESIGN VALIDATION

In this subsection, the Hardware-In-the-Loop tests are carried out by considering as design parameters $\lambda_{L12} = 20\%$ and $x = 5\%$, resulting in the LCL filter values reported in Table 4. In Fig. 11, the voltage THD maps for each modulation strategy over the defined working range are reported. By comparing the couples of figures a-b, c-d, and e-f, it can be noted that

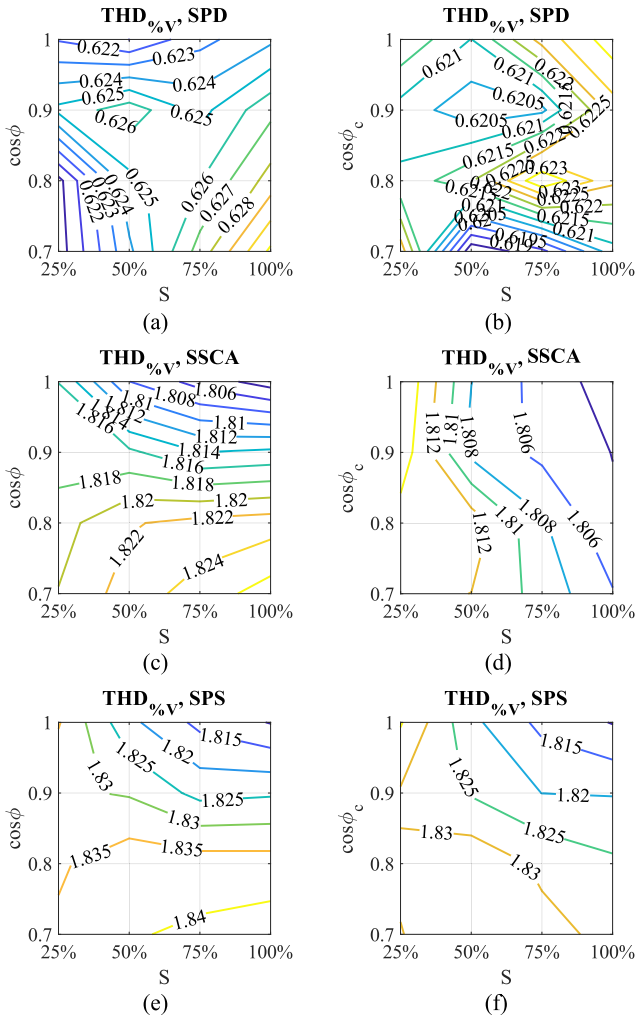

FIGURE 11. Voltage THD maps as a function of apparent power *S* and *cosϕ*: (a) SPD with inductive power factor; (b) SPD with capacitive power factor; (c) SSCA with inductive power factor; (d) SSCA with capacitive power factor; (e) SPS with inductive power factor; (f) SPS with capacitive power factor.

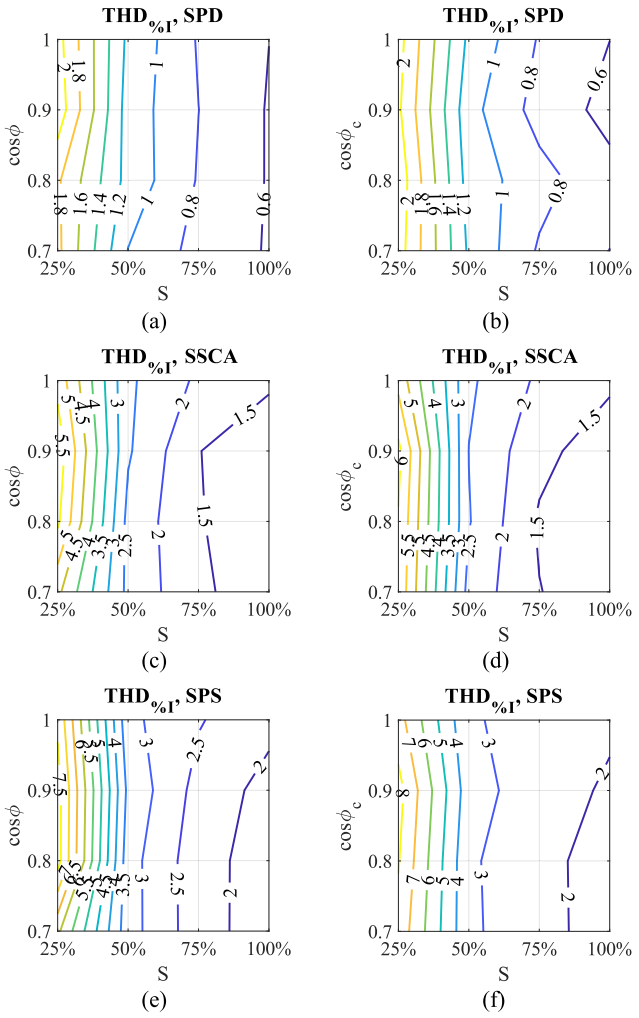

FIGURE 12. Current THD maps as a function of apparent power *S* and *cosϕ*: (a) SPD with inductive power factor; (b) SPD with capacitive power factor; (c) SCA with inductive power factor; (d) SSCA with capacitive power factor; (e) SPS with inductive power factor; (f) SPS with capacitive power factor.

per each WP the voltage THD doesn't vary significantly over the defined working range, when capacitive and inductive power factors are considered. Moreover, per each modulation strategy, the THD is quite independent of the considered WP. This behavior is justified by taking into account that the grid voltage is fixed, thus the inverter amplitude modulation index has a negligible variation when the power S varies over the defined range. Concerning the modulation strategy, SPD-PWM guarantees the lowest THD compared to SPS-PWM and SSCA-PWM which are characterized by similar behavior over the entire working range. This behavior is correlated to the different harmonic content produced by each modulation strategy. In Fig. 12 the grid-side current THD maps for each modulation strategy are reported.

Although the current THD is not adopted as an analysis tool by the previously discussed standards, it is a commonly adopted index in the literature since it allows for correlating the total distortion with the fundamental harmonic value. Concerning the dependency of the power factor nature, similar considerations to the previous figure can be carried out. Fig. 12 shows a strong correlation between the apparent power and the current THD values, the current THD decreases as the power S increases. Comparing the modulation strategies, it can be noted that SPD guarantees the lowest values of current THD over the entire working range, with values that go from 2% to 0.6%. SSCA and SPS present higher values which go from 5.5% to 1.5% and from 7.5% to 2%, respectively. This behavior can be correlated to the dead-time effect, which determines low-frequency harmonics that the filter cannot attenuate. The dead time effect is more evident in SSCA and SPS strategies, where a stronger deviation between switching frequency and virtual switching frequency occurs and the single pulse-modulated voltage width becomes comparable

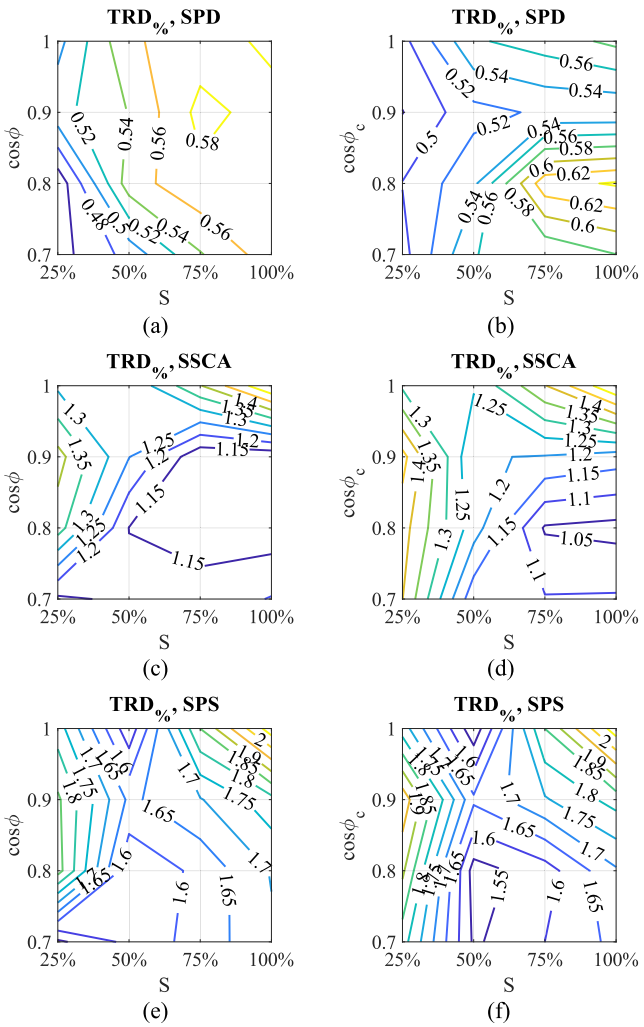

FIGURE 13. Current TRD maps as a function of apparent power S and $cos\phi$: (a) SPD with inductive power factor; (b) SPD with capacitive power factor; (c) SCA with inductive power factor; (d) SSCA with capacitive power factor; (e) SPS with inductive power factor; (f) SPS with capacitive power factor.

to the dead time [35]. In Fig. 13, the grid-side current TRD maps for each modulation strategy are presented. It can be noted that the TRD is poorly influenced both by the injected power since it has always the same denominator, and by the power factor. By comparing the MC-PWM strategies, the same considerations of the current THD can be carried out, i.e., the TRD increase moving from SPD to SSCA and SPS for every considered WP. Concerning the consideration made so far about voltage THD, current THD, and current TRD, it follows that the power factor has a negligible impact on the harmonic behavior of the filter. Thus, for further analysis, only one power factor representative value is adopted, that is 0,9 capacitive. It follows that only WPs 5, 6, 7, and 8 are considered. Moreover, with respect to the grid-side voltage, time and frequency trends are reported only for the WP 5. Fig. 14 shows a comparison of grid-side voltages for WP5 in steady state, examining harmonic spectra and considering both high-frequency (second row) and low-frequency (third row) harmonic distributions for each adopted modulation scheme.

In detail, with respect to the frequency domain, two spectra per figure are reported: the first shows the spectrum up to the 2000th harmonic (i.e., up to 100 kHz), thus, it is possible to observe the harmonics placement over the spectra due to the adopted MC-PWM strategy; the second shows the spectrum, up to the 25th harmonic and up to the 50th harmonic for the voltage and current spectra, respectively. Moreover, low-frequency harmonics are compared with the limits of the standard, to verify the standards requirements. It is interesting to note that voltage harmonics are centered around the carrier's frequency and its multiples, twice the carrier's frequency and its multiples, and four times the carrier's frequency and its multiples, when SPD, SSCA, and SPS are considered, respectively, according to the discussion regarding the virtual switching frequency. Moreover, voltage harmonics amplitudes are lower than 1% over the entire spectrum when SPS and SSCA are considered, and lower than 0.5 % when SPD is considered.

Figs. 15–17 show the current trends in the time domain and the respective harmonic spectrum, considering different WPs, per each MC-PWM strategy, respectively. It should be noted that current harmonics amplitude decreases when the apparent power increases and, in the worst case, they are always lower than 1%, 2%, and 4%, when SPD, SSCA, and SPS are considered, respectively. Moreover, by adopting the LCL filter values reported in Section III, all three modulations meet regulatory requirements by a wide margin, in terms of voltage THD, current TRD and also by considering each harmonic amplitude, in every WP. It can be noticed that the control algorithms can produce very close values of injected current in all working points despite the different modulation strategies.

In terms of fundamental voltage, it can be seen that similar results are obtained across all WPs since the control works at a modulation index near to one, and also there is little difference between the three modulation strategies.

B. LCL FILTER OPTIMIZATION

According to the previously discussed results, it can be stated that, by adopting the commonly used LCL filter design parameters in the literature λ_{L12} and x, standards requirements are largely satisfied. Therefore, in this subsection, a parametric analysis is carried out to further reduce the LCL filter parameters, satisfying both standard requirements and performance constraints. In detail, two design parameters introduced in Section III, the maximum current ripple λ_{L12}, expressed in percent of the rated current, and maximum reactive power relative to the inverter rated power x, are varied to find the optimal parameter values which allow addressing the requirements of the standards without oversizing the filter. To carry out this analysis, sixteen couples of Design Parameters (DP) are adopted and summarized in Table 10. Table 10 is used to build maps of voltage THD and current TRD to find the optimal DP for the system taken into consideration.

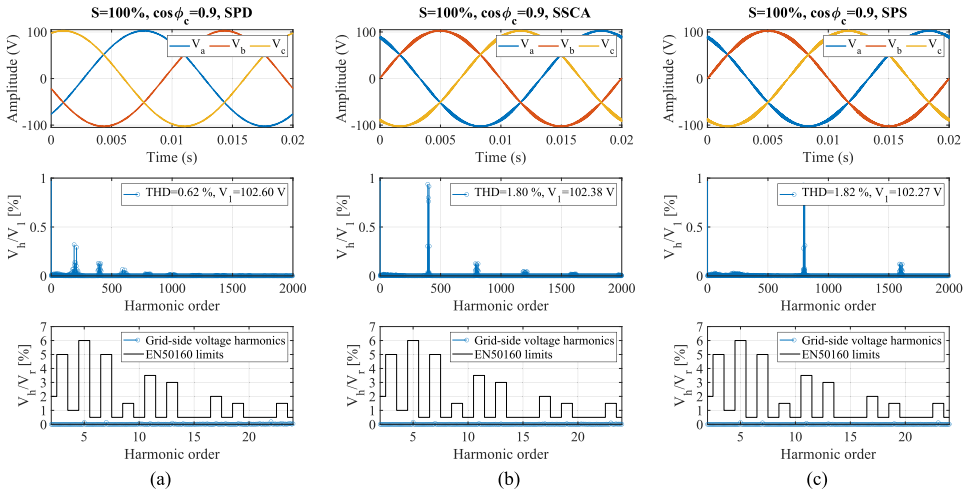

FIGURE 14. Grid-side voltages: (a) SPD in WP5; (b) SSCA in WP5; (c) SPS in WP5.

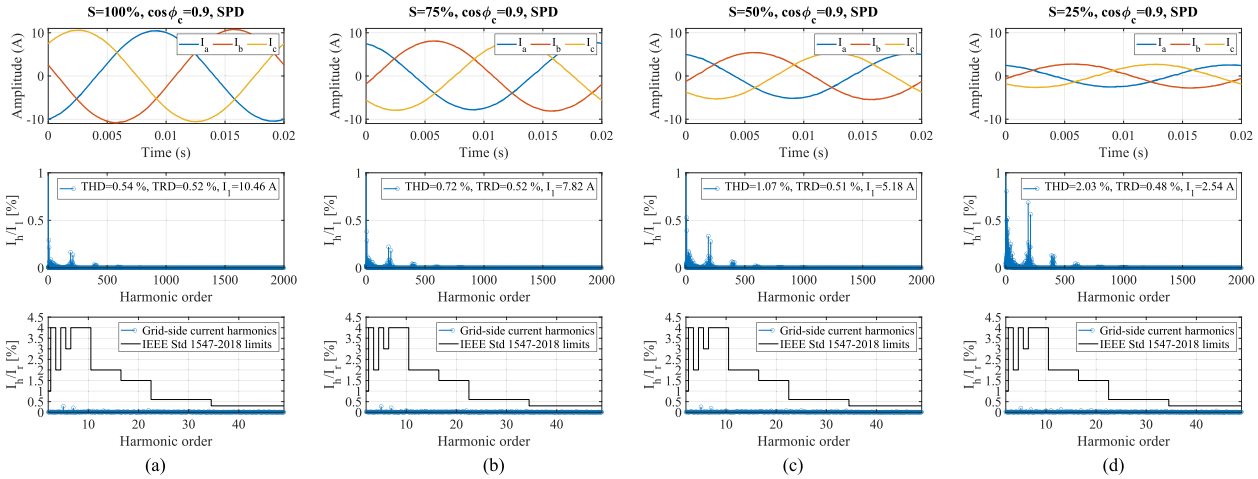

FIGURE 15. Grid-side currents obtained with SPD in: (a) WP5; (b) WP6; (c) WP7 and (d) WP8.

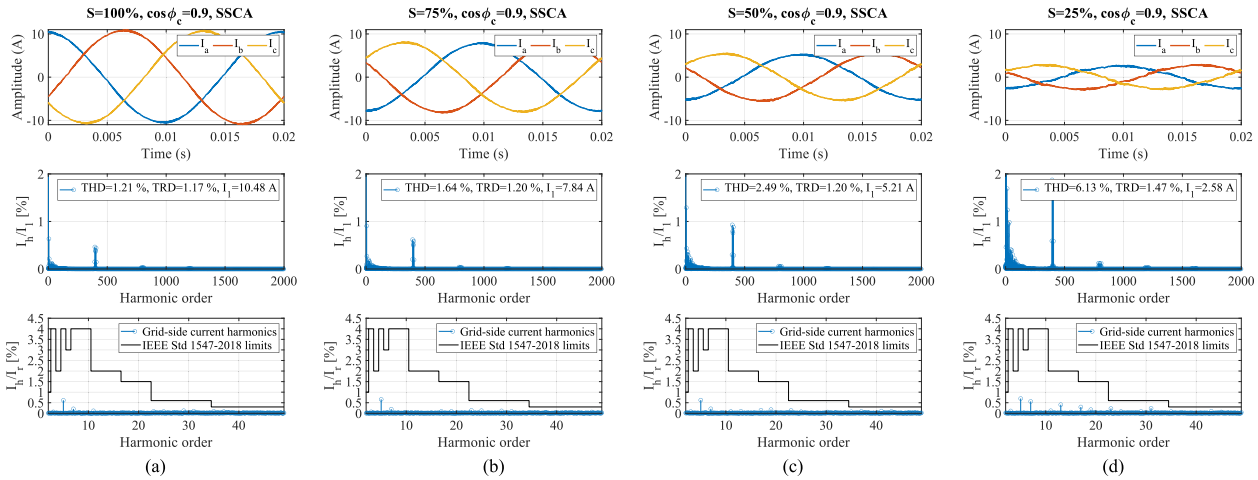

FIGURE 16. Grid-side currents obtained with SSCA-PWM in: (a) WP5; (b) WP6; (c) WP7 and (d) WP8.

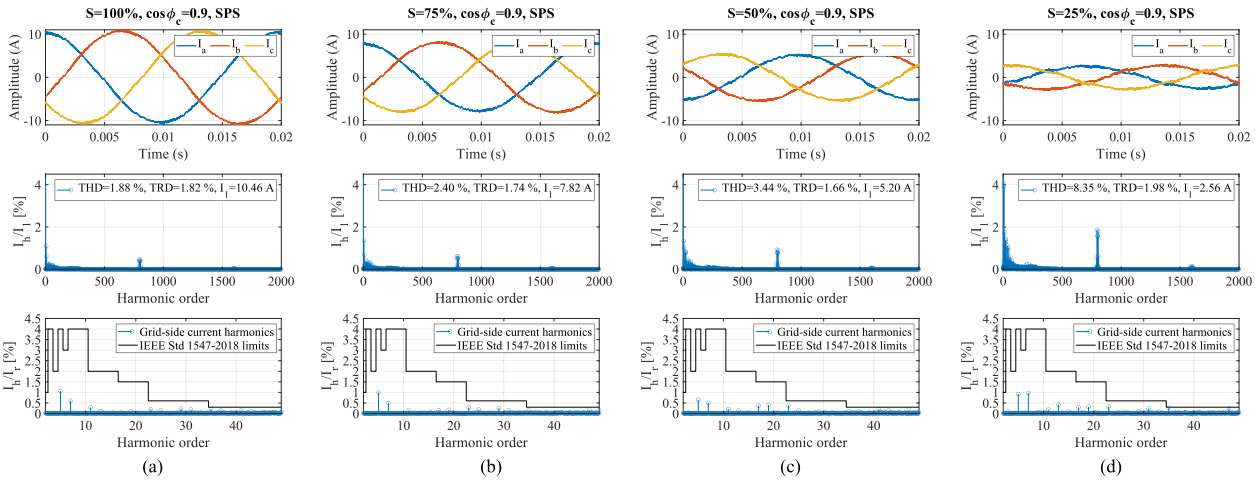

FIGURE 17. Grid-side currents obtained with SPS-PWM in: (a) WP5; (b) WP6; (c) WP7 and (d) WP8.

Looking at the previous graphs, voltage THD and current TRD variation over the defined working range are negligible, thus, DP maps are considered only for WP5 and reported in Fig. 18. Standards specify a maximum voltage THD of 8% and a maximum current TRD of 5%. The optimization procedure starts by taking into account the THD and TRD limits. Concerning Fig. 18, areas of the maps that do not meet the requirements of the standards are highlighted in red. Maps show that the current TRD values result in a stricter requirement to meet, if compared to the voltage THD, hence the couple of values chosen for optimization are related to the TRD. The DP that satisfies standard TRD limits is indicated with a cross.

Such DP can be confirmed or discarded, whether it allows to even meet the voltage and current spectra requirements or not. Also, constraints related to the voltage drop across the filter and the filter resonance frequency, reported in (37) and (38), must be met to accept a certain DP. In detail, the constraint (37) is automatically met, since lower inductances result in lower voltage drops across the filter, thus only constraint (38) will be taken into account below. With respect to the maps, the red cross represents a discarded DP and the green cross represents the accepted DP such that all standards requirements and resonance frequency constraints are met. With respect to the SPD -PWM, looking at Fig. 18(a) and (b), it can be noted that all the available DPs meet the THD and TRD requirements, thus the DP13 ($\lambda_{L12} = 40\%$, $x = 2\%$) is chosen. Since the resonance frequency is equal to 6.87 kHz with those parameters, the filter design does not satisfy the relation (38). Therefore, although harmonic requirements are met, DP13 has to be discarded. Then, to maintain the filter inductances as low as possible, DP9 is considered. It can be seen that harmonic requirements are met but (37) is not satisfied because the resonance frequency is equal to 5.61 kHz. Then, DP5 is chosen ($\lambda_{L12} = 40\%, x = 4\%$). In Figs. 19(a) and 20, the voltage and current spectra are reported, respectively,

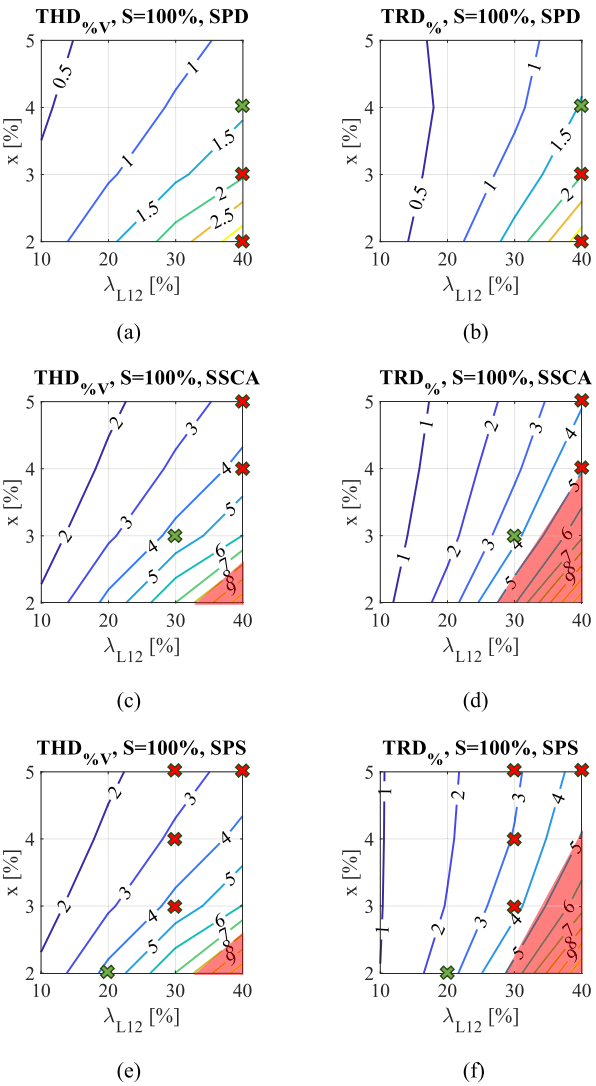

FIGURE 18. Voltage THD and Current TRD(x, λL12): (a) SPD voltage THD; (b) SPD current TRD; (c) SSCA voltage THD; (d) SSCA current TRD); (e) SPS voltage THD; (f) SPS current TRD.

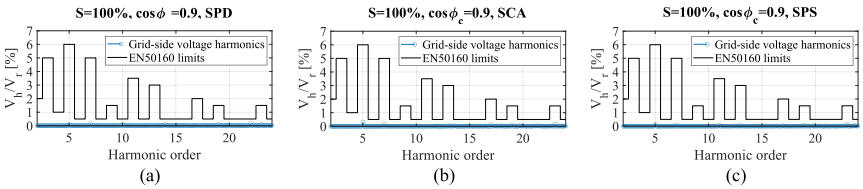

FIGURE 19. Voltage harmonics comparison with standards limitations: (a) SPD in WP5; (b) SCA in WP5; (c) SPS in WP5.

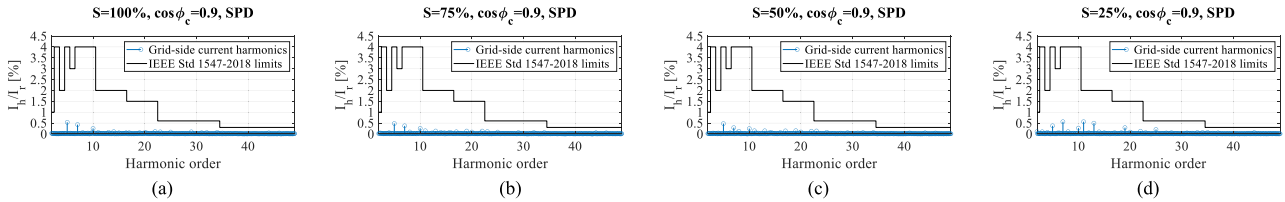

FIGURE 20. SPD Current harmonics comparison with standards limitations for DP5: (a) WP5; (b) WP6; (c) WP7; (d) WP8.

TABLE 10. Design Parameters

x [%] - λ_{L12} [%]	10	20	30	40
5	DP4	DP3	DP2	DP1
4	DP8	DP7	DP6	DP5
3	DP12	DP11	DP10	DP9
2	DP16	DP15	DP14	DP13

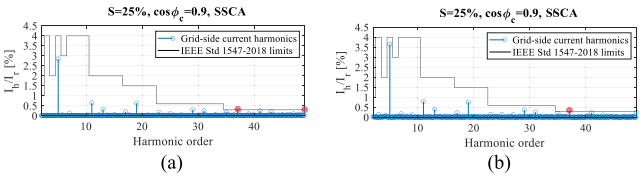

FIGURE 21. SSCA Current harmonics comparison with standards limitations: (a) DP1 in WP8; (b) DP5 in WP8.

and it can be asses that DP5 met the harmonics standard limits.

With respect to SSCA-PWM, looking at Fig. 18(c) and (d), DPs 13 ($\lambda_{L12} = 40\%$, $x = 2\%$), 9 ($\lambda_{L12} = 40\%$, $x = 3\%$), 14 ($\lambda_{L12} = 30\%$, $x = 2\%$) and 5 ($\lambda_{L12} = 40\%$, $x = 4\%$) must be excluded because the TRD requirements are not met. DP1 and DP5 satisfy the TRD requirement but, as can be seen from Fig. 21, some harmonics are higher than the standard limits, hence these two DPs must be discarded. Thus, the DP10 ($\lambda_{L12} = 30\%$, $x = 3\%$) is adopted. In Figs. 19(b) and 22, the voltage and current spectra are reported, respectively.

It can be noted that DP10 meet all the standard requirements, thus it is accepted. With respect to SPS-PWM, looking at Fig. 18(e) and (f), DPs 13, 9, 14 and 5 must be excluded. Thus, the DP10 is adopted. In Figs. 19(c) and 23, the voltage and current spectra are reported respectively. In this case, it can be noted that current spectra do not meet the standard limits in almost all the WPs adopted for this analysis. Thus, also the DP 10 is discarded and, since the TRD varies slower when moving vertically on the map, DP6 ($\lambda_{L12} = 30\%$, $x = 4\%$) is the new design parameter. By repeating the same analysis, it results that DP6 and DP2 ($\lambda_{L12} = 30\%$, $x = 5\%$) must be discarded, and DP15 ($\lambda_{L12} = 20\%$, $x = 2\%$) is accepted. Voltage and current spectra related to DP15, which meet the standard requirements, are reported in Figs. 19(c) and 24. The optimal LCL filter design values obtained by this investigation are reported in Table 11. Table 11 shows that the filter inductances and capacitance values decrease from SPD to SSCA and to SPS modulation.

If compared with values in Table 4, it can be noted that the conducted parametric analysis allowed for a drastic reduction in filter parameters. In detail, concerning SPD, the new values of inductances are half the previous, and the new value of capacitance is closer to the previous. However, it must be underlined that the resonance frequency increased and it is very close to the frequency constraint upper limit although (38) is satisfied for all three modulation techniques. A smoother parameter reduction is recorded for SSCA and SPS. Looking at Table 11, although SPS required the most severe DP, it required the lowest values of both inductances and capacitance.

To validate the effectiveness of the proposed optimal LCL filter design procedure, the system stability analysis is repeated, according to Section IV-A. Fig. 25 shows the open loop current transfer function frequency response for each considered MC-PWM schemes, where gain and phase margins are shown. Looking at Fig. 25, it can be noted that the Gain Margins (GM) are equal to 16.3 dB, 21.6 dB and 26.9 dB for SPD, SSCA and SPS, respectively. Moreover, the Phase Margins (PM) are equal to 73.2°, 65.3° and 51.7° for SPD, SSCA and SPS, respectively. It must be underlined that this analysis confirms that the proposed optimal LCL filter design procedure still ensure robust system stability independently of the adopted MC-PWM strategy. Moreover, it is interesting to note that an increment in gain margins is recorded, demonstrating the benefits of the proposed optimal method also in terms of system robustness.

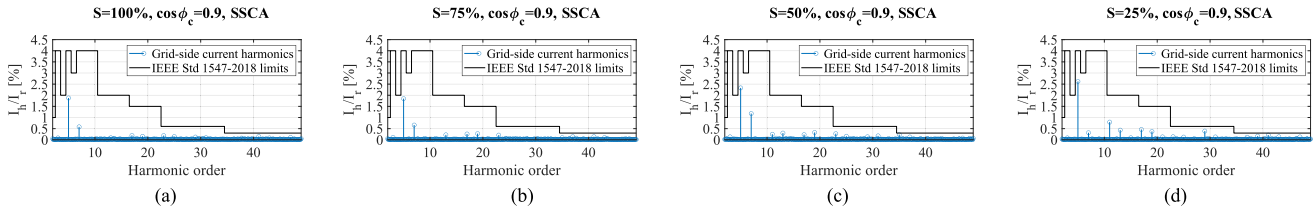

FIGURE 22. SSCA Current harmonics comparison with standards limitations for DP10: (a) WP5; (b) WP6; (c) WP7; (d) WP8.

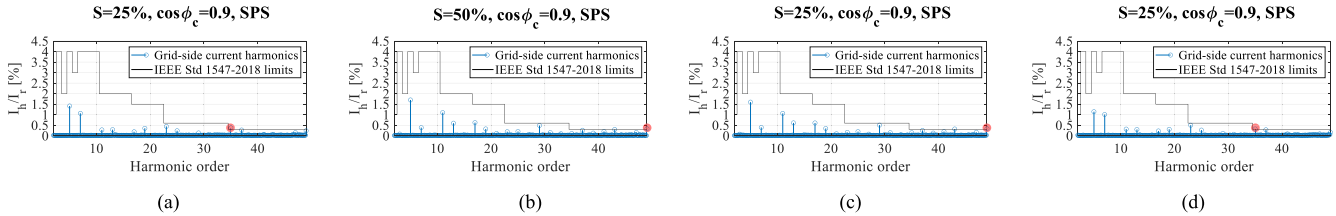

FIGURE 23. SPS Current harmonics comparison with standards limitations: (a) DP1 in WP8; (b) DP2 in WP7; (c) DP6 in WP8; (d)DP10 WP8.

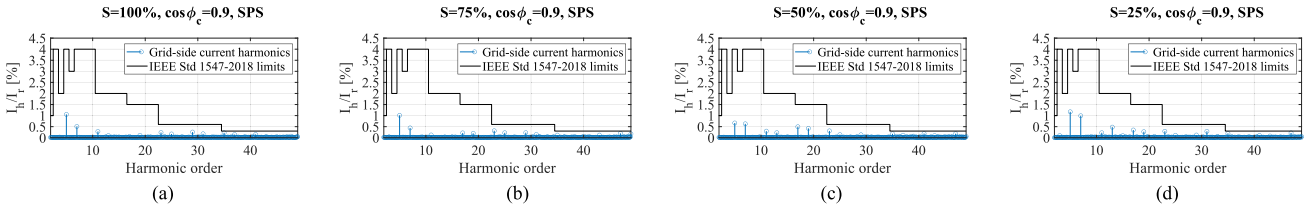

FIGURE 24. SPS Current harmonics comparison with standards limitations for DP15: (a) WP5; (b) WP6; (c) WP7; (d) WP8.

C. OPTIMAL LCL FILTER DESIGN GUIDELINES

By looking at the results presented in the previous subsections, it is possible to summarize the main considerations discussed so far and provide an optimal LCL filter design procedure. The main design considerations are summarized below:

- the voltage THD and the current TRD are poorly influenced by the power factor and by the injected apparent power. Then, it can be stated that one WP, e.g., WP 5, can be representative of the whole working range and such parameters can be computed only in one WP;
- The voltage harmonic spectrum is poorly influenced by the power factor and by the injected apparent power, since the grid voltage does not vary significantly and, consequently, the inverter works with quite a constant amplitude modulation index. Then, it can be stated that the voltage harmonic spectrum can be investigated only in one representative WP, e.g., the WP 5;
- The current harmonic spectrum is influenced by the injected apparent power such that the amplitude of the current harmonics decreases when the injected apparent power increases. Standards recommend checking the harmonic limits only in the rated working conditions. However, since the injected apparent power could vary depending on the grid conditions, it is recommended to check the current harmonic limits over a wide working range;
- Taking into account the MC-PWM strategy allows for matching the standard requirements with different LCL filter parameters, which are customized to the adopted MC-PWM strategy. Such a result is guaranteed only if proper coordination between the designed LCL filter and the PI tuning parameters is carried out;
- The proposed design procedure guarantees a reduction of the LCL filter parameters for every considered MC-PWM strategy. In other words, the proposed LCL filter design procedure allows for matching the standard requirements by adopting more relaxed DPs. Then, it is suggested to start the design procedure by adopting very relaxed DPs and modifying them progressively until the standard requirements and constraints are matched;
- The proposed design procedure guarantees an improvement also in terms of control system robustness, as can be seen by looking at gain and phase margins.

According to the considerations made so far, it is possible to provide an optimized LCL filter design procedure that aims to fulfill the following goals: for fixed design parameters λ_{L12} and x, it allows for customizing the filter according to the adopted MC-PWM strategy; moreover, for fixed MC-PWM strategy, the proposed optimization procedure allows for

TABLE 11. LCL Filter Design Optimized Values

Symbol	Quantity	Modulation		
		SPD	SSCA	SPS
L_1	Converter-side inductance [μH]	160	106	79
L_2	Grid-side inductance [μH]	160	106	79
C_f	Filter capacitance [μF]	13.4	5.04	1.68
R_d	Damping resistance [Ω]	0.81	1.08	1.62
f_{res}	Resonance frequency [kHz]	4.86	9.72	19.4

obtaining the lowest LCL filter parameters which satisfy the standards and the design constraints. The algorithm consists of the following steps:

1) The system parameters, i.e., the rated apparent power, the number of inverter voltage levels, the DC link voltage, the switching frequency, and the adopted MC-PWM strategy, are set as input values of the design procedure;
2) The desired values of current ripple λ_{L12} and maximum reactive power relative to the inverter rated power x are set to design the filter inductances, capacitance, and damping resistance. It must be noted that the current ripple λ_{L12} should not exceed 40 % of the inverter rated current to guarantee a limited amount of grid-side current ripple. Moreover, the value of x should not be greater than 5% of the inverter-rated power to avoid a high inverter power factor reduction;
3) The filter inductances, capacitance, and dumping resistor are calculated for the previously adopted values of λ_{L12} and x by applying (25), (26), (34), (35), and (36);
4) Equations (37) and (38) are adopted to verify the filter voltage drop constraint and the filter resonance constraint, respectively. If at least one of the constraints is not met, the design procedure restarts at point 2) and new values of λ_{L12} and x must be chosen. In detail, if (37) is violated, a higher value of λ_{L12} must be chosen to obtain a value of L_{12} which satisfies the constraint (37). If (38) is not met, two options are available: if x can still be increased, then a higher value of x must be chosen, for fixed λ_{L12}; otherwise, λ_{L12} must be reduced and the value of x is set to the lowest value to maintain to minimize the filter capacitance;
5) If the two constraints are met then standards EN50160 and IEEE Std 1547–2018 must be verified. In case of failure the procedure restarts at point 2) again by choosing new values of λ_{L12} and x. It should be noted that lower values of λ_{L12} result in lower grid-side current harmonics achieved with higher values of filter inductances, as can be seen from (25). Moreover, higher values of x result in lower grid-side voltage harmonics achieved with higher filter capacitance values, as can be seen from (34). Therefore, the design values have to be chosen wisely.

In Fig. 26 a flow chart of the design procedure is shown.

The proposed LCL filter design procedure allows for matching the standard requirements by adopting more relaxed

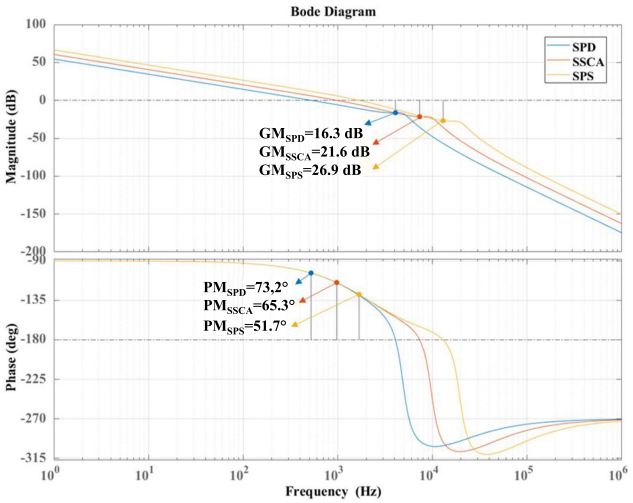

FIGURE 25. Optimal open loop transfer function Bode plots.

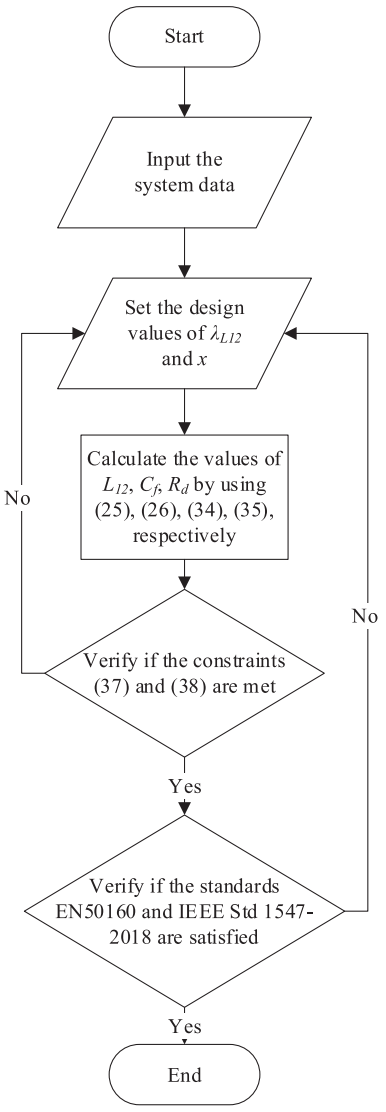

FIGURE 26. Proposed filter design method flow chart.

TABLE 12. Typical and Optimal LCL Filter Design

DP	Typical values [28]	optimal values		
		SPD	SSCA	SPS
λ_{L12} [%]	20	40	30	20
x [%]	5	4	3	2

design parameters (λ_{L12} relaxed if higher than typical value, x relaxed if lower than typical value), if compared to that typically adopted in the literature. It follows that, by considering the specific MC-PWM strategy in the filter design process, it is possible to drastically reduce the filter weight, bulk, and cost. A comparison between typical and optimal design values is reported in Table 12. It can be noted that DP relaxing is guaranteed for every considered MC-PWM strategy.

VI. CONCLUSION

In this work, a novel LCL filter design method for grid-connected CHBMI is proposed. The proposed design method aims to maximize the system steady-state performance in terms of harmonic distortion, without oversizing the filter, which impacts the system bulk, weight, and cost. The key novelty of the proposed method deals with generalizing the design process by taking into account the number of MI voltage levels, the adopted MC-PWM strategy, the DC link voltage, and the switching frequency. The proposed design procedure is based on an analytical approach that adopts two main design parameters, i.e., the maximum current ripple λ_{L12}, expressed in percent of the rated current, and maximum reactive power relative to the inverter rated power x. In detail, the dependency on the MC-PWM strategy of such design parameters is explained through a simple and easy-of-use coefficient C_{MC} which allows for updating the filter values depending on the harmonic shift over the spectrum that the adopted MC-PWM strategy determines. Moreover,the C_{MC} allows for taking into account the adopted MC-PWM impact also in the PI tuning process, such that the PI tuning parameters are coordinated with the designed LCL filter, guaranteeing optimal steady-state behaviour without oversizing the LCL filter. Derived formulas have been generalized for any MC-PWM strategy. It must be highlighted that the filter design procedure is carried out for grid-connected CHBMI, however, it can be applied to any MI topology.

To validate the proposed approach, several HIL tests have been carried out. In detail, the SPD, SPS, and SSCA PWM strategies are selected as representative MC-PWM strategies. As comparison tools, the voltage THD, the current TRD, and the grid voltage and current spectra have been deeply investigated and compared to the standards limits reported in the EN50160 and the IEEE Std 1547–2018. Two main analyses have been carried out. At first, the LCL filters are designed for every considered MC-PWM strategy with a couple of design parameters commonly adopted in the literature (i.e., $\lambda_{L12} = 20\%$ and $x = 5\%$). The system behavior is analyzed over a working range defined by 16 WPs, identified by the injected apparent power and the power factor. This analysis showed that the adopted modulation strategy has a significant impact on the design process; indeed, each MC-PWM strategy requires a custom filter, which is optimized with respect to voltage and current harmonic displacement over the spectra. Moreover, results show that the adopted couple of design parameters determine a filter oversizing, i.e., the standard requirements are matched with a wide margin.

Thus, the second analysis deals with finding a couple of design parameters that meet standards constraints without oversizing the filter. For this purpose, sixteen DPs are adopted and per each one, the previous analysis in terms of voltage THD, current TRD, and voltage and current spectra, is carried out. Results show that, depending on the adopted MC-PWM strategy, it is possible to drastically reduce the filter parameters, with a subsequent reduction of the filter bulk, weight, and cost.

In addition, in both analyses, the control system stability is verified by investigating the open-loop current transfer function. Results related to the second analysis show an improvement in the system stability in terms of gain margins, for every considered MC-PWM strategy.

Finally, the main results obtained in previous analyses are summarized and the proposed LCL filter design procedure is synthesized in a block diagram to provide guidelines for effective filter design for multilevel inverters.

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