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# A ZVS High Step-Down Converter With Reduced Component Count and Low Ripple Output Current

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**ABSTRACT** In this paper, a new synchronous rectified converter with ultra-low output current ripple and high voltage attenuation is proposed. The presented converter can achieve soft switching without requiring any additional active components, leading to high efficiency while maintaining the simplicity of conventional converters. Other main features of the proposed circuit are inherent shoot-through protection, reduced current stress of the semiconductors due to the coupled inductor, and low voltage stress across the low-side MOSFET. In addition, a pulse frequency modulation control scheme is used, which allows for an extended soft-switching range without imposing an excessive circulating current at light loads. The steady-state analysis and experimental results from a 120 W prototype are presented in this paper.

**INDEX TERMS** High step-down converter, coupled inductor converter, duty cycle extension, synchronous rectification, zero voltage switching.

## I. INTRODUCTION

There has been a considerable and growing demand for low-voltage high-current DC power supplies in various applications, including battery chargers, data centers, LED drivers, and electric vehicles over the past decade. As a result, the performance improvement of high step-down converters has drawn the interest of many researchers [1], [2], [3], [4]. Unless safety considerations require galvanic isolation of the input and output, isolated converters are not suitable for such applications due to their high cost, complexity, volume, and losses [5], [6].

In step-down applications, buck converters are traditionally used due to their simple structure, continuous output current, and cost-effectiveness. However, they suffer from several disadvantages, primarily caused by their narrow duty cycles and hard switching conditions. These drawbacks include decreased efficiency, reduced power density, poor dynamic response, high current stress on the switch, and control and gate drive complications [7], [8]. Several non-isolated high step-down converters are proposed to resolve the issues of conventional converters. Nonetheless, they generally suffer from either of the following disadvantages: 1) narrow operating duty cycle, 2) low efficiency, 3) high component count, and 4) complexity [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32].

Interleaved buck converters (IBCs) are one of the approaches widely used in high output current applications to achieve reduced conduction losses, output current ripple cancellation, and improved dynamic response [9]. Nevertheless, IBCs in high step-down applications suffer from a high component count, and control complications along with the narrow operating duty cycle, which results in poor current ripple cancellation [10].

Cascaded converters are the simplest method to extend the operating duty cycle of conventional converters. However, this approach suffers from a high component count and low efficiency [11]. The series converters are combined in quadratic topologies to reduce the number of switches [12], [13]. Nonetheless, the switch has to withstand high voltage and current stresses in quadratic structures, which reduces the converter efficiency. Another approach to enhance the voltage

gain of the conventional interleaved buck converters is to employ series capacitors, which can also decrease the voltage stress across the MOSFETs [14], [15], [16]. Nevertheless, these converters suffer from the hard switching condition of MOSFETs and a high component count. A series-resonant structure is introduced in [17], [18], [19] to reduce the switching losses of the conventional series capacitor converters. However, the high-side (HS) MOSFETs in [17], [18] still suffer from hard switching turn-on, and the low-side MOSFETs turn on under zero current switching (ZCS), which does not affect the output capacitance losses of the switch. To effectively eliminate the switching losses of the MOSFET, it should operate under zero voltage switching (ZVS), in which not only the voltage-current overlap is eliminated, but also the output capacitance losses become negligible [20].

Another beneficial approach to extending the duty cycle of conventional synchronous rectifier (SR) buck converters is to utilize coupled inductors (CI) or tapped-inductors (TI) [21], [22], [23]. This method can also be used in combination with the series capacitors [24], [25], [26], [27], [28], [29], [30], [31], [32]. The main strategy for extending the duty cycle in these step-down converters is to generate a voltage source opposite to the input voltage. This approach reduces the effective voltage applied to the output inductor during the power transfer to the output. In CI converters, a portion of the energy is directly transferred through the coupled inductor to the output, which helps improve efficiency. The other main advantages of the CI topologies are their simplicity, low component count, and flexibility. A comparative analysis is conducted in [33] between various high step-down converters for battery charging applications, concluding that TI buck converters are the most efficient method. Nevertheless, the TI buck converter suffers from voltage spikes over the drain source of the main MOSFET at turn-off instants caused by the parasitic leakage inductances [21], [22], [23]. Lossless passive clamp circuits are an effective way to absorb the excessive energy stored in the leakage inductance, and consequently suppress the voltage spike over the drain source of the HS MOSFET [29]. Lossless snubber and active clamp circuits are other methods widely used not only to eliminate the voltage overshoot across the main MOSFET but also to provide soft switching conditions for it [24], [25], [26], [27], [28], [30]. However, all these methods require additional circuitry, which complicates the converter. Another drawback of the coupled inductor converters introduced in [21], [22], [24], [25], [32] is the pulsating output current, which causes excessive Equivalent Series Resistance (ESR) losses of the output capacitance and reduces its lifespan.

This paper aims to introduce a new coupled inductor synchronous rectifier converter with continuous output current which achieves duty cycle extension along with the ZVS operation of the MOSFETs under a wide load range. Achieving ZVS operation of the MOSFETs is significant since it leads to a major reduction of the switching losses and electromagnetic interferences (EMI). The proposed converter does not require additional semiconductors or complex circuits to provide ZVS for the MOSFETs, which further enhances the simplicity and efficiency of the converter. The MOSFETs are driven by simple boot-strap gate drivers, eliminating the need for relatively more complex transformer-isolated or opt-isolated gate drivers. Furthermore, the reverse recovery losses of the proposed converter are negligible owing to the leakage inductances.

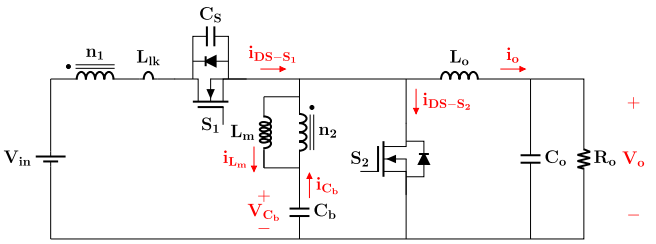


**FIGURE 1.** Proposed high step down converter.

## II. OPERATION PRINCIPLE OF THE PROPOSED HIGH STEP-DOWN CONVERTER

The proposed high step-down converter is presented in Fig. 1. The proposed converter contains one high-side MOSFET, $S_1$, one synchronous rectifier, $S_2$, a coupled inductor with windings $n_1$ and $n_2$, one blocking capacitor, $C_b$, an output inductor, $L_o$, and one output capacitor, $C_o$. a snubber capacitor, $C_s$, is also placed in parallel of the HS MOSFET to provide the zero voltage switching (ZVS) at turn-off instants.

Fig. 2 illustrates the Theoretical waveforms of the proposed converter, which include the control pulses along with the drain-source voltages and currents of each MOSFET, and the current flowing through the blocking capacitor, $i_{C_b}$ .

According to Fig. 2, the proposed converter contains 6 modes of operation in each switching period. The equivalent circuit during each operating mode is presented in Fig. 3. The following assumptions are made to simplify the theoretical analysis of the proposed converter:

1) $C_b$ and $C_o$ are relatively large enough that the voltage across them is considered constant.
2) $L_o$ is relatively large and the output current ripple is negligible.
3) The coupled inductors are modeled as an ideal transformer with turns ratio $n_1$ and $n_2$, where $n = \frac{n_2}{n_1+n_2}$, a magnetizing inductance $L_m$, and a leakage inductance $L_{lk}$.
4) All the semiconductor and passive devices are considered to be ideal.

The operation principle of the proposed converter is described as follows. It should be noted that prior to $t_0$, it is assumed that $S_1$ is on and the synchronous rectifier (SR), $S_2$, is off. Thus, $n(V_{in} - V_{C_b})$ is applied to the magnetizing inductance, which increases its current to $I_{L_m(\max)}$ at $t_0$. The value of $I_{L_m(\max)}$ is derived in Section III.

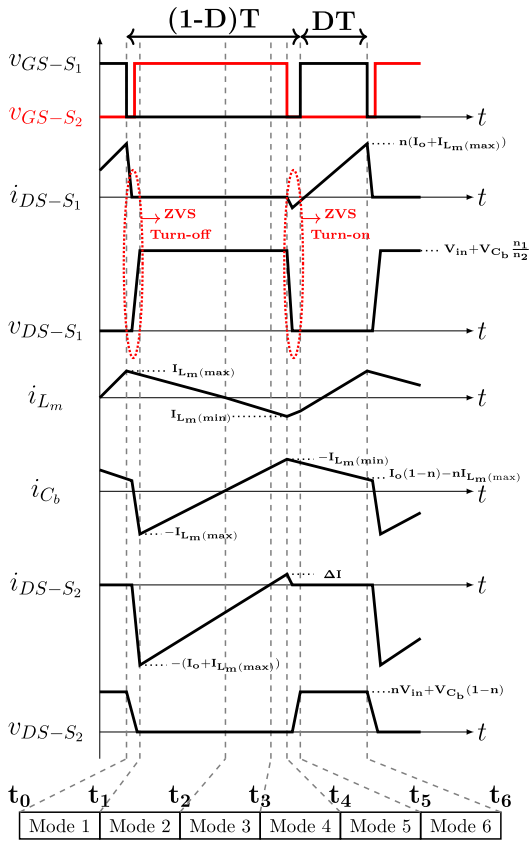


**FIGURE 2.** Key waveforms of the proposed converter.

#### 1) MODE 1 ($t_0 \leq t < t_1$) [FIG. 3(A)]

At the beginning of this mode, $S_1$ is turned off under ZVS condition, due to the existing snubber capacitor, $C_s$, in parallel with the switch. As the drain-source current of $S_1$ decreases, $C_s$ is charged and the voltage across $S_2$ is reduced, then the body diode of $S_2$ starts to conduct. This provides the condition for $S_2$ to be turned on under ZVS. As $S_2$ is turned on, its current increases until it reaches the sum of the magnetizing inductance current and the output current, $I_{L_m(\max)} + I_o$. It should be noted that, since this interval is relatively small, the magnetizing inductance current is assumed to be constant and equal to $I_{L_m(\max)}$ during this mode to simplify the analysis.

During this interval, a resonance between $C_s$ and $L_{lk}$ occurs, in which the voltage across $C_s$ rises. It should be noted that the drain source voltage of $S_1$ is equal to $v_{C_s}$. This mode ends when $v_{DS-S_1}$ reaches $V_{in} + V_{C_b}\frac{n_1}{n_2}$. The voltage across $C_s$ and the resonance current during this mode can be calculated by:

$$v_{C_s}(t) = \left(V_{in} + V_{C_b}\frac{n_1}{n_2}\right)(1 - \cos(\omega_{res}(t - t_0))) + Z_{res} n \left(I_{L_m(\max)} + I_o\right)\sin(\omega_{res}(t - t_0)), \quad (1)$$

$$i_{in}(t) = \left(\frac{V_{in} + V_{C_b} n_1/n_2}{Z_{res}}\right)\sin(\omega_{res}(t - t_0)) + n\left(I_{L_m(\max)} + I_o\right)\cos(\omega_{res}(t - t_0)), \quad (2)$$

where $\omega_{res}$ is the resonant frequency ($\omega_{res} = \frac{1}{\sqrt{L_{lk}C_s}} = 2\pi f_{res}$), and $Z_{res}$ is the characteristic impedance of $L_{lk}$ and $C_s$, ($Z_{res} = \sqrt{\frac{L_{lk}}{C_s}}$).

#### 2) MODE 2 ($t_1 \leq t < t_2$) [FIG. 3(B)]

In this mode, the voltage across $C_b$ is induced over $L_m$, which linearly decreases its current. This mode ends when the magnetizing inductance current reaches zero. The duration of this mode can be calculated by:

$$t_2 - t_1 = L_m \frac{I_{L_m(\max)}}{V_{C_b}}. \quad (3)$$

#### 3) MODE 3 ($t_2 \leq t < t_3$) [FIG. 3(C)]

At $t_2$, the voltage across $C_b$ continues to charge $L_m$ in the opposite direction. Therefore, the polarity of $i_{L_m}$ changes to negative. This mode ends when the magnetizing inductance current reaches $-I_o$, and the current of $S_2$ becomes zero. The duration of this mode can be calculated by:

$$t_3 - t_2 = L_m \frac{I_o}{V_{C_b}}. \quad (4)$$

#### 4) MODE 4 ($t_3 \leq t < t_4$) [FIG. 3(D)]

During this mode, $S_2$ remains on. Therefore, the voltage across $C_b$ still charges $L_m$ in the opposite direction until $i_{L_m}$ reaches to its minimum value, $I_{L_m(\min)}$, at $t_4$. The value of the magnetizing inductance current at $t_4$ can be defined as:

$$I_{L_m(\min)} = -(I_o + \Delta I). \quad (5)$$

The duration of this mode can be calculated by:

$$t_4 - t_3 = L_m \frac{\Delta I}{|V_{C_b}|}. \quad (6)$$

It is noteworthy to mention that the main objective of reducing the magnetizing inductance current to $I_{L_m(\min)}$ is that it can provide the output current while the excess current, $\Delta I$, can fully discharge the snubber capacitor and provide the condition for $S_1$ to turn on under ZVS. Thus, $\Delta I$ should be high enough so that $L_m$ has enough energy to discharge the snubber capacitor and make the body diode of $S_1$ start conducting. However, increasing $\Delta I$ excessively leads to a higher current stress of $S_2$ and increased conduction losses. Therefore, it is desired to design $\Delta I$ to be the minimum value to guarantee the soft switching condition for $S_1$. The optimum value of $\Delta I$ is derived in section V. However, to simplify the analysis and regarding the fact that the output current of high step-down converters is relatively large, $\Delta I$ can be neglected.

$$I_{L_m(\min)} \simeq -I_o. \quad (7)$$

#### 5) MODE 5 ($t_4 \leq t < t_5$) [FIG. 3(E)]

This mode starts when $S_2$ is turned off. It should be noted that $S_2$ is a high-current low-voltage MOSFET, which typically has a high drain-to-source capacitance. Therefore, the inherent high capacitance in parallel with the MOSFET along with $C_s$ provides the ZVS turn-off condition for the MOSFET.

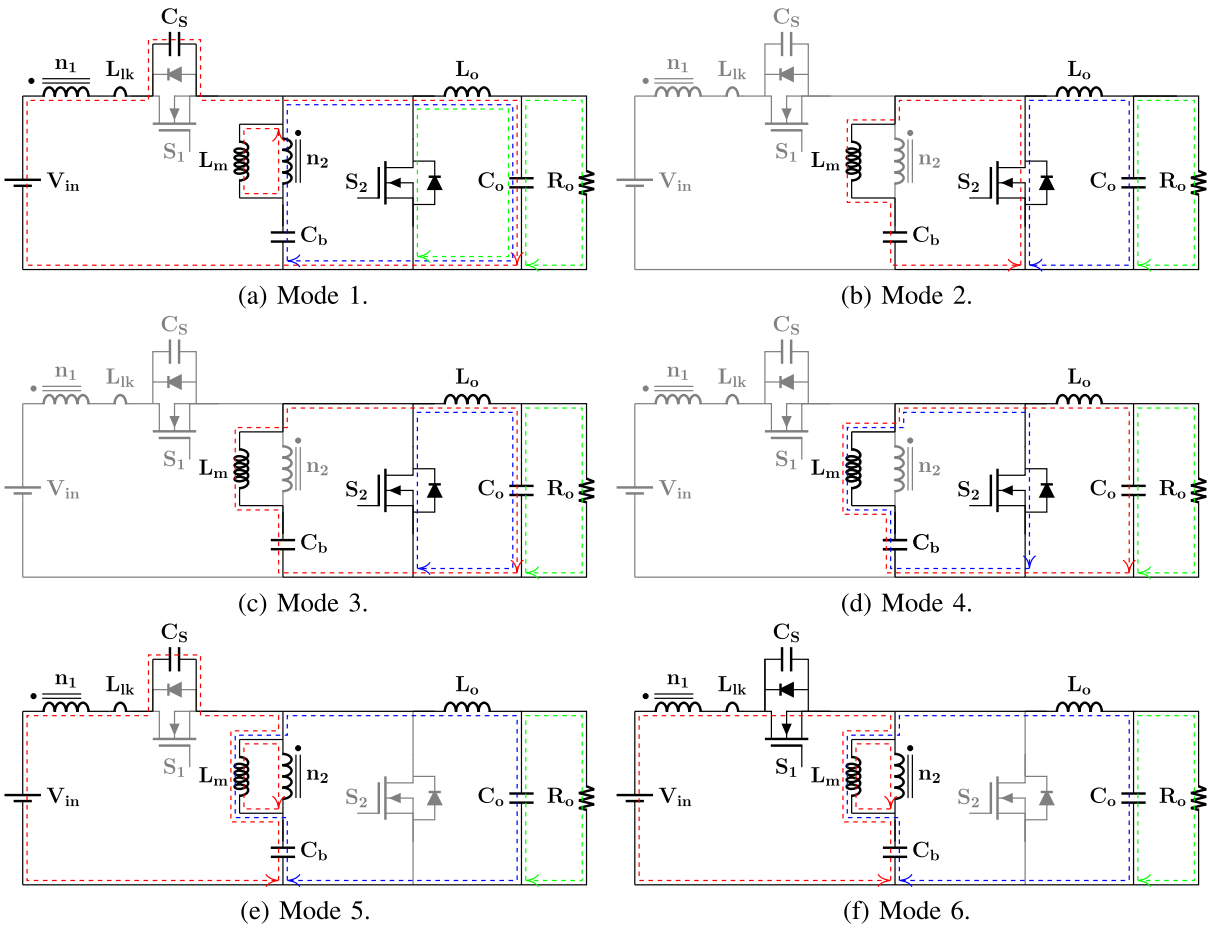


**FIGURE 3.** Equivalent circuit of the proposed converter during each operating mode. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

During this mode, $\Delta I$ flows through $C_s$ and discharges it. Therefore, the drain-source voltage of $S_1$ reaches zero, and the main switch can be turned on under ZVS.

### 6) MODE 6 ($t_5 \leq t < t_6$) [FIG. 3(F)]

In This mode, $S_1$ is turned ON under ZVS. During this mode, the energy is transferred from the input to the load. also the current in $L_m$ increases linearly, with the slope of $\frac{n(V_{in}-V_{C_b})}{L_m}$, until it reaches $I_{L_m(\max)}$ at $t_6$. This interval's duration is equal to $DT$, where $D$ is the duty cycle.

## III. STEADY-STATE ANALYSIS

As previously mentioned, the value of $C_b$ is considered large enough that $V_{C_b}$ remains approximately constant. The average voltage across $C_b$ can be derived by applying the volt-second balance for $L_m$ as follows:

$$V_{C_b} = nV_{in}\frac{D}{1-D+nD}. \tag{8}$$

Neglecting mode 5in which both $S_1$ and $S_2$ are OFF, the voltage gain of the proposed converter can be derived by applying the volt-second balance for $L_o$ and substituting $V_{C_b}$ with (8) as following:

$$M = \frac{V_o}{V_{in}} = \frac{nD}{1-D+nD}. \tag{9}$$

Therefore, $V_{C_b}$ is equal to the output voltage, $V_o$. Fig. 4 illustrates the voltage gain of various step-down converters against the proposed converter at different duty cycles.

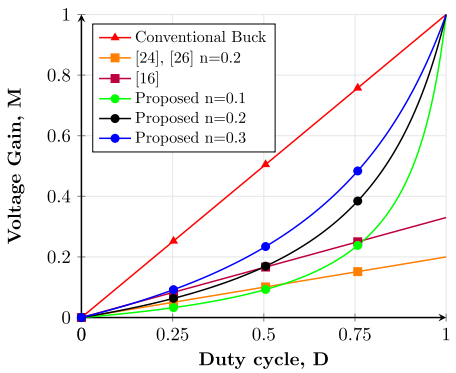


**FIGURE 4.** Voltage gain for various step-down converters versus the operating duty cycle.

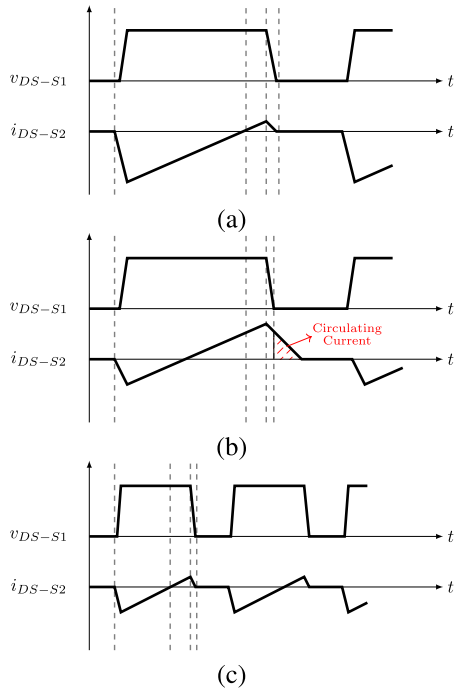


**FIGURE 5.** Drain-source voltage of $S_1$ and the current of $S_2$ at different conditions, (a) Full-load, (b) Light-load with TCM control method, and (c) Light-load with QSW-ZVS control method.

The maximum current of the magnetizing inductance, $I_{L_m(\max)}$ can be derived by using the charge balance of $C_b$.

$$I_{L_m(\max)} = I_o \frac{1 + D - nD}{1 - D + nD}. \tag{10}$$

As previously mentioned, the current of $L_m$ increases/decreases linearly during the operation modes of the proposed converter. Therefore, the average value of the magnetizing inductance current can be written as follows:

$$I_{L_m(mean)} = \frac{I_{L_m(\max)} + I_{L_m(\min)}}{2}. \tag{11}$$

Therefore, the average current of $L_m$ can be calculated by using the (10) and (11), and with regarding the assumption made in (7) as follows:

$$I_{L_m(mean)} = I_o \frac{D - nD}{1 - D + nD}. \tag{12}$$

As explained, to provide the soft switching condition for the main MOSFET of the proposed converter, $i_{L_m}$ is required to become lower than $-I_o$ at $t_4$. Therefore, in case the output load decreases, the magnetizing inductance current reaches the desired value in a shorter time. This gives two approaches for the operation of the converter at light load conditions:

1) Triangular Current Mode (TCM) [See Fig. 5(b)]: The time interval of modes 2 to 4, $t_{41} = t_4 - t_1$, can be kept constant at the light load condition. Thus, the magnetizing inductance current is reduced to values much lower than $-(I_o + \Delta I)$ at $t_4$, which results in a circulating current and in turn reduces the efficiency of the converter at light loads. The main advantage of this approach is its simplicity since the operating switching frequency is kept constant at different load conditions.
2) Quasi-Square Wave mode (QSW-ZVS) [See Fig. 5(c)]: The second approach is to reduce $t_{41}$ in accordance with the output load. In other words, the switching period of the proposed converter should be reduced as the output current decreases. This way, $i_{L_m}$ is reduced just enough to provide the soft switching condition. Thus, the excessive magnetizing inductance current of the first approach is eliminated, which results in the efficiency enhancement of the converter under wide load conditions.

Based on the mentioned advantages of the second approach, it is considered more beneficial for the proposed converter and is selected as its control strategy.

As explained, in the second method, $t_{41}$ is designed so that the magnetizing inductance current reaches from $I_{L_m(\max)}$ to $-I_o$ at $t_4$. As shown in Fig. 3, $t_{54}$ is equal to $DT_{sw}$. Thus:

$$t_{54} = \frac{2L_m I_o}{n\,(V_{in} - V_o)\,(1 - D + nD)} = DT_{sw}. \tag{13}$$

The operating duty cycle of the converter can be written based on (9) as follows:

$$D = \frac{V_o}{n\,(V_{in} - V_o) + V_o}. \tag{14}$$

Substituting (14) in (13) gives the switching period of the converter as follows:

$$T_{sw} = \frac{1}{f_{sw}} = \frac{2I_o L_m (n\,(V_{in} - V_o) + V_o)^2}{n^2 V_{in} V_o\,(V_{in} - V_o)}. \tag{15}$$

According to (15), the switching frequency is inversely related to the output current, since all the other parameters are considered constant during the converter operation.

As discussed, during Mode 4, the extra energy of the magnetizing inductance should be enough to fully discharge $C_s$ and the output capacitance of $S_1$, $C_{oss-S_1}$, from $V_{in} + \frac{n_1}{n_2}V_o$, while charging the output capacitance of $S_2$, $C_{oss-S_2}$, to $nV_{in} + V_{C_b}(1 - n)$. Thus, $\Delta I$ should be designed to guarantee the soft switching condition for $S_1$ at all operating conditions. The worst-case scenario for that is when the converter is working at light load conditions, and the energy stored in the magnetizing inductance is minimal. Thus:

$$\frac{1}{2}L_m\left(\left(I_{o(LL)} + \Delta I\right)^2 - {I_{o(LL)}}^2\right) = \frac{1}{2}\left(C_s + C_{oss-S_1}\right) \times \left(V_{in} + \frac{n_1}{n_2}V_o\right)^2 + frac12C_{oss-S_2}(nV_{in} + V_o\,(1 - n))^2, \tag{16}$$

where $I_{o(LL)}$ is the output current at light load condition. Solving (16) results in the optimal value of $\Delta I$ to ensure that the proposed converter operates under ZVS at the full load range, as follows:

$$\Delta I = \left(\frac{C_s + C_{oss-S_1} + n^2 C_{oss-S_2}}{2I_{o(LL)}L_m}\right)\left(V_{in} + \frac{n_1}{n_2}V_o\right)^2. \tag{17}$$

**TABLE 1.** Voltage and Current Stress of Semiconductor Devices

| | Maximum Voltage | Maximum Current |
|---|---|---|
| $\mathbf{S_1}$ | $V_{in}+\frac{n_1}{n_2}V_o$ | $I_o\frac{2(n(V_{in}-V_o)+V_o)}{V_{in}}$ |
| $\mathbf{S_2}$ | $nV_{in}+V_o\,(1-n)$ | $I_o\frac{2(n(V_{in}-V_o)+V_o)}{nV_{in}}$ |

To mitigate the impact of line variation on the ZVS operation of the proposed converter, $\Delta I$ is designed at the maximum input voltage in (17). This ensures that the magnetizing inductance energy is sufficient to fully discharge the $C_s$ and the output capacitance of $S_1$, thereby turning on the body diode even at lower input voltages.

According to to (15), the value of the magnetizing inductance $L_m$, can be obtained at full load condition as follows:

$$L_m=\frac{n^2D^2V_{in}(V_{in}-V_o)}{2I_{o(FL)}V_of_{sw}}. \tag{18}$$

where $I_{o(FL)}$ is the output current at full load condition.

The values of $C_b$, $C_o$, and $L_o$ are obtained by the following equations:

$$C_b=\frac{I_oD}{\Delta V_{C_b}f_{sw}}, \tag{19}$$

$$C_o=\frac{I_o(1-D)}{\Delta V_of_{sw}}, \tag{20}$$

$$L_o=\frac{V_o(1-D)}{\Delta I_of_{sw}}, \tag{21}$$

where $\Delta V_{C_b}$ is the voltage ripple of the blocking capacitor, $\Delta V_o$ is the output voltage ripple, and $\Delta I_o$ is the output current ripple. It is important to note that the output inductor is designed to ensure that the maximum peak-to-peak output current ripple is less than 30% of the load, thereby achieving a low ripple output current.

The voltage and current stress equations of the semiconductor devices of the proposed converter are given in Table 1.

## IV. LOSS ANALYSIS

In this section, a detailed loss analysis of the proposed converter is presented. Regarding the ZVS condition of $S_1$ and $S_2$, the switching losses of the proposed converter are negligible. Thus, the total losses of the proposed converter consist of the conduction losses of the MOSFETS, $P_{cond}$, the capacitors ESR losses, $P_{ESR}$, the coupled inductor losses, $P_{ind}$, and the gate drive losses, $P_{gate}$. It is noteworthy to mention that the leakage inductance of the coupled inductor and the value of $\Delta I$ are considered insignificant in obtaining the losses of the proposed converter, hence they are neglected.

### A. CONDUCTION LOSSES

The RMS currents flowing through $S_1$ and $S_2$ can be derived by:

$$I_{rms-S_1}\simeq\frac{2P_o}{V_{in}}\sqrt{\frac{1}{3D}}, \tag{22}$$

$$I_{rms-S_2}\simeq\frac{2P_o}{nDV_{in}}\sqrt{\frac{(1-D)}{3}}. \tag{23}$$

The conduction Losses of the MOSFETs can be expressed as:

$$P_{cond-S_1}=R_{ds-S_1}I^2_{rms-S_1}, \tag{24}$$

$$P_{cond-S_2}=R_{ds-S_2}I^2_{rms-S_2}, \tag{25}$$

where $R_{ds-S_1}$ and $R_{ds-S_2}$ are the on-resistances of $S_1$ and $S_2$, respectively.

Thus, the total conduction losses are equal to:

$$P_{cond}=P_{cond-S_1}+P_{cond-S_2}. \tag{26}$$

### B. CAPACITOR ESR LOSSES

The RMS currents of $C_b$ and $C_o$ can be derived by:

$$I_{rms-C_b}\simeq I_o\frac{\sqrt{3}}{(1-D+nD)}, \tag{27}$$

$$I_{rms-C_o}=\frac{\Delta I_o}{\sqrt{12}}. \tag{28}$$

The ESR losses of $C_b$ and $C_o$ is equal to:

$$P_{ESR-C_b}=ESR_{C_b}I^2_{rms-C_b}, \tag{29}$$

$$P_{ESR-C_o}=ESR_{C_o}I^2_{rms-C_o}. \tag{30}$$

where $ESR_{C_b}$ and $ESR_{C_o}$ are the equivalent series resistances of $C_b$ and $C_o$, respectively.

Therefore, the total ESR losses can be expressed as:

$$P_{ESR}=P_{ESR-C_b}+P_{ESR-C_o}. \tag{31}$$

### C. COUPLED INDUCTOR LOSSES

The coupled inductor losses include the wire and the core losses.

#### 1) WIRE LOSSES

The RMS and average currents of the windings of the coupled inductor can be approximately derived by:

$$I_{rms-n_1}\simeq\frac{2nI_o}{(1-D+nD)}\sqrt{\frac{D}{3}}, \tag{32}$$

$$I_{rms-n_2}\simeq\frac{2(1-n)I_o}{(1-D+nD)}\sqrt{\frac{D}{3}}, \tag{33}$$

$$I_{avg-n_1}\simeq\frac{nDI_o}{(1-D+nD)}, \tag{34}$$

$$I_{avg-n_1}\simeq\frac{(1-n)DI_o}{(1-D+nD)}. \tag{35}$$

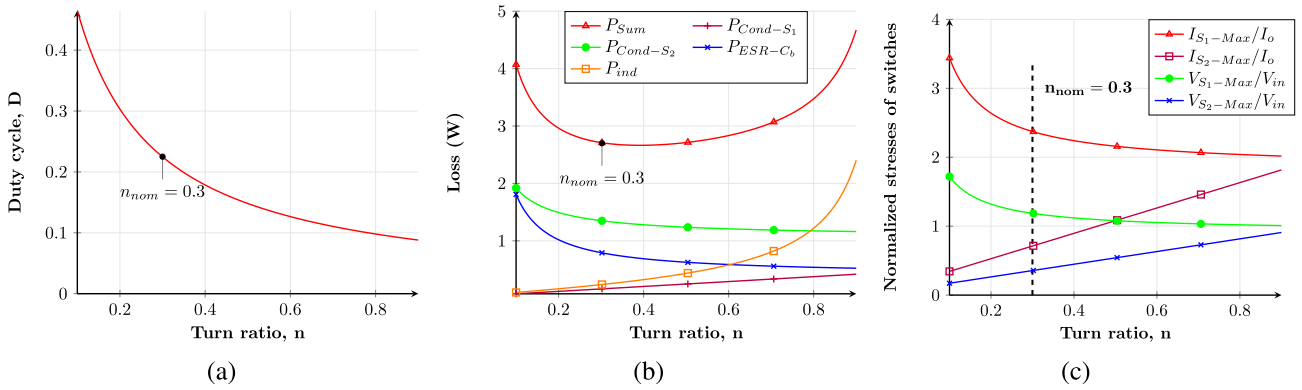


**FIGURE 6.** Turn ratio multi-objective design curves, (a) Operating duty cycle versus *n*, (b) Various power losses along with the total power loss against *n*, and (c) Normalized voltage and current stresses of semiconductors at full load versus *n*.

The wire losses of each winding of the coupled inductors can be obtained by:

$$P_{wire} = R_{DC} I_{avg}^2 + R_{AC} I_{rms}^2, \tag{36}$$

where $R_{DC}$ and $R_{AC}$ are the DC-resistance and the AC-resistance of each winding.

#### 2) CORE LOSSES

The ferrite core losses can be expressed by:

$$P_{core} = K_1 {f_{sw}}^{\alpha} \Delta B^{\beta} V_e, \tag{37}$$

where $K_1$ is a constant parameter that depends on core material, $\Delta B$ is the maximum flux density variation in Gauss, $\alpha$ is the frequency exponent, $\beta$ is the flux density exponent, and $V_e$ is the effective core volume in $cm^3$. Thus, the total coupled inductor losses, $P_{ind}$, is equal to:

$$P_{ind} = P_{wire} + P_{core}. \tag{38}$$

### D. OUTPUT INDUCTOR LOSSES

The RMS current of the output inductor is obtained as follows:

$$I_{rms-L_o} = \sqrt{I_o^2 + \frac{\Delta I_o^2}{12}}. \tag{39}$$

The conduction losses of $L_o$ can be calculated by:

$$P_{L_o} = DCR_{L_o} I_{rms-L_o}^2, \tag{40}$$

where $DCR_{L_o}$ is the DC resistance of the output inductor.

### E. GATE LOSSES

The gate-drive losses for the proposed converter can be calculated by:

$$P_{gate} = (Q_{g-S1} + Q_{g-S2}) V_{drive} f_{sw}, \tag{41}$$

where $Q_{g-S1}$ and $Q_{g-S2}$ are the total gate charges of $S_1$ and $S_2$, and $V_{drive}$ is the gate driving voltage.

Therefore, the total losses of the proposed converter can be expressed by:

$$P_{Sum} = P_{cond} + P_{ESR} + P_{ind} + P_{L_o} + P_{gate}. \tag{42}$$

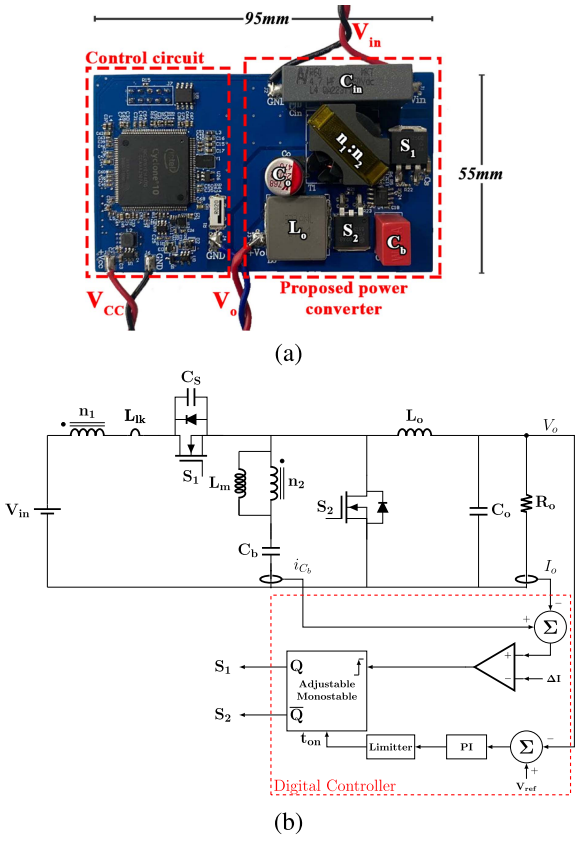


**FIGURE 7.** Prototype of the proposed converter. (a) Implemented prototype. (b) Circuit diagram with proposed control block.

## V. DESIGN PROCEDURE

In this section, a complete design guideline of the proposed converter is presented. The proposed procedure mainly consisted of designing the coupled inductor parameters. The following parameters are considered for the converter: $V_{in} = 150V$, $V_o = 12V$, $P_{o(rated)} = 120W$, and $P_{o(light-load)} = 48W$.

First, the switching frequency of the proposed converter must be selected. Increasing the switching frequency is desirable because it enhances the power density and dynamic

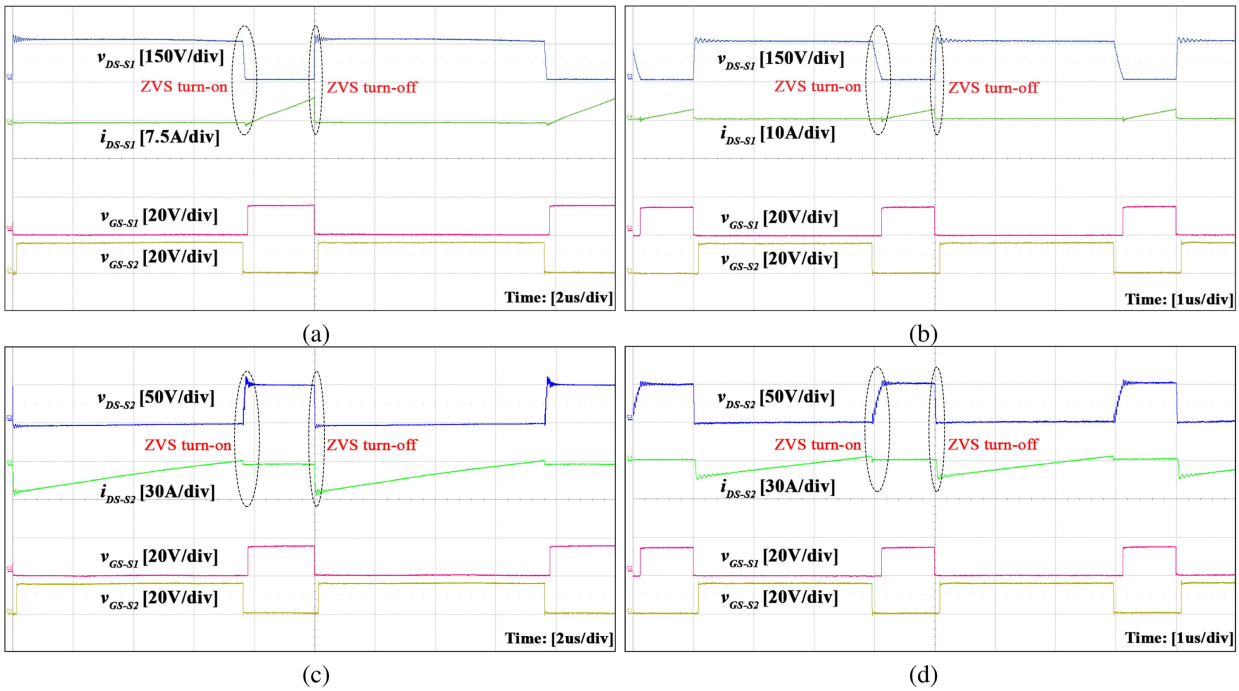


**FIGURE 8.** Experimental results of the proposed converter. (a) Gate signal, drain-source voltage, and current of $S_1$ at full load. (b) Gate signal, drain-source voltage, and current of $S_1$ at light load. (c) Gate signal, drain-source voltage, and current of $S_2$ at full load. (d) Gate signal, drain-source voltage, and current of $S_2$ at light load.

response of the converter. However, there are limitations to increasing the $f_{sw}$. Higher switching frequencies can complicate control and gate drive circuits especially in high step-down applications as the turn-on time of the switch becomes too short. Additionally, switching-related losses increase, though these are negligible at ZVS operation. Furthermore, according to (15), in QSW-ZVS mode control, the switching frequency is increased at light loads. Therefore, to expand the ZVS region of the converter and prevent excessive circulating currents, it needs to operate at a significantly higher switching frequency under light loads compared to full load. This introduces a tradeoff between improving power density and dynamic performance and preventing circulating currents at light loads. Consequently, the switching frequency at full load is set to $f_{sw} - 100kHz$, and the ZVS region to cover 70% of the full load with no circulating current. Thus, the maximum operating switching frequency is limited to 300kHz. If the output current drops below this level, ZVS can still be maintained, but the magnetizing inductance becomes overcharged. This overcharge causes excess current to flow back to the input and reduces the light-load efficiency.

The next step of the design procedure is to determine the turn ratio of the coupled inductors. As shown in (9), there is an inverse relation between $n$ and $D$ for a specific voltage gain. Thus, reducing the turn ratio results in a more extended duty cycle, the benefits of which are discussed in section I. Fig. 6(a) depicts the duty cycle of the converter versus the turn ratio. Moreover, decreasing the turn ratio value lowers the conduction losses of $S_2$ and the ESR losses of $C_b$, according to the loss analysis. On the other hand, based on the loss analysis, reducing $n$ causes the conduction losses of $S_1$ and coupled inductor losses to increase. Fig. 6(b) illustrates the total losses of the proposed converter along with the turn ratio-dependent losses for various values of $n$. Changing the value of the turn ratio also influences the voltage and current stresses of the switches. The normalized voltage and current stress of each MOSFET against the turn ratio is presented in Fig. 6(c).

Regarding the impact of the coupled inductor turn ratio on the operating duty cycle, the power losses of the proposed converter, and the voltage and current stresses of the semiconductor devices, selecting the nominal coupled inductor turn ratio, $n_{nom}$, consists of a multi-objective trade-off between all the mentioned parameters. The main objective of the design is to extend the duty cycle as much as possible without imposing excessive power losses or voltage and current stresses on the converter. Based on the data shown in Fig. 6, the nominal value for the turn ratio is selected equal to $n_{nom} = 0.3$. Thus, the duty cycle of the converter is 22.5%.

The next step is to obtain the value of the magnetizing inductance. $L_m$ is derived Based on the (18), and it should be designed so that the converter operates with 100 kHz switching frequency at full load ($I_o = 10$ A). Thus, the magnetizing inductance is calculated equal to $L_m = 3.425\ \mu$H. The design parameters of the proposed converter are presented in Table 2. Based on the designed parameters of the proposed converter and according to the (17), $\Delta I$ is calculated equal to 1.17 A.

## VI. EXPERIMENTAL RESULTS

Experimental tests of the proposed converter with the parameters of Table 2 are carried out to verify the theoretical analysis.

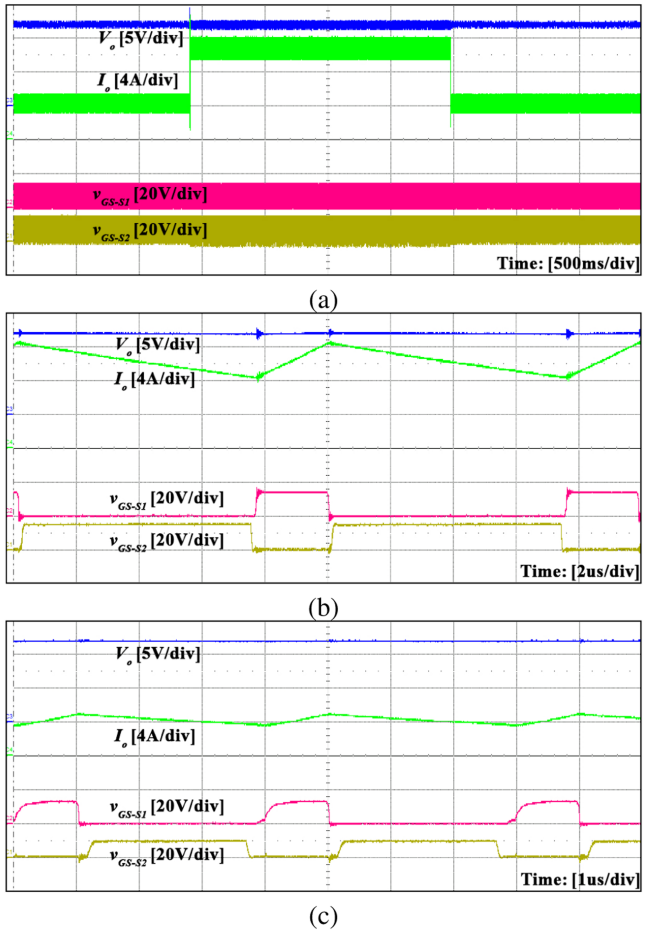


**FIGURE 9.** Experimental results of the proposed converter. (a) Output voltage, output current, and Gate signals during step load change from light-load to full-load and vice versa. (b) Zoomed waveforms at full-load steady state. (c) Zoomed waveforms at light-load steady state.

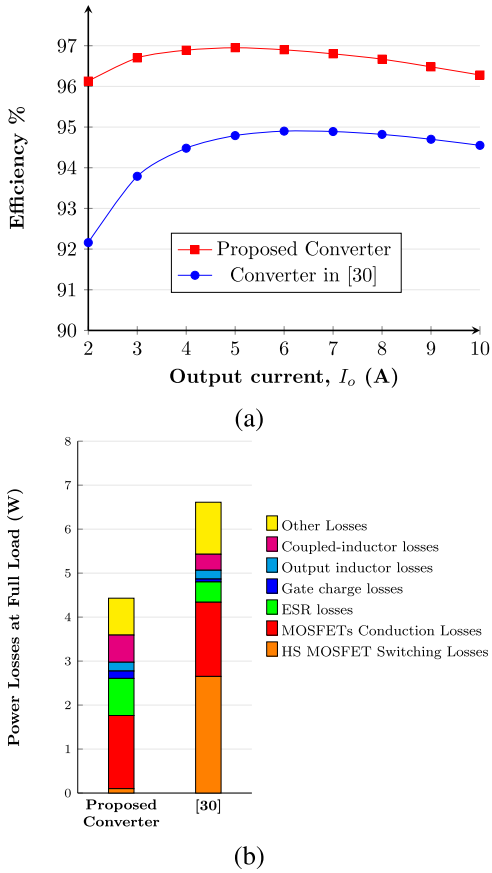


**FIGURE 10.** Efficiency and loss breakdown comparison between the proposed converter and [30].

Fig. 7 shows the implemented prototype of the proposed Converter and its corresponding circuit diagram. As illustrated in Fig. 7(b), the proposed Pulse Frequency Modulation (PFM) control scheme includes a current loop and a voltage control loop. The current loop adjusts the switching frequency to ensure the MOSFETs operate under ZVS conditions. Meanwhile, the voltage control loop sets the turn-on time of the high-side (HS) MOSFET, thus controlling the duty cycle.

The experimental waveforms of the proposed converter are presented in Fig. 8. The drain-source voltage and current of HS MOSFET along with its gate-source waveform at full load ($I_o = 10A$) and light load ($I_o = 4A$) conditions are illustrated in Fig. 8(a) and (b), respectively. As shown, $S_1$ operates under ZVS condition, and the current stress of the main switch has reduced compared to that of the conventional buck converter. The drain-source voltage, drain current and gate-source voltage of $S_2$ at full load and light load conditions are presented in Fig. 8(c) and (d), respectively. The soft-switching operation of $S_2$ and its reduced voltage stress compared to that of the conventional buck can be noted in the experimental figures.

**TABLE 2.** Design Parameters of the Proposed Converter

| Parameter | Symbol | Value |
|---|---|---|
| Input voltage | $V_{in}$ | $150V$ |
| Output voltage | $V_o$ | $12V$ |
| Rated power switching frequency | $f_{sw}$ | $100kHz$ |
| Rated power | $P_{o(rated)}$ | $120W$ |
| Light-load power | $P_{o(light-load)}$ | $48W$ |
| Output inductance | $L_o$ | $33\mu H$ |
| Output capacitance | $C_o$ | $470\mu F$ |
| Energy transferring capacitor | $C_b$ | $10\mu F$ |
| High-side MOSFET | $S_1$ | SUM10250E |
| Synchronous rectifier | $S_2$ | FDB86135 |
| Snubber Capacitor | $C_s$ | $610pF$ |
| Coupled-inductor turn ratio | $n_1$:$n_2$ | 7:3 |
| Magnetizing inductance | $L_m$ | $3.425\mu H$ |

Fig. 9(a) presents the transient response of the proposed converter during a step load change from light-load to full-load and back to light-load. Additionally, the zoomed steady-state waveforms of the output voltage and current, along with

**TABLE 3. Comparison Between Step-Down Converters**

| | SR Buck | [16] | [19] | [26] | [30] | [32] | Proposed |
|---|---|---|---|---|---|---|---|
| Topology | Conventional | Series cap | Series resonant | CI+SC | CI+SC | CI+SC | CI+SC |
| Voltage gain | $D$ | $\frac{D}{3}$ | $\frac{D}{2(1+D)}$ | $\frac{n_2 D}{n_1+n_2}$ | $\frac{n_2 D}{(n_1+n_2)(1-D)}$ | $\frac{n_2 D}{(n_1+n_2)(1-D)}$ | $\frac{n_2 D}{n_1+n_2-n_1 D}$ |
| Voltage stress of switches | $V_{in}$ | $\frac{V_{in}}{3}$ | $\frac{(2+D)V_{in}}{2+2D}, \frac{V_{in}}{2+2D}, \frac{V_{in}}{2}$ | $V_{in}, nV_{in}$ | $(2-n)V_{in}, \frac{V_o}{D}$ | $V_{in}, nV_{in}, V_o$ | $\frac{V_{in}}{1-D}, \frac{nV_{in}}{1-D}$ |
| Current stress of switches | $I_o$ | $\frac{I_o}{3}, \frac{DI_o}{3(1-D)}$ | $(1-D)I_o, \frac{(1-D)I_o}{2}$ | $nI_o, \frac{n(1-D)V_{in}}{L_{lk} f_{sw}}$ | $\frac{nI_o}{1-D}, \frac{I_o}{1-D}$ | $\frac{nI_o}{1-D}, \frac{I_o}{1-D}, \frac{2I_o}{(1-D)^2}$ | $\frac{2nI_o}{1-D}, \frac{2I_o}{1-D}$ |
| MOSFET count | 2 | 5 | 8 | 4 | 2 | 5 | 2 |
| Power diode count | 0 | 1 | 0 | 0 | 2 | 0 | 0 |
| Magnetic core count | 1 | 2 | 4 | 2 | 2 | 2 | 2 |
| Low ripple current | ✓ | ✓ | ✓ | ✓ | ✓ | ✗ | ✓ |
| Shoot-through protection | ✗ | ✗ | ✗ | ✗ | ✓ | ✗ | ✓ |
| Phase shedding | ✓ | ✗ | ✗ | ✓ | ✓ | ✓ | ✓ |
| Common Ground | ✓ | ✓ | ✗ | ✓ | ✓ | ✓ | ✓ |
| Control | PWM | PWM | PWM | PWM | PWM | PWM | PFM |
| Switching condition | Hard | Hard | ZVS | ZVS | ZCS | ZVS & Hard | ZVS |
| Implemented prototype | - | 80W<br>90V/14V | 160W<br>48V/8V | 33W<br>48V/3.3V | 150W<br>310V/12V | 33W<br>48V/3.3V | 120W<br>150V/12 |
| Reported max. $\eta$ | - | 92.7% | 96.3% | 94.1% | 95.5% | 95.8% | 97% |
| Estimated power density | - | - | 102W/inch$^3$ | 8.4W/inch$^3$ | 10.3W/inch$^3$ | 9.5W/inch$^3$ | 42W/inch$^3$ |

the gate signals, are illustrated in Fig. 9(b) for the full-load condition and in Fig. 9(c) for the light-load condition.

## VII. COMPARATIVE ANALYSIS

As illustrated in Fig. 4, the proposed converter effectively expands the operating duty cycle compared to that of the conventional buck converter with continuous output current while the converters in [19], [21], [22], [24], [25], [32] suffer from high ripple output currents. Another main advantage of the proposed converter is achieving ZVS of the main switch at a wide range of load conditions, which leads to the major reduction of both the switching losses and EMI. Achieving soft switching condition at light load is specifically substantial in battery-operated devices where the converter operates the majority of the time in light load conditions to preserve the battery energy. Additionally, the proposed converter does not require additional semiconductors or complex circuits to provide the ZVS condition of the MOSFETs, which further enhances the simplicity and efficiency of the converter compared to the converters in [19], [24], [26], [27], [28], [29], [30], [32]. Other benefits of the proposed converter are the low current stress of high-side MOSFET and the reduced voltage stress across synchronous rectifiers compared to that of the conventional buck converter. Furthermore, the reverse recovery losses of the converter are negligible owing to the leakage inductances of the applied coupled inductor. Finally, simple boot-strap drivers can be utilized to drive the MOSFETs, averting the need for complex transformer-isolated or opt-isolated gate drivers which are essential in the converters introduced in [16], [21], [22], [27], [31], [32].

A control technique proposed to enhance the efficiency of interleaved converters over a wide load range is phase-shedding, in which the number of active phases can be changed based on the output current. This technique can be applied to the proposed converter, whereas the active phases of the converters in [16], [17], [18], [23], [31], [32] are fixed. A comparison between the proposed converter and the converters in [16], [19], [26], [30], [32] is presented in Table 3.

The most notable advantage of the proposed converter is the efficiency improvement at all load conditions. The efficiency curve of the proposed converter and the converter in [30] for various output currents along with their loss break-down at full load is provided in Fig. 10(a) and (b), respectively. It is noteworthy to mention that the efficiency data in Fig. 10 is obtained based on the parameters given in Table 2. As shown, the efficiency at full load condition is improved by 1.73%, and it is increased by 3.97% at a load current of 2$A$. The efficiency improvement of the proposed converter is mainly caused by the negligible switching of the MOSFETs, especially at light loads, although the ESR losses of the proposed converter are incremented compared to that of [30] due to the increased RMS current of the magnetizing inductance.

## VIII. CONCLUSION

This paper presented a non-isolated high step-down converter with several attractive features, such as ZVS soft switching over a wide load range, high attenuation, low current ripple, and a reduced component count. The proposed converter also reduces the current stress of the high-side MOSFET and provides reduced voltage stress across the low-side MOSFET. Additionally, the switches are driven with a simple boot-strap gate driver, further contributing to the simplicity of the converter. The proposed converter also achieves inherent shoot-through protection owing to the leakage inductance in the MOSFET leg limiting the current slope at switching instants.

A design guideline was presented to obtain the optimal values for the coupled inductor, for which the voltage gain is improved while the power losses are minimized, and the voltage and current stress of the MOSFETs remain in the desired range. Finally, a 150$V$ to 12$V$/120$W$ prototype with a power density of 42W/inch$^3$ was implemented based on the

proposed design to confirm the theoretical analysis, and to display the advantages of the proposed converter.

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