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Modulation Improvements for High-Phase-Count Series-Capacitor Buck Converters

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ABSTRACT This article presents three modulation improvements for the series-capacitor buck (SCB) converter and its topological derivatives. The first consists of various phase activation sequences (PHACTSs) which raise the maximum input-to-output voltage conversion ratio of an N-inductor, N-phase SCB converter beyond the traditional limit of $1/N^2$, without incurring any additional voltage stress to the switches. Phase counts up to 16 are analyzed with conversion ratios increasing by a factor of up to 7. Due to the inherent link between the converter's maximum attainable output voltage and maximum output current slew rate, these PHACTSs offer a significant improvement to the load-voltage transient response. Utilizing the flying capacitors that link adjacent inductors, a second modulation technique is introduced that effectively increases the digital pulse-width-modulator's (DPWM) output-voltage resolution, by a factor of N, by employing a novel method of minimum duty increments (MDIs). Despite the commonly-held assumption of automatic steady-state inductor-current-balancing present in an N-inductor SCB, large-signal modelling reveals that slight current imbalances inevitably arise, even in lossless configurations, with three or more output inductors. After elucidating its origin, this article introduces a third modulation technique that can reduce these inductor current imbalances through a particular implementation of MDI. A discrete prototype of an 11-inductor, 48 V-to-1.0 V, 275 A-load, SCB converter was fabricated to experimentally demonstrate and validate the simulated results of the increase in both the output voltage ceiling and DPWM resolution, as well as to evaluate the MDI-DPWM output-voltage linearity. Finally, the maintenance of both inductor current balancing and low switch-voltage-stress is experimentally substantiated when using MDI.

INDEX TERMS Current balancing, digital pulse-width-modulation, flying capacitors, multiphase, resolution, series-capacitor buck, soft charging, star sequencing, transient response, voltage regulator module.

I. INTRODUCTION

The multiphase, dc–dc series-capacitor buck (SCB) converter (Fig. 1) was first introduced in the early 2000s [1], [2] as an alternative to the well-established, conventional multiphase buck (CMB) converter, promising a more efficient way of performing non-galvanically-isolated, high-step-down voltage conversion. Such gains in power-processing efficiency are primarily achieved through the reduction of switch-voltage-stresses, allowing for the use of power-transistors with better figures-of-merit (e.g., lower $R_{ON}Q_g$). This reduction in voltage stress is accomplished through the addition of $N-1$ flying capacitors $\{C_1, C_2, \ldots, C_{N-1}\}$ for the already-existing set of N output-inductors $\{L_1, L_2, \ldots, L_N\}$ in the topology. Through the natural build-up of voltage across these added capacitors (annotated on Fig. 1), the transistors of the SCB are spared from bearing the full brunt of the input voltage, V_{in}, during their OFF-states. This is in stark contrast to what the switches of a CMB must endure (i.e., nominally V_{in}).

Unlike the power-transistors during their ON/OFF state-transitions in hard-switched scenarios, the flying capacitors do not suffer from high voltage-current-overlap power-losses due to their reactive nature. Thus, it is preferable, from a steady-state power-efficiency perspective, for the reactive components to process the majority of the high voltage-conversion—a prevailing theme with emerging hybrid flying-capacitor converters—rather than relying exclusively on the switches as is done in CMB converters.

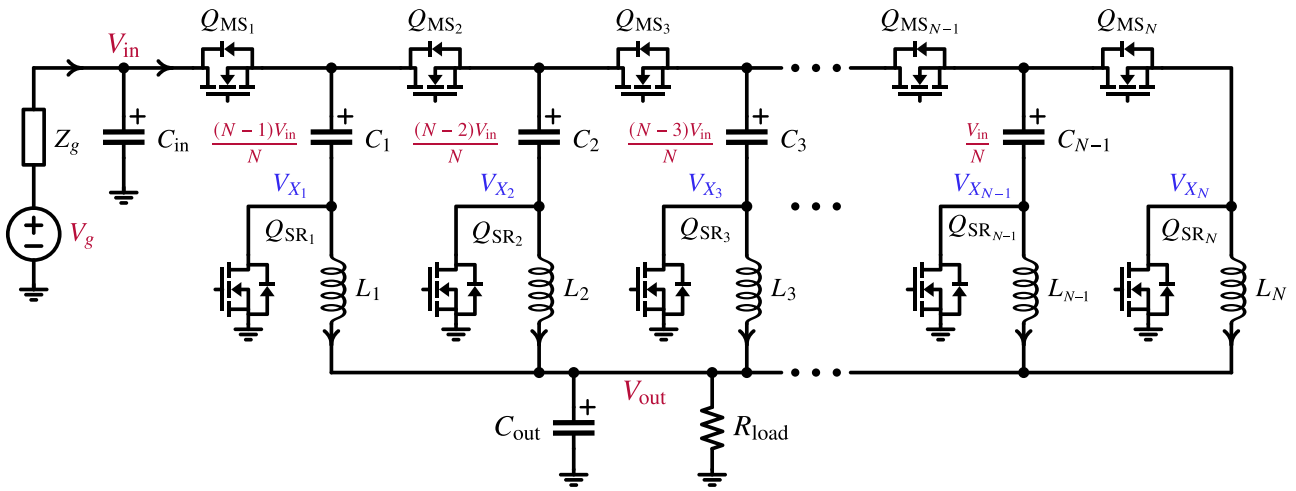


FIGURE 1. ***N*-inductor series-capacitor buck (SCB) converter.**

In SCB converters, the nominal voltage stress reduction, compared to CMB converters, is proportional to the quantity of output inductors, N. Specifically, since the high-level voltage applied to each inductor switching node (V_X) is nominally reduced by a factor of N, the blocking voltage of all synchronous rectifiers (Q_{SR}) and the input-interfacing main switch (Q_{MS_1}) is by definition reduced by the same factor of N. However, all other main switches (i.e., Q_{MS_2}, Q_{MS_3}, ..., Q_{MS_N}) experience a nominal blocking voltage reduction of a factor of only $N/2$. (The increase in blocking voltage to Q_{MS_k} occurs when L_{k-1} is being magnetized, where $k \in \{2, 3, \ldots, N\}$.) Although the blocking voltage of these main switches is twice that of Q_{MS_1}, the crossover voltage (i.e., highest V_{DS} of the switch during ON/OFF transitions) remains at the same lowered level as Q_{MS_1}, thus granting *all* high-side switches a nominal crossover voltage reduction of a factor of N over CMB converters.

Such a scalable voltage-stress-reduction with increased output-inductor-count (and hence, with increased load-current) is particularly well-suited to converter solutions requiring both high voltage-step-down *and* high load-current. Unsurprisingly, the SCB [3], [4] and its topological derivatives [5], [6], [7], [8], have recently garnered much consideration as viable candidates for emerging applications that require converters possessing these characteristics. Notable examples include future non-isolated, *single-stage*, 48 V-to-1 V voltage regulator modules (VRMs) that are designed to power emerging high-performance-computing (HPC) and artificial-intelligence (AI) accelerators. As shown in Fig. 2, these compute accelerator modules are trending to soon exceed an average power consumption of 1 kW. These VRMs must, therefore, not only achieve extreme voltage-step-down ratios with tight output-regulation, they must also efficiently supply ever-increasing loads. However, the scalability of voltage-stress-reduction, offered by the SCB converter, should not be overzealously applied when implementing future VRM solutions around this topology for reasons explained in the following subsection.

A. LIMITED OUTPUT VOLTAGE RANGE

Just as the output voltage, V_{out}, of a CMB is bounded-above by the high-level voltage applied to each inductor's switching node (nominally equal to the input voltage, V_{in}), the output voltage of SCB converters is similarly bounded-above by the nominal high-level voltage applied to each of *its* inductors' switching nodes. Given that the high-level voltage on each V_X is nominally reduced from V_{in} to V_{in}/N, the output voltage of the SCB is automatically bounded-above by V_{in}/N. Indeed, if this was the true output-voltage limit, the needs of power designers—specifically, those implementing 48 V-to-1 V converters for ultra-high-load applications—would be more than satisfied with a *single* (non-paralleled) SCB converter, since configurations with 40+ inductors would technically be permitted. Unfortunately, this limit is a gross over-estimate of what the SCB is actually capable of, for the following reasons:

1) Since the energization of each inductor occurs exclusively through flying-capacitor energy transfer, the main-switch's ON-time-to-switching-period duty ratio, D, must always remain well-below 100% to adhere to capacitor-charge-balance (CCB). Thus, given the linear relationship between the duty ratio and output voltage, the maximum output voltage will be proportionately less than V_{in}/N for the necessary decline in $\max(D)$.
2) To maintain switch-voltage-stresses inline with the aforementioned nominal ratings, adjacent inductors (i.e., L_{k-1} and L_{k+1}) to any given inductor, L_k, must remain in their de-energizing states while L_k is energizing. In other words, $Q_{MS_{k-1}}$ and $Q_{MS_{k+1}}$ must be turned-OFF while Q_{MS_k} is engaged, and vice-versa. Fig. 3(a) illustrates the main-switch gating-sequence for a 3-inductor SCB that adheres to this rule, while Fig. 3(b) shows the consequences (e.g., increased switch-voltage-stresses) when this rule is ignored. In [9], the authors

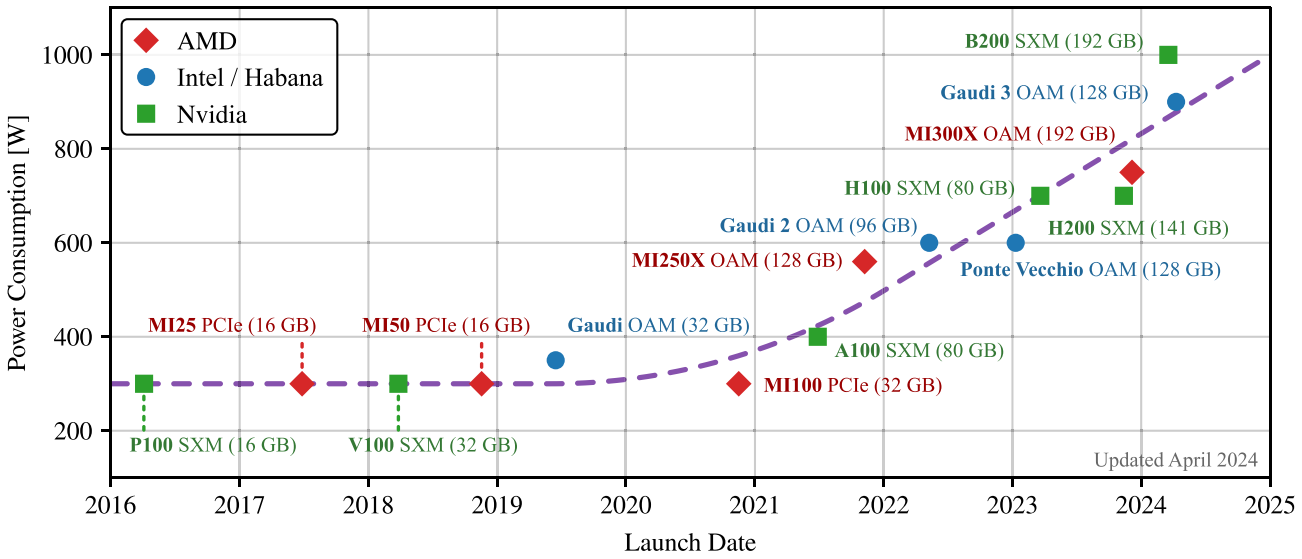


FIGURE 2. Trend of increasing power consumption (per compute module) of commonly-deployed families of HPC/AI accelerators. Parenthesized values denote the amount of co-packaged high-bandwidth memory (HBM), in gigabytes. Note that "launch date" is not necessarily indicative of date of widespread availability.

further delve into additional complications associated with modulation strategies that intentionally incorporate adjacent inductor energization overlap. These include vastly different interphase duty ratios which are necessary to maintain steady-state inductor current balancing.

Given the duty ratio limit (i.e., $D < 1/3$) imposed on the 3-inductor SCB in Fig. 3(a), we can anticipate that, if we continue to operate with the lowest-possible switch-voltage-stress, the main-switch duty ratio will become increasingly constrained as more inductors are added to the SCB. Foreseeing this trend, it is not unreasonable to conclude that the maximum duty ratio, for an N-inductor, N-phase SCB converter, is limited by

$$\max(D) = \frac{1}{N}, \tag{1}$$

where each main-switch is assumed to have the same duty ratio. Since it has been already established that each inductor's maximum switching-node voltage is also nominally reduced by a factor of N, over a CMB, to a value equal to V_{in}/N, the maximum output voltage would correspondingly be

$$\max\left(V_{\text{out}}\right) = \max(D)\frac{V_{\text{in}}}{N} = \frac{V_{\text{in}}}{N^2}. \tag{2}$$

This constraint presents a major challenge when implementing high-current, high-conversion-ratio converters for both conventional 12 V-bus applications and emerging systems operating with higher bus voltages.

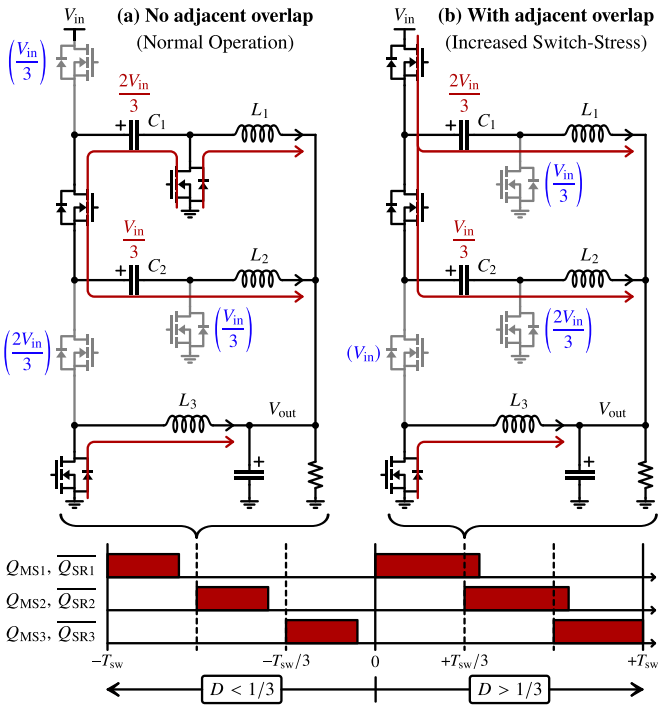


FIGURE 3. Increased switch-voltage-stress from attempting to magnetize adjacent inductors simultaneously from $t = 0$ and onwards as exemplified using a 3-inductor SCB converter. Nominal switch-voltage-stresses are indicated in blue *with* parentheses and nominal flying-capacitor voltages in red *without* parentheses.

1) PRIOR ART: ATTEMPTS AT RAISING MAXIMUM V_{OUT}

When the SCB converter was introduced, 12 V was—and still is to a large extent today in modern consumer computers, hybrid electric vehicles (HEV), and legacy HPC systems—the primary distribution-bus-voltage. According to (2), SCB VRM solutions powering 1 V loads (typically found in computing environments) are limited to a maximum of 3-inductors (exactly as shown in Fig. 3) since the maximum attainable output voltage for a 4-inductor, 4-phase SCB is only 0.75 V with a 12 V-input. Unlike today's microprocessors which are typically regulated to sub-1 V, the load voltages in the mid-2000 s were in the neighbourhood of 1.4 V. In response, a 4-inductor SCB was proposed in [10], where every-other

inductor energization (i.e., L_k and L_{k+2}) occurred in-sync. This effectively dropped the phase-count from four to two, while still maintaining the voltage-stress reduction offered by a 4-inductor configuration. In this specific case, the phase reorganization resulted in the maximum duty ratio being raised from 25% to that of a 2-phase (i.e., $1/2 \equiv 50\%$), doubling the maximum output voltage from 0.75 V to 1.5 V. For an SCB being operating as a 2-phase converter, the maximum duty ratio becomes independent of the inductor-count. Correspondingly, the maximum output voltage of a 2-phase, N-inductor SCB is

$$\text{2-phase:} \quad \max\left(V_{\text{out}}\right) = \frac{V_{\text{in}}}{2N}. \tag{3}$$

This approach of operating an N-inductor configuration as a 2-phase converter to raise the maximum output voltage, has since been replicated in [3] for the same 4-inductor SCB configuration as in [10]. However, rather than operating with the increasingly-outdated 12 V-input, [3] operates with the emerging 48 V-input distribution-bus-voltage and targetting a 5 V-output (where a 4-phase would be limited to 3 V).

This increasingly-prevalent 48 V (or even 54 V) distribution-bus-voltage is found in the racks of modern datacenters, cable harnesses of fully-electric vehicles (EVs), and soon-to-be-released consumer electronics that adopt the USB PD Rev. 3.1 (or newer) specification. This voltage-potential is gaining broad adoption because it offers the following advantages:

1) reduction in Ohmic (I^2R) losses for iso-cross-section;
2) reduction in material cost (most-commonly copper);
3) reduction in cabling mass and increased flexibility; and
4) low enough voltage potential to not require galvanic isolation.

Conveniently, SCB converters also benefit from the increase in V_{in}, by being permitted to be configured with more inductors/phases, while simultaneously reaching the same output-voltage as with a 12 V-input. This is of great advantage because more inductor currents can be naturally-balanced in steady-state operation. However, due to the $1/N^2$ factor in (2), the number of phases can *only* be doubled for the 4-fold increase in V_{in}. That is, an SCB converter, designed for 48 V-to-1 V conversion, can only be configured with a maximum of 6 phases—a considerable disparity from the 40+ inductors as predicted earlier. Furthermore, since the switch-voltage-stress reduction (for a given increase to inductor-count) does not scale down as quickly as the maximum output-voltage, the switch-voltage-stress for a 48 V-input, $2N$-inductor configuration would be twice that of a 12 V-input, N-inductor configuration.

Due to its inability to efficiently supply in excess of 1 kA at sub-1 V from a 48 V-input, a 6-inductor SCB converter is simply inadequate to power future microprocessors, such as those that can be extrapolated from Fig. 2. Of course, multiple 6-inductor SCB converters can be paralleled and interleaved until the current-rating is reached. However, by foregoing *single* SCB configurations with greater inductor-counts, one loses out on benefits like: inherent inductor-current-convergence across a greater number of inductors, reduced switch-voltage-stresses, and ultimately, reduced conversion losses. Such a realization has led the authors of [11] to implement a 48 V-to-1 V, 20-inductor SCB variant (an inductor-count increase to the base configuration introduced in [6]). Since this variant is limited by the same inductor/phase-count constraint imposed by (2), the 2-phase approach was carried over from [10], raising the maximum output voltage, according to (3), from 0.12 V to 1.2 V.

2) PRIOR ART: SHORTCOMINGS OF 2-PHASE OPERATION

Unfortunately, operating an N-inductor SCB as a 2-phase converter presents its own set of challenges:

1) *Increased output voltage ripple:* Since half of the inductors are energized in-sync with each other, it is equivalent to reducing the per-phase inductance by a factor of $N/2$ (where N is even). Since the duty ratio of each main-switch remains unchanged whether the SCB is operating as an N-phase or 2-phase converter, the reduced equivalent per-phase inductance of an N-inductor, 2-phase design results in higher peak-to-peak output-current-ripple. This is expressed as

$$\Delta I_{\text{out},2} = N\left[\frac{V_{\text{in}}/(2N) - V_{\text{out}}}{V_{\text{in}}/N - V_{\text{out}}}\right]\Delta I_{L,\text{eff}}, \tag{4}$$

where $N \leq \lfloor V_{\text{in}}/(2V_{\text{out}})\rfloor$. Furthermore, $\Delta I_{L,\text{eff}}$ is defined as the *effective peak-to-peak current ripple per inductor as viewed from the output*, and is expressed as

$$\Delta I_{L,\text{eff}} = \frac{N\left(V_{\text{in}}/N - V_{\text{out}}\right)V_{\text{out}}}{V_{\text{in}}L_k f_{\text{sw}}}, \tag{5}$$

which is *independent* of whether each inductor is discrete or coupled. That is, L_k is either the inductance of each discrete inductor, or the leakage inductance of each of the coupled inductors. f_{sw} is the per-phase switching frequency. For an N-inductor, N-phase SCB, the output-current-ripple, $\Delta I_{\text{out},N}$, normalized to (5), is

$$\frac{\Delta I_{\text{out},N}}{\Delta I_{L,\text{eff}}} = \frac{\left(\lceil N^2M\rceil - N^2M\right)\left(N^2M - \lfloor N^2M\rfloor\right)}{N^2\left(1 - NM\right)M}, \tag{6}$$

where M is the input-to-output voltage conversion ratio, $V_{\text{out}}/V_{\text{in}}$. For a hypothetical N-inductor, N-phase SCB configuration that is not constrained by (1) or (2), it can be seen from Fig. 4 that a 2-phase configuration always results in *significantly* worse output-current ripple. Since the output capacitor, C_{out}, is meant to absorb the majority of this output-current-ripple, its parasitic equivalent-series-resistance (ESR) and equivalent-series-inductance (ESL)—in addition to the output capacitance itself—become significantly more excited by a 2-phase operation. For a fixed peak-to-peak inductor current ripple *as experienced by the individual inductor itself*, these excitations are only made worse with coupled inductors because their leakage inductances are often much lower than the inductances of their discrete counterparts, resulting in a greater value of (5).

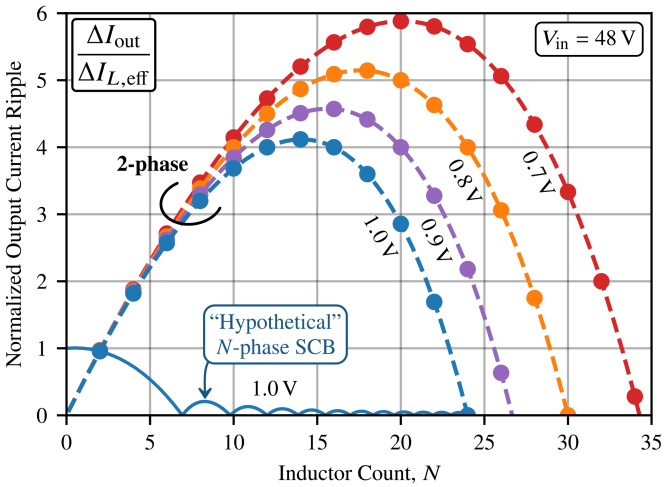


FIGURE 4. Plotting the output current ripple (normalized to the *effective* current ripple per inductor) of an *N*-inductor SCB running as a 2-phase converter with different output voltages. (Lower ripple is better.)

2) *Increased power loss:* The increased RMS current through the ESR of the output capacitor (when running an *N*-inductor SCB as a 2-phase) increases the steady-state Ohmic losses in the capacitors.
3) *Uneven ripple for odd inductor-counts:* The effects are exacerbated when the SCB is configured with an odd-number of inductors. Since the number of inductors that are energized in-sync varies every half-period from $\lfloor N/2 \rfloor$ to $\lceil N/2 \rceil$, the output voltage ripple exhibits what might be described as a 1.5-phase design due to inconsistent ripple cancellation. With the reduced effective phase-count, the output-capacitor current-ripple, power-loss, and voltage-ripple, are all greater.

All three of these challenges are concisely illustrated in Fig. 5 which presents a 5-inductor SCB operating as either a 5-phase or 2-phase converter. In future converter-in-package (CiP) endeavours and vertical power delivery (VPD) implementations where the amount of output capacitance is highly constrained and the control bandwidth is high-enough (through decreased output inductance, proactive charge injection/extraction [12], etc.) such that load -step-induced voltage-undershoots/overshoots are of similar magnitude to the steady-state ripple, 2-phase-operated SCBs may present challenges.

In light of these challenges, Section II introduces several new phase activation sequences (PHACTS) that serve to extend the maximum input-to-output voltage conversion ratio well beyond what the traditional phase-limiting factor of $1/N^2$ otherwise imposes. *This is all achieved while maintaining N phases* and without relegating to adjacent-inductor-energization, unlike what is shown in Fig. 3(b).

B. DIGITAL CONTROL CHALLENGES

In the pursuit of higher microprocessor-power-efficiency and increased compute-performance-per-area, each new microprocessor entrant is generally manufactured with a more

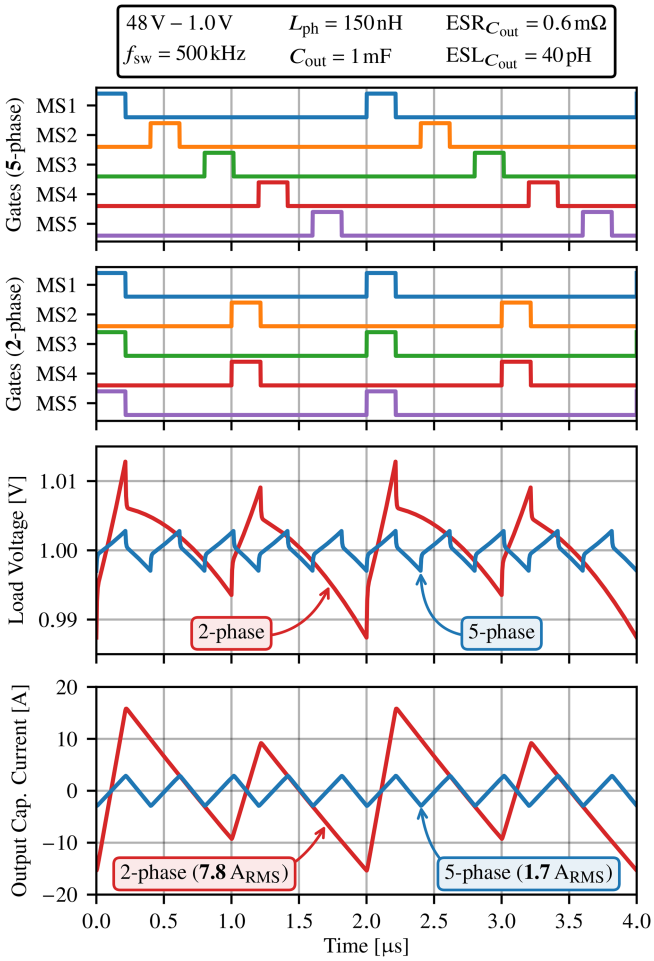


FIGURE 5. Comparing the effects on output voltage ripple and output capacitor current when operating a 5-inductor SCB with five phases or with two phases. It also illustrates the *unevenness* when attempting to operate an odd-inductor-count configuration as a 2-phase converter.

advanced semiconductor lithography than the last. At a high level, this advancement typically involves the shrinking of complementary metal-oxide semiconductor (CMOS) feature sizes. This results in more "sensitive" transistors, allowing for the reduction of operating supply voltage, V_{out}. With the resultant decrease in both the CMOS transistor's gate capacitance, C_g, and the supply voltage, the energy required to activate a given logic transistor, E_g, is reduced based on

$$E_g \sim C_g V_{out}^2. \tag{7}$$

With the core voltages of microprocessors falling below 1 V, their absolute voltage tolerance becomes tighter. According to (7), the best compute efficiency is attained when the microprocessor's supply voltage is regulated to as low a value as possible. However, falling below a critical threshold will cause the microprocessor to crash and/or result in data corruption. To properly function while being fed with a voltage *just above* this critical threshold, it is necessary to precisely measure and detect minute load voltage excursions. In this way, the controller can more accurately determine the load current variations and quickly correct for such disturbances. The better

the regulation, the closer the nominal supply voltage can be to the critical threshold.

Analog controllers have historically been implemented to regulate the core voltage of microprocessors. Unfortunately, analog controllers are highly noise-sensitive, are generally accompanied by many external passives for its compensator (occupying valuable PCB area), and are not easily tunable to variations in system parameters. These characteristics can make designing the high-density platforms (of emerging microprocessors) more challenging than it already is.

Digital VRM controllers are gaining popularity due to their on-demand programmability (e.g., autotuning), reduction of external passives, increased noise-immunity, and ability to easily implement advanced nonlinear algorithms. Additionally, they are especially well-suited to be paired with converter topologies (e.g., SCB) that are more complex than the conventional buck. This is because digital controllers can better accommodate the more elaborate phase-sequencing, sensing, and control algorithms, that are required to make the most of these new topologies. However, one of the fundamental challenges—particularly as it relates to digitally regulating voltage to emerging, highly-demanding, low-voltage microprocessors—is the ever-increasing analog-to-digital converter (ADC) resolution necessary to detect the aforementioned minute load-voltage excursions.

The limiting factor to increasing the output voltage sensing-resolution is the controller's digital pulse-width-modulator (DPWM) resolution. Specifically, increasing the ADC's resolution of the output voltage beyond that of the DPWM would unacceptably introduce output-voltage instability in the form of limit-cycling [13], [14], [15], [16]. To address this, Section III introduces a modulation technique—known as the *method of minimum duty increments (MDI)*—that increases the effective DPWM resolution of N-inductor SCB converters by a factor of N, further incentivizing the use of high inductor-count SCB converters. This technique is enabled by the tight capacitive coupling between physically adjacent inductors of the SCB via its $N-1$ flying capacitors—a topological characteristic notably absent from CMBs, or between any set of paralleled converters.

II. RAISING THE MAXIMUM OUTPUT VOLTAGE

Traditionally, SCB implementations have consisted of 2- to 4-phase configurations due to the maximum output voltage being limited by (2). In configurations with $2 \leq N \leq 4$ equally-separate phases, there exists no such phase activation sequence (PHACTS) that allows all main-switch duty ratios to exceed (1), without resorting to increased switch-voltage-stresses. For example, none of following PHACTS: {1, 2, 3, 4}, {1, 3, 2, 4}, {1, 3, 4, 2}, etc., permit the main-switch duty ratios of a 4-inductor SCB to extend past 25%. (The numbers within these sequences are the subscripts of the main-switches in Fig. 1, and will interchangeably be called *phases*.) However, as it turns out, the duty ratio restriction of (1) is no longer valid once we consider SCB phase-counts of $N \geq 5$. While maintaining the same minimized switch-voltage-stress as if $D < 1/N$, these greater phase-counts give rise to PHACTS that allow D to surpass the conventional limit of $1/N$ by an integer factor of Φ whose value is entirely dependent on the PHACTS. To visually compare different PHACTS, we shall represent them as *directed Hamiltonian graphs*, each possessing the following characteristics:

- Each graph, $\mathcal{G}$, contains N nodes, where each node uniquely corresponds to a main-switch of Fig. 1.
- Each node, φ, is labelled according to its main-switch's subscript (i.e., "1" for Q_{MS1}, "2" for Q_{MS2}, etc.).
- The nodes are circularly-arranged clockwise, in numerical order, such that nodes 1 and N become adjacent.
- Each node is connected by two directed edges: one of which leads *into* the node, and one that leads *out*.
- Traversal between nodes occurs every T_{sw}/N seconds, where T_{sw} is the converter switching period.
- Arriving at a node symbolizes turning-ON the respective main-switch. However, departing a node does not necessarily imply turning it OFF.

Starting at node "1", the conventional PHACTS that results in the duty ratio restriction of (1) simply involves traversing to the next adjacent node in the graph in a clockwise direction. This phase-update rule can be expressed as $\varphi[k+1] = \varphi[k]+1$, where $k \in \{0, 1, \ldots, N-1\}$ and $\varphi[0] = 1$. To enforce periodicity, $\varphi[N] = \varphi[0]$. An example of the resultant main-switch gating-sequence of this update-rule is illustrated in the "5-phase" operation of Fig. 5.

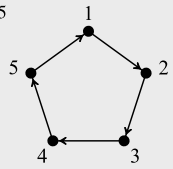
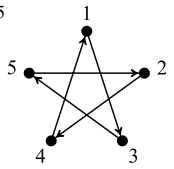
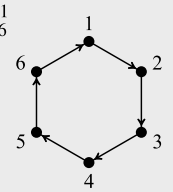
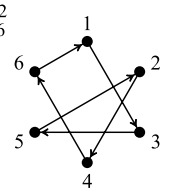
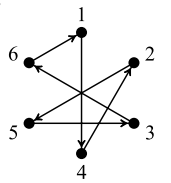
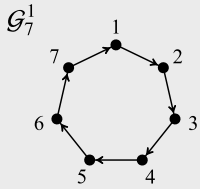
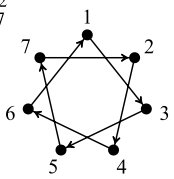
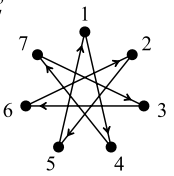
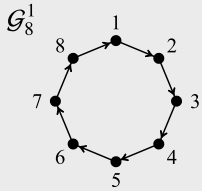
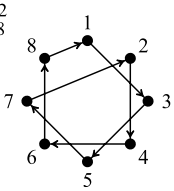
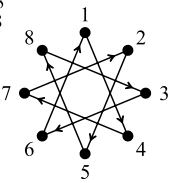
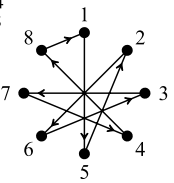
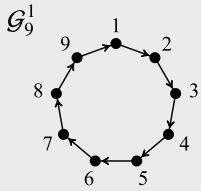
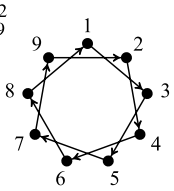
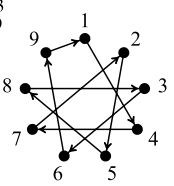
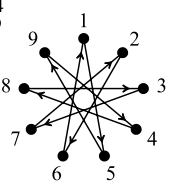
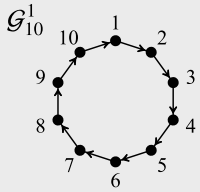
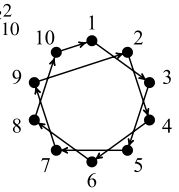
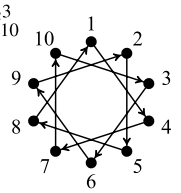
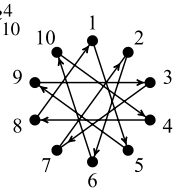
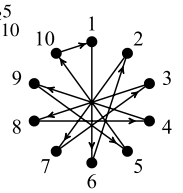
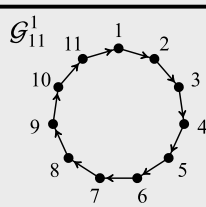
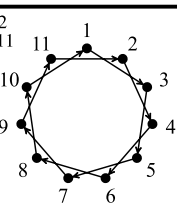
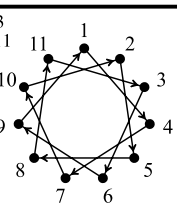
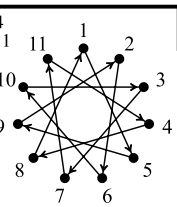
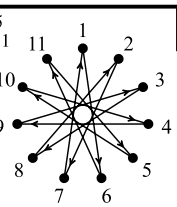
Rather than restricting ourselves to simply traversing to the next adjacent node in the graph, we can define a general, positive or negative, integer-valued *phase-increment*, p, such that the update rule can be re-expressed as $\varphi[k+1] = \varphi[k]+p$, where $1 \leq |p| \leq \lfloor N/2 \rfloor$. To account for the fact that $\varphi[k+1]$ will eventually evaluate to an invalid value when $|p| \geq 2$ (i.e., $\varphi[k+1] \notin \{1, 2, \ldots, N\}$), this update rule must be refined to that of (8), shown at the bottom of this page, with the initial condition,

$$\varphi[0] = \begin{cases} 1, & \text{if } p \text{ is positive; or} \\ N, & \text{if } p \text{ is negative.} \end{cases} \tag{9}$$

Table 1 presents the PHACTS graphs (denoted as $\mathcal{G}_N^p$) for phase-counts between $5 \leq N \leq 11$, and for *positive* phase-increment values between $1 \leq p \leq 5$. (Negative-valued

$$\textbf{PHACTS Update Rule: } \varphi[k+1] = \begin{cases} (\varphi[k]+p-1) \bmod (N)+2, & \text{if } (\varphi[k]+p-1) \bmod (N)+1 \in \bigcup_{i=0}^{k} \varphi[i] \\ (\varphi[k]+p-1) \bmod (N)+1, & \text{otherwise} \end{cases} \tag{8}$$

TABLE 1. Directed Hamiltonian Graphs Representing Various Phase-Activation Sequences (PHACTS) for Select Phase-Counts (N) and Positive-Valued Phase-Increments (p)

$\mathcal{G}_N^p$	$p = 1$	$p = 2$	$p = 3$	$p = 4$	$p = 5$
$N = 5$	$\mathcal{G}_5^1$  1	$\mathcal{G}_5^2$  2	N/A	N/A	N/A
$N = 6$	$\mathcal{G}_6^1$  1	$\mathcal{G}_6^2$  2	$\mathcal{G}_6^3$  2	N/A	N/A
$N = 7$	$\mathcal{G}_7^1$  1	$\mathcal{G}_7^2$  3	$\mathcal{G}_7^3$  2	N/A	N/A
$N = 8$	$\mathcal{G}_8^1$  1	$\mathcal{G}_8^2$  3	$\mathcal{G}_8^3$  3	$\mathcal{G}_8^4$  2	N/A
$N = 9$	$\mathcal{G}_9^1$  1	$\mathcal{G}_9^2$  4	$\mathcal{G}_9^3$  3	$\mathcal{G}_9^4$  2	N/A
$N = 10$	$\mathcal{G}_{10}^1$  1	$\mathcal{G}_{10}^2$  4	$\mathcal{G}_{10}^3$  4	$\mathcal{G}_{10}^4$  2	$\mathcal{G}_{10}^5$  2
$N = 11$	$\mathcal{G}_{11}^1$  1	$\mathcal{G}_{11}^2$  5	$\mathcal{G}_{11}^3$  4	$\mathcal{G}_{11}^4$  3	$\mathcal{G}_{11}^5$  2

Annotated nodes correspond to the inductors of Fig. 1. Shaded cells that contain graphs signify conventional "circular" sequences while unshaded cells display the new "star" sequences. The value in the upper-right corner of each cell is the value of Φ which is the factor by which the maximum output voltage increases over the conventional sequence of the same phase-count. The corresponding negative-valued phase-increments are omitted here for brevity as they produce the same PHACTS graphs as the positive-valued phase-increments, but oppositely-traversed.

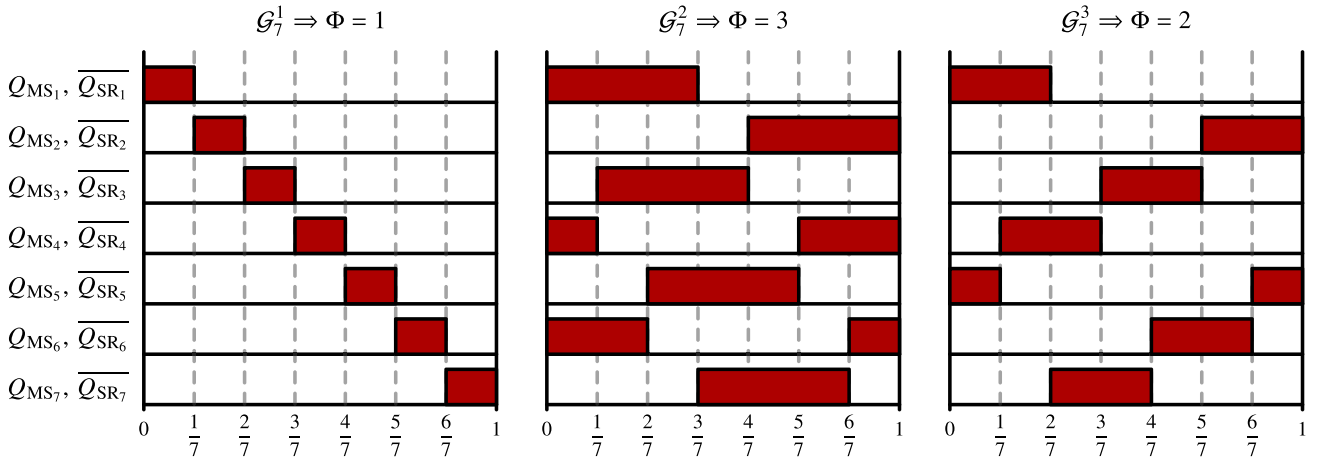


FIGURE 6. Idealized time-domain digital gating waveforms for a 7-phase SCB comparing the *maximum* allowable main-switch ON-times (normalized to one switching period) of different PHACTS ensuring that no adjacent main-switch ON-times overlap to maintain the minimum switch-voltage-stress.

phase-increments result in the same graph shapes, but oppositely-directed.) As shown in the first shaded column (i.e., $p = 1$) of Table 1, the conventional PHACTS always produces a graph shaped as a regular polygon. As the number of nodes/vertices of a regular polygon increases, the shape of the $\mathcal{G}_N^1$ graph approaches a circle. Thus, the conventional PHACTS will also be referred to as the *circular sequence*.

For the other columns (i.e., $p \geq 2$), all the graphs are self-intersecting, denoting that *adjacent main-switches are never subsequently activated*. (Note that phases 1 and N are adjacent only in this abstract formulation; they are not truly adjacent within the topology since they do not share a common flying capacitor.) If adjacent phases are never subsequently activated, the main-switch duty ratios are suddenly no longer bounded-above by $1/N$. That is, the maximum ON-time of each main-switch is permitted to extend to additional phase-divisions, each of length T_{sw}/N. The *maximum number of phase-divisions* that every main-switch is allowed to occupy for a given $\mathcal{G}_N^p$, is denoted by the aforementioned integer quantity, Φ, and is listed in the upper-right corner of each PHACTS cell in Table 1.

All PHACTS that are generated using a phase-increment of $|p| \geq 2$, result in the main-switch duty ratios being allowed to extend beyond the constraint imposed by (1). Due to their common-looking graph shapes, these *new* phase-activation sequences will be collectively referred to as *star sequences*.

Fig. 6 provides a comparison of three valid gating sequences for a 7-phase SCB. Derived from $\mathcal{G}_7^1$, $\mathcal{G}_7^2$, and $\mathcal{G}_7^3$, respectively, this figure exemplifies the utility of star sequences in extending the maximum duty ratio, all while adhering to the adjacent phase overlap restriction. Warranting a redefinition of (1), the generalized maximum duty ratio of SCB converters is

$$\max(D) = \frac{\Phi(N, p)}{N}, \tag{10}$$

with Φ being a function of both N and p. Using small-ripple approximation (SRA), the corresponding steady-state expression for the maximum-attainable average-output-voltage of a hypothetically lossless N-inductor, N-phase SCB, is

$$\max(V_{out}) = \max(D)\frac{V_{in}}{N} = \Phi(N, p)\frac{V_{in}}{N^2}. \tag{11}$$

Table 2 further quantifies Φ over a wider range of SCB[1] inductor-counts, and through cell colouring, offers a way to visually compare the effects of both N and p on the values of Φ, $\max(D)$, and $\max(V_{out})$, with a 48 V-input.

Through a quick inspection of either Tables 1 or 2, it can be concluded that a phase-increment of $p = 2$ yields the greatest increase to the maximum main-switch duty ratio, and ultimately, maximum output voltage. For this specific phase-increment, Φ can be expressed as

$$\Phi(N, 2) = \text{ceil}\left(\frac{N}{2} - 1\right), \quad \forall N \geq 5. \tag{12}$$

By simply migrating from the circular-sequence to a star-sequence, the duty ratio and output voltage ceiling is raised by as much as 7× for 15- and 16-phase configurations. Indeed, with a phase-increment of $p = 2$, the maximum duty ratio approaches 50% as the phase-count increases. As shown in the final column of Table 2, this brings the maximum-output-voltage of high-phase-count, $\mathcal{G}_N^2$-operated SCBs inline with N-inductor, 2-phase configurations.

> *In fact, if N is odd, then an N-inductor, N-phase, $\mathcal{G}_N^2$-operated SCB can practically match the maximum-output-voltage of an $(N + 1)$-inductor, 2-phase SCB.*

This large increase in permissible phase-counts results in a significant reduction in output-current-ripple as illustrated in Fig. 4. Moreover, this reduced output-current-ripple brings with it a reduction in output voltage ripple, increased power

[1]The values in Table 2 apply equally to the cascaded series-capacitor buck (CSCB) converter in [6], [11]. Although CSCB converters have always been presented with even-numbered inductor-counts, they can be made to have odd-numbered inductor-counts by configuring one of its two SCB branches to have one more (or one less) inductor than the other.

TABLE 2. Quantities for Maximum-Allowable Phase-Divisions (Φ), Maximum Main-Switch Duty Ratios (D), and Maximum Output Voltage, for a Range of Inductor-Counts (N) and Phase-Increments (p)

Inductor Count, N	V_X swing (nom.) [V]	$\Phi(N,p)$			max(D) [%]			max(V_{out}) [V]			
		$p=1$	$p=2$	$p=3$	$p=1$	$p=2$	$p=3$	$p=1$	$p=2$	$p=3$	2-phase
2	24	1	—	—	50	—	—	12	—	—	12
3	16	1	—	—	33	—	—	5.33	—	—	—
4	12	1	1	—	25	25	—	3	3	—	6
5	9.6	1	2	—	20	40	—	1.92	3.84	—	—
6	8	1	2	2	16	33	33	1.33	2.67	2.67	4
7	6.86	1	3	2	14	43	28	0.98	2.94	1.96	—
8	6	1	3	3	12	37	37	0.75	2.25	2.25	3
9	5.33	1	4	3	11	44	33	0.59	2.37	1.78	—
10	4.8	1	4	4	10	40	40	0.48	1.92	1.92	2.4
11	4.36	1	5	4	9.1	45	36	0.4	1.98	1.59	—
12	4	1	5	4	8.3	42	33	0.33	1.67	1.33	2
13	3.69	1	6	4	7.7	46	31	0.28	1.7	1.14	—
14	3.43	1	6	4	7.1	43	29	0.24	1.47	0.98	1.71
15	3.2	1	7	5	6.7	47	33	0.21	1.49	1.07	—
16	3	1	7	5	6.3	44	31	0.19	1.31	0.94	1.5

Input voltage is set to 48 V. Inductor-counts equal to or greater than 5 are star-sequence-capable. Green cells are best.

efficiency, and the ability to reduce both the output capacitance and converter volume.

Another prominent takeaway from Table 2 is the 60% increase in maximum duty ratio that a 5-phase configuration has over a 4-phase, when employing $\mathcal{G}_5^2$ star sequencing. This large increase in duty ratio is enough to make up for reduction in V_X swing (i.e., 12 V $\rightarrow$ 9.6 V), ultimately allowing a 5-phase to exceed a 4-phase in terms of maximum output voltage. It is also interesting to notice that $\mathcal{G}_7^2$ can achieve nearly the same output voltage as $\mathcal{G}_4^1$, even after the inductor switching-node high-level voltages are reduced by 43%.

> *In general, higher odd-numbered phase-counts are preferred over lower even-numbered phase-counts when using $\mathcal{G}_N^2$ star-sequencing due to being able to achieve greater maximum-output-voltage.*

Moreover, there are incentives to running *any* general multiphase buck converter with *odd* phase-counts when the intention is to parallel multiples of the same for added output-current capability.

A. CONSIDERATIONS WHEN PARALLELING

Even with a high-inductor-count SCB (i.e. $N \geq 10$ inductors), it is unlikely that a single N-inductor SCB will have the capability of efficiently supplying current to emerging microprocessors when operating at their maximum-sustained loads. As a result, K-paralleled, N-inductor SCBs will likely be implemented as a way of not only increasing the total output-current rating of the VRM, but to also offer the chance of *input*-current-ripple cancellation, along with a further reduction of *output*-current-ripple, through interleaving. Due to the resultant layout symmetry, it is often the case that K is an even number (e.g., 2$\times$ or 4$\times$ N -inductor SCBs). Given that odd numbers are indivisible by even numbers, SCBs with odd phase-counts offer the advantage of both increased input-current-ripple cancellation *and* output-current-ripple cancellation, when paralleled and interleaved. For example, interleaving 4$\times$ 11-phase SCBs would effectively result in a 44-phase VRM. On the other hand, interleaving 4$\times$ 12-phase SCBs would result in the same 12-phases, but with increased output-current-ripple. For a general K-paralleled, N-phase buck converter, the total effective phase-count, Θ, as seen from the output, is

$$\Theta = \text{LCM}\,(N, K), \tag{13}$$

where LCM denotes the *least-common multiple*. Furthermore, the assumption is made that each N-phase buck converter is equally time-shifted by $\Delta t = T_{\text{sw}}/K$.

Of course, if both N and K are even, an effective output-phase-count of $\Theta = NK$ can still be achieved by time-shifting the K-inputs according to

$$\Delta t = \frac{T_{\text{sw}}}{N}\left(1 - \frac{1}{K}\right). \tag{14}$$

This technique has been adopted in [11], [17], but at the expense of higher input-current-ripple (due to uneven input-current-ripple cancellation), and consequently, slightly higher input-loss. Fortunately, this can be mitigated by carefully choosing a more appropriate combination of N and K (e.g., odd N and even K).

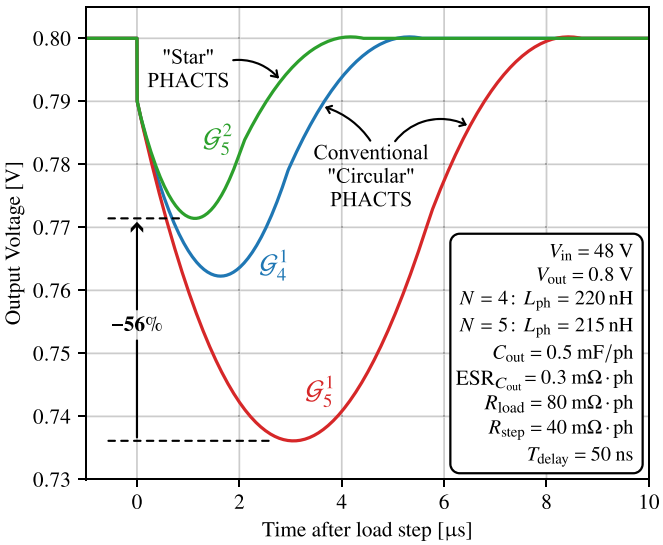


FIGURE 7. Comparing the nonlinear, time-optimal/minimum-deviation transient responses of 4- and 5-phase SCBs, with and without star-sequencing, when each is subjected to a resistive load-step equivalent to +20 A *per inductor*. (Per-phase discrete inductances are chosen such that per-phase current ripples are identical between 4- and 5-phase configurations.)

B. EFFECTS ON THE TRANSIENT RESPONSE

As a result of a simple sequence change, the increase in output voltage also enables a significantly faster load-step-up transient-recovery when compared to $\mathcal{G}_N^1$-operated SCB converters. With the extension in maximum duty ratio, more volt-seconds can be applied to each inductor over a given time. This translates into an increase in the maximum output-current-slew-rate as shown in the following expression.

$$\max\left(\sum_{k=1}^{N}\frac{\mathrm{d}i_{L_k}}{\mathrm{d}t}\right)\approx\frac{\max(V_{\text{out}})-v_{\text{out}}(t)}{L_{\text{ph}}/N},\qquad(15)$$

where L_{ph} is the discrete inductance per discrete output inductor, or the leakage inductance of each coupled output inductor. The increase in output-current-slew-rate allows the inductors to more-quickly reach their new steady-state current, effectively reducing the amount of charge pulled from the output capacitor.

Fig. 7 compares the output-voltage regulation between a 4- and 5-inductor SCB converter, after each is subjected to a light-to-heavy load-step. For a fair comparison, the resistive load-step is configured such that *each* inductor is subjected to a 20 A-rise in current. Furthermore, assuming that the per-phase switching frequency is the same, the discrete inductances are set such that the per-inductor current ripples are identical across converters. When both converters are run with the circular sequence, Table 2 shows that the maximum-output-voltage of a 5-inductor SCB is less than that of a 4-inductor SCB. Dividing both sides of (15) by N, it is clear that the corresponding 5-inductor SCB will have a lower rising-current-slew-rate *per inductor*, despite the reduced inductance of each of its inductors. Intuitively, the current of each inductor of the 5-inductor, $\mathcal{G}_5^1$-operated SCB should take longer to rise by 20 A, than the 4-inductor. Unsurprisingly, Fig. 7 shows that the 5-inductor SCB fairs worse than the 4-inductor when both are run with the circular sequence. However, with the introduction of star-sequencing, and the resultant doubling of the maximum-output-voltage for a 5-inductor SCB, both the voltage deviation and settling-time are halved. This even allows the $\mathcal{G}_5^2$-operated SCB to exceed the transient response of a $\mathcal{G}_4^1$-operated SCB.

C. THE CASE FOR HIGHER PHASE-INCREMENTS

Based on the previous discussions, the phase-increment of $|p|=2$ seems to result in the most favourable outcome as it generally enables the highest output-voltage. Naturally, this leaves one to question the utility of phase-increments greater than $|p|=2$.

Provided that $|p|=3$ offers enough duty ratio headroom for the intended operation, it should be evaluated as a potential sequence candidate. Subject to the implementation of the output inductors and the size of the power stage, $\mathcal{G}_N^3$ can be more effective than $\mathcal{G}_N^2$ in terms of:

- output voltage/current ripple cancellation;
- reducing the magnetic-flux-density hot-spots in the cores of large, asymmetrical coupled-inductors;
- lowering the current density on the PCB planes; and
- decreasing the RMS current in the distributed output capacitor bank.

These go hand-in-hand in collectively reducing losses. To understand why, let us consider the scenario where the "accordion"-style power-stage layout (see Fig. 14) is implemented for an N-inductor SCB. Moreover, rather than coupling together all N-inductors of an SCB, it is hypothetically decided that the inductors with even-numbered subscripts (left bank) are separately-coupled from those with odd-numbered subscripts (right bank). Employing $\mathcal{G}_N^2$ would cause high peak currents in both sets of coupled-inductors. This is similar to what has been documented in [18] which implements a dual-entry TLVR (transformer/inductor voltage regulator) and describes the drop in power-efficiency associated with a similar PHACTS. Of course, if all the inductors were coupled, this issue would be greatly minimized.

As for higher phase-increments (i.e., $|p|\geq 4$), it is likely that their associated drop in $\max(D)$ (see Table 1), relative to that provided by either $\mathcal{G}_N^2$ or $\mathcal{G}_N^3$, will make them unworthy of consideration. Thus, phase-increments of $|p|\in\{2,\ 3\}$ should really only be considered.

III. INCREASING THE EFFECTIVE DPWM RESOLUTION

Having a high DPWM resolution for the closed-loop digital controller is imperative as it allows the ADC resolution to be equally high. This allows the controller to more-precisely detect, and recover from, system disturbances. There are a few general techniques to increase the controller's DPWM resolution.

The first technique is to simply increase the controller's clock frequency, f_{ctrl}, while using a purely counter-based DPWM. However, the DPWM resolution will only be raised by *at most* the same factor by which the controller's clock frequency is raised. With lower VRM output-voltage-tolerances and converter switching frequencies approaching, or exceeding, 1 MHz becoming more commonplace, it is within the realm of possibility that f_{ctrl} be pushed into the multi-GHz range to simply meet the counter-based DPWM target resolution. This would significantly increase both the power consumption and design cost of the controller's integrated circuit (IC), ultimately making it impractical when both high frequency and high resolution are required.

To overcome this, a hybrid DPWM architecture uses a conventional clock-driven counter for the most-significant bits (MSBs) and a delay line for the least-significant bits (LSBs) [19], [20]. Compared to a purely counter-based solution, this hybrid architecture significantly reduces clock frequency requirements, and consequently, increases the controller's power efficiency. However, the delay line portion is particularly sensitive to lithography *process* corners, supply *voltage*, and operating *temperature* (PVT), potentially leading to a noticeably nonlinear output voltage resolution. In the future, if the controller IC is co-packaged with the power components (i.e., power switches, inductors, flying capacitors, and gate drivers), the higher thermal coupling can exacerbate the DPWM's linearity-dependence on temperature. To correct for temperature-induced delay-drift, complexity must be added to the controller in the form of online calibration.

Another approach is to use multiple clocks of the same frequency, but phase shifted from each other, to clock the DPWM [21]. This effectively raises the DPWM's resolution by a factor equal to the number of equally phase-shifted clocks. However, this can complicate the design due to different clock domains and ensuring synchronization.

The DPWM's effective output-voltage-resolution can also be increased using Σ–Δ modulation and dithering techniques [22], [23], [24]. These vary the duty ratio over time producing an average that would otherwise only be possible with higher resolution DPWMs of the aforementioned architectures. However, these time-averaging modulation techniques, like spread-spectrum modulation, can generate lower-frequency harmonics on the output voltage spectrum which can make it challenging to filter out, especially when supplying to noise-sensitive loads [25].

Despite the numerous advantages that digital controllers have over analog controllers, the complications associated with the aforementioned DPWM resolution-increase techniques might be regarded as hurdles to the designer, ultimately preventing a digital controller implementation.

A. METHOD OF MINIMUM DUTY INCREMENTS (MDI)

The introduced method presented here raises the DPWM output-voltage-resolution of an N-inductor SCB by intentionally allowing each main-switch duty ratio to differ by *at most* one least-significant bit (LSB) of ON-time from that of every other. In this way, N-additional discrete-output-voltage-steps are inserted between every larger conventional step corresponding to when all main-switch ON-times are equally-incremented together. As will be elaborated upon, *this approach works in synergy with the inherent high-gain negative-feedback that exists between currents of adjacent inductors under the influence of the SCB's inter-inductor flying capacitors*. The result is that current-imbalances—arising from slight duty-ratio-mismatches—are significantly limited, or even *reduced* to levels below those attained in the absence of duty-ratio-mismatches. Furthermore, since flying-capacitor-voltage-deviations are inter-related with inductor-current-imbalances, flying capacitor voltages (and thus, switch-voltage-stresses) remain unchanged from a practical perspective, especially in high inductor-count configurations. On top of this, the introduced method does not require a high-frequency controller clock, demanding computations, or multiple clocks. Finally, it does not introduce low-frequency harmonics, and is immune to PVT. In the following subsections, analyses are performed to verify the resultant output-voltage-resolution increase, to establish conditions that ensure voltage-step-linearity, and to quantify the extent to which both flying-capacitor-voltage-deviations and inductor-current-imbalances occur when implementing this method of *minimum duty increments* (MDI).

1) OUTPUT VOLTAGE RESOLUTION

If we denote the ordered set $\mathcal{D} = \{D_1, D_2, \ldots, D_N\}$ to contain the ON-time-to-switching-period duty-ratios of each of the N main-switches of a lossless SCB, the small-ripple-approximation (SRA) of the average output voltage, over one switching period, is

$$V_{\text{out}} = \left(\sum_{k=1}^{N} \frac{1}{D_k}\right)^{-1} V_{\text{in}} \equiv \mathcal{H}(\mathcal{D}) \frac{V_{\text{in}}}{N}, \tag{16}$$

where $\mathcal{H}$ denotes the harmonic mean of its argument, $\mathcal{D}$, which is evidently nonlinear with respect to variations of any individual element within its argument set. Incidentally, deriving (16) immediately points to what the nominal, high-level voltage is (i.e., V_{in}/N) at each inductor-switching-node of the SCB, and provides a connection to (11).

By overdriving m of N inductors with a main-switch duty ratio of $D + \Delta D$, while the rest remain at the nominal D, the SCB converter's average output voltage can be expressed by

$$V_{\text{out}} = \frac{DV_{\text{in}}}{N}\left(\frac{1+\delta}{1+\frac{N-m}{N}\delta}\right), \qquad \text{where } \delta = \frac{\Delta D}{D}. \tag{17}$$

Provided that $\delta \ll 1$, we can recognize that both the numerator and denominator, of the parenthesized factor in (17), are equal to the linearized approximations of the natural exponential function with respect to δ and centred around $\delta = 0$ (i.e., the Maclaurin series truncated to the first order). Therefore, simplifying the numerator and denominator with the natural exponential function, we obtain

$$V_{\text{out}} \approx \frac{DV_{\text{in}}}{N}\frac{\exp(\delta)}{\exp\left(\frac{N-m}{N}\delta\right)} = \frac{DV_{\text{in}}}{N}\exp\left(\frac{m}{N}\delta\right). \tag{18}$$

Reapplying the linearization to (18), we arrive at

$$V_{\text{out}} \approx \frac{DV_{\text{in}}}{N}\left(1+\frac{m}{N}\delta\right) = \frac{V_{\text{in}}}{N}\left(D+\frac{m}{N}\Delta D\right) \tag{19}$$

$$= \frac{V_{\text{in}}}{N}\left(\frac{1}{N}\sum_{k=1}^{N} D_k\right) \equiv \mathcal{A}(\mathcal{D})\frac{V_{\text{in}}}{N}, \tag{20}$$

where $\mathcal{A}$ denotes the arithmetic mean which, unlike the harmonic mean, is a linear function of all its arguments. Comparing (20) with (16), it is evident that $\mathcal{H}(\mathcal{D}) \approx \mathcal{A}(\mathcal{D})$ if $\delta \ll 1$. This is an important conclusion; rather than the input-to-output voltage conversion ratio of an SCB converter being a nonlinear function of its individual duty ratios, we can safely work under the assumption that the conversion ratio is a linear combination of its individual main-switch duty ratios (each with an equal weighting of $1/N$) if $\delta \ll 1$. Since the output voltage can now be assumed to increase approximately linearly with the number of main-switches being incrementally overdriven, this implies that the DPWM's output-voltage-resolution, ΔV_{out}, *increases by a factor of the number of inductors*, N, when using MDI. That is,

$$\Delta V_{\text{out}} = \frac{V_{\text{in}}}{NT_{\text{sw}}^{\diamond}} \xrightarrow[\text{MDI}]{} \frac{V_{\text{in}}}{N^2 T_{\text{sw}}^{\diamond}}, \tag{21}$$

where $T_{\text{sw}}^{\diamond}$ denotes the converter's switching period and the $\diamond$ superscript symbolizes the quantity's discrete fixed-point integer representation, or number of *effective* controller clock cycles. With a purely counter-based DPWM, $T_{\text{sw}}^{\diamond}$ is equal to the integer number of controller clock cycles in one switching period. For example, with a controller clock frequency of $f_{\text{ctrl}} = 100\,\text{MHz}$ and a desired converter switching frequency of $f_{\text{sw}} = 500\,\text{kHz}$, then $T_{\text{sw}}^{\diamond} = f_{\text{ctrl}}/f_{\text{sw}} = 200$. Alternatively, in a hybrid DPWM architecture that contains a counter for the MSBs of the control command, and a delay line for the LSBs, $T_{\text{sw}}^{\diamond}$ would equate to the integer number of controller clock cycles in one switching period multiplied by 2^{ℓ} (number of delay cells), where ℓ is the number of LSBs (i.e., $T_{\text{sw}}^{\diamond} = 2^{\ell} f_{\text{ctrl}}/f_{\text{sw}}$).

With the increase in the DPWM's output-voltage-resolution, the ADC resolution of the sensed output-voltage can be increased by the same factor. Fig. 8 shows the elimination of steady-state limit-cycling when employing MDI on a 48 V-to-1 V, 11-phase, $\mathcal{G}_{11}^{2}$-operated SCB, with a purely counter-based DPWM, a controller clock frequency of $f_{\text{ctrl}} = 125\,\text{MHz}$, and a switching period of $T_{\text{sw}}^{\diamond} = 352$ clock cycles. Without MDI, the DPWM's output voltage resolution is only 12.4 mV, or 1.24% of the output voltage. With MDI, the resolution is 11× greater, or 1.13 mV.

2) FLYING-CAPACITOR VOLTAGE BALANCE

To determine the flying capacitor voltage variation as a result of MDI duty-ratio "disturbances", we first use SRA to calculate the steady-state average voltage of each flying capacitor,

$$V_{C_r} = \frac{\mathcal{H}(\mathcal{D})}{\mathcal{H}\big(\mathcal{D}\setminus\{D_1,\ldots,D_r\}\big)}\frac{N-r}{N}V_{\text{in}} \approx \frac{N-r}{N}V_{\text{in}}, \tag{22}$$

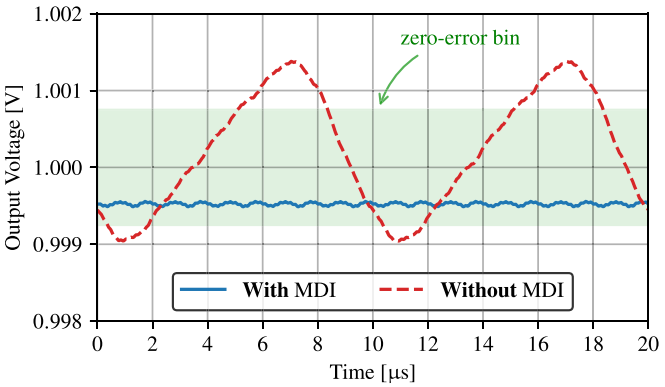


FIGURE 8. Limit-cycling avoidance through MDI as seen in the high-frequency-filtered output voltage of a 48 V–1.0 V, 11-phase SCB with 220 A load. Output-voltage ADC resolution is 1.5 mV (sampled every 2 μs) and the DPWM resolution is either 12.4 mV (without MDI) or 1.13 mV (with MDI.)

where $r \in \{1, 2, \ldots, N-1\}$, and the greyed-out expression denotes its nominal value. Although, there are $2^N - 2$ different combinations, ranging from only one main-switch being overdriven to $N-1$, the deviation of each flying capacitor (normalized to their nominal values) is found to be bounded-above by,

$$\left|\left(\frac{N}{N-r}\right)\frac{V_{C_r}}{V_{\text{in}}} - 1\right| < \delta. \tag{23}$$

This puts an upper-bound on the *nominal* switch-voltage-stress-increase to a factor of $(1+\delta)$ for $N = 2$, and $(1+2\delta)$ for $N \geq 3$ in the worst-case scenario.

3) INDUCTOR CURRENT BALANCE

The MDI method takes advantage of the tight capacitive coupling between each adjacent inductor of an SCB. The flying capacitors form a negative feedback action [26] with high gain between all inductor currents preventing large current imbalances from an effective steady-state *disturbance* (ΔD) in inductor duty ratios. To quantify any current imbalance caused by MDI, we proceed by first calculating the steady-state average current through each inductor, under the assumption that small-ripple approximation holds.

$$I_{L_k} = \frac{\mathcal{H}(\mathcal{D})}{D_k}\frac{I_{\text{load}}}{N} \approx \frac{I_{\text{load}}}{N}, \qquad k \in \{1, \ldots, N\} \tag{24}$$

where $I_{\text{load}} = V_{\text{out}}/R_{\text{load}}$ is the average resistive-load current, and the greyed-out expression denotes the nominal value for each inductor's average current. It is apparent from (24) that if the duty ratio, D_k, of an inductor, L_k, is less than the harmonic mean over the set of all duty ratios, $\mathcal{H}(\mathcal{D})$, then the corresponding inductor's average current, I_{L_k}, is higher than its nominal value. (This observation may seem counterintuitive because it is the exact opposite of what occurs in a CMB.) To further quantify the inductor current deviations, we can separate the expressions for the average currents of inductors whose duty ratios are being overdriven by ΔD, from those that

remain at the nominal value of D.

$$I_{L_k} = \begin{cases} \frac{I_{\text{load}}}{N}\left(\frac{1}{1+\frac{N-m}{N}\delta}\right), & \text{if } D_k = D + \Delta D \\ \frac{I_{\text{load}}}{N}\left(\frac{1+\delta}{1+\frac{N-m}{N}\delta}\right), & \text{if } D_k = D \end{cases} \tag{25}$$

for $m \in \{0, 1, \ldots, N\}$. Applying the natural exponential approximation to (25), under the assumption of $\delta \ll 1$ as was done in (18), and finally linearizing as in (19), we obtain

$$I_{L_k} \approx \begin{cases} \frac{I_{\text{load}}}{N}\left(1 - \frac{N-m}{N}\delta\right), & \text{if } D_k = D + \Delta D \\ \frac{I_{\text{load}}}{N}\left(1 + \frac{m}{N}\delta\right), & \text{if } D_k = D, \end{cases} \tag{26}$$

clearly showing that inductors do indeed have less than their nominal currents if they are being overdriven. Furthermore, all inductors that share the same duty ratio (i.e., D or $D + \Delta D$) have approximately the same average current.

Subtracting the two conditional equations in (25), we find that the absolute difference between the average current in one inductor from that of any other inductor, and normalized to their nominal value of I_{out}/N, is conservatively bounded above by δ as shown in

$$\left|\frac{I_{L_k} - I_{L_j}}{I_{\text{out}}/N}\right| \leq \left|\frac{\delta}{1+\frac{N-m}{N}\delta}\right| < \delta, \tag{27}$$

for any combination of $j, k \in \{1, \ldots, N\}$. Since the main-switch duty-discrepancies are *small by design*, the inductors of an SCB will not experience any significant current imbalance. This is in stark contrast to CMBs, or any other multiphase topology without passive negative feedback of inductor currents, as the state of their inductors' current-balancing is particularly sensitive to main-switch duty differences. Limited only by the losses in the converter, large inductor current imbalances would arise in CMBs if the MDI-DPWM resolution increase method was otherwise implemented.

From (17), (23), and (27), it can be ascertained that decreasing δ: increases the DPWM output voltage linearity, reduces inductor current imbalances, and decreases flying capacitor voltage deviations. Given a fixed conversion ratio, $V_{\text{out}}/V_{\text{in}}$, fixed switching frequency, f_{sw}, and fixed controller clock frequency, f_{ctrl}, this critical quantity, δ, may be diminished by increasing the inductor-count, N, as this forces a higher duty ratio (i.e., $D = NV_{\text{out}}/V_{\text{in}}$). Note that the increase in inductor-count pertains to a *single* N-inductor SCB; the reduction in δ cannot be achieved by paralleling one or more SCB converters whose sum of inductor-counts equals N. Thus, the designer is incentivized to design SCBs with the highest inductor-count to not only increase the number of balanced inductor-currents and reduce the switch-voltage-stress, but to also directly enable a higher ADC output-voltage resolution by a factor of N^2.

B. DIGITAL IMPLEMENTATION OF MDI

Normally, the digital-compensator's output, $t^{\diamond}_{\text{cmp}}$, is fed directly into the N, phase-shifted, counter-based DPWMs, each

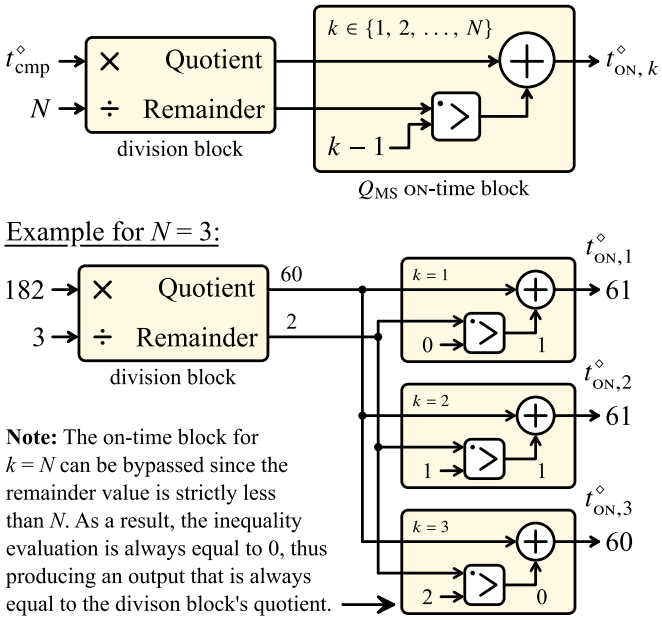


FIGURE 9. Possible logic implementation for determining the discrete ON-time of each of the N main-switches, from the compensator output.

of bit-length equal to

$$n_{\text{DPWM}} = \text{ceil}\left[\log_2\left(\frac{f_{\text{ctrl}}}{f_{\text{sw}}}\right)\right]. \tag{28}$$

This results in each of the N main-switches having the same ON-time (i.e., $t^{\diamond}_{\text{ON},k} = t^{\diamond}_{\text{cmp}}\ \forall k \in \{1, \ldots, N\}$). However, MDI specifically allows main-switch ON-times to differ by at most 1 LSB. Therefore, a custom digital block must be inserted between the compensator and the DPWMs to allow for this capability.

To determine the MDI-based main-switch ON-times for a given digital-compensator output, Fig. 9 provides a possible high-level logic implementation. As seen from the included numerical example for a 3-inductor SCB, the implementation consists of N simple combinatorial blocks, and a single division block. Since the dividend (i.e., the compensator output) is an integer value, and the divisor (i.e., the SCB's inductor-count) is always a *fixed* integer value, the complexity of the digitally-implemented division block is greatly reduced. With the inserted division block, the feedback loop (not shown) forces the compensator's output to now be approximately $t^{\diamond}_{\text{cmp}} \approx Nt^{\diamond}_{\text{ON},k}$. This requires the division block to have a bit-length of

$$n_{\text{div}} = \text{ceil}\left\{\log_2\left[\frac{Nf_{\text{ctrl}}}{f_{\text{sw}}}\max(D)\right]\right\}. \tag{29}$$

In the provided numerical example of Fig. 9, the main-switches being overdriven were arbitrarily assigned based on their subscript values. That is, for the two of three main-switches that need to be overdriven, Q_{MS1} and Q_{MS2} were arbitrarily chosen. However, to achieve the best performance, the overdrive assignments must be strategically chosen based on the converter's operating properties.

C. MINIMUM DUTY INCREMENT (MDI) ASSIGNMENTS

It is generally assumed that the inductor currents of an N-inductor SCB automatically settle to a common average value (i.e., I_{load}/N) provided that the duty ratios are equal. After all, finding the unique dc solutions for the inductor currents, as done in (24), (25), and (26), re-enforces this assumption. The underlying caveat, however, is that small-ripple approximation (SRA) is assumed to remain valid throughout the analysis. Although it significantly facilitates analyses and often produces *good-enough* insights, SRA does not necessarily yield truly accurate results simply because the assumption of small ripple does not always hold true. Consequently, subtle details can become obfuscated, independent of whether they are insignificant or profound.

With the HPC industry's insatiable desire for higher VRM densities and higher load currents, the SCB will very likely have high ripple *on both* its inductors' current and flying capacitors' voltage. Since a CMB only has high ripple on its inductor currents, it is conceivable that more subtle details will become hidden when applying SRA to an SCB given that *both* its inductor currents *and* flying capacitor voltages undergo large ripple. However, this is not to say that the previous analyses in Section III-A are no longer applicable.

Class-II multilayer ceramic capacitor (MLCCs) are the preferred choice for the flying capacitors due to their high energy density compared to those with Class-I dielectrics. However, unlike Class-I MLCCs, their capacitance is highly nonlinear with applied DC bias, i.e., their capacitance drops-off considerably with applied voltage. Therefore, assuming each flying capacitor of the SCB is composed of the same Class-II MLCCs and of the same quantity, C_1 will have a lower operating capacitance than C_{N-1} of Fig. 1. This effect is magnified for higher inductor-count SCB configurations since the difference between the minimum and maximum bias voltage grows with N as shown by

$$V_{C_1} - V_{C_{N-1}} = \left(1 - \frac{2}{N}\right) V_{\text{in}} \xrightarrow[\text{High } N]{} V_{\text{in}}. \tag{30}$$

This is compounded by the fact that the effective flying capacitance seen at the switching node of L_2 is the series combination of C_1 and C_2, producing a value of $\mathcal{H}\{C_1, C_2\}/2$, where $\mathcal{H}$ denotes the harmonic mean as defined in (16). This low effective flying capacitance can affect the accuracy of SRA on the flying capacitor voltage, potentially invalidating the assumption of inductor-current-balance.

Fig. 10 plots the total inductor-current-imbalance of a *lossless* 12 V–0.8 V, 3-phase SCB over range of $\{C_1, C_2\}$ combinations. (See Appendix for details on large-signal modelling.) As each flying capacitor increases in capacitance, the lower the voltage ripple, and thus, higher convergence of inductor currents. Perhaps the most important takeaway from Fig. 10 is that there is *never perfect* current balance for inductor-count configurations of $N \geq 3$, due to at least one inductor seeing a series combination of flying capacitances.

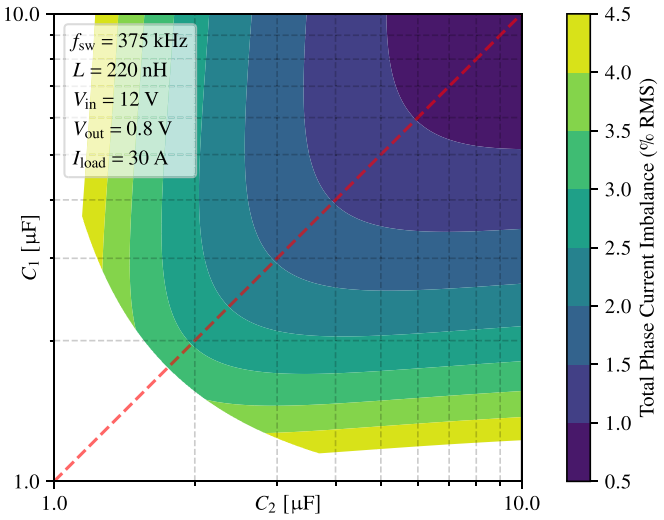


FIGURE 10. Total inductor-current-imbalance for a *lossless* 3-inductor SCB caused solely by differences in effective flying capacitance seen per inductor. Blank areas indicate invalid operation as the inductor switching nodes enter discontinuous voltage mode (DVM) from excessive flying capacitor voltage swing. The dashed red line of symmetry indicates points of equal C_1 and C_2. Region of interest is lower right since typically $C_1 < C_2$ from derating.

> *In general, when all main-switch* ON *-times are identical, the inductors which see the least effective flying capacitance (the highest impedance) have the lowest average current, while those that see the highest capacitance (the least impedance) have the highest current.*

This is analogous to a lossy CMB where phases with the highest parasitic resistance have the lowest current, and vice-versa (assuming all phases are otherwise identical and no active current balancing is employed).

The previous analysis implies that a non-negligible inductor current imbalance has the potential to arise in higher inductor-count SCB configurations, due to larger effective flying capacitance differences seen at the switching nodes. To address this issue, we must strategically implement the introduced DPWM resolution increase technique so that MDIs do not further exacerbate the imbalance shown by (25). Suppose we want to incrementally increase the output voltage in the smallest possible increments. A seemingly inconsequential approach might be to arbitrarily overdrive main-switches in increasing order of their subscripts (i.e., $Q_{\text{MS1}} \rightarrow Q_{\text{MS2}} \rightarrow Q_{\text{MS3}} \ldots$), as done in Fig. 9. However, we know from (25) that overdriving a main-switch's ON-time actually reduces its inductor's average current. This is a similar counterintuitive effect to that which causes flying capacitor voltage instability in multilevel flying capacitor converters [28]. Thus, overdriving the main-switches whose inductors already have the lowest current (i.e., L_2, L_3, L_4, etc.) prior to the main-switches whose inductors have the highest current (i.e., L_N, L_{N-1}, etc.) would further increase the total-current-imbalance.

To minimize the total current imbalance when applying the method of MDIs, we developed a main-switch overdrive assignment that is based around the steady-state properties

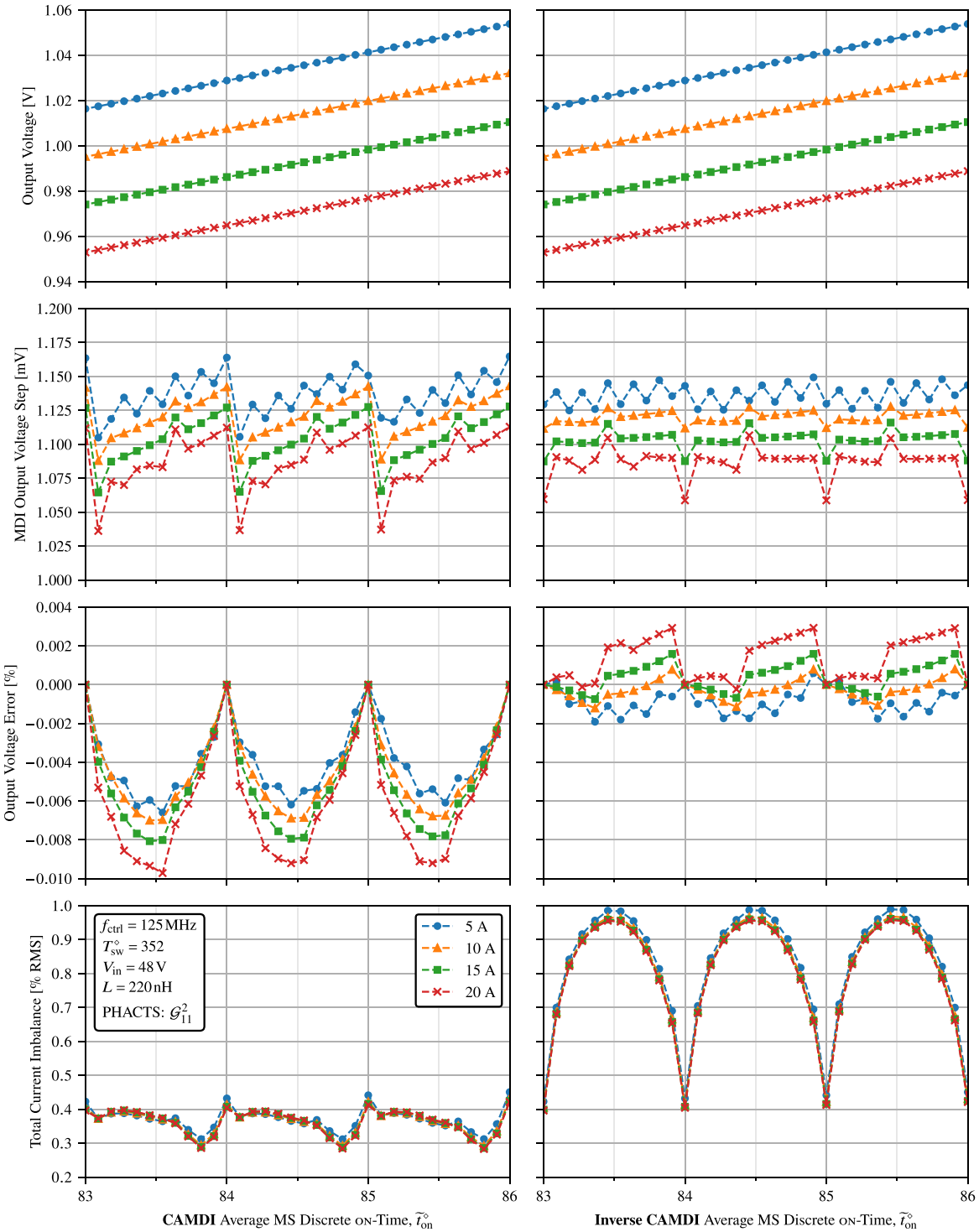


FIGURE 11. Simulated 11-phase SCB (with conduction losses only) comparing the effects of CAMDI vs. Inverse-CAMDI on the total current-imbalance and DPWM output-voltage linearity over a range of average main-switch discrete ON-times and nominal per-inductor current loads.

of the SCB converter. This MDI assignment is in order of *decreasing effective flying capacitance* seen by each inductors' switching node. This order is termed *capacitance-aware minimum duty increment*, or CAMDI. An example of such an assignment is demonstrated in Table 3 (and illustrated in Fig. 12) for an 11-inductor 48 V SCB topology, using 6×10 µF Class-II MLCCs [27] for each flying capacitor.

As for the digital implementation, Fig. 13 presents the modification to the 3-inductor example in Fig. 9. Since the main-switch overdrive assignments are static (i.e., the designer hardcodes them based on knowledge of the flying capacitor properties), no additional computational complexity is added—only net reassignments are involved as shown in Fig. 13.

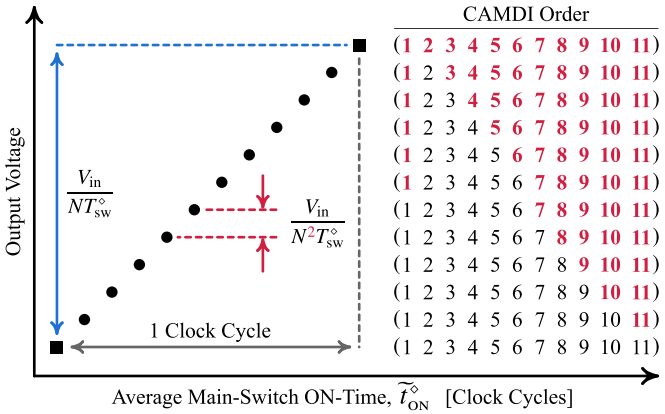
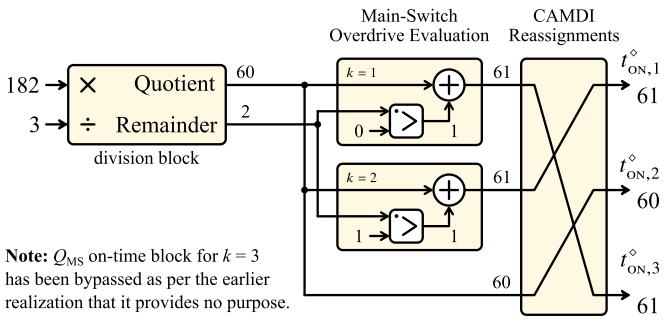


FIGURE 12. Example of the DPWM's output voltage resolution increase using the CAMDI order of Table 3 of an 11-phase SCB. Bolded red numbers indicate which phases' main-switch ON-times are being overdriven by one effective clock cycle for the corresponding output voltage set-point.

TABLE 3. Capacitance-Derating Nature of 6× Parallel 10 µF Class-II MLCCs [27] in a 48 V-Input, 11-Inductor SCB, and the Wide Variation of Effective Flying Capacitance Seen by Each Inductor

Flying Cap.	Bias Voltage (nom.) [V]	Derated C_{fly} [µF]	Output Inductor	Effective C_{fly} [µF]	CAMDI Order
C_1	43.6	18	L_1	18	6
C_2	39.3	19.8	L_2	10.2	11
C_3	34.9	22.9	L_3	11.7	10
C_4	30.5	25.9	L_4	12.2	9
C_5	26.5	30.1	L_5	13.9	8
C_6	21.8	35	L_6	16.2	7
C_7	17.5	40.8	L_7	18.8	5
C_8	13.1	46.8	L_8	21.8	4
C_9	8.7	53.1	L_9	24.9	3
C_{10}	4.4	58	L_{10}	27.7	2
—	—	—	L_{11}	58	1

The corresponding CAMDI order is also displayed for this specific implementation indicating which phase's on-time is subsequently overdriven when incrementally-increasing the output voltage.



Note: Q_{MS} on-time block for $k = 3$ has been bypassed as per the earlier realization that it provides no purpose.

FIGURE 13. Example of main-switch ON-time reassignments, as enforced by CAMDI, being applied to a 3-inductor SCB with $C_1 < C_2$.

The simulated effects of CAMDI are illustrated in Fig. 11 for the 48 V, 11-phase SCB converter, across a range of nominal per-inductor current loads. They are also contrasted against the effects produced by the opposite MDI assignment—*Inverse*-CAMDI. As expected, the current-imbalance is minimized through the use of CAMDI. In fact, over this particular range of average ON-times, $\widetilde{t}_{ON}^{\diamond}$, CAMDI actually results in lower total-current-imbalance relative to when all main-switch ON-times are the same (i.e., when $\widetilde{t}_{ON}^{\diamond}$ is an integer). Conversely, it can be seen that Inverse-CAMDI worsens the current imbalance. Interestingly, the opposite is true for the MDI-DPWM output voltage linearity as Inverse-CAMDI actually results in more consistent output-voltage-steps compared to CAMDI. This unexpected behaviour is the result of higher-order terms coming into play, which remain hidden from SRA-only analyses. However, the difference in DPWM linearity (between CAMDI and Inverse-CAMDI) is only approximately 0.01%. This is 50× smaller than the difference in current imbalance of approximately 0.5%. Thus, CAMDI is the preferred main-switch ON-time-overdrive assignment compared to Inverse-CAMDI.

IV. EXPERIMENTAL RESULTS

A discrete 48 V, 11-inductor SCB was fabricated (see Fig. 14 and Fig. 16)[2] using the components listed in Table 4 to validate the modulation techniques presented in Sections II and III. An open-loop controller was implemented on an FPGA running with a modest clock frequency of 125 MHz feeding 11 purely counter-based 9-bit DPWMs. With a counter period of $T_{sw}^{\diamond} = 352$ clock cycles, a switching frequency of 355 kHz was ultimately generated. Additionally, star sequencing was implemented to raise the output voltage ceiling, allowing the converter to generate a 1 V output while maintaining 11 phases. Otherwise, the output voltage would be limited to 0.4 V using the conventional circular PHACTS.

Figs. 15 and 17 show the experimental steady-state waveforms for the $\mathcal{G}_{11}^2$ star-sequence. With an extended duty ratio of nearly 25% (well within the permissible limits stated in Table 2), this star-sequence clearly forms a valid PHACTS since it ensures that adjacent main-switch ON-times do not overlap. This is evidenced in Fig. 15, both by the same nominal voltage swing appearing on all inductor switching nodes, and the absence of adjacent inductor switching node voltage swing overlap. Evidence of a non-valid PHACTS would be a combination of:

- unequal nominal voltage swings at the switching nodes of the inductors;
- abrupt switching node voltage jumps when inductors are being energized; and
- an appreciable imbalance of inductor currents when using equal duty ratios.

Note that only the currents for L_2 and L_{11} are shown in Fig. 17. Given that L_2 and L_{11} have the lowest and highest average currents, respectively, plotting only their currents is sufficient to infer the persistence of steady-state current balancing among all inductors when using MDI.

[2]Rather than a pure SCB, photos of the *multilevel* series-capacitor buck (MLSCB) converter [8] are shown. The extra components of the MLSCB remain unused for the experiments in this article (i.e. Q_{TRP} turns-ON/OFF in-sync with Q_{MS1}, while each Q_{TMS} remains permanently OFF).

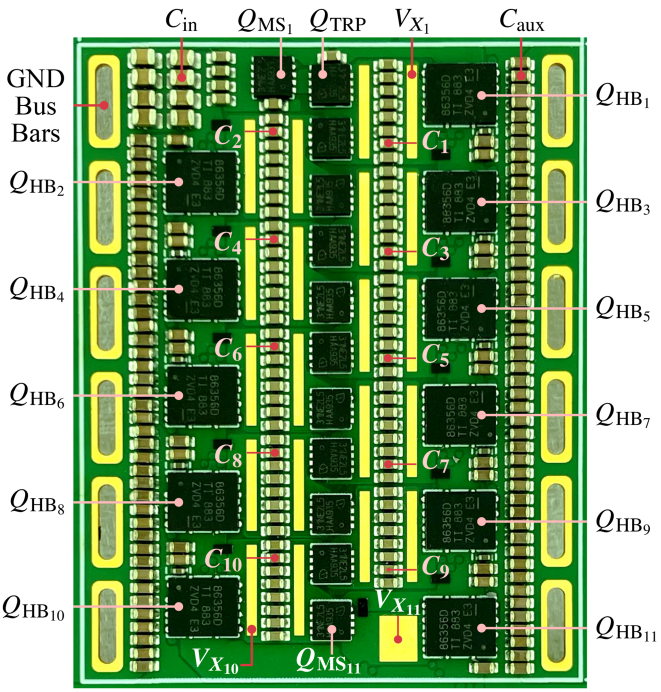


FIGURE 14. Photograph of 11-phase MLSCB switching platform (top). The Q_{SR}/Q_{TMS} half-bridges are denoted by Q_{HB}. Dimensions of the outer enclosing silkscreen rectangle are 43 × 55 mm. Inductors (not shown) are mounted vertically to each V_X connecting the switching platform to the load platform (placed directly above) which contains the output capacitors and load steps.

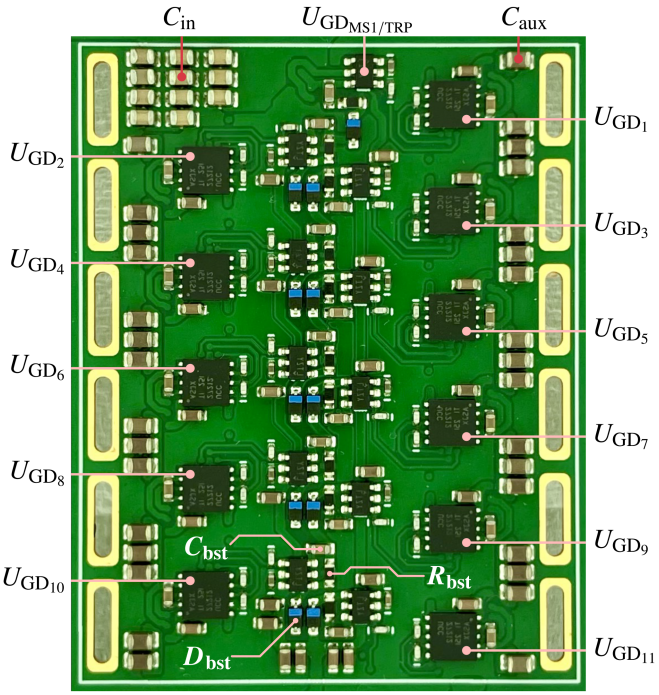


FIGURE 16. Flipped photograph of 11-phase MLSCB switching platform (bottom) showing the Q_{MS} high-side gate drivers, as well as their conventional cascaded bootstrap circuits, and Q_{SR}/Q_{TMS} half-bridge gate drivers. In the experiments, only the low-side Q_{SR} is toggled; Q_{TMS} remains OFF by biasing it drain at 12 V.

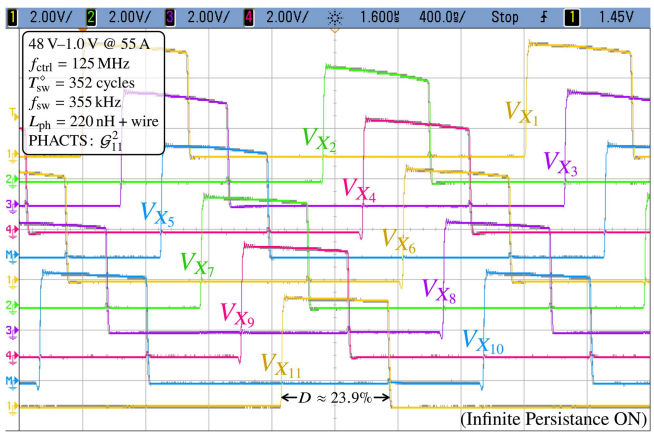


FIGURE 15. Annotated oscilloscope screenshot of all 11 inductor switching node voltages while increasing the *average* discrete main-switch ON-time over 84–85 clock cycles using the CAMDI order. *Infinite persistence* is maintained throughout the minimum duty increments to quantify the extent of flying capacitor voltage shifts that might increase switch voltage stress.

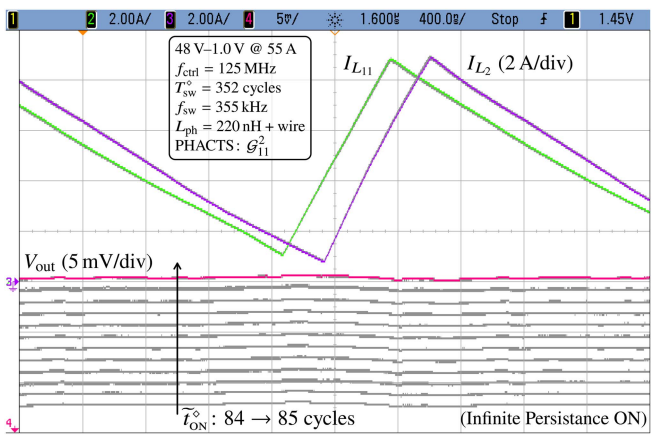


FIGURE 17. Annotated oscilloscope screenshot of inductor currents for L_2 and L_{11} along with the rising output voltage (visible through *infinite persistence*) from increasing the *average* discrete main-switch ON-time over 84–85 clock cycles using the CAMDI order. This measurement is performed to quantify the extent of current imbalances that occur from intentional duty ratio inequalities.

These two scopeshots also show the effects of CAMDI. The effects are made visible by setting infinite persistence on the oscilloscope while individually raising the $t^{\diamond}_{ON}$ of each main-switch by one clock cycle (from 84 to 85) according to the order presented in Fig. 12, for a total of $N = 11$ steps. Fig. 17 shows the corresponding successive rise in output voltage over the 11 steps. According to (23) and (27), the normalized flying capacitor voltage deviation and interphase inductor current imbalance should both be less than δ. In this experimental setup, $\delta = 1/t^{\diamond}_{ON} \approx 1.2\%$, which would explain the lack of any noteworthy variability in either the inductor switching node voltage waveforms of Fig. 15 and inductor currents of Fig. 17. This shows that if δ is sufficiently small, there will be no practical increase to switch-voltage-stress or inductor-current-imbalance.

With a switching period of $T^{\diamond}_{sw} = 352$, a DPWM resolution of 1.127 mV can be expected according to (21). As seen in Fig. 18, an output voltage of around 1.0 V was

TABLE 4. List of Prominent Components Used in the 11-Phase SCB Discrete Prototype

Item	Manufacturer	Part Number	Notable Specifications
Output Inductor	Würth Elektronik	7443082022	L = 220 nH, DCR = 0.18 mΩ, f_{res} = 52 MHz, I_{sat} = 40 A @ 125°C
Main Switch, Q_{MS}[§]	Infineon	BSZ031NE2LS5	$R_{DS(on)}$ = 3.7 mΩ, BV_{DSS} = 25 V, Q_G = 13 nC, C_{OSS} = 800 pF
Trans. Rev. Pol. Switch, Q_{TRP}[†]	Infineon	BSZ031NE2LS5	$R_{DS(on)}$ = 3.7 mΩ, BV_{DSS} = 25 V, Q_G = 13 nC, C_{OSS} = 800 pF
Transient Main Switch, Q_{TMS}[‡] Synchronous Rectifier, Q_{SR}[¶]	Texas Instruments	CSD86356Q5D	Q_{TMS}: $R_{DS(on)}$ = 4.2 mΩ, BV_{DSS} = 25 V, Q_G = 10 nC, C_{OSS} = 850 pF Q_{SR}: $R_{DS(on)}$ = 1.8 mΩ, BV_{DSS} = 25 V, Q_G = 24 nC, C_{OSS} = 2 nF
Flying Capacitor	Murata	GRM32EC72A106KE05L	10 µF (± 10%), 100 V, 1210, X7S (×6) (*before derating*)
Q_{SR} Schottky Diode	Diodes Inc.	SDM2U20CSP-7	20 V_{RR}, 2.0 A_F, 0.47 V_F, 114 pF @ 4.5 V, 25°C
Q_{MS} Gate Drivers	Analog Devices	LTC4440ES6	80 V_{BST}, 1.85 Ω_{SNK}, 1.1 A_{SRC}
Q_{MS} Bootstrap Diode	Infineon	BAS3010	30 V_{RR}, 1.0 A_F, 0.41 V_F, 22 pF @ 10 V, 25°C
Q_{TMS} / Q_{SR} Gate Driver	Texas Instruments	UCC27212D	120 V_{BST}, 4.0 A_{SNK}, 4.0 A_{SRC}
Output Capacitor	Panasonic Samsung	EEF-GX0E471L CL10A226KQ8NRNE	470 µF (± 20%), 2.5 V, 2917, 3 mΩ, 3-term. (×18) 22 µF (± 10%), 6.3 V, 0603, X5R (×82) (*before derating*)

§ The main-switch's drain-source ON-resistance, $R_{DS(on)}$, and gate-charge, Q_G, are based on avg(V_{GS}) = 10 V @ T_C = 125°C. The output charge, C_{OSS}, is based on V_{DS} = 4.5 V.
† The transient reverse polarity protection switch, Q_{TRP}, exists in series with Q_{MS1}, forming a 4-quadrant switch that interfaces with the input voltage. In this experiment, it is toggled in-sync with Q_{MS1}.
‡ The transient main switch, Q_{TMS}, is the high-side switch in the CSD86356Q5D half-bridge which also contains Q_{SR} for each inductor. Each Q_{TMS} remains permanently OFF by biasing the drain with 12 V_{aux}.
¶ The synchronous rectifier's drain-source ON-resistance, $R_{DS(on)}$, and gate-charge, Q_G, are based on V_{GS} = 7 V @ T_C = 125°C. The output charge, C_{OSS}, is based on V_{DS} = 4.5 V.
Greyed-out components are part of the Multilevel SCB (MLSCB) [8].

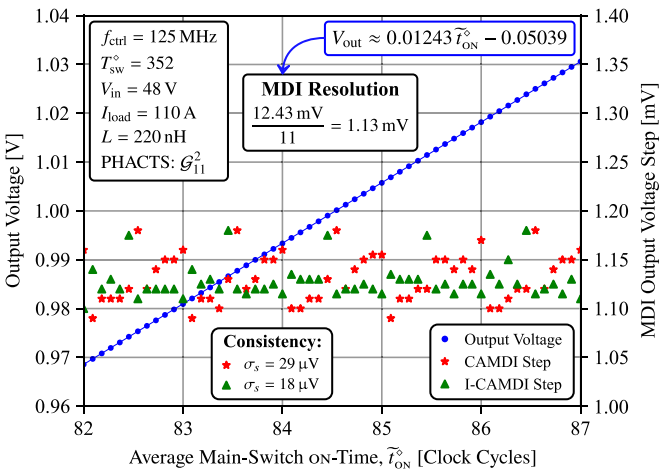


FIGURE 18. MDI experimental results highlighting the linearity of the output voltage with respect to the average discrete main-switch ON-time over all phases.

attained (enabled by $\mathcal{G}^2_{11}$) and the MDI-DPWM resolution is 1.13 mV, with a sample standard deviation of 29 µV and 18 µV, for CAMDI & Inverse-CAMDI, respectively. The maximum absolute differential nonlinearity, |DNL|, for CAMDI and Inverse-CAMDI is 0.053 LSB and 0.047 LSB, respectively, indicating excellent linearity and no missing codes. These results confirm the large increase in effective output-voltage resolution, showing the ability of MDI in achieving highly-accurate voltage regulation.

V. CONCLUSION

Three modulation techniques are presented in this article for an N-inductor series-capacitor buck (SCB) converter. The first modulation technique raises the maximum output voltage while maintaining N equally-separated phases. The technique eliminates the constraints of traditionally-used sequencing techniques, thereby enabling the use of high-inductor-count *and* high-phase-count SCB converters in emerging high-step-down, high-current applications. This is achieved through a modulation scheme, termed *star-sequencing*, which arises for SCB inductor-counts of $N \geq 5$. It was also found that *higher odd-numbered phase-counts* are more effective than *lower even-numbered phase-counts* in extending the output-voltage-range.

Since the SCB requires more sophisticated control that the conventional buck topology, digital control is often a preferred solution. However, to achieve the sufficiently-high voltage-regulation required by emerging microprocessors, a very-high-resolution DPWM might be required, which itself could be hardware-demanding. The second modulation technique increases the DPWM's effective output-voltage-resolution by a factor of N through a method of *minimum duty increments* (MDI). By working synergistically with the SCB's inherent properties, there is very little hardware complexity associated with the digital implementation of MDI.

This article also unveils how, in high-inductor-count SCB converters, slight inductor-current-imbalances can arise due to differences in effective-flying-capacitances seen by each inductor. Despite populating each flying capacitor of the SCB with the same type and quantity of capacitors, these variations of effective-flying-capacitances seen by each inductor arise from voltage-induced capacitance-derating and series-combinations of flying capacitances occurring when $N \geq 3$. The resulting variation in voltage ripple between effective-flying-capacitances generates small, but detectable, inductor-current-imbalances as a result of higher-order effects not captured by SRA-based analyses. To prevent further current imbalances as a result of MDI-induced main-switch duty-ratio-mismatches, a third modulation technique is

introduced. This technique is named Capacitance-Aware MDI (CAMDI) and describes the MDI implementation based on the flying capacitances. CAMDI minimizes inductor-current-imbalances when employing MDI, or even reduces them to levels below those attained without main-switch duty-ratio-mismatches. Inverse-CAMDI was found to achieve the most linear output voltage step, but at the expense of higher current imbalances. The presented experimental results correlate well with the theories, confirming: (1) extension of the output voltage range while maintaining N-phases without an increase to switch-voltage-stresses, (2) significant increase in output-voltage-resolution, and (3) maintenance of inductor-current-balancing.

APPENDIX: LARGE-SIGNAL MODELLING

The following supplementary content provides a general formulation to calculate the exact, open-loop, steady-state operating point of converters whose switching instances are not reliant upon the time-dependent states of its own reactive elements. Therefore, forced continuous inductor-current mode (CCM) and continuous capacitor-voltage mode (CVM) are assumed to hold. Since the following analysis does not make the assumption that small-ripple approximation (SRA) holds, subtle intricacies may be revealed with respect to the converter's operating point that may otherwise remain hidden under SRA. The utility of this analysis is that revelations may arise that can subsequently inform various design and/or controller implementations. For example, the inevitable inductor-current-imbalance in SCB converters with more than two inductors—a consequence of unequal effective flying capacitances/impedances seen by each inductor—is revealed only through large-signal analysis. This phenomenon then informs the inductor-overdrive assignments (when implementing the method of minimum duty increments) to strategically reduce the total current imbalance across all inductors.

A. GENERAL DERIVATION OF TIME-DEPENDENT STATE VALUES

To aid in the general formulation of the steady-state value(s) of the reactive element(s) in a converter, we shall fittingly consider a 2-inductor SCB. It's steady-state operation can be considered as alternating between the following three distinct topological switching states:

- Q_{MS1} is turned-ON while Q_{MS2} is turned-OFF;
- Q_{MS1} is turned-OFF while Q_{MS2} is turned-ON; and
- Q_{MS1} and Q_{MS2} are both turned-OFF.

Recall from Section II that we are restricting ourselves from simultaneous activation of adjacent main-switches to prevent increased switch voltage stresses. Therefore, turning-ON both Q_{MS1} and Q_{MS2} is not a switching state that will be considered in this analysis.

The time-evolution of each reactive component in the converter can be described by the following linear system of non-homogeneous ordinary differential equations:

$$\frac{\mathrm{d}\mathbf{x}(t)}{\mathrm{d}t} = \mathbf{A}_k\mathbf{x}(t) + \mathbf{B}_k\mathbf{v}(t) \tag{31}$$

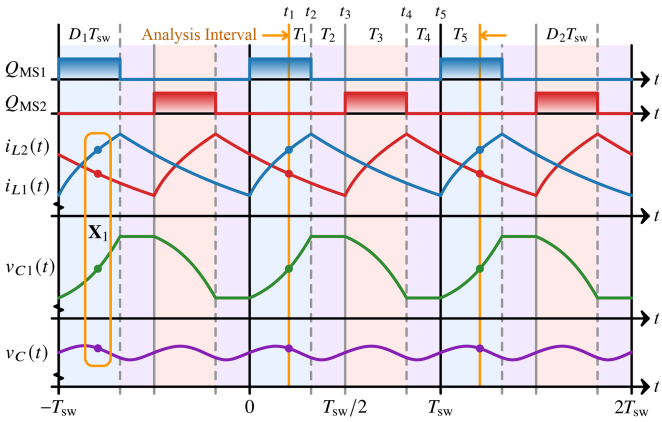


FIGURE 19. State diagram of a 2-inductor SCB converter in steady-state.

$$\mathbf{y}(t) = \mathbf{E}_k\mathbf{x}(t) + \mathbf{F}_k\mathbf{v}(t), \tag{32}$$

where $\mathbf{x}(t) = [i_{L1}(t) \quad i_{L2}(t) \quad v_{C1}(t) \quad v_C(t)]^\intercal$ is the state vector, $\mathbf{v}(t)$ is the input vector, and $\mathbf{y}(t)$ is the output vector. $k \in \{1, \ldots, M\}$ denotes the time interval where M is the number of time intervals traversed in one switching period. M can vary depending on where the steady-state operating point is assigned to be (e.g., on a modulation edge, somewhere in between modulation edges as in Fig. 19, etc.). It is also assumed that coefficients $\mathbf{A}_k$, $\mathbf{B}_k$, $\mathbf{E}_k$, and $\mathbf{F}_k$, remain constant within a given time interval. That is, capacitances, inductances, resistances, etc. are approximated as being independent of time and on their own state values (i.e., voltage for capacitors and current for inductors) *within the time interval*.

Using either the method of integrating factors or variation of parameters, the solution to (31) is

$$\mathbf{x}(t) = e^{\mathbf{A}_k(t-t_k)}\mathbf{x}(t_k) + \int_{t_k}^{t} e^{\mathbf{A}_k(t-\tau)}\mathbf{B}_k\mathbf{v}(\tau)\,\mathrm{d}\tau, \tag{33}$$

where $t \in [t_k,\ t_k + T_k]$. t_k is defined as either the beginning of a switching state (i.e., at one of the modulation edges), or in the case of t_1, the beginning of the analysis window, which may or may not be at a modulation edge; in the case of Fig. 19, t_1 resides between modulation edges. Finally, T_k is defined as the length of the kth time interval. In the case of T_1, it is the difference between t_1 and the next modulation edge. In the case of T_M, it is the difference between the end of the analysis window and t_M. For all other values of $k \in \{2, \ldots, M-1\}$, T_k is the duration of a switching state.

Since our focus is on steady-state operation, the input vector is constant (i.e., $\mathbf{v}(t) = \mathbf{V}$). This simplification allows us to solve the convolution integral in (33) to attain the following closed-form expression for the large-signal, time-domain state evolution,

$$\mathbf{x}(t) = e^{\mathbf{A}_k(t-t_k)}\mathbf{x}(t_k) + \left[e^{\mathbf{A}_k(t-t_k)} - \mathbf{I}\right]\mathbf{A}_k^{-1}\mathbf{B}_k\mathbf{V}. \tag{34}$$

By definition, $\mathbf{x}(t) = \mathbf{x}(t + T_{sg})$ in steady-state operation, where T_{sg} is the global switching period. In the case of the SCB, the global switching period is equal to just the main-switch period, T_{sw}, as shown in Fig. 19. For other topologies with different modulations (i.e., multiphase converters fed by an upstream network(s) of flying capacitors [17], [29], [30]),

the global switching period may be greater than T_{sw} to enforce steady-state inductor current balancing.

Without loss of generality, our desired steady-state operating point, $\mathbf{x}(t_1) = \mathbf{x}(t_M + T_M) = \mathbf{x}(t_5 + T_5) \equiv \mathbf{X}_1$, is some time when Q_{MS1} is ON as indicated in Fig. 19. To determine $\mathbf{X}_1$, we proceed by recursively calculating the state vector throughout the global switching period of M time-intervals. For the operating point in Fig. 19, these recursions are:

$$\mathbf{x}(t_2) = e^{\mathbf{A}_1 T_1}\mathbf{X}_1 + \left[e^{\mathbf{A}_1 T_1} - \mathbf{I}\right]\mathbf{A}_1^{-1}\mathbf{B}_1\mathbf{V} \tag{35}$$

$$\mathbf{x}(t_3) = e^{\mathbf{A}_2 T_2}\mathbf{x}(t_2) + \left[e^{\mathbf{A}_2 T_2} - \mathbf{I}\right]\mathbf{A}_2^{-1}\mathbf{B}_2\mathbf{V} \tag{36}$$

$$\mathbf{x}(t_4) = e^{\mathbf{A}_3 T_3}\mathbf{x}(t_3) + \left[e^{\mathbf{A}_3 T_3} - \mathbf{I}\right]\mathbf{A}_3^{-1}\mathbf{B}_3\mathbf{V} \tag{37}$$

$$\mathbf{x}(t_5) = e^{\mathbf{A}_4 T_4}\mathbf{x}(t_4) + \left[e^{\mathbf{A}_4 T_4} - \mathbf{I}\right]\mathbf{A}_4^{-1}\mathbf{B}_4\mathbf{V} \tag{38}$$

$$\mathbf{X}_1 = e^{\mathbf{A}_5 T_5}\mathbf{x}(t_5) + \left[e^{\mathbf{A}_5 T_5} - \mathbf{I}\right]\mathbf{A}_5^{-1}\mathbf{B}_5\mathbf{V}. \tag{39}$$

In this example, some matrix coefficients are equal across time intervals because they belong to the same switching states (i.e., $\mathbf{A}_1 = \mathbf{A}_5$, $\mathbf{B}_1 = \mathbf{B}_5$, $\mathbf{A}_2 = \mathbf{A}_4$, and $\mathbf{B}_2 = \mathbf{B}_4$). Furthermore, $\mathbf{B}_2 = \mathbf{B}_3 = \mathbf{B}_4 = \mathbf{0}$ since there is no input filter. Similar realizations for simplification can be applied to general converters to facilitate analyses.

Substituting (38) into (39), then (37) into that, and so on, we arrive at the following form,

$$\mathbf{X}_1 = \mathbf{\Psi}\mathbf{X}_1 + \mathbf{\Gamma}\mathbf{V}. \tag{40}$$

Equation (40) can be rearranged to finally solve for the *exact* steady-state operating point at t_1,

$$\mathbf{X}_1 = (\mathbf{I} - \mathbf{\Psi})^{-1}\mathbf{\Gamma}\mathbf{V}. \tag{41}$$

$\mathbf{\Psi}$ is the *state-propagation matrix* and is defined as

$$\mathbf{\Psi} = \overset{\curvearrowleft M}{\prod_{k=1}} e^{\mathbf{A}_k T_k}. \tag{42}$$

The anti-clockwise arrow in (42) instructs that subsequent matrix exponentials shall be prepended. Based on the chosen location for t_1 in Fig. 19, the state-propagation matrix is

$$\mathbf{\Psi} = e^{\mathbf{A}_5 T_5} e^{\mathbf{A}_4 T_4} e^{\mathbf{A}_3 T_3} e^{\mathbf{A}_2 T_2} e^{\mathbf{A}_1 T_1}. \tag{43}$$

$\mathbf{\Gamma}$ is the *input-to-steady-state matrix* and is defined as

$$\mathbf{\Gamma} = \sum_{k=1}^{M}\left[\overset{\curvearrowleft M}{\prod_{i=k+1}} e^{\mathbf{A}_i T_i}\right]\left(e^{\mathbf{A}_k T_k} - \mathbf{I}\right)\mathbf{A}_k^{-1}\mathbf{B}_k. \tag{44}$$

Based on the location for t_1 in Fig. 19,

$$\begin{aligned}\mathbf{\Gamma} = {} & e^{\mathbf{A}_5 T_5} e^{\mathbf{A}_4 T_4} e^{\mathbf{A}_3 T_3} e^{\mathbf{A}_2 T_2}\left(e^{\mathbf{A}_1 T_1} - \mathbf{I}\right)\mathbf{A}_1^{-1}\mathbf{B}_1 \\ & + e^{\mathbf{A}_5 T_5} e^{\mathbf{A}_4 T_4} e^{\mathbf{A}_3 T_3}\left(e^{\mathbf{A}_2 T_2} - \mathbf{I}\right)\mathbf{A}_2^{-1}\mathbf{B}_2 \\ & + e^{\mathbf{A}_5 T_5} e^{\mathbf{A}_4 T_4}\left(e^{\mathbf{A}_3 T_3} - \mathbf{I}\right)\mathbf{A}_3^{-1}\mathbf{B}_3 \\ & + e^{\mathbf{A}_5 T_5}\left(e^{\mathbf{A}_4 T_4} - \mathbf{I}\right)\mathbf{A}_4^{-1}\mathbf{B}_4 \\ & + \left(e^{\mathbf{A}_5 T_5} - \mathbf{I}\right)\mathbf{A}_5^{-1}\mathbf{B}_5.\end{aligned} \tag{45}$$

B. GENERAL DERIVATION OF LARGE-SIGNAL-AVERAGE STATE VALUES

Equation (40) gives us the state value at one time point within the global switching period. With (32), the desired output values may be calculated at the same location. To instead find the output's large-signal steady-state-average[3] value, $\overline{\mathbf{Y}}$, we simply integrate (32) over the global switching period and normalize it with respect to the global switching period.

$$\overline{\mathbf{Y}} = \frac{1}{T_{sg}}\int_{t}^{t+T_{sg}} \mathbf{y}(\tau)\,\mathrm{d}\tau \tag{46}$$

To aid in the computation of the integral, it is helpful to split the integrand into its M intervals where it is differentiable,

$$\overline{\mathbf{Y}} = \frac{1}{T_{sg}}\sum_{k=1}^{M}\int_{t_k}^{t_k+T_k} \left[\mathbf{E}_k\mathbf{x}(t) + \mathbf{F}_k\mathbf{V}\right]\,\mathrm{d}t. \tag{47}$$

Substituting (34) into (47) allows us to find the closed-form solution of the kth definite integral,

$$\begin{aligned}\int_{t_k}^{t_k+T_k} \left[\mathbf{E}_k\mathbf{x}(t) + \mathbf{F}_k\mathbf{V}\right]\,\mathrm{d}t = {} & \left(\mathbf{F}_k - \mathbf{E}_k\mathbf{A}_k^{-1}\mathbf{B}_k\right)\mathbf{V}T_k \\ & + \mathbf{E}_k\mathbf{A}_k^{-1}\left(e^{\mathbf{A}_k T_k} - \mathbf{I}\right)\left(\mathbf{X}_k + \mathbf{A}_k^{-1}\mathbf{B}_k\mathbf{V}\right),\end{aligned} \tag{48}$$

where $\mathbf{X}_k \equiv \mathbf{x}(t_k)$. Note that $\mathbf{X}_k$ (where $k \in \{2, \ldots, M\}$) can be determined using (34) or (35)–(38), with the already-calculated $\mathbf{X}_1$. Therefore, the explicit solution to (46) is

$$\begin{aligned}\overline{\mathbf{Y}} = \frac{1}{T_{sg}}\sum_{k=1}^{M}\Big[& \mathbf{E}_k\mathbf{A}_k^{-1}\left(e^{\mathbf{A}_k T_k} - \mathbf{I}\right)\left(\mathbf{X}_k + \mathbf{A}_k^{-1}\mathbf{B}_k\mathbf{V}\right) \\ & + \left(\mathbf{F}_k - \mathbf{E}_k\mathbf{A}_k^{-1}\mathbf{B}_k\right)\mathbf{V}T_k\Big].\end{aligned} \tag{49}$$

C. EMULATING CLOSED-LOOP RESPONSES

Given a fixed input voltage, the switching state durations need to be known to attain a targetted average output voltage, $V_{out}^{\odot}$. Unfortunately, it is challenging to derive the closed-form expression for the duration of each switching state, T_k, from the large-signal average-output of (49). A decent first guess is to calculate them using the standard SRA dc averaging procedure. However, after plugging in the SRA-calculated switching-state durations into (49), one will typically find that the result slightly differs from $V_{out}^{\odot}$. This is exemplified in the 2-inductor SCB case study of Fig. 20, where the SRA-calculated durations result in a 2.8% error in average output voltage. This discrepancy is not because the large-signal analysis is incorrect; rather, it is due to the assumptions of small voltage/current-ripple not holding up to reality (especially so in hybrid switched-capacitor topologies like the SCB where

[3] Since time-averaging is a linear operation, a closed-form matrix solution can be found. However, it is sometimes desired to know the RMS value of a state variable to accurately determine power loss. Unfortunately, due to its nonlinearity, the RMS value cannot be formulated as a closed-form matrix expression, and must instead be approximated using Riemann sums. Nonetheless, determining the instantaneous and time-averaged values are arguably more appropriate since they are typically what the controller "sees" and reacts upon, not the RMS value.

Case Study: If the target average output voltage is $V_{\text{out}}^{\odot} = 1.0\,\text{V}$, what is the corresponding main-switches' duty-ratio, $D_1 = D_2 = D$, given that the switching frequency is 500 kHz and the conversion efficiency is 100%?

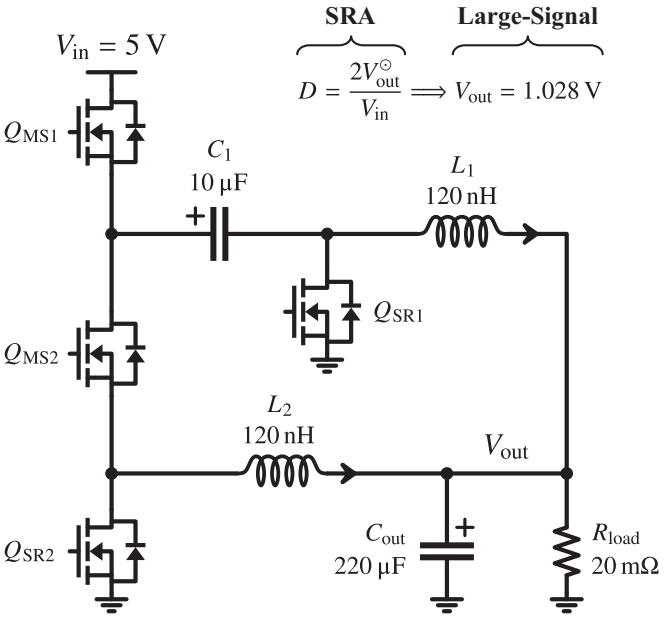


FIGURE 20. A simple case study to demonstrate the inaccuracy of SRA where the task is to determine what the actual main-switch duty-ratio is for a lossless 2-inductor SCB to achieve a desired average output voltage.

both large capacitor-voltage-ripple and large inductor-current-ripple coexist). Consequently, it should not come as a surprise that the SRA-based switching-state durations are inaccurate.

To determine the true switching-state durations that result in the desired large-signal average output, an iterative numerical procedure must be performed until the iteratively-calculated durations result in (49) falling within some predetermined normalized tolerance, ζ, of the targetted output. If the output in question is the load voltage, then the targetted average output is denoted as $V_{\text{out}}^{\odot}$, like in Fig. 20. We can define the error function as

$$\varepsilon_n = \overline{\mathbf{Y}}_n^{(i)} - V_{\text{out}}^{\odot}. \tag{50}$$

The subscript, $n \in \{0,\ 1,\ 2,\ \ldots\}$, denotes the iteration-count, and the superscript, (i), denotes the index of the column vector's entry that corresponds to the output quantity of interest. The initial condition is denoted by $n = 0$, with $\overline{\mathbf{Y}}_0$ being the large-signal average-output calculated using the state-durations estimated by SRA dc averaging. Although we would like to reduce the error to ideally zero, it is, unfortunately, impractical. Instead, we shall aim to minimize the error according to

$$\left|\frac{\varepsilon_n}{V_{\text{out}}^{\odot}}\right| < \zeta. \tag{51}$$

To achieve a good trade-off between computation time and final accuracy, it is advised that ζ be no greater than 0.01%.

Since the average value is independent of where t_1 is defined within the global switching period, it is convenient to strategically place it at one of the switching edges, as this reduces the number of time-intervals by one. For example, landing t_1 on a switching edge of Fig. 19 corresponds to the number of time intervals within the analysis window being $M = 4$. On the other hand, if t_1 was situated between switching edges, as is done in Fig. 19, the number of time intervals would be $M = 5$. Accordingly, we shall set $t_1 = 0$ to facilitate subsequent calculations.

For our example 2-inductor SCB, we can define the nth-iteration's set of chronologically-ordered time-intervals (spanning T_{sg}) as

$$\mathcal{T}(\tau_n) \equiv \mathcal{T}_n = \{T_1 + \tau_n,\ T_2 - \tau_n,\ T_3 + \tau_n,\ T_4 - \tau_n\}. \tag{52}$$

τ_n is the nth-iteration's extension to each main-switch's ON-time (assuming that the output voltage is regulated under constant switching frequency). By definition of the initial condition, $\tau_0 = 0$. Therefore, $\mathcal{T}_0 = \{T_1,\ T_2,\ T_3,\ T_4\}$ is just the set of switching-state durations estimated by SRA dc averaging. For the lossless SCB of Fig. 20,

$$\mathcal{T}_0 = \left\{D_1 T_s,\ \left(\frac{1}{2} - D_1\right) T_s,\ D_2 T_s,\ \left(\frac{1}{2} - D_2\right) T_s\right\}, \tag{53}$$

where $D_1 = D_2 = D$. We can use the following Newton's method to successively refine each switching state's duration:

$$\tau_{n+1} = \tau_n - \varepsilon_n \Bigg/ \left(\frac{\partial \overline{\mathbf{Y}}_n^{(i)}}{\partial \tau}\right), \tag{54}$$

where the derivative is evaluated at $\mathcal{T}_n$. Although it is possible to derive the closed-form expression of the first derivative in (54), it is far easier, and less computationally-expensive, to simply approximate it using a finite-difference method. As an example, the central-difference method is given by

$$\frac{\partial \overline{\mathbf{Y}}_n^{(i)}}{\partial \tau} \approx \frac{\overline{\mathbf{Y}}^{(i)}\left[\mathcal{T}\left(\tau_n + \frac{h_n}{2}\right)\right] - \overline{\mathbf{Y}}^{(i)}\left[\mathcal{T}\left(\tau_n - \frac{h_n}{2}\right)\right]}{h_n}, \tag{55}$$

where $h_n < |\tau_n - \tau_{n-1}|$ should be very small for convergence.

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