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# Modular Fault Tolerant DC/DC Transformer Enabled by Natural Power Sharing

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**ABSTRACT** The use of a DC/DC Transformer (DCX), composed of low-power individual modules with automatic voltage and power sharing will be presented as a possible solution to increase the input voltage and output power ranges of DCX systems. The input voltage range will be increased through just Input Series – Output Parallel (ISOP) connection and the increased power handling capability will be achieved by Input Parallel – Output Parallel (IPOP) connection. With these modules, it is possible to achieve natural power and voltage sharing using only a common synchronization signal between modules. Thanks to this natural equalization, ISOP and IPOP concepts are extended to form a DCX with a matrix structure which will be tolerant to the loss of one module without compromising the power handling capabilities. The proposed topology is analyzed in detail, including the mechanisms that can affect the distribution of voltages and currents. A reliability analysis and the response of the modular system under a failure situation have also been included. The validation of this proposal has been carried out using a modular prototype for an input voltage and an output voltage of 56 V and 28 V respectively, for a rated power of 200 W, and for a switching frequency of 365 kHz.

**INDEX TERMS** Fault tolerance, ISOP, IPOP, voltage adapter, DC transformer, electronic transformer, resonant converter.

## I. INTRODUCTION

The unregulated fixed ratio DC/DC converters, also known as DC/DC Transformers (DCXs) have gained popularity in recent years. They provide a convenient and efficient way to have an isolated and load independent voltage that can be used in many configurations, as shown in Fig. 1 [1]. In fields where a significant voltage scaling is needed, they can operate alongside other converters, which will perform the regulation with a much-reduced voltage transformation. DCXs can serve as a first stage in a two-stage approach (Fig. 1(a)) [2], with the rear side converter performing the regulation task. Thus, being used in a post-regulation scheme. The opposite, pre-regulation, can be also achieved, with the front-end converter performing the regulation (Fig. 1(b)) [3], and ever introducing AC/DC conversion (Fig. 1(c)) [4]. Also, they can be used in a partial power processing scheme (Fig. 1(d)) [5], in which the converter that performs the regulation only processes part of the power achieving an overall high efficiency. Furthermore, they can also work alone in situations in which voltage regulation is not needed. The usage of DCXs, which usually are smaller and more efficient than regulated DC/DC converters, offers new degrees of freedom that can be used for system optimization [6]. The range of applications in which DCXs are used spans EV applications [7], [8], [9], datacenter power distribution [10], photovoltaic inverters [11], solid state transformers [12], [13], and aerospace [14] under the novel "New Space" paradigm [15] among others.

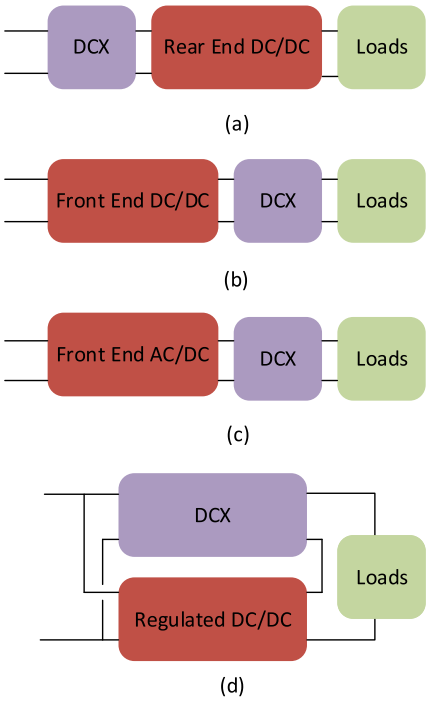



**FIGURE 1.** **Overview of DCX use as (a) first stage; (b) second stage; (c) second stage in an AC/DC scheme, (d) partial power processing unit.**

Besides, modular power conversion systems are also interesting for a variety of reasons. The limited availability of devices that can withstand high voltage or high current, introducing redundancy for increasing reliability, the availability of off-the-shelf building blocks to reduce design times, increment of the surface to improve the dissipation capability, etc. This type of designs have been widely used in high-power converters (traction, distribution networks) [16], [17], [18], where the use of complex control systems to ensure the equal distribution of currents and voltages among the modules does not penalize the design, at least in terms of cost. In fact, it is a common and trending approach nowadays. Many of the features offered by modular high-power systems could be useful at lower power levels. However, in low power systems, the increase in the number of sensors and control loops to achieve an even distribution of voltage and power is a drawback from the point of view of cost, size, and design time. Nevertheless, there are many critical loads whose consumption is in the kilowatt range (medical equipment, spacecrafts, communications) that can take advantage of the reliability provided by the redundancy of a low-power modular system. Moreover, the use of standardized modules that can be combined to achieve the desired requirements would reduce the cost and design times of power systems for such applications [19], [20]. However, a low-power modular solution will be interesting only if the modularity does not complicate the control system or increase the cost of the final solution.

Again, the interconnection of several smaller converters in series and/or parallel to achieve different transformation ratios and power scalability is not new [20], [21], [22]. In [21], a structure of several 1:1-DCX blocks is proposed using the Input Parallel Output Parallel (IPOP) and Input Series Output Parallel (ISOP) connections to increase the overall power and voltage of the system. The topology used in [21] needs to be bidirectional, thus more complex, to facilitate its association [23], whereas the topology presented in this work is unidirectional but simpler.

This paper shows a modular system that works as a unidirectional modular DC/DC transformer. It will be composed of individual DCX modules and a common output filter. The latter is only necessary to remove the unwanted output voltage ripple. Given their design, the DCX modules only require a simple common synchronization signal for reaching an accurate voltage and power sharing. This way of achieving voltage distribution in the ISOP connection and current distribution in the IPOP connection allows the construction of the DCX in a very simple way.

Fault tolerant DCX would be needed to bring the benefits of its usage in power architecture such as the ones represented in Fig. 1. Moreover, reliability must consider faults in the control too. Therefore, the usage of simplified controls with natural power sharing techniques like the one presented in this work would ease the protection implementation against failures. The proposed DCX has fault tolerance capabilities which assures that it could be used in high reliability environments such as space applications.

The concept of unregulated fixed ratio DC/DC converters for having a fixed voltage scaling is very common and receives many names [1], [2], [3], [5], such as Electronic Transformer (ET), Electronic-Embedded Transformer (EET) or DC/DC Transformer (DCX), being the last one the most common. These terms could be easily interchangeable. For easing the reader's task, throughout the paper the following nomenclature will be used. The final product, the DC/DC transformer composed of individual modules connected in series and parallel will be called DCX. The individual smaller power DCXs which constitute the final product will be called modules.

Most isolated DC/DC converters can be adapted for its usage as modules for a DCX [24], [25], [26], [27], [28], [29], [30], [31]. The LLC resonant converter [24] working at its resonant frequency is one of the most widely used unidirectional topologies for DCX construction [25]. However, its IPOP association is not easy [26], especially when no information is shared between the different power modules, as proposed in this paper. Modifications to the LLC topology are presented in [27] to achieve current and voltage sharing by sharing trigger signals. In [28], the authors propose adding coupled inductors between each two stages to force current sharing. Nonetheless, this solution increases the number of magnetic components. In [29], the coupled inductors of [28] work as resonant inductors, reducing the required number of components but adding design complexity. Finally, in [30] the coupling of all the resonant inductors is presented, which leads to a magnetic design that could be complicated with a high number of stages. In [25] the transformer is shared, making the final implementation not totally modular. Additionally,

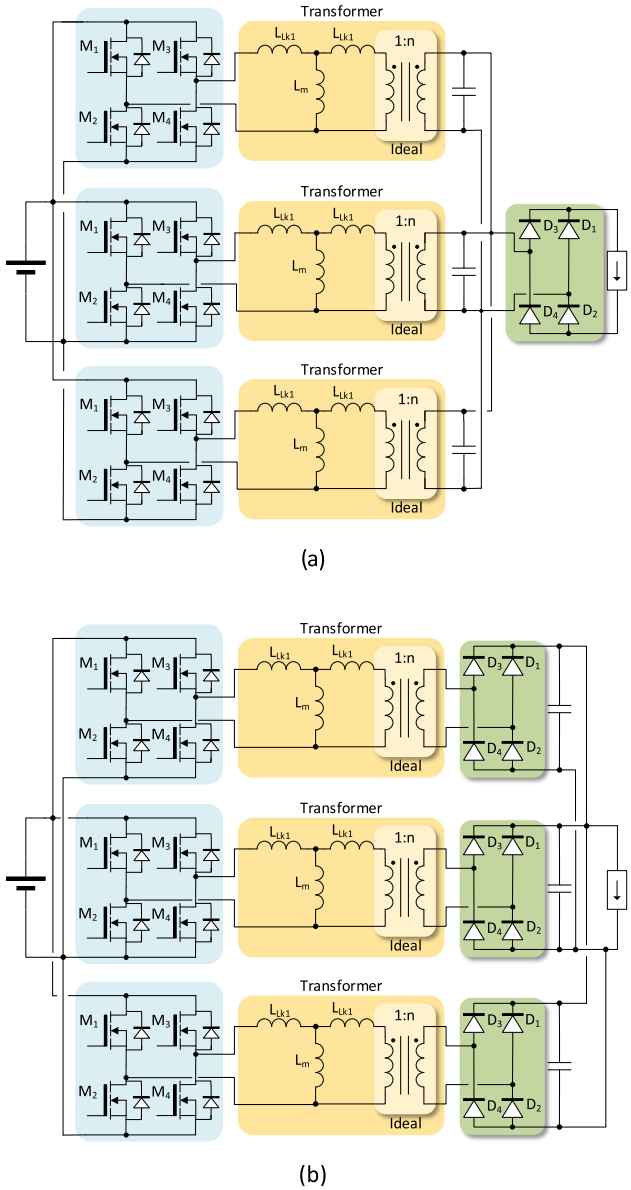



**FIGURE 2. (a) Partially-modular converter based on PRC with the output capacitor being the resonant capacitor and (b) modification to reach full modularity by placing the output/resonant capacitor after the rectifier of each module. (Only IPOP configuration represented).**

from these papers it can be derived that when elements of the resonant tank are shared, the distribution of loads among converters is better.

It can be concluded that for IPOP and ISOP connections, the easiest element to share would be a capacitor, which leads the authors to look for a resonant topology with an easily associable capacitor when the outputs are parallel connected. One possibility would be using a parallel resonant converter (PRC) connected as shown in Fig. 2(a), being the output capacitor the resonant capacitor as well. However, this solution is not fully modular since it has one rectifier shared by all the converters. For the sake of clarity, the modules in this figure have been represented in IPOP configuration only, but the explanation is valid for the ISOP configuration as well.

As shown in Fig. 2(b), by placing the PRC resonant capacitor after the rectifier of each converter (i.e., module), a fully modular DCX is achieved. It is worth to mention that the $L_m$ and the $L_{Lk}$ values in Fig. 2 are generic values for the magnetizing and leakage inductances of the transformers. While the rectifier diodes are on, all the resonant tanks share one resonant element, as all the capacitors are parallel connected. In this way, they keep their resonant behavior while the load sharing among the modules is enhanced, as will be seen later. It is worth noting that since the output capacitor is also the resonant capacitor the load will affect the resonant process, especially if the load is a DC/DC converter with an input capacitor. Independence of the resonant process could be achieved if the load behaves as a current source, as shown in Fig. 2. This current source behavior can be achieved also by placing a single inductive filter between the output of the full DCX composed by individual modules and the load. This filter could be the EMI input filter of any potential following stage.

The proposed module topology is not new since it was proposed in [32]. However, to the author's best knowledge, its IPOP and ISOP connection and the corresponding detailed analysis has not been published. To this respect, it is important to highlight that preliminary results of this research were presented in [14]. Nonetheless, the technical and mathematical analysis included in that paper was superficial. On the other hand, this paper addresses precisely the usage of the converter proposed in [32] in ISOP and IPOP configurations to form the proposed modular DCX. Furthermore, the role of component tolerance and other mismatching effects have been studied to assess its effects in the power sharing capabilities without a dedicated complex control. It will be proved that the proposed architecture presents good power sharing.

This paper is organized as follows. Section II presents a review of the topology selected for implementing the modules. In Section III, a description of the DCX concept based on the interconnection of individual DCXs modules is given. Also, the requirements imposed to these modules will be explained as a way of assessing the advantages and disadvantages of the selected topology. Section IV describes the modular operation of the DCX. Section V presents the experimental results regarding the individual modules and the full DCX. Finally, in Section VI the conclusions are shown.

## II. REVIEW OF THE CONVERTER TOPOLOGY PRESENTED IN [32]

Fig. 3 shows the proposed module, derived from Fig. 2, and its most important waveforms. The topology is already presented in [32], being a derivation from the PRC. A full review will be made here to ease the task of the reader. Furthermore, this analysis will serve as a basis to fully analyze the modular operation. The topology consists in a full bridge operating with fixed duty cycle and fixed switching frequency ($f_{sw}$). This full bridge works as a DC/AC (inverter) stage, driving the magnetic transformer. In the secondary side, a center-tap rectifier connects the transformer with the output filter. For

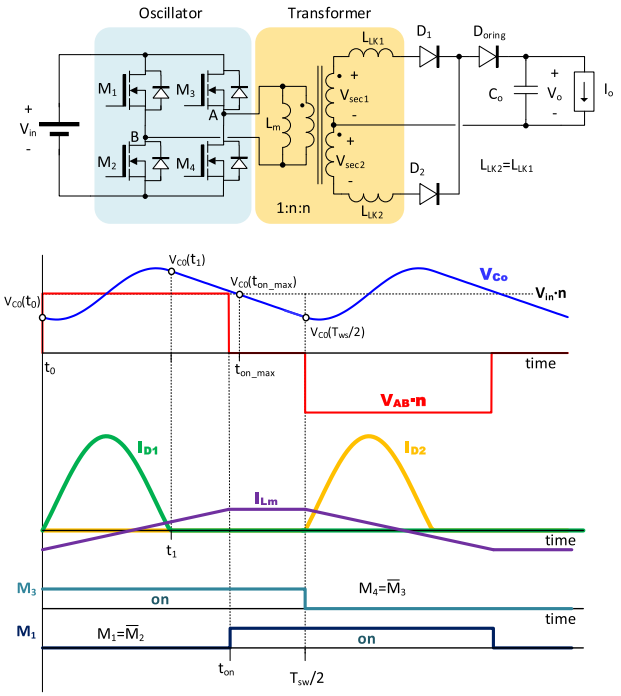



**FIGURE 3.** (Top) schematic of the electronic transformer module; (bottom) main waveforms in steady state.

protection purposes, an "OR-ing" diode is added to the rectifier, but it is not required for the operation of the topology. Together with turning off all the MOSFET control signals, a failed module can be isolated. In this context a failed module is one in which a single component has become either an open or a short circuit. A detailed explanation is shown in Section IV-E. The DC/AC stage is a full bridge for two reasons: First, as said, the module can be isolated even when one of the MOSFETs is the component under a short-circuit failure. Secondly, as it will be seen later, applying zero volts to the primary side of the magnetic transformer (i.e., short-circuiting the magnetic transformer) is necessary to achieve ZCS (Zero Current Switch) in the rectifier diodes under certain operating conditions. This is also a new analysis performed in this paper.

For the sake of clarity, some simplifications, aligned with previous explanations and considering the intended application, are made in this analysis. The schematic is depicted in Fig. 3. As will be seen in Section II-A, to reduce the ripple in the resonant capacitor ($C_o$), which is also the output capacitor, the leakage inductance of the transformer, which is also the resonant inductor, must be very small. With a small leakage inductance, the L equivalent of the transformer can be used [33]. The resonance takes place between the output capacitor $C_o$ and the corresponding leakage inductance ($L_{LK1}$ and $L_{LK2}$) for each semi-period. Therefore, it can be assumed that the magnetizing inductance is directly connected to the bridge as in in Fig. 3. In that way, the magnetizing inductance does not play any role in the resonant tank. This is a relevant advantage over the LLC resonant converter [25], often used for the same application. As the transformer magnetizing inductance is not a resonant element, the design constraints of the transformer are alleviated and eases the integration of the resonant inductance and the transformer in a single core. The magnetizing inductance is only tied to the condition of reaching ZVS (Zero Voltage Switching) under any load condition, so its value can be wisely adjusted.

In [32] the operation of the converter is analyzed when the resonant frequency ($f_r$) is twice the switching frequency ($f_{sw}$), achieving this way the highest efficiency of the converter. However, modular operation and the component tolerances may make the resonant frequency to be slightly different from twice the switching frequency. Thus, a new analysis of the topology becomes necessary. This analysis will serve as the basis for assessing on the effects of different resonant component values and the modular operation, explained in Section IV.

### A. DETAILED TEMPORAL ANALYSIS

The operation of the topology will be addressed in this section for each of the different states, according to the main waveforms shown in Fig. 3.

#### 1) TIME INTERVAL ($T_0$-$T_1$)

Switches $M_3$, $M_2$, and diodes $D_1$ and $D_{oring}$ are on. This connects the transformer to the $V_{in}$ voltage, exciting the resonant circuit formed by $L_{LK1}$ and $C_o$ with a voltage $V_{in} \cdot n$, where n is the turn ratio of the transformer. It will be assumed that the leakage inductances have the same value, so $L_{LK1} = L_{LK2} = L_{lk}$, The inductor current and the output voltage can be calculated as:

$$i_{lk1}(t) = \frac{V_{in} \cdot n - V_o(t_0)}{Zc} \sin(\omega t) + I_o \cdot (1 - \cos(\omega t)) \quad (1)$$

$$V_o(t) = V_{in} \cdot n - I_o \cdot Zc \cdot \sin(\omega t) - (V_{in} \cdot n - V_o(t_0)) \cdot \cos(\omega t) \quad (2)$$

The characteristic impedance, the conduction angle of the diode and the resonance frequency are:

$$Zc = \sqrt{\frac{L_{lk}}{C_o}} \quad \theta = \omega \cdot t_1 \omega = \sqrt{\frac{1}{C_o \cdot L_{lk}}} = 2\pi \cdot f_r \quad (3)$$

The conduction angle of the diode $\theta$ is included for simplifying the mathematical expressions but given that there is not a fixed ratio between the conduction time and the resonant period, it is not advisable for representing Fig. 3 axis. The interval ends at $t_1$, when the current in the inductor reaches zero. Using this condition in (1), (4) is obtained:

$$\frac{V_{in} \cdot n - V_o(t_o)}{Zc \cdot I_o} = \frac{\cos(\theta) - 1}{\sin(\theta)} = \sqrt{A} \quad (4)$$

where the parameter A is defined to represent the trigonometric functions shown in (5):

$$\cos(\theta) = \frac{1 - A}{1 + A} \quad \sin(\theta) = \frac{-2\sqrt{A}}{1 + A} \quad (5)$$

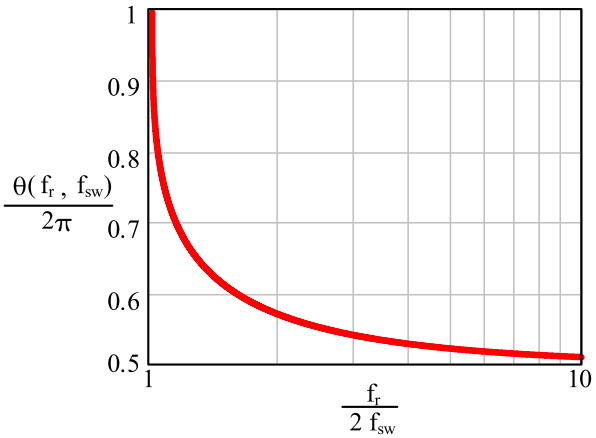



**FIGURE 4.** Normalized conduction angle $\theta/(2\pi)$, as a function of the ratio between half the resonance frequency ($f_r/2$) and the switching frequency ($f_{sw}$).

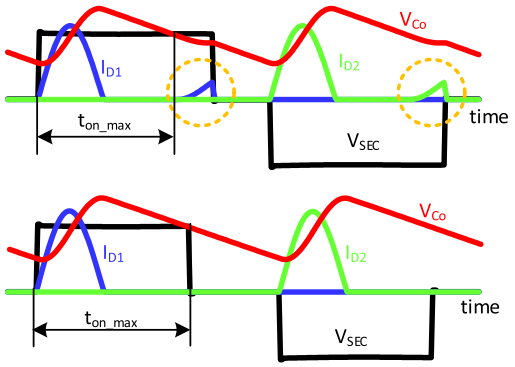



**FIGURE 5.** Resonant current behavior (blue and green traces) once the resonance has finished. (Top) when the capacitor voltage (red trace) may be lower than the voltage at the secondary side of the transformer (black trace): $t_{on} > t_{on\_max}$; (bottom) when the output voltage is never lower than the transformer voltage: $t_{on} \leq t_{on\_max}$.

Substituting $t_1$ and using the trigonometric functions as a function of A in (1), (6) is obtained:

$$\frac{V_o(t_1) + V_o(t_o)}{2} = V_{\text{in}} \cdot n \tag{6}$$

which allows a simple relationship between the most important voltage values in the circuit.

In steady state, the output capacitor averaged current must be zero, so the averaged rectifier output current must be the output current $I_o$.

$$\overline{I_{D1} + I_{D2}} = \frac{2}{T_{\text{sw}}} \int_0^{t1} i_{lk1}\ (t)\, dt = I_o \tag{7}$$

Solving (7) and simplifying using $V_o(t_1)$ :

$$V_o(t_1) - V_o(t_o) = I_o \cdot \text{Zc} \cdot \left( \frac{T sw}{2} \cdot \omega - \theta \right) \tag{8}$$

From (8), it can be derived that the output voltage ripple is proportional to $I_o$ and $Z_c$. This encourages the usage of transformers with low leakage inductance because for the same resonance frequency, the capacitor voltage ripple will be lower.

From (4), (6) and (8):

$$\frac{f_r}{2f_{\text{sw}}} = \frac{\cos(\theta) - 1}{\sin(\theta) \cdot \pi} + \frac{\theta}{2\pi} \tag{9}$$

This equation shows that the conduction angle ($\theta$) only depends on the ratio between resonance frequency and the switching frequency. For this reason, equations will be expressed in terms of $\theta$ whenever possible.

As Fig. 4 shows, when resonance frequency is two times the switching frequency, diodes are conducting during the entire resonance period (i.e., half the switching period, leading to maximum efficiency). As the switching frequency decreases, the conduction time approaches half the resonance period. These results are in agreement with [32].

### 2) TIME INTERVAL ($T_1$-$T_{ON}$)

During this interval, $D_1$ and $D_{\text{oring}}$ are off and remain reverse biased until the capacitor voltage ($V_{Co}$) becomes lower than $V_{\text{sec1}} = (V_{\text{in}} \cdot n)$. This instant has been labelled as $t_{\text{on\_max}}$. As Fig. 5(top) shows, where the voltage in the secondary side of the transformer, the current through both diodes and the resonant capacitor voltage are represented, when $t_{\text{on}}$ is longer than $t_{\text{on\_max}}$, $D_1$ and $D_{\text{oring}}$ become forwardly biased, and the resonance between $L_{LK1}$ and $C_o$ starts again. This must be avoided as it prevents the diodes from reaching ZCS and increases switching losses. This situation could be solved by short-circuiting the transformer through the input full-bridge which will take place between $t_{\text{on}}$ and $T_{\text{sw}}/2$ as indicated in Fig. 3. For this reason, only the desired case with ZCS, represented in Fig. 5(bottom), will be studied in this analysis. In this time interval, all the load current is provided by the capacitor, which is discharged according to (10):

$$V_o(t) = V_o(t_1) - \frac{I_o}{C_o} \cdot (t - t_1) \tag{10}$$

### 3) TIME INTERVAL ($T_{ON}$-$T_{SW}/2$)

As mentioned, this analysis is valid in the case that the diodes are reversed bias until $T_{\text{sw}}/2$. That is, the current through $D_1$ and $D_{\text{oring}}$ is zero when the bridge voltage is reversed at $T_{\text{sw}}/2$. As explained, this current will be zero if no new resonance starts (Fig. 5(bottom)). This could be achieved by short-circuiting the transformer by commanding switches $M_1$ and $M_3$ to be turned on between $t_{\text{on}}$ and $T_{\text{sw}}/2$, as indicated in Fig. 3. Then, the input voltage to the resonant tank is 0. This strongly alleviates the condition to avoid restarting the resonance because to forward bias $D_1$ and $D_{\text{oring}}$, the capacitor voltage must fall below zero volts.

By short-circuiting the transformer, the switching frequency of the converter becomes decoupled from the resonant frequency. This takes care of changes in the resonant frequency due to component variation and ageing, as will be discussed Section IV-D. Furthermore, $t_{\text{on}}$ determination is also

eased since it is only needed to select a fixed $t_{on} \leq t_{on\_max}$(see Fig. 3). Determination of $t_{on\_max}$ is addressed though resonant element variation in Section IV-D.

During this time, current through the magnetizing inductance is kept constant, as shown in Fig. 4 and the capacitor voltage is still represented by (10).

In steady state, the capacitor voltage at $T_{sw}/2$ must be equal to the voltage at $t_0$. Once the equation for output voltage is defined in all the intervals, its average value is obtained:

$$\overline{V_o} = \frac{2}{T_{sw}} \int_0^{\frac{T_{sw}}{2}} V_o(t)\, dt = V_{in} \cdot n \tag{11}$$

It must be highlighted that load and $t_{on}$ values have no effect on the capacitor average voltage as long as $t_{on}$ is greater than $t_1$ and shorter than $t_{on\_max}$. This behavior simplifies the ISOP association and ensures an equal distribution of input voltages.

#### 4) TIME INTERVAL ($T_{sw}/2$- $T_{sw}$)

As the current through $D_1$ and $D_{oring}$ is held to 0 thanks to short-circuiting the transformer this interval is first governed by the same resonant process as the one in between $t_0$ and $t_1$. But with a voltage in the secondary $V_{SEC} = -V_{in} \cdot n$. This is enabled by having switches $M_1$ and $M_4$ on, and thus, $D_2$and $D_{oring}$ will be on too. As before, the inductor current can be calculated by (1) with output voltage by (2). After the current becomes 0 the diodes $D_2$and $D_{oring}$ become reverse biased and the capacitor $C_o$ discharges following (11). Again, having the transformer short-circuited once $t_{on} \leq t_{on\_max}$ has elapsed enables the process to start again with zero current though the diodes at $T_{sw}$ when switches $M_3$, $M_2$ are turned on.

## III. DESCRIPTION OF THE MODULAR DCX CONCEPT

The key issue of this work is the use of a topology that under minimum control and design requirements achieves a good voltage and current equalization between modules and allows an easy (i.e., modular) input and output voltage adaptation. In this case, the voltage adaptation provided by the DCX is achieved by serially connecting several standard modules at their inputs (see Fig. 6) while keeping all their outputs in parallel, as well as by wisely choosing a static gain ($G_v$) value, common to all of them [20]. This last issue is granted by the topology chosen for implementing the modules and introduced in Section II, in which the static gain $G_v$ is equal to the turns ratio, $n$, of its magnetic transformer.

The common static gain and common output voltage assure that the input voltages of all the modules are equal, as shown in (12) [14]:

$$\begin{aligned} V_{in\_i} &= V_o/G_v = V_{in\_j} \\ V_o &= V_{in\_i} \cdot G_v = V_{in\_T}/(m_s) \cdot G_v = V_{in\_T} \cdot G_{vDCX} \end{aligned} \tag{12}$$

where $V_o$ and $V_{in\_i}$ (and $V_{in\_j}$) are the average output voltage and input voltage of each module, and $V_{in\_T}$ is the total input voltage. $V_o$ is common to all the modules and, consequently, is the output voltage of the DCX, while $V_{in\_T}$ is its input voltage.

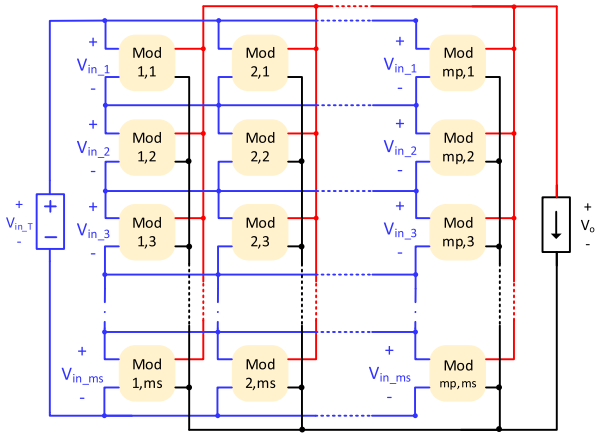



**FIGURE 6. Schematic of the proposed voltage adaption through modular connection of standard fixed-gain modules.**

As the overall input voltage ($V_{in\_T}$) is fixed, then the input voltage of each module ($V_{in\_i}$) is fixed too and will be equal to $V_{in\_T}/(m_s)$. Thus, in serially connected modules a perfect sharing of the input voltage is achieved. As can be deduced from (12), the number of modules in series ($m_s$) along with the individual common static gain ($G_v$), allows to adapt the overall gain of the system $G_{v\_DCX}$ (i.e., the DCX) and the final value of the output voltage (12).

The voltage scaling is achieved by selecting the number of modules in series $m_s$ and $G_v$. From the analogy to the solar arrays, a set of $m_s$ modules with its input in series and its output in parallel will be called a string. The strings can be parallelized $m_p$ times to reach power scalability (see Fig. 6). Each of the individual modules is labelled as Modi, j. Where $j \in [1, m_s]$ represents the position of the module in a string and $i \in [1, m_p]$ represents the string in which the module is present. Please note that there is a connection between the correspondent modules of each string. In other words, modules with the same i will have their inputs connected in parallel. This is done for reliability reasons and will be explained in Section IV-E.

The chosen number of serialized modules results in a coarse adaptation of the voltage, given that only an integer number of modules can be used. Therefore, for this proposal to be feasible, the module topology must be able to provide fine off-line (i.e., during assembly stage) voltage adaptation by adjusting the constant gain $G_v$, but without forcing the redesign of the whole converter (semiconductor devices, layout, etc.). This can be easily done with a limited set of predesigned magnetic transformers. Also, as described, all the modules need to have the same static gain, which means that it cannot be affected by tolerances in components or driving signals. This topic will be addressed in Section IV.

## IV. MODULAR OPERATION ANALYSIS UNDER REAL CONDITIONS

Using the presented module topology, when the modules are arranged under IPOP and ISOP connections with just a common simple synchronization signal (i.e., when there are no

dedicated control loops for load or voltage sharing), three factors can affect current or voltage sharing, namely, differences in inductor value, input voltage differences, and synchronization errors. In this section, these factors are analyzed in depth together with reliability and the effect of tolerances and aging on components. In this analysis the effect of $D_{\text{oring}}$ is negligible. Moreover, it should be considered that both the ISOP and IPOP connections leads to all the resonant capacitors (output capacitors) to be always connected in parallel [14].

### A. MODULE INPUT CURRENT DIFFERENCE DUE TO RESONANT COMPONENT VARIATION

To achieve a correct modular operation, there must be load sharing among modules, thus all the modules must process the same power [24]. In this analysis, it is assumed that there are two modules with leakage inductors and output capacitors (i.e., resonant inductors and resonant capacitors) whose values are not equal due to tolerances. Also, it is important to remind that all modules share a synchronization signal that allows the bridge legs switching at $t_0$ and $T_{\text{sw}}/2$ to take place at the same time in all the modules. As explained in Section III, all the modules have the same input voltage since its outputs are connected in parallel. This input voltage is then translated to the secondary of the transformers which have an equal turn ratio of n. This generates voltages $\text{V}_{\text{sec\_1}}(\text{t})$ for the first module and $\text{V}_{\text{sec\_2}}(t)$ for the second one, as depicted in Fig. 7(a). Thus $V_{\text{sec\_1}}(t) = V_{\text{sec\_2}}(t) = V_{\text{sec}}(t)$. This assumption is easy to fulfill given that this voltage only depends on the turn ratio of the transformer, which is a parameter easy to replicate without differences and very robust against tolerances, aging, and other sources of value drifts. Also, since the outputs are connected in parallel, there is a common output voltage.

While the diodes are conducting, one of the terminals of the inductors is connected to the capacitors in parallel $C_{eq} = C_1 + C_2$. Then the circuit evolves according to (13):

$$\begin{cases} V_{\text{in}} \cdot n = L_{LK1} \frac{di_{L1}(t)}{dt} + v_o(t) \\ V_{\text{in}} \cdot n = L_{LK2} \frac{di_{L2}(t)}{dt} + v_o(t) \\ i_{L2}(t) + i_{L1}(t) = C_{eq} \frac{dv_o(t)}{dt} + I_o \end{cases} \tag{13}$$

which forces the currents to evolve according to (14):

$$\frac{L_{LK1}}{L_{LK2}} = \frac{i_{L2}(t)}{i_{L1}(t)} \tag{14}$$

Since the currents ratio is constant, both currents cross zero at the same time. An alternative explanation would be that, as the switches are synchronized, voltages $V_{\text{sec\_1}}(t)$ and $V_{\text{sec\_2}}(t)$ in Fig. 7(a) are equal in amplitude and phase ($V_{\text{sec\_1}}(t) = V_{\text{sec\_2}}(t) = V_{sec}(t)$). Therefore, the positive terminal of the voltage sources can be connected in parallel. When the diodes are on, time interval between $t_0$ and $t_1$, the load-side terminals of inductors $L_{LK1}$ and $L_{LK2}$ are also connected, so the inductors can be also considered in parallel.

This approach can be generalized for a number $m_t$ of modules. It should be noted that the number of modules with

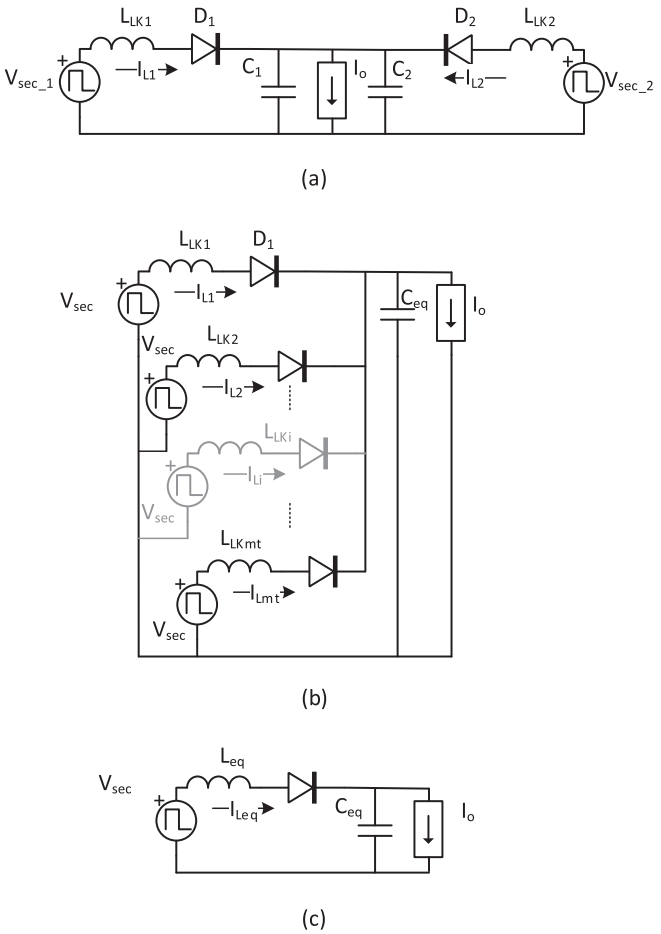



**FIGURE 7. (a) Simplified resonant circuit of two IPOP or ISOP modules; (b) simplified resonant circuit of $\mathbf{m_t}$ modules in ISOP or IPOP; (c) equivalent resonant circuit of $\boldsymbol{m_t}$ modules.**

inputs in series is $\text{m}_\text{s}$ and the number of strings is $\text{m}_\text{p}$, but all of them have the outputs in parallel as explained in Section III. Therefore $m_t = m_p \cdot m_s$. Given that all the voltage sources are the same, they can be connected in parallel giving $V_{sec}$. As Fig. 7(b) and (c) show, the equivalent capacitor ($C_{eq} = \sum_{i=1}^{m_t} C_i$) is the parallel of all capacitors and the equivalent inductor ($L_{eq} = \sum_{i=1}^{m_t} 1/L_{LKi}$) is the parallel combination of all resonant inductors (leakage inductances of the transformers). It is important to note that capacitors do not affect current sharing, since all converters see the same $C_{eq}$. Hence, as a relevant advantage of this proposal, the current mismatch would be due to variations induced by the tolerance and the aging in the inductors, but not in the capacitors. Whilst the current mismatch will not be affected by $C_{eq}$ the equivalent resonant pulsation $\omega$ will be determined by $C_{eq}$ and $L_{eq}$ and thus will be susceptible to tolerance and aging. This is further explained in Section IV-D.

The value of $i_{Leq}(t)$ in Fig. 7(c) is obtained by replacing in (1) the values of characteristic impedance and resonant frequency with those resulting from $L_{eq}$and $C_{eq}$. The current flowing through each inductor is calculated considering the

current divider that it forms with the rest of the parallel-connected inductors (15):

$$i_{LK_i}(t) = i_{Leq}(t) \cdot \frac{\left[\left(\sum_{j=1}^{j=m_t} \frac{1}{L_{LK_j}}\right) - \frac{1}{L_{LK_i}}\right]^{-1}}{\left[\left(\sum_{j=1}^{j=m_t} \frac{1}{L_{LK_j}}\right) - \frac{1}{L_{LK_i}}\right]^{-1} + L_{LK_i}} \quad (15)$$

The converter with the lowest impedance carries the highest current. So, in a modular converter with $m_t$ modules in parallel the worst-case current imbalance occurs when $m_t - 1$ modules have the maximum impedance, and only one has the minimum impedance. Following Fig. 7(a), all the modules with maximum impedance could be grouped into a single equivalent one, which will be represented by source $V_{in} \cdot n$ and inductor $L_{LK1}$. The one with the lowest impedance will be represented by the inductor $L_{LK2}$ and the other source of value $V_{in} \cdot n$. Assuming an inductor value tolerance of $\pm d_{rL}$, the worst-case current imbalance will appear when the equivalent inductance $L_{LK1}$ is the parallel of $m_t - 1$ inductors of maximum value:

$$L_{LK1} = \frac{L_{nom} \cdot (1 + d_{rL})}{m_t - 1} \quad (16)$$

while the other branch is the inductor $L_{LK2}$ of minimum value:

$$L_{LK2} = L_{nom} \cdot (1 - d_{rL}) \quad (17)$$

The current in each inductor will be:

$$i_{LK1} = \frac{I_o \cdot L_{LK2}}{L_1 + L_{LK2}} = \frac{I_o \cdot (1 - d_{rL}) \cdot (m_t - 1)}{(1 + d_{rL}) + (1 - d_{rL}) \cdot (m_t - 1)} \quad (18)$$

$$i_{LK2} = \frac{I_o \cdot L_{LK1}}{L_{LK1} + L_{LK2}} = \frac{I_o \cdot (1 + d_{rL})}{(1 + d_{rL}) + (1 - d_{rL}) \cdot (m_t - 1)} \quad (19)$$

while the maximum current deviation from an ideal current distribution can be expressed as:

$$\Delta i_{\max} = i_{LK2} - \frac{I_o}{m_t} = \\ = I_o \cdot \frac{m_t - 1}{m_t} \cdot \frac{2 \cdot d_{rL}}{2 \cdot d_{rL} + m_t \cdot (1 - d_{rL})} \quad (20)$$

It is important to note that the worst current sharing occurs with only two modules. As the number of modules increases, the current distribution improves. This is a very interesting feature for a modular application. As the number of modules increases, current sharing becomes more tolerant to differences between its components.

### B. MODULE INPUT CURRENT DIFFERENCE DUE TO INPUT VOLTAGE VARIATIONS

In modular operation, all the modules share the same output voltage. Thus, only the transformer secondary voltage differences will affect the current sharing among modules. These input voltage differences may be caused by a poor distribution of voltages in the ISOP connection or by differences in the voltage drop of the semiconductor devices. Not by the transformer turn ratio, which defines the static gain of the modules, as it is a highly replicable and robust parameter against fabrication tolerances.

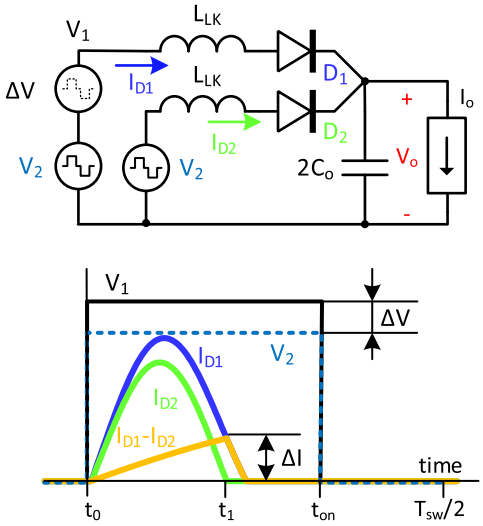



**FIGURE 8.** Currents with voltage differences. (Top) circuit; (bottom) main waveforms.

As shows Fig. 8 (Top), two different secondary voltages feed two identical resonant circuits, thus both circuits have the same inductance value $L_{LK}$. While both diodes $D_1$ and $D_2$ are on, period $(t_0 - t_1)$ in Fig. 3, it can be assumed that the circuit with the higher voltage is supplied by two series-connected voltage sources $V_2$and $\Delta V$. The one with the lowest voltage is solely supplied by a voltage source of value $V_2$. In this circuit, the current through the inductor, and thus diode $D_2$, will be $I_{D2}$. The current through diode $D_1$, $I_{D1}$, could be calculated using the superposition theorem. Then it would be the sum of $I_{D2}$, current due to $V_2$, plus $I_{D1} - I_{D2}$ current due to $\Delta V$. Therefore, the $\Delta I_v$ can be calculated using (21):

$$\Delta I_v = I_{D1} - I_{D2} = \frac{\Delta V}{L_{LK}} t_1 \quad (21)$$

The averaged current difference between the two diodes is calculated approximately as:

$$\overline{\langle \Delta I_v \rangle}_{Tsw/2} = \frac{\Delta V}{L_{LK}} {t_1}^2 \cdot f_s = \frac{\Delta V}{L_{LK}} \left(\frac{\theta}{\omega}\right)^2 f_{sw} \quad (22)$$

where current for times above $t_1$ has not been considered to simplify the expression.

Equation (22) reinforces the validity of the individual DCXs modules for its ISOP association. Since the module with the highest voltage supplies the highest current to the output, its input capacitor is discharged faster, diminishing its input voltage. This facilitates a balanced voltage distribution among modules. Moreover, as the individual input voltages become equalized, the input currents become equalized too, achieving power equalization.

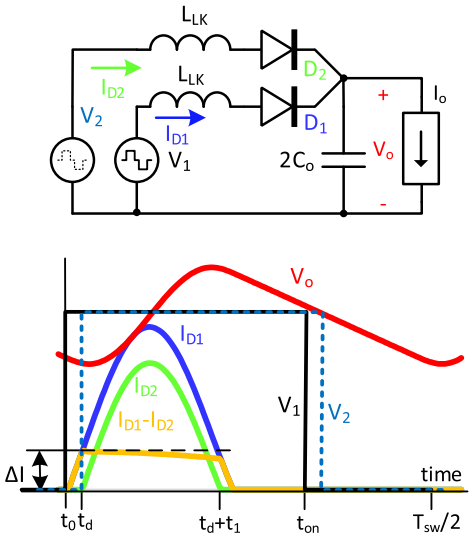



**FIGURE 9.** Currents with synchronization error. (Top) circuit; (bottom) main waveforms.

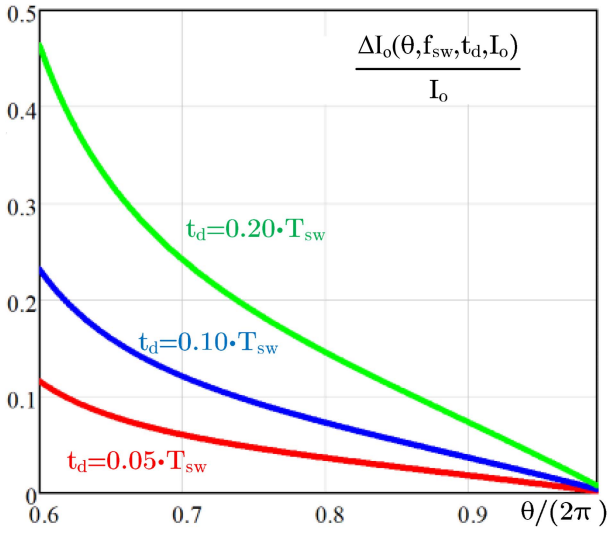



**FIGURE 10.** Normalized current increment for $t_d$=0.05·$T_{sw}$ (red); $t_d$=0.1·$T_{sw}$ (blue); $t_d$=0.2·$T_{sw}$ (green). $I_o$ is the average current of a module with ideal sharing.

### C. MODULE INPUT CURRENT DIFFERENCE DUE TO TIMING VARIATIONS

A synchronization signal is responsible for all the modules to turn-on their transistors in a synchronized way, paramount to analyze the modular operation in the system as explained in this section. In a switching period all the modules switch their bridge legs at the same time, $t_o$, the beginning of each switching period. Then, after $T_{sw}/2$ is elapsed all modules switch again their bridge legs. The cycle repeats itself each $T_{sw}$. While pulse width is not critical (the $t_{on}$ for each bridge leg could be different for each module as long as $t_1 \leq t_{on} \leq t_{on\_max}$ as explained in Section II-A) for current sharing, timing errors in trigger signals are. Differences in the trigger circuits, layout, transistors, etc., cause delays in the trigger signals that affect current sharing. If one module turns switches a leg before others it will draw more current.

Fig. 9 shows the equivalent of two modules with the same passive components. One is supplied by voltage source $V_1$ and the other by $V_2$. Both have the same amplitude but voltage $V_2$ is delayed a time $t_d$ with respect to voltage $V_1$. For the analysis, it is assumed that $t_d$ is much smaller than $t_1$. Hence, $t_1$ can be roughly calculated assuming delay-free operation using (9).

Between $t_0$ and $t_d$, only $D_1$ is on. As $t_0 - t_d \approx 0$, the sine on the sinusoidal evolution of the current can be approximated by the angle ($\sin x \approx x$). Thus, the increment of current can be calculated as:

$$\Delta I_d = \frac{V_{in} \cdot n - V_o(t_0)}{L_{LK}} t_d \tag{23}$$

which using (4) can be expressed as:

$$\Delta I_d = \frac{Zc \cdot I_o}{L_{LK}} \frac{\cos(\theta) - 1}{\sin(\theta)} t_d \tag{24}$$

The inductors become parallel-connected when $D_2$ turns-on at $t_d$. However, one of them already carries an initial current $\Delta I_d$. As $V_1$ and $V_2$ have the same value it can be considered that the evolution of the current in the two inductors is the same, so that $I_{D1} - I_{D2}$ remains practically constant, with $I_{D1} - I_{D2} \approx \Delta I_d$, until $t_d + t_1$. At that instant, $D_2$ turns-off while $D_1$ continues conducting until the excess current is eliminated. In order to obtain an easy-to-use expression, the averaged value of the current difference has been obtained considering only sections where $I_{D1} - I_{D2}$ is constant:

$$\langle \overline{\Delta I_d} \rangle_{\frac{T_{sw}}{2}} \cong \frac{2\Delta I_d \cdot (t_1)}{T_{sw}}; t_1 \gg t_d \tag{25}$$

Using (24), (25) can be expressed as:

$$\langle \overline{\Delta I_d} \rangle_{T_{sw}/2} = 2\theta \frac{\cos(\theta) - 1}{\sin(\theta)} I_o \cdot f_{sw} \cdot t_d \tag{26}$$

Fig. 10 shows how the diode conduction angle ($\theta$) affects the current imbalance. As the conduction angle becomes smaller, the system becomes more sensitive to synchronization error. In real designs, it is advisable to keep $\theta/(2\pi)$ above 0.8.

### D. EFFECTS OF AGING AND TOLERANCE

In Section IV-A, it was demonstrated that the connection of DCX modules in series or in parallel at their input does not affect the resonant behavior of each module as long as a synchronization signal exists, and their outputs are connected in parallel. In this previous analysis, it was considered that $t_1 \leq t_{on} \leq t_{on\_max}$. However, because of the tolerances between components or their own aging, $L_{eq}$ and $C_{eq}$ values can change. This change would modify the value of $t_1$ and $t_{on\_max}$. Therefore, to ensure ZCS in the diodes, the fulfillment of the inequality must be ensured for all the possible values that $L_{eq}$ and $C_{eq}$ can adopt, taking into account the maximum expected

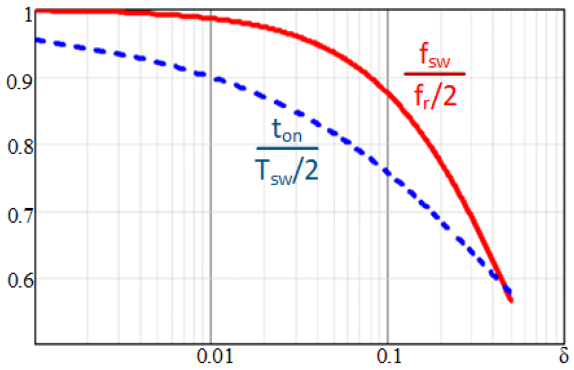



**FIGURE 11.** Normalized switching frequency (bold line); normalized $t_{on}$ (thin line) as a function of tolerance $\delta = d_{rL} = d_{rC}$, which correspond to the resonant inductor and capacitor tolerances respectively.

variations due to tolerances and aging. This leads to:

$$\frac{1}{L_{eq}} = \frac{1}{L_{Lk}} \cdot \sum_{i=0}^{m_t} \frac{1}{1 + dr_{L_i}} \tag{27}$$

$$C_{eq} = C_o \cdot \sum_{i=0}^{m_t} 1 + dr_{C_i} \tag{28}$$

where $m_t$ is the total number of modules, and $dr_{L\_i}$ and $dr_{C\_i}$ are the relative drift (positive or negative) of the inductor and the capacitor in module i. Therefore:

$$\omega_r = \sqrt{\frac{1}{L_{Lk} \cdot C_o} \cdot \sum\nolimits_{i=0}^{m_t} \frac{1}{1 + dr_{L_i}} \cdot \frac{1}{\sum_{i=0}^{m_t} 1 + dr_{C_i}}} \tag{29}$$

Assuming that $dr_L$ and $dr_C$ are expressed in absolute value and represent the maximum variation expected for the nominal values of the resonant tank elements, the maximum and minimum resonance frequencies can be calculated as:

$$f_{r\max} = \frac{1}{2\pi}\sqrt{\frac{1}{L_{Lk} \cdot C_o} \cdot \frac{1}{1 - dr_L} \cdot \frac{1}{1 - dr_C}} \tag{30}$$

$$f_{r\min} = \frac{1}{2\pi}\sqrt{\frac{1}{L_{Lk} \cdot C_o} \cdot \frac{1}{1 + dr_L} \cdot \frac{1}{1 + dr_C}} \tag{31}$$

Thanks to the symmetry of $V_o$(Fig. 3), it is easy to calculate $t_{on\_max}$:

$$t_{on\_max} = t_1 + \frac{\frac{T_{sw}}{2} - t_1}{2} = \frac{\theta}{2\omega_r} + \frac{T_{sw}}{4} \tag{32}$$

In order to keep$t_1 < t_{on} < t_{on_max}$ solvable under the entire operating range, $f_{sw}$ must be selected to meet:

$$t_{on\_max}\left(f_{sw}, f_{r\max}\right) = t_1\left(f_{sw}, f_{r\min}\right) \tag{33}$$

Assuming that $d_{rL} = d_{rC}$, the total maximum variation can be combined into a single tolerance value $\delta = d_{rL} = d_{rC}$. Then for different tolerance values of $\delta$, (32) has been solved numerically. The results are shown in Fig. 11, where the switching frequency appears normalized by half the nominal resonance frequency. As the tolerance increases, a lower switching frequency is needed and the time that the transformer remains short-circuited increases, reducing the value of $t_{on}$. Thus, for the same output current the rms current is increased, which is associated with lower efficiency. Moreover, voltage ripple on the capacitor will become higher. If it grows so much that equals its average value, the proposed equations will not be valid.

A value of $t_{on} \leq t_{on\_max}$ ensures that the resonance is not restarted for any drift value which smaller than $\delta$ (Fig. 11). However, choosing $t_{on} = t_{on\_max}$ minimizes the rms value of the current and thus increases the efficiency of the module. This method does not compromise modularity or simplicity. Conditions for ZVS in the primary switches are dependent on the magnetizing current only (not on load current) and short-circuiting the primary side keeps the magnetizing current at the value it had when the short-circuit was applied. Therefore, ZVS is not affected either.

### E. FAILURE PROTECTION

In high reliability applications, a failure analysis is mandatory to ensure that the failure of one element does not compromise the operation of the system and does not propagate to other elements. Space applications is one example of environments in which high reliability is mandatory and in which this topology has shown its potential [14] under the "new Space" paradigm [15]. The failure analysis must consider that every possible element (MOSFET, transformer, etc.) can fail in every possible mode (short circuit, open circuit, etc.). A Failure Mode Effects and Criticality Analysis (FMECA) following the recommendations of [34] will be used as a guide. According to [34], only one element is considered to fail at the same time. This single failure may compromise the module operation where the element is located but shall not propagate to the rest of modules or the whole DCX, whether by internal action or external one (e.g., fuse).

As will be explained, in the proposed DCX reliability is assured thanks to both, the matrix structure proposed in Fig. 6, where modules in the same row have their inputs connected in parallel and modules in the same column have them in series, and by the open circuit behavior of the input and output ports of the modules once an internal failure is detected. This allows to safely deactivate any failing module from the DCX structure. With an adequate power sizing of the individual modules, the operation of the DCX is not compromised even after this deactivation because the remaining modules increase its processed power, as in any redundant system.

To achieve the open circuit behavior at the input, the use of a full bridge turns relevant. Whenever a component fails and the failure is detected, the four switches will be commanded to turn off. This action will transform the input port into an open circuit. This will also force the output port to behave as an open circuit, thanks to the rectifier diodes.

A short-circuit in one of the switches of the bridge could be detected by an overcurrent protection at the input of the module. The same overcurrent protection will trigger if one

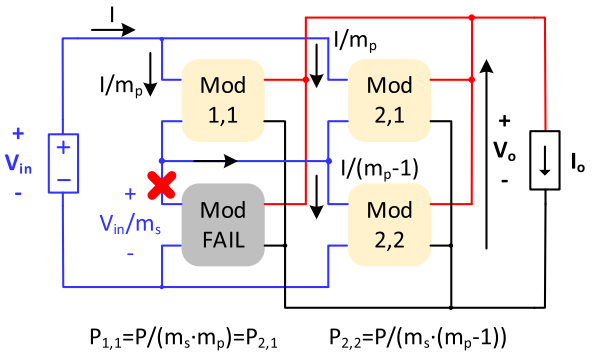



**FIGURE 12. Current and voltage sharing in a four DCX modules connection when one of them fails ($m_p = m_s$=2).**

of the bridge switches fails to open. In such a case, the transformer will not be driven in a balanced way and eventually will saturate, demanding an excess of current that will trigger the protection. Therefore, the only protection circuit that must be added to reach the aforementioned reliability is a current sensor at the input to detect an overcurrent, thus implementing an overcurrent protection. Upon detecting an overcurrent, the protection must turn off all the switches in the input bridge.

The OR-ing diode ($D_{\text{oring}}$) protects the module against a short-circuit failure in one of the rectifier diodes. If this happens, when the bridge legs switch both transformer secondaries will be connected. This situation will produce an overcurrent at the input that can be detected through the said overcurrent protection and cleared by commanding all the primary switches off. Thus, isolating the input port through the full bridge and the output port through $D_{\text{oring}}$.

Whenever one of the rectifier diodes fails in open circuit the whole current will be supplied only by one of the diode branches. This means that during one switching semicycle the module is not drawing current from the input but in the other it will supply double the current. So, on average, the module is processing the same power. Upon detection, the fault can be cleared by turning off the four primary-side switches, leading to the same situation, isolating the input port and thus the module from the matrix.

Finally, any kind of failure in the transformer or any other element (e.g., the OR-ing diode) can be solved again by turning off the full bridge (in fact, the OR-ing diode failure in short-circuit has no significant effect on the module operation).

As said, reliability is also based on the matrix structure. The $2 \times 2$ matrix of Fig. 12 will be used for the explanation; it can be regarded as a simplification of the general matrix shown in Fig. 6. This also replicates the setup used in the experimental results shown in Section IV-E. In nominal conditions, each module will have an input voltage of $\frac{V_{\text{in}}}{m_s}$ and will draw from its input a current $\frac{I}{m_p}$. Each module delivers $\frac{I_o}{m_p \cdot m_s}$ to the output. Please remember that in the matrix connection $m_s$ is the number of modules in series per string and $m_p$ the number of strings. In this simplified scheme, $m_s = 2$ and $m_p = 2$. When the module (1,2) fails, opening its four primary switches will allow their input and output port to behave as an open circuit, as explained. Thus, the module is removed from the DCX. As all the output ports are connected in parallel, the Module Under Failure (MUF) will not compromise the DCX operation and the only effect is a variation in the power distribution among modules, since they will have to compensate for the current that the MUF was injecting in the output capacitor.

Module (1,1) is serially connected to the MUF, at first sight it seems that open-circuit behavior of the MUF may represent a problem since it will interrupt the current flow to the input of module (1,1) and will change the even input voltage distribution in which each module withstands ($V_{\text{in}}/m_s$). However, due to the matrix connection, the voltage at the input port of the MUF is kept to its nominal value ($V_{\text{in}}/m_s$) thanks to the input of module (2,2), connected in parallel. Therefore, the input voltage of module (1,1) is then kept at its nominal value ($V_{\text{in}}/m_s$). The input current of this module (1,1) is driven by module (2,2) instead of by module (1,2) (i.e., MUF), so its operation is not significantly affected if a reasonable number of modules are used.

Regarding module (2,2), it will have to compensate for the loss of the MUF. It will have to drive half the overall power instead of one fourth because it must deliver its current plus the current that the MUF was delivering before failure.

Since the same presented reasoning could be applied to any module that becomes the MUF, it can be said that the failure of a module does not compromise the operation of the DCX.

Given the number of strings, and the assumption that only one module can fail, the rated power for each module can be defined without compromising the whole DCX rated power. As a rule of thumb, power conversion systems with high reliability requirements are made up of three converters operating in parallel, each of them sized for handling $\frac{1}{2}$ of the total system power, In nominal operation, each converters processes $\frac{1}{3}$ of the power so upon the failure and disconnection of one of them, the remaining ones handle $\frac{1}{2}$. The same reasoning could be applied in this application for selecting and sizing the number of strings in parallel $m_p$. With $m_p = 3$ and modules rated for $\frac{P}{(m_p-1)\cdot m_s}$, being $P$ the total rated power for the DCX. With such module sizing the operation for the system is guaranteed after one failure. An optimization of the $m_p$ number with regards to the power capability and mass of the system is outside the scope of this paper. The number of modules per string $m_s$ could be chosen to guarantee that the maximum allowed input voltage for the input bridges is never achieved.

To sum up, although the topology was already proposed in [32], the idea of ISOP and IPOP configurations, the use of its static gain for a robust matrix structure, its tolerance immunity analysis (derived from a static gain only dependent on the turn ratio of the transformer), and the method for preventing the loss ZCS due to tolerances in the resonant tank components are considered as the new contributions of this work.

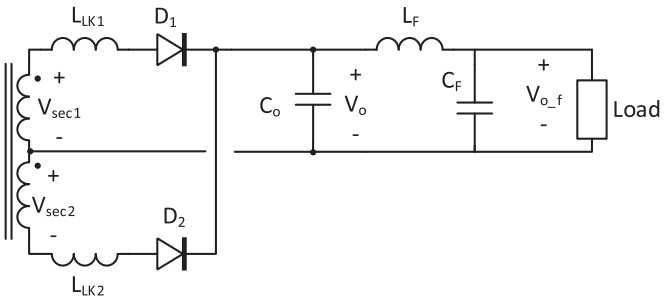



**FIGURE 13.** Secondary of topology with filter formed by $L_f$ and $C_f$.

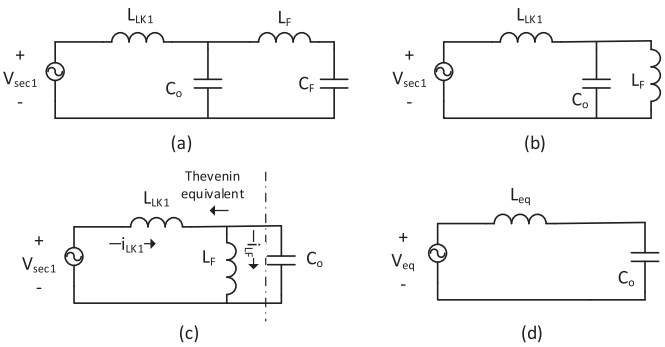



**FIGURE 14.** Analysis of the filter effect: (a) filter, (b) removal of $C_f$, (c) thevenin equivalent definition, (d) thevenin equivalent.

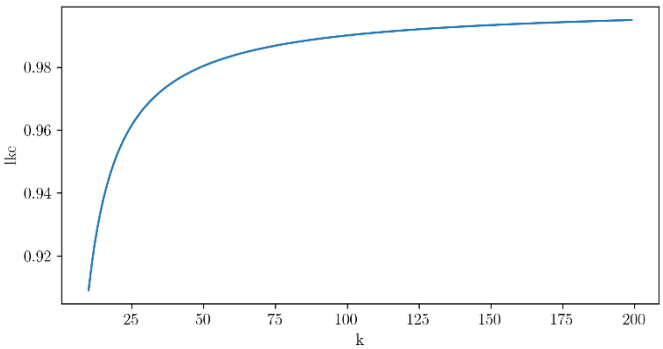



**FIGURE 15.** $l_{kc}$ vs $k$ ratio between $L_f$ and $L_{LK}$.

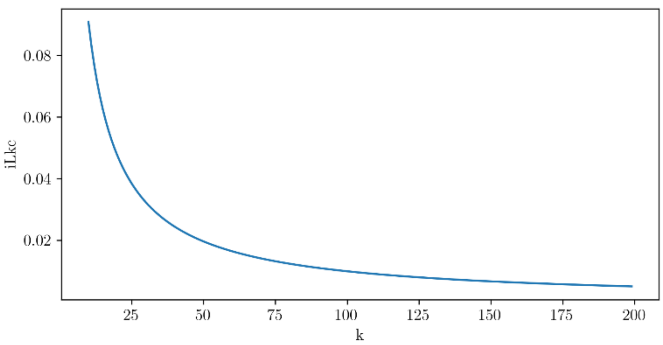



**FIGURE 16.** $i_{Lkc}$ vs $k$ ratio between $L_f$ and $L_{LK}$.

### F. OUTPUT FILTER ANALYSIS

Both, modules and DCX, present many advantages. However, they exhibit a big drawback. As the resonant capacitor is also the output capacitor, the output voltage ripple is significant. Moreover, any load that has an input capacitor will affect the resonance. Furthermore, the topology will work at its best when the load behaves as a current source. This is why on Figs. 2 and 3 the load is a current source.

For the sake of clarity, it is important to remark that the current source behavior must only take place at the resonant frequency used for designing the topology. Then, any load could behave as a current source when placed after a filter. The filter must have at least a filter inductance $L_f$. This will decouple the resonant capacitor from whichever load is connected afterwards. Combined with a filter capacitor $C_f$ it will remove the output voltage ripple. Of course, the filter could be further improved, for example introducing damping networks, but to achieve the current source behavior only an inductance $L_f$ would be needed.

Such a filter is represented in Fig. 13 and in a simplified version in Fig. 14(a). It is important to note that the analysis could be simplified if it is assumed that $C_f$ is big enough that its impedance at the resonant frequency $f_r$ is negligible. This is what it is represented at Fig. 14(b). The circuit can be rearranged as in Fig. 14(c). Taking the Thevenin equivalent renders Fig. 14(d). With these the values of $L_{eq}$ and $V_{eq}$, if $L_f = k \cdot L_{LK1}$, and noting that $L_f$ is in parallel with $L_{LK1}$ then:

$$L_{eq} = \frac{L_{LK1} \cdot L_f}{L_{LK1} + L_f} = L_{LK1} \cdot \frac{k}{1+k} = L_{LK1} \cdot lkc \tag{34}$$

$$V_{eq} = V_{sec1} \cdot \frac{L_f}{L_{LK1} + L_f} = V_{sec1} \cdot \frac{k}{1+k} = V_{sec1} \cdot lkc \tag{35}$$

Using the Thevenin equivalent represented in Fig. 14(c). It is possible to calculate how much current at the resonant frequency is flowing through inductor $L_f$:

$$i_{Lf} = i_{LK1} \cdot \frac{\frac{1}{L_f \cdot \omega_o \cdot j}}{1 + C_o \cdot \omega_o \cdot j} = i_{LK1} \cdot \frac{1}{1 - L_f \cdot C_o \cdot \omega_o^2} \tag{36}$$

Using (3) $\omega_o^2 = 1/C_o \cdot L_{LK1}$ and applying absolute value:

$$\left|i_{Lf}\right| = |i_{LK1}| \cdot \left|\frac{1}{1 - \frac{L_f}{L_{K1}}}\right| = |i_{LK1}| \cdot \frac{1}{1+k} = |i_{LK1}| \cdot ilkc \tag{37}$$

The evolution of $lkc$ and $ilkc$ against $k$ is represented in Figs. 15 and 16 respectively. It is apparent that for $k \geq 100$, the presence of $L_f$ does not affect the resonant operation of the converter. Considering $k = 100$, then $lkc = 0.99$ and $Leq = 0.99 \cdot L_{LK1}$. As $L_{LK1}$ is the leakage inductance of a transformer, it would be rather small; thus, even with high $k$ values, $L_f$ value will be small, and so it will be the inductor size. Moreover, in these same conditions ($k \geq 100$), $L_f$ will carry a negligible amount of AC current at the resonant frequency. For $k = 100$, $ilkc = 0.0099$ and thus $i_{Lf} = 0.0099 \cdot i_{LK1}$. The $L_f$ inductor current will be mostly DC, leading to a simplified inductor design since the losses and the saturation will be determined mostly by the DC operation.

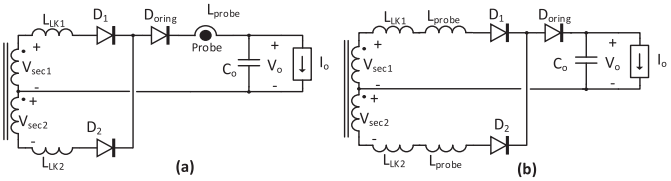



**FIGURE 17.** Current probe modifies the circuit. (a) probe position in circuit; (b) analyzed circuit.

Therefore, the input EMI filter of any converter connected to the output of this topology will not play any effect on its operation. Furthermore, it will make the load behave as a current source at the frequency of operation This latter issue is shown in Section V-A.

## V. EXPERIMENTAL RESULTS

To properly assess the operation of the converter the current through the rectifier diodes is very relevant. However, in this type of converter, the measurement of the diode currents modifies the converter operation Fig. 17(a). The leakage inductance of the transformers is part of the resonant circuit, and its small value is comparable to the inductance added by the current probe [35]. Therefore, and only for the purpose of being able to measure the rectifier output current, the inductance of the current probe has been considered as part of the resonant circuit. Considering that the resonant current always reaches zero, Fig. 17(a), which shows the real position of the probe in the circuit, can be represented as in Fig. 17(b) for simplifying the analysis.

This section is structured in three parts. On Section V-A experimental results for a single module are shown. In Section V-B several modules are connected in Input-Parallel Output-Parallel (IPOP) and Input-Series Output-Parallel (ISOP) configurations to form a DCX. Finally, Section V-C shows how a failure in one module does not propagate to the other ones and the DCX can continue with its operation.

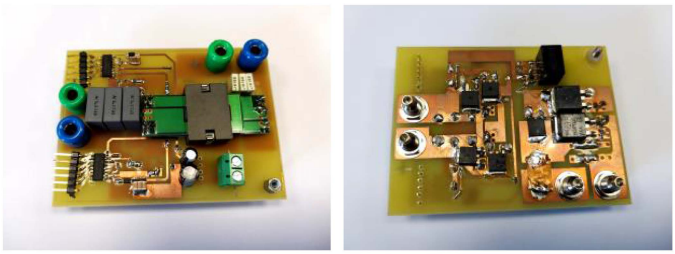
### A. EXPERIMENTAL RESULTS FOR A SINGLE MODULE

Four prototypes of DCX modules with two different layouts have been designed and built according to the schematic in Fig. 3. The main reasons for these two different layouts are based on the use of two different drivers (see Table I) and two different designs of the magnetic transformer during the experimental tests. Its mains characteristics are listed in Table I. Regarding the drivers, the typical propagation delay for IR2110 is 120 ns while for SI8238BB is 30 ns. This is very important as this delay will lead to a timing error, as described in Section IV-C and experimentally shown in Section V-B. A photograph of the prototypes can be seen in Fig. 18.

Fig. 19 shows a detail of the $V_{DS}$ and $V_{GS}$ transition of one of the MOSFETs, where ZVS is achieved. Fig. 20 shows the drain-source voltage in $M_4$ primary transistor ($V_{DSM4}$), the resonant currents through the rectifier diodes ($I_{LK}$), and the output voltage ($V_O$) behavior. Experimental results are in good agreement with calculated waveforms, as the dashed

**TABLE I** Main Specifications of the Module Designed

| | |
|---|---|
| **Input voltage ($V_{in}$)** | 56 V |
| **Output voltage ($V_O$)** | 28 V |
| **Rated power ($P_O$)** | 200 W |
| **Switching frequency ($f_{SW}$)** | 365kHz |
| **Clock Source** | ALTERA MAX 10M50DAF484C7G |
| **Leakage inductance ($L_{LK1}$, $L_{LK2}$)** | 55nH |
| **Current Probe Impedance (800 kHz)** | (77nH)+76mΩ |
| **Output capacitor ($C_O$)** | 300nF |
| **MOSFETs ($M_1$, $M_2$, $M_3$ y $M_4$)** | PSMN063-150D |
| **Rectifier diodes ($D_1$, $D_2$)** | NRVBB60H100CTT4G |
| **Or-ing diode** | V35PW60HM3/I |
| **Magnetic core** | EIR22/6/16 |
| **Magnetic material** | N97 |
| **Drivers** | IR2110 / SI8238BB |
| **Turns ratio** | 4:2 |
| **Resonant frequency (Fr)** | 790kHz |
| **$2t_{on}/T_{sw}$** | 0.73 |
| **θ** | 4.626 Rad |
| **Synchronization error $t_d$** | 90ns |



(a) (b)

**FIGURE 18.** Photograph of one of the prototypes. (a) top side and (b) bottom side.

traces on Fig. 20 indicate. However, in the equations, an efficiency of 100% has been assumed, hence the experimental results appear more damped. The current probe adds a resistance of 78 mΩ at high frequency. This is half of the total equivalent resistance of the circuit.

It is possible to see that the output voltage ripple is not negligible in the DCX topology, however this ripple can be easily filtered. Fig. 21 shows the same waveforms as Fig. 20 but a damped LC filter has been added at its output. This LC filter was sized as a typical input EMI filter, so it emulates the presence of a converter placed at the output of the module. Note that the inductance of the filter is $L_f = 150\ \mu H$, and the

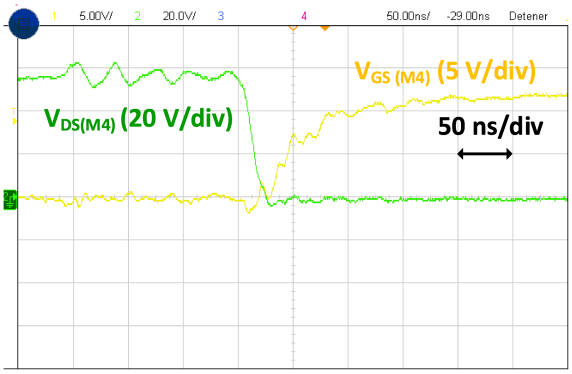



**FIGURE 19.** ZVS operation on primary side switches. Nominal operating conditions as described in Table I.

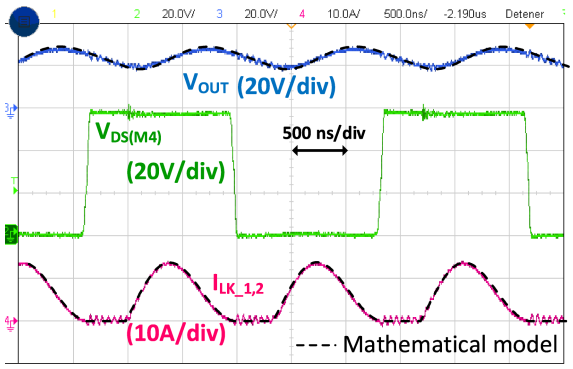



**FIGURE 20.** $V_{DS}$ (M4), $V_O$ and $I_{LK\_1,2}$ without output filter. Nominal operating conditions as described in Table I.

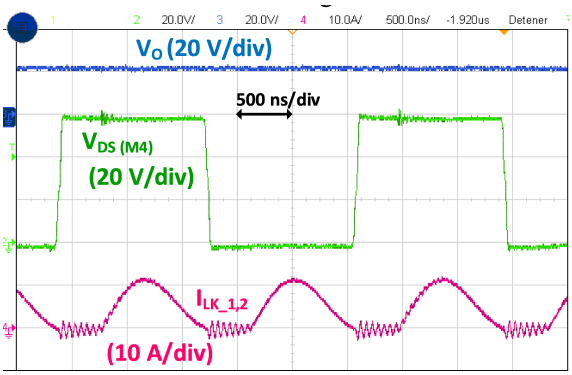



**FIGURE 21.** $V_{DS}$ (M4), $V_{OUT}$ and $I_{LK\_1,2}$ considering an output filter. Nominal operating conditions as described in Table I.

leakage inductance is $L_{LK1} = 55$nH then k = 1549 in ( 34 ) (Actually the presence of the current probe makes k = 645). This proves that the presence of the filter does not affect the resonant process whilst removing the output ripple and making the module operate with a constant current load.

As can be seen, ZVS can be reached in primary switches and ZCS in secondary ones. Therefore, the tested efficiency of each module is high, as shown in Fig. 22, reaching 96% at the rated power and near 95% at half of the rated power (the OR-ing diode is not considered in this case). There is the possibility of optimizing semiconductors, so efficiency could be higher.

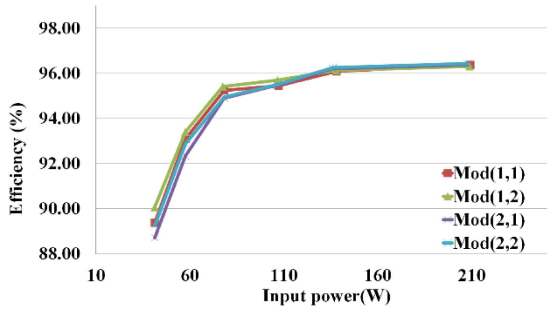



**FIGURE 22.** Efficiency comparison between modules. Measured independently at nominal conditions for the whole power range.

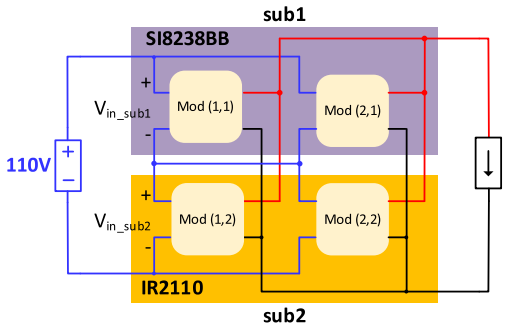



**FIGURE 23.** Schematic of four modules in matrix configuration.

### B. EXPERIMENTAL RESULTS USING FOUR MODULES

The four modules could be combined in several ways. The matrix connection represented in Fig. 6 will be used. The DCX nominal input voltage is twice (i.e., 110 V) the nominal voltage of one module (i.e., 55 V), while the output voltage is still equal to 27.5 V, the nominal voltage of one module, thanks to the input series connection. At the same time, the rated power of the whole DCX (i.e., 800 W) is four times the rated power of a single module (i.e., 200 W). Fig. 23 shows the combination of four modules in the matrix configuration. Sub 1 and Sub 2 blocks represent the IPOP combination of a pair of modules, while both blocks are serialized at their input.

The MOSFETs drivers of Sub1 introduce a delay of 30 ns while the drivers of Sub2 introduce a delay of 120 ns (according to manufacturer's data sheet). Fig. 24 shows the input voltages in both subsystems ($V_{in_sub1} = 54.96$V; $V_{in_sub2} = 55.81$V) and the filtered output voltage of the whole system ($V_o$). The input voltage is shared among the modules connected in series with high accuracy; yet a small difference occurs, and the reason is straightforward. Fig. 25 shows the resonant currents through the rectifying diodes in the four modules. The dashed line indicates when the switches in Mod (1,1) and Mod (2,1) change its state. As can be seen, $I_{Mod1,1}$ and $I_{Mod2,1}$ are in advance of $I_{Mod1,2}$ and $I_{Mod2,2}$. According to (26), modules with early trigger signals provide more output current and, consequently, power. However, sub1 and sub2 are series connected and the same average input current must flow

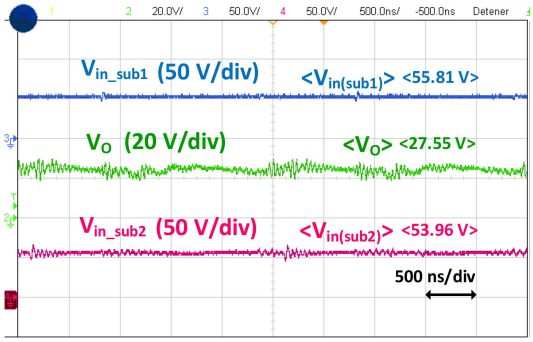



**FIGURE 24.** Input voltages for sub1 and sub2 and DCX output voltage ($V_O$). $V_{in\_sub1} = 53.96V$; $V_{in\_sub2} = 55.81V$. Nominal operating conditions for each module as described in Table I.

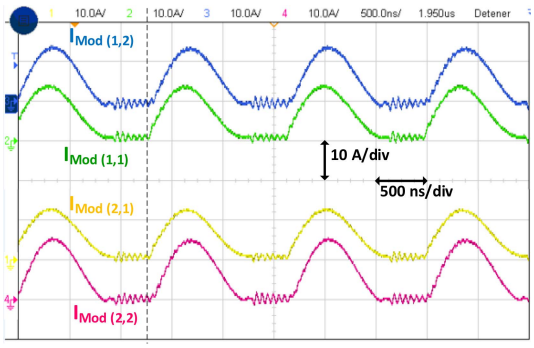



**FIGURE 25.** Resonant currents through the rectifier diodes in the four modules. Nominal operating conditions for each module as described in Table I.

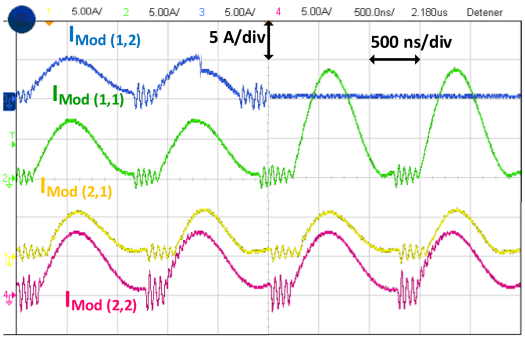



**FIGURE 26.** Resonant currents through the rectifier diodes. Module Mod 12 fails due to short circuit in $M_3$. Conditions described in Table I apply to module (2,1) after the failure and with half the rated power to all the modules before failure (redundancy 1+1).

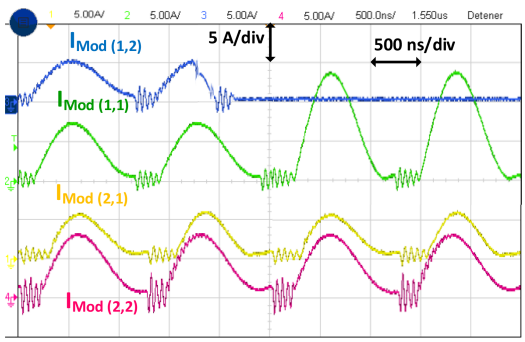



**FIGURE 27.** Resonant currents through the rectifier diodes. Module Mod 12 fails due to $M_2$ and $M_3$ are in OFF state permanently. Conditions described in Table I apply to module (2,1) after the failure and with half the rated power to all the modules before failure (redundancy 1+1).

through them. Therefore, a corrective mechanism appears. Modules with trigger signals in advance must reduce their input voltage until the input currents achieve equalization. This voltage reduction can be calculated using (22).

Assuming that parallel-connected modules are identical, the current unbalance that produces the synchronism error can be expressed as:

$$\begin{cases} I_{ET1} = I_{ET2} \cdot \left(1 + 2\theta \frac{\cos(\theta)-1}{\sin(\theta)} f_{\text{sw}} \cdot t_d\right) \\ I_{ET1} + I_{ET2} = 13 \\ I_{ET1} = 7.424A;\ I_{ET2} = 5.576A;\ \Delta I = 1.848A \end{cases} \tag{38}$$

Using this current error, the input voltages are obtained:

$$\begin{cases} Vin_{sub1} = \frac{Vin}{2} - \frac{\Delta V}{2 \cdot n};\ Vin_{sub2} = \frac{Vin}{2} + \frac{\Delta V}{2 \cdot n} \\ \frac{\Delta V}{L_{LK}} \left(\frac{\theta}{w_r}\right)^2 f_{\text{sw}} = \Delta I = 1.848A \\ \Delta V = 1.52\ V;\ Vin_{sub1} = 54.24\ V;\ Vin_{sub2} = 55.76\ V \end{cases} \tag{39}$$

The difference between the two voltages in the laboratory is 1.85V, the difference calculated with the equations presented in this work where lossless operation is assumed is 1.52 V. By simulation, a difference of 1.79 V has been obtained.

### C. FAILURE EFFECT OF A MODULE IN A MATRIX CONFIGURATION

For this analysis, two possible failure modes (short circuit and open circuit) have been emulated in one of the MOSFETs of module Mod 12 in Fig. 23, following [34]. Fig. 26 represents the resonant currents through the four DCX modules for a short circuit failure while Fig. 27 shows the results for the open circuit failure.

In both cases, failure occurs when the resonant currents are at their peak value, as it can be considered the worst case. As can be seen, both situations are satisfactorily cleared by forcing the four driving signals of the MOSFETs to turn off, as described in Section III-D. Obviously, only three of the MOSFETs will follow the gate driving command, while the fourth one will be kept either open or closed, emulating its failure. The whole situation is easily implemented through the module controller. The isolated module Mod (1,2) does not compromise the DCX operation, as the rest of the modules continue with its regular resonant behavior. Modules Mod (2,1) and Mod (1,1) are not affected in the power sharing while module Mod (2,2), which is in parallel to Mod (1,2), increases its resonant current so the total power delivered to the load remains constant. This power increment depends on the number of parallelized modules at the input, thus introducing a redundancy level. This test also verifies that the

dynamic behavior of the proposed topology is excellent. From the perspective of Mod (1,1), a 100% load step has occurred, and it adjusts its resonant current in just one switching cycle, without transitory, which means that the output current is adjusted in one cycle as well.

It is important to note that there is a slight difference between the evolution of the resonant current once the module is isolated. As can be seen, in the short circuit failure the resonant current of module Mod (1,2) needs more time to reach zero. This is because when one of the MOSFETs fails in short circuit, the primary side of the transformer is short circuited due to the parasitic diode that drives the current along with the failing MOSFET. When the MOSFET fails in open circuit, the primary side of the transformer is negatively biased through two of the parasitic diodes, leading to a faster demagnetization of the leakage inductance (resonant inductance). Once this current reaches zero, the module is properly isolated.

## VI. CONCLUSION

The proposed DC/DC Transformer (DCX) is based on the matrix connection of fixed-design DCX modules based on an isolated resonant topology. Voltage adaptation is achieved by series connection of modules at the input, forming the so-called string, while power scalability is achieved by parallel connection of strings. All the modules are connected in parallel at the output, leading to a combination of ISOP and IPOP connections. Furthermore, the matrix configuration in which all the modules in a string have its inputs connected to the inputs of the correspondent modules of the other strings introduced an increased reliability.

The topology of the module is based on an isolated resonant topology whose static gain is fixed and only dependent on the turn ratio of its transformer. This allows the modules to perfectly share the power and the input voltage, without a specific or complex control apart from a simple common clock signal (synchronization signal). As the resonant capacitor is the output capacitor, all the modules have their resonant capacitors in parallel. Consequently, voltage sharing at the input is not affected by tolerances in the resonant components and power sharing is only affected by inductance tolerances. Moreover, no dedicated control, besides a common synchronization signal, is dedicated to power sharing. The main disadvantage is a non-negligible high frequency voltage ripple in the DCX output. Nonetheless, it is easily filtered by an inductor or EMI filter. The matrix structure of the DCX, the topology chosen for the modules, the fixed static gain only dependent on the turn ratio of the magnetic transformer (a parameter robust against tolerances and aging), and the absence of complex control loops make the system highly fault tolerant.

The overall efficiency is high, being especially high at full load. The current probe modifies the converter behavior. Therefore, it has been considered as part of the circuit. The experimental results are in good agreement with the analysis performed.

The DCX proposed is considered very reliable thanks to three features. The possibility of isolating a module by commanding all the switches open upon overcurrent detection at the input of a module. Natural power sharing, without the need of complicated power sharing control loops and finally the matrix connection. As analyzed and proved, upon the loss and isolation of one module the rest of the modules automatically compensate for its loss without disturbing the power delivery. This makes this proposal very interesting for high reliability applications such as space ones.

## ACKNOWLEDGMENT

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