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# Ripple Reduction of Active Split DC-Link 4-Wire Inverters by Phase-Shifted Multi-Carrier Modulation

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**ABSTRACT** This paper considers a multi-carrier modulation in which the phase-shifts between the carriers are adjusted to reduce the rms current flowing into the active split dc-link capacitors of four-wire three-phase inverters when the neutral node is modulated with the third harmonic. Capacitors current reduction is beneficial in terms of volume, losses, and components stresses. Considering the current ripple combination of the phases and neutral currents, the proposed approach reduces the rms current through the split dc-link capacitors compared to a standard single-carrier pulse-width modulation. It is shown that the amount of reduction depends on the modulation index and the ratio between the neutral and the output inductors. Besides, it is not significantly influenced by the unbalancing current, in the considered topology, in which the split dc-link capacitors are aimed to regulate the neutral-point voltage. Guidelines for selecting suitable phase-shifts in practical cases based on the inverter operating point are discussed. The results are demonstrated on an experimental prototype.

**INDEX TERMS** Four-leg inverter, carrier phase-shift, split current reduction.

## I. INTRODUCTION

Four-wire three-phase (4W3Φ) inverters are widely used in grid-tied applications, such as microgrids and photovoltaic systems [1], [2], [3], [4], [5], [6], [7] and for electric drives [8], [9]. The typical 4W3Φ structure is composed of three inverter legs plus a neutral connection provided by the mid-point of the series connection of two capacitor banks, constituting a split dc-link [10]. The split dc-link is designed to allow the circulation of the neutral current, which typically implies bulky capacitor banks [11]. To allow better neutral-point regulation and reduce capacitor size, a fourth leg is often used.

Different kinds of four-legs inverters exist [12], [13]. The topology displayed in Fig. 1 is considered in this work, where the neutral connection is created by an active filter made of the two switches $S_{1N}$, $S_{2N}$ and the second-order filter

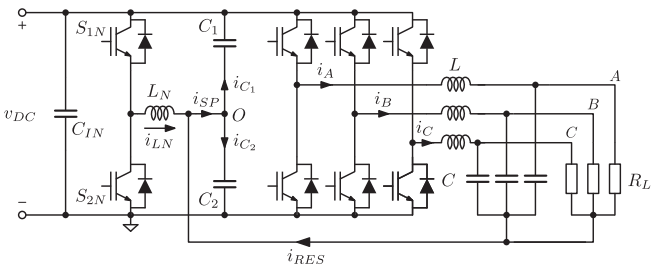


**FIGURE 1.** Four-wire three-phase inverter (4W3Φ) with active split dc-link.

$L_N, C_1, C_2$, herein referred to as active split dc-link. At the cost of the additional inductance $L_N$, the converter provides a better dc-link voltage exploitation by the use of third-order harmonic injection, and, since most of the unbalancing current

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flows through the neutral-leg [14], it is effective in supplying unbalanced loads [15], [16].

Remarkably, the active split dc-link capacitors may constitute the whole dc-link capacitor bank [17], [18], [19], as done with 4W3Φ topologies. In this case, the total capacitance value should be enough to stabilize the dc-link voltage. Differently, in the considered structure, the capacitors $C_1$ and $C_2$ are used solely to generate the neutral point voltage $v_O$. Besides, by controlling $v_O$, the connection between the midpoint of the dc-link and the common output voltage reduces the effect of the switching frequency noise between the dc-bus voltage terminals and the ground connection [15], [20]. Additionally, compared to the standard 4W3Φ inverters, the neutral-leg inductance allows to reduce the electromagnetic interference (EMI) [15]. It is worth remarking that, the said neutral-leg inductance does not correspond with the neutral inductor found in other topologies, like [3], [11], where the fourth leg is used to control the voltage of the neutral wire.

This paper discusses the compensation of the ripple of the split dc-link current $i_{SP}$ flowing through the split capacitors $C_1$ and $C_2$ by properly phase-shifting the carriers of phase-legs modulators and the neutral-leg modulator.

A lack of literature that directly consider the outline problem in four-leg inverters is reported. Instead, there are several papers addressing similar challenges considering three-leg inverters, which is a closely related problem and sets the motivation and the basis for the further analyses presented herein. Among those papers, [21], [22] analyze the ripple of the three-phase inverter with three or four legs, but the computation of the split dc-link capacitors currents is not addressed. The residual ripple while operating with third-harmonic injection is not considered too. In [23], a carrier-based approach is used for a seven-level cascaded half-bridge inverter, where the output current ripple is reduced by applying a phase-shift to a carrier signal, obtaining a lower ripple profile on the total current. In [24], the authors apply phase-shifts between the modulation carriers of a three-phase inverter and an input boost converter stage to reduce the inverter's input capacitor current. A similar approach is used in [25] to reduce the dc-link ripple in a six-phase inverter for a six-phase electrical machine. In [26], a multi-carrier pulse-width modulation (PWM) is used with a 4W3Φ inverter with carriers phase-shifted by 180°, but in a different topology with the neutral-leg inductor not directly connected to the center of the split dc-link capacitors, showing the advantages on the common mode voltage and current as compared to the use of a unique carrier. In [27], the ripple is reduced by means of interleaved carriers (i.e., phase-delay equal to $2\pi/n$, where $n$ is the number of legs). A similar result is pursued in [28], where a probabilistic approach is proposed to study the neutral current ripple in 4W3Φ inverters and find the minimum global ripple for the interleaved operation of the three-phases; the same result is found in [29] investigating the minimization of the load current ripple with a typical three-phase interleaved dc-dc converter.

Remarkably, these works consider inverters with three half-bridge legs; differently, operation with a fourth half-bridge leg to achieve active split dc-link control is investigated herein. In this case, interleaved carriers modulation is not always the best choice for minimizing the split dc-link current ripple, then a multi-carrier approach is proposed and analyzed in the following to reduce the split dc-link current ripple, without introducing hardware or control modifications.

In the remainder of this paper, Section II presents the ripple calculation results and discusses practical solutions for rms current reductions; Section III demonstrates the proposal by measurements on an experimental setup, Section IV concludes the paper.

## II. INVERTER CURRENT RIPPLE

### A. SPLIT DC-LINK RIPPLE MODELING

Considering the 4W3Φ topology displayed in Fig. 1, the half-bridge legs are modulated to produce symmetrical three-phase voltages $v_{xO}$ at the output terminals $x = A, B, C$. Their amplitudes $V_{xO}^{pk}$ depend on the maximum variation of the duty-cycles $d_x$, namely, the modulation index $M_x = d_x^{\max} - d_x^{\min}$, and the dc-link voltage $v_{DC}$. Assuming a negligible voltage drop across the output filter inductors at the grid frequency $f_g$, the three duty-cycles $d_x$ vary sinusoidally in the interval $1/2 \pm M_x/2$, such that

$$v_{xO}(t) = [2d_x(t) - 1]\,\frac{v_{DC}}{2} = \frac{m_x(t)}{M_x} V_{xO}^{pk}\,, \tag{1}$$

where $m_x$ is the modulating signal defined as $m_x = 2d_x - 1$. The residual current $i_{RES}$ is the sum of the currents in the three phases. In this topology, capacitors $C_1$ and $C_2$ are used for the closed-loop regulation of the split dc-link voltage $v_O$, instead, dc-link voltage stabilization is provided by the capacitor $C_{IN}$ [30]. Additionally, in typical applications, the neutral voltage $v_O$ is closed-loop controlled, making it independent from the exhanged current $i_{RES}$.

Consistently, the grid-frequency current component (i.e., unbalanced current at the fundamental grid frequency) mainly flows through $L_N$. Neglecting the unbalanced current, $i_{RES}$ can be represented as the combination of the three relative ripples. Considering the third-harmonic injection (THI) on the neutral leg, the voltage of the neutral node $O$ referred to the negative dc-link terminal in Fig. 1 (i.e., the voltage on capacitor $C_2$) and the current on the split dc-link capacitors can be written as:

$$v_O(t) = \frac{v_{DC}}{2} + k_3 M_x \frac{v_{DC}}{2} \sin(3\omega_g t), \tag{2}$$

$$i_{3g}(t) = \frac{v_O(t) - v_{DC}/2}{2 \cdot 3\omega_g C_N} \sin(3\omega_g t), \tag{3}$$

where $k_3$ is the relative magnitude of the third harmonic component (e.g., $k_3 = 1/6$ for best dc-bus utilization [15]), $\omega_g = 2\pi f_g$, and $C_N = C_1 = C_2$. The equivalent circuits in Fig. 2(a) and (b) can be drawn for the neutral and the phases, respectively. The voltages across the phases and the neutral-leg inductors can be written as:

$$v_{Lx} = v_x - v_{xO} - v_O, \tag{4}$$

$$v_{LN} = v_N - v_O, \tag{5}$$

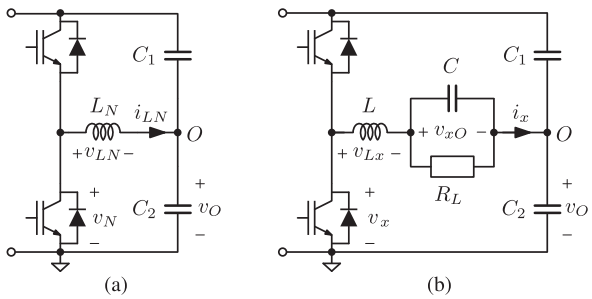


**FIGURE 2.** Equivalent model for (a) the neutral and (b) the phase circuits.

with $v_x$ and $v_N$ denoting the generated voltages. Considering a symmetric output filter (i.e., equal $L$ and $C$ for all phases) and the injection of the third-harmonic component, the residual and the neutral-leg inductance currents are:

$$i_{RES}(t)=\frac{1}{L}\sum_x\int_{t-T_g}^{t} v_{Lx}(\tau)\,\mathrm{d}\tau, \tag{6}$$

$$i_{LN}(t)=\frac{1}{K_L L}\int_{t-T_g}^{t} v_{LN}(\tau)\,\mathrm{d}\tau, \tag{7}$$

where $x \in \{A, B, C\}$, and $K_L = L_N/L$ is the inductance ratio between the neutral and the output filter inductors. From (6) and (7), the split capacitors current is:

$$i_{SP}(t) = \frac{1}{L}\int_{t-T_g}^{t}\left(\sum_x v_{Lx}(\tau) + \frac{1}{K_L}v_{LN}(\tau)\right)\mathrm{d}\tau. \tag{8}$$

Equation (8) shows that, by changing the phase-shifts among the generated voltages, the ripples $i_{LN}$ and $i_{RES}$ combine differently, thus modifying the shape of $i_{SP}$.

It is worth noting that, disregarding possible small regulation errors, the current $i_{SP} = i_{C1} + i_{C2}$ does not depend on the load value, including unbalances, being $v_O$ closed-loop controlled.

### B. HARMONIC ANALYSIS OF THE CURRENT RIPPLE

The rms of the current ripple on the phases and the split capacitors are preliminary analyzed in this section using a first harmonic approximation. The analysis formalizes the problem and motivates the convenience of exploring phase-shifted multi-carrier modulation to reduce the rms of the split dc-link current, which is solved in the subsequent sections by a numerical approach.

Neglecting the low-frequency components, a generic current ripple in a switching period can be expressed by its Fourier series:

$$i(t) = \sum_{n=-\infty}^{\infty} c_n \exp(j2\pi n f_{sw} t), \tag{9}$$

where $c_n$ are the complex Fourier coefficients and $f_{sw}$ is the switching frequency. Restricting at this stage to only the first component at $f_{sw}$ (i.e, $n = 1$), the current $i$ can be approximated by its fundamental component during the switching period:

$$i^{(1)}(t) = 2|c_1|\cos(2\pi f_{sw} t + \angle c_1). \tag{10}$$

Considering the currents through the phases and the neutral, the first harmonic Fourier coefficients are functions of the duty cycles of each leg $d_x$, with $x$ representing the phases and the neutral; it can be shown that:

$$c_{1x} = \frac{v_{DC}}{2\pi^2 f_{sw} L}(e^{-j2\pi d_x} - 1 + j2\pi d_x). \tag{11}$$

Noticeably, the duty cycles $d_x$ change along the grid period, and so do the Fourier coefficients in (11). Lets assume grid periods partitioned into $H$ switching periods (i.e., $f_{sw} \simeq H f_g$ with suitable integer $H$, assumption easily met in practice, typically being $f_{sw} \gg f_g$ in applications) and the PWM carriers of the inverter legs phase-shifted by an angle $\varphi_x$, considering phase $C$ as the reference. The amplitude of the first harmonic component of $i_{SP} = i_{RES} + i_{LN}$ during the $h$-th period $T_h$ can be written as:

$$i_{SP}^{(1)}[T_h] = \sum_x c_{1x}[T_h]\exp(j\varphi_x)\ , \tag{12}$$

where the notation $[T_h]$ specifies the considered switching period. The rms of the current can be calculated by the Parseval's theorem, since the considered quantities have finite energy. Under the previously introduced approximation $f_{sw} \simeq H f_g$, the integral of the square of the current over a grid period $T_g$ can be calculated as:

$$\int_{T_g} i_x^2(t)\,\mathrm{d}t = \frac{1}{H}\sum_{h=1}^{H}\sum_{n=1}^{\infty}|c_{nx}[T_h]\exp(j\varphi_x)|^2\ . \tag{13}$$

Limiting the second summation to the first index (i.e., to the fundamental harmonic of the ripple), the rms values of the phase currents $i_x$ can be derived from (13) as:

$$i_{x,\mathrm{rms}} = \sqrt{\frac{1}{HT_g}\sum\nolimits_{h=1}^{H}|c_{1x}[T_h]|^2}\ , \tag{14}$$

where the phase of the PWM carrier does not contribute. Finally, the rms value of the current $i_{SP}$ can be calculated from (12), obtaining:

$$i_{SP,\mathrm{rms}} = \sqrt{\frac{1}{HT_1}\sum\nolimits_{h=1}^{H}\left|\sum\nolimits_x c_{1x}[T_h]\exp(j\varphi_x)\right|^2}\ , \tag{15}$$

with $x$ including the three phases and the neutral. Remarkably, (15) shows that the angles $\varphi_x$ of the PWM carriers are involved in determining the computed rms quantity, and can be tailored for reducing the rms value of the split capacitor current.

Based on the considerations above, this paper aims at improving the inverter operation in terms of rms current ripple through the split dc-link capacitors without implementing provisions implying control or hardware modifications, but by showing how to suitably phase-shifting the modulation carriers. This goal is pursued in the following by a numerical analysis to solve the considered $i_{SP}$ ripple minimization problem, also including a numerical evaluation of the effectiveness of the found solutions with respect to other possible choices.

### C. EFFECT OF PHASE-SHIFT MODULATION

As previously shown in (8), the current $i_{SP}$ is mainly composed of the ripples combinations of $i_{RES}$ and $i_{LN}$, thus,

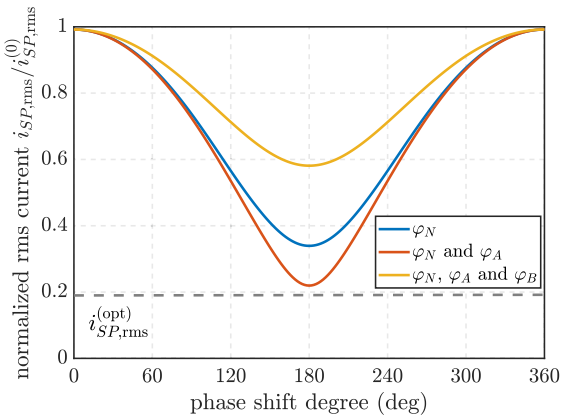


**FIGURE 3.** Normalized rms ripple currents varying the carriers phase-shifts, considering variations of the neutral carrier (i.e., $\varphi_N$), the carrier of the neutral plus a phase (i.e., $\varphi_N$ and $\varphi_A$), and the neutral plus two phases (i.e., $\varphi_N$, $\varphi_A$ and $\varphi_B$). Phase-shifts are referred to phase $C$ and equal for all the shifted carriers. Operating condition $K_L = 1$, $M_x = 0.8$.

in the following, the third harmonic component $i_{3g}$ is neglected. A numerical approach considering the sweep of each carrier phase-shift (i.e., neutral $\varphi_N$ and phases $\varphi_x$) has been implemented to find the phase-shift that corresponds to the optimum rms ripple of $i_{SP}$ (i.e., $i^{(\mathrm{opt})}_{SP,\mathrm{rms}}$). Numerical approaches, as done, for example, in [31], allow to achieve useful results tackling the challenges of the considered optimization problem. It is worth remarking that, while the motivation and problem formalization of the study is described in Section II-B focusing of the first harmonic of the ripple, including the other harmonics is crucial for an effective rms current minimization. The extension to higher order harmonics and the pursuit of a closed-form generic solution to the problem involve cumbersome mathematical treatment and more complex solutions, that imply additional complexity in practical applications while giving negligible further advantages in the minimization, as shown in the following in Section II-D. Fixing the inductance ratio and the modulation index, applying the above-mentioned sweep, a hyperplane of points $\Phi = (\varphi_N, \varphi_A, \varphi_B, \varphi_C)$ is obtained. These coordinates change with $K_L$ and $M_x$, resulting in a different optimal $\Phi$ changing the operating condition. For example, for $K_L = 1$, by performing a sweep for each phase-shift with a step of 9°, the optimum rms current corresponds to $\Phi = (144, 234, 0, 0)^\circ$ for $M_x = 0.8$ and, to $\Phi = (198, 162, 0, 0)^\circ$ for $M_x = 0.6$. Fig. 3 displays a section of the hyperplane for $K_L = 1$ and $M_x = 0.8$; here, considering the carrier of the phase $C$ as the reference one, the considered carriers are phase-shifted by the same angle (e.g., $\varphi_N = \varphi_A = 180^\circ$ means 180° phase-shift applied to the neutral and phase $A$ carriers with respect to phase $C$) and are compared to the absolute minimum found for $(144, 234, 0, 0)^\circ$ coordinates, named $i^{(\mathrm{opt})}_{SP,\mathrm{rms}}$.

To extend the comparison with the common choice of interleaved carriers (see, e.g., [27]), Fig. 4 displays the current $i_{SP}$ for cases 0, N, NP, and the current $i_{SP}$ resulting by adopting carriers phase-shifted by $\Phi = (0,\ 0,\ 120,\ -120)^\circ$ for the additional case I3 and $\Phi = (0,\ 90,\ 180,\ 270)^\circ$ for the case I4. The comparison is performed in the operating condition $K_L = 1$ and $M_x = 0.8$ for the above-cited cases.

**TABLE 1.** Phase-Shifts Cases Considered in Section II-D Together With Normalized Current $i_{SP,\mathrm{rms}}/i^{(0)}_{SP,\mathrm{rms}}$ for N, NP, N2P, I3, and I4 Case for the Operative Points for Different Operating Points

| Case | $\Phi$ | | | | $M_x = 0.8$ | $M_x = 0.6$ |
|---|---|---|---|---|---|---|
| | $\varphi_N$ | $\varphi_A$ | $\varphi_B$ | $\varphi_C$ | $K_L = 1$ | $K_L = 0.5$ |
| 0 | 0 | 0 | 0 | 0 | 1.00 | 1.00 |
| N | 180 | 0 | 0 | 0 | 0.37 | 0.15 |
| NP | 180 | 180 | 0 | 0 | 0.23 | 0.28 |
| N2P | 180 | 180 | 180 | 0 | 0.59 | 0.64 |
| I3 | 0 | 0 | 120 | -120 | 0.40 | 0.47 |
| I4 | 0 | 90 | 180 | 270 | 0.25 | 0.34 |

In addition, Table 1 reports the resulting rms current reduction, normalized with respect to case 0 (i.e., $i_{SP,\mathrm{rms}}/i^{(0)}_{SP,\mathrm{rms}}$), for operating conditions $M_x = 0.8$ $K_L = 1$ and $M_x = 0.6$ $K_L = 0.5$. As expected, the interleaved cases I3 and I4 are outperformed by other phase-shift configurations.

In summary, in order to reach the optimal rms current, an independent phase-shift for each digital PWM of the inverter legs is needed. Remarkably, for proper control, this would commonly imply also different sampling instants of the controlled inductor currents for each related analog-to-digital converter (ADC). Fig. 5 illustrates the issue considering triangular carriers with double sampling [32]. The situation with no phase-shift for the reference phase $x$ and an arbitrary phase-shift $\varphi$ for phase $y$ is considered, highlighting the related sampled inductor currents $i_x$ and $i_y$, respectively. The sampling for phase $x$ corresponds to the classical operation not exploiting the carriers phase-shift, with sampling instants, marked by solid dots, corresponding to the average inductor current. Differently, due to the applied arbitrary phase shift $\varphi$, the current samples for phase $y$, marked by solid squares, do not correspond to the current average value, which is detrimental for control and requires dedicated solutions (e.g., to resynchronize the sampling processes of the several legs with the modulation), potentially leading to involved microcontroller implementations. Of course, the desirable feature of the no phase-shift case (i.e., case 0) would be maintained by applying phase-shifts multiple of 180° for all the other phases (i.e., phase $y$ in this example). Then, suboptimal solutions are pursued herein that overcome the additional complication of using different sampling-times for the four legs. Still, in Section II-D (e.g., see Table 2) a comparison with optimal phase shifts is presented to show that only negligible advantages would be obtained in the minimization by using optimal phase shifts, not presenting the aimed feature related to the required sampling time.

### D. MODULATION INDEX AND INDUCTANCE RATIO DEPENDENCY

Limited the phase-shift value at 0° and 180°, the study continued analyzing the $K_L$ and $M_x$ dependency. For the following

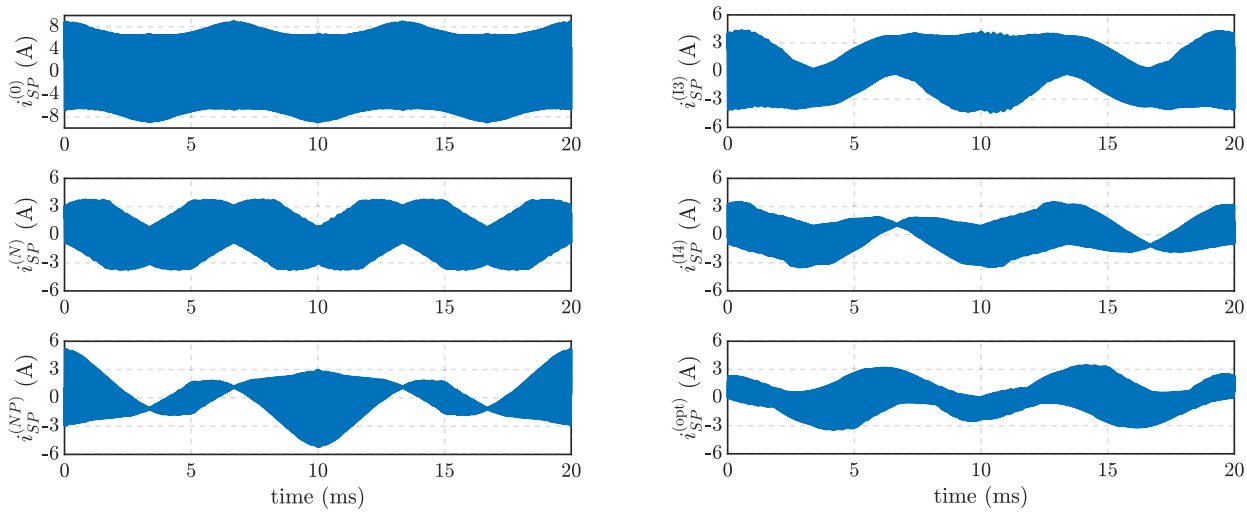


**FIGURE 4.** Ripple of $i_{SP}$ for unitary inductance ratio $K_L$ (i.e., $L_N/L$) and modulation index $M_x = 0.8$ for cases 0, N, NP, I3 (three phases interleaved [28]), I4 (four-phases interleaved), and minimum current coordinates $\Phi = (144, 234, 0, 0)^\circ$ found by numerical approach.

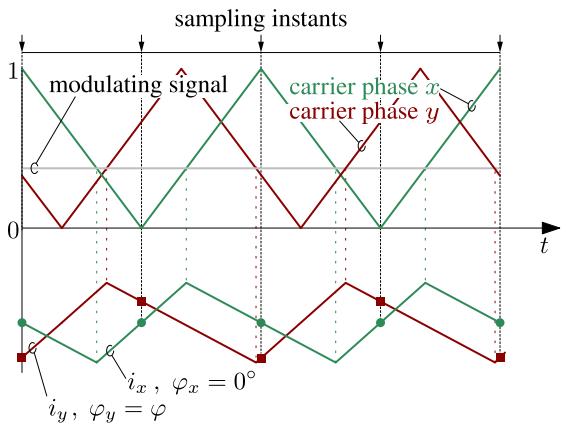


**FIGURE 5.** Sampling scheme of two phases with carriers phase-shifted by $0^\circ$ and $\varphi$. The inductor current samples of phase $y$ are shifted compared to those of phase $x$ and do not correspond to the average value of the current through phase $y$.

**TABLE 2.** Proposed Solution N /NP in Fig. 7 Compared With the Optimal Phase-Shifts (opt.)

| modulation index $M_x$ | inductance ratio $K_L$ | $i_{SP,\mathrm{rms}}/i_{SP,\mathrm{rms}}^{(0)}$ opt. | N/NP | $\%\epsilon_{\text{opt-N/NP}}$ |
|---|---|---|---|---|
| 0.4 | 0.4 | 0.076 | 0.08 | 0.4% |
| | 0.7 | 0.15 | 0.15 | 0% |
| | 1 | 0.07 | 0.09 | 2% |
| 0.6 | 0.4 | 0.11 | 0.12 | 1% |
| | 0.7 | 0.12 | 0.21 | 9% |
| | 1 | 0.13 | 0.15 | 2% |
| 0.8 | 0.4 | 0.18 | 0.21 | 3% |
| | 0.7 | 0.16 | 0.22 | 6% |
| | 1 | 0.18 | 0.23 | 5% |

The obtained normalized rms current ripple $i_{SP,\mathrm{rms}}/i_{SP,\mathrm{rms}}^{(0)}$ is reported at representative values of $M_x$ and $K_L$. Difference $\%\epsilon_{\text{opt-N/NP}}$ is also reported, showing relatively minor differences among the optimal solution and the proposed one.

sections the phase-shift notation is changed and reported in the Table 1; thus, to refer to the split current in one of the cases in Table 1, the notation changes consequently (i.e., $i_{SP,\mathrm{rms}}$ when the case N is considered is denoted with a superscript).

Fig. 6 displays the graphs of the normalized rms current $i_{SP,\mathrm{rms}}$, for the phase-shifts cases N, NP and N2P for $K_L$ and $M_x$ variation. As can be seen, for these phase-shifts the rms current is always less than the standard case and, dependently from the operative condition, we reach lower rms current for different phase-shifts (e.g., for $K_L \approx 0.35$ and $M_x \approx 0.8$ the N case achieves lower current). Noticeably, the minimum rms current occurs for the N or NP case, instead case N2P shows higher rms current and it will be discarded hereinafter.

Fig. 7 reports the best normalized split ripple rms for each value of $K_L$ and $M_x$. The red curve represents the boundary condition where cases N and NP cause the same current reduction, and it is computed such as the difference between $i_{SP,\mathrm{rms}}^{(\mathrm{N})}$ and $i_{SP,\mathrm{rms}}^{(\mathrm{NP})}$ is lower than 0.25%. If the operative point is placed on the left of that boundary condition, choosing case N ensures lower current; otherwise, when it is placed on the right, the favorable case becomes NP.

As reported the Table 2, the current reduction corresponding to the cases N or NP is close to the absolute minimum found by the optimal phase-shifts, with a slight increase in the percentual rms current reduction, measured as:

$$\epsilon_{\text{opt-N/NP}} = \frac{i_{SP,\mathrm{rms}}^{(\mathrm{opt})} - i_{SP,\mathrm{rms}}^{(\mathrm{N/NP})}}{i_{SP,\mathrm{rms}}^{(0)}} , \tag{16}$$

which is limited below 10% in the considered operating points. Such minor improvements, at the cost of a more complex management of the converter control, sampling, and modulation, limit the convenience of using phase shifts that are not multiple of 180°, as anticipated in Section II-C.

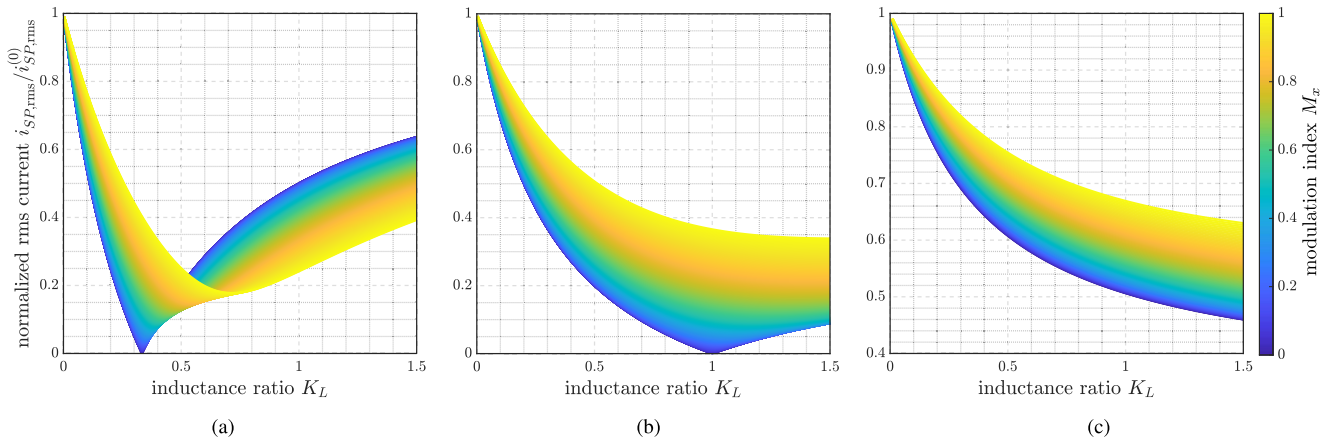


**FIGURE 6.** Normalized rms current ripple $i_{SP,\mathrm{rms}}/i^{(0)}_{SP,\mathrm{rms}}$ as a function of the inductance ratio $K_L$ (i.e., $L_N/L$) varying the modulation index $m_x$ for (a) case N, (b) case NP, and (c) case N2P, defined in Table 1. Phase-shifting the neutral carrier (i.e., N) or the neutral and a phase-carrier (i.e., NP) allows better rms current reduction than phase-shifting a single phase-carrier (i.e., N2P).

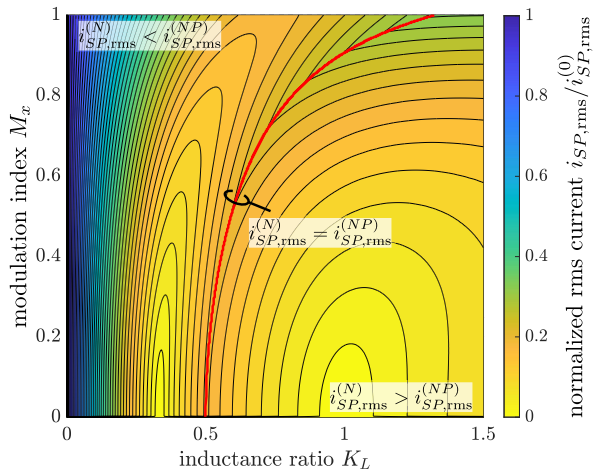


**FIGURE 7.** Normalized rms current $i_{SP,\mathrm{rms}}/i^{(0)}_{SP,\mathrm{rms}}$ as a function of the inductance ratio $K_L = L_N/L$ and the modulation index $M_x$.

## III. EXPERIMENTAL VERIFICATION

In order to verify the carrier phase-shift effectiveness on reducing the capacitor ripple, a flexible power electronic converter (PEC) system with rapid control prototyping [33] has been used. Each of these systems is composed by three half-bridges with rated 650 V Gallium Nitride switches with integrated output filters (i.e., $L$ and $C$). The digital control consists of B-Board Pro by Imperix that allows easy duty-cycle and phase-shift variations. An external board with the split dc-link capacitors $C_1$ and $C_2$ is connected to create the neutral connection $O$, whose voltage will be modulated with the third-harmonic as shown in Fig. 8. The voltage $v_O$, defined in Fig. 1, is regulated by a proportional regulator with a resonance at the third harmonic, as often done in inverter control [34].

The control for the Imperix boards is generated in the Matlab/Simulink environment and comprehends the controls of the four-legs voltages. Double-rate update digital PWM with triangular carriers are used for every inverter [32], allowing a separate variation of their phase-shifts. The electrical parameters of the system are reported in Table 3. Further details on

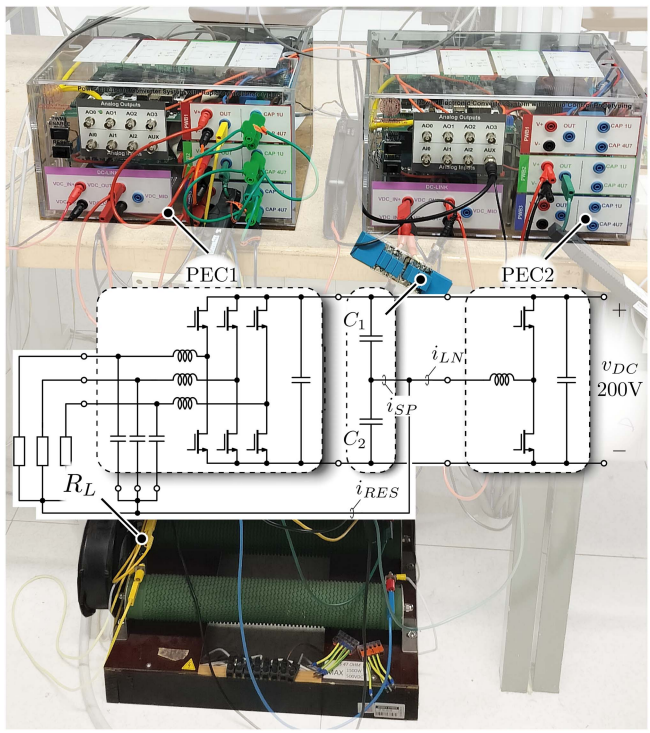


**FIGURE 8.** Experimental setup of the 4W3Φ inverter with active split dc-link used for testing the proposed multi-carrier modulation. The two electronic power converters [33] (PEC) constituting the three phase-legs and the neutral-leg, the external split dc-link capacitors $C_1$ and $C_2$, and the three-phase load are highlighted.

**TABLE 3.** Experimental Parameters

| Parameter | Value | | Parameter | Value | |
|---|---|---|---|---|---|
| $v_{DC}$ | 200 | V | $L$ | 340 | $\mu$H |
| $V_{xO}$ | 80 | V | $C$ | 5.7 | $\mu$F |
| $f_g$ | 50 | Hz | $L_N$ | 340 | $\mu$H |
| $f_{sw}$ | 25 | kHz | $C_{1,2}$ | 39 | $\mu$F |
| $k_3$ | 0.15 | – | $R_L$ | 47 | Ω |

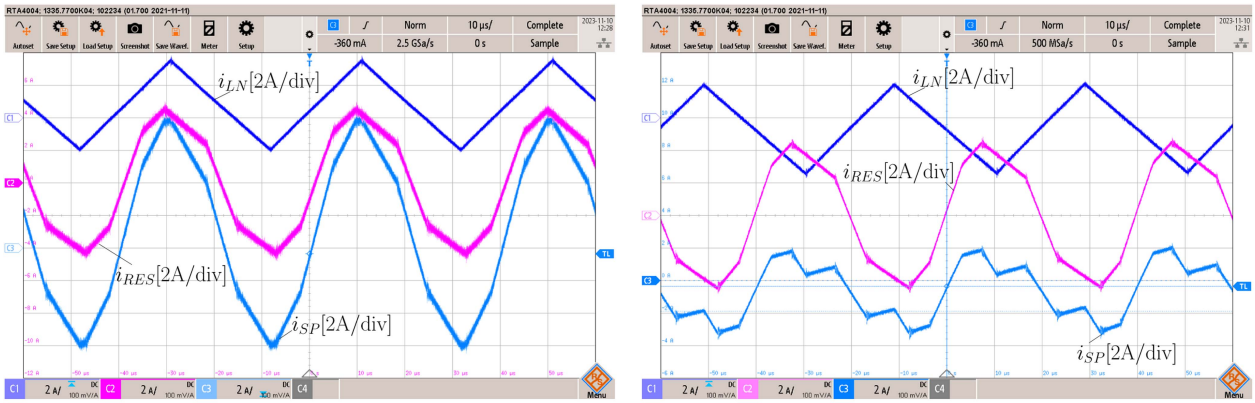


**FIGURE 9.** Zoomed current waveforms $i_{LN}$, $i_{RES}$ and $i_{SP}$ in cases 0 and N with balanced load showing the different ripple compensation due to the neutral carrier phase-shift. Symbols as defined in Fig. 1.

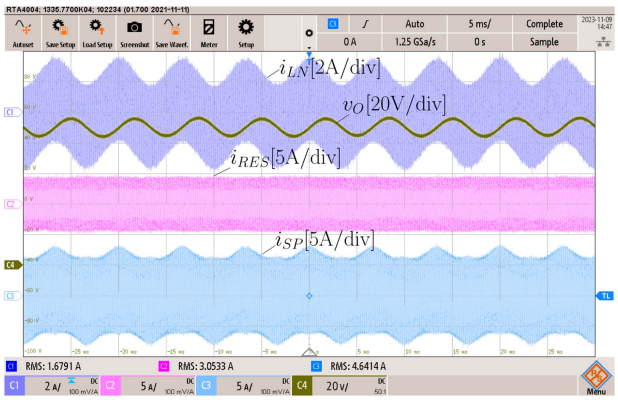


**FIGURE 10.** Waveforms in case 0 with balanced load. Symbols as defined in Fig. 1.

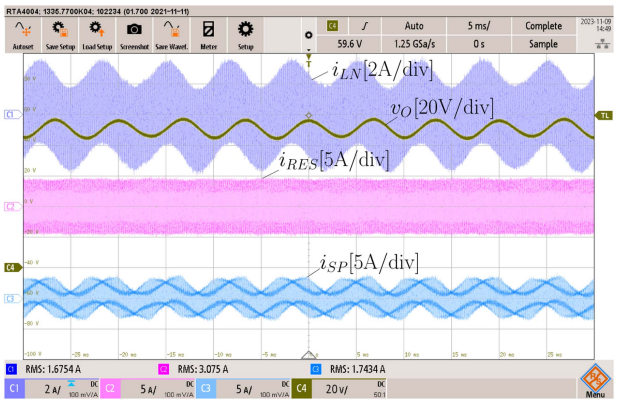


**FIGURE 11.** Waveforms in case N with balanced load. Symbols as defined in Fig. 1.

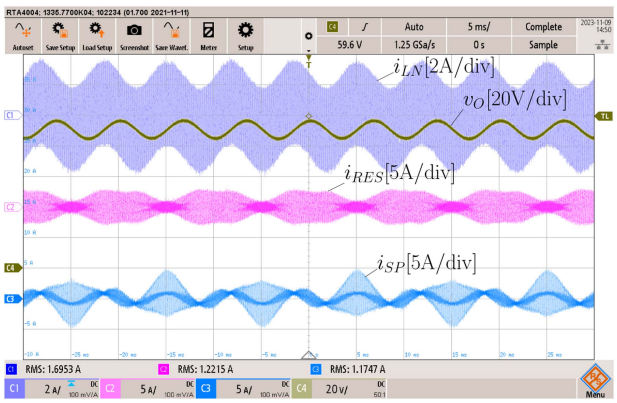


**FIGURE 12.** Waveforms in case NP with balanced load. Symbols as defined in Fig. 1.

the used PEC and integrated measurement circuits for control are available in [33].

Fig. 9 shows the currents $i_{LN}$, $i_{RES}$ and $i_{SP}$ when the cases 0 and N are applied. Although the inductor and residual currents maintain the same value in both cases, their ripple is partially compensated in case N, showing a lower value for $i_{SP}$.

Figs. 10, 11, and 12 report the currents $i_{LN}$, $i_{RES}$ and $i_{SP}$ and the voltage $v_O$ in the cases 0, N and NP with balanced load. In Figs. 13, 14, and 15, the same waveforms are shown during unbalanced operation, specifically, the load phase $C$ is decreased by 50% (i.e., $R_L^C = R_L/2$). As can be seen, the current flowing through $L_N$ contains the first harmonic component, thus, its envelope and the rms value change substantially from the balanced waveforms; moreover, there is no substantial difference in the current $i_{SP}$ between the balance and unbalanced case, as already expected in the previous section. Besides, a 50 Hz component is present in the voltage $v_O$ too; this is due to the parasitic components of the neutral circuit (i.e., the on resistances of the switches and the parasitic resistances of $L_N$, $C_1$ and $C_2$) and it can be abated, for example, by including a resonant regulator to the split dc-link voltage control loop. Being this a secondary effect, not relevant to the perspective of the study herein reported, it is not further considered.

The current $i_{SP}$ changes considerably its envelope, thus, its rms value, with the carrier phase-shifts variation. In this case (i.e., $K_L = 1$ and $M_x = 0.8$), the minimum ripple occurs for the NP case, with the normalized rms value of 0.25, as expected in the Fig. 7 with a value of 0.23. The difference

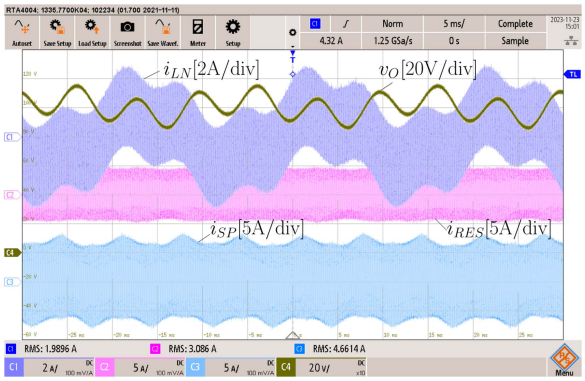


**FIGURE 13.** Waveforms in case 0 with 50% of phase C unbalance (i.e., $R_L^C = R_L/2$). Symbols as defined in Fig. 1.

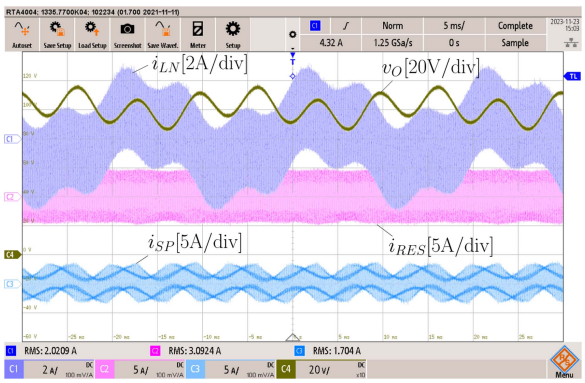


**FIGURE 14.** Waveforms in case N with 50% of phase C unbalance (i.e., $R_L^C = R_L/2$). Symbols as defined in Fig. 1.

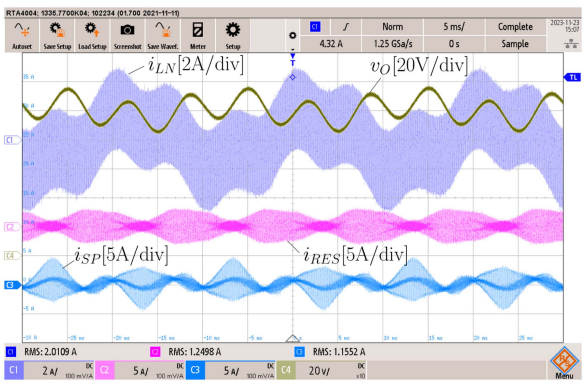


**FIGURE 15.** Waveforms in case NP with 50% of phase C unbalance (i.e., $R_L^C = R_L/2$). Symbols as defined in Fig. 1.

from the expectation is explained by the consideration, in the experimental measurements, also of the third-harmonic component, differently from the graphs of Fig. 7, where, in order to have a general result, only the ripple is evaluated.

## IV. CONCLUSION

A simple method to reduce the rms current of the split capacitors of a four-leg three-phase inverter is presented in this paper. By phase-shifting one or two carriers with a corresponding multi-carrier modulation, the split capacitor current's ripples can be compensated and the resulting rms current reduced. It is demonstrated that the optimal carriers' phase-shifts needed to reduce the current ripple on the split dc-link capacitors vary with the operating conditions. It is shown that phase-shift values of 0° or 180° correspond to a local current minima that provide a significant decrease in the ripple current compared to the standard single carrier modulation and also preserve the possibility of using simple double-update modulation. In the considered two-level inverter, the local optimal phase-shift coincides with case N or the NP. This behavior is also demonstrated through experimental measurements, showing the different current ripple combinations and remarking the effectiveness of the multi-carrier approach, also in the unbalanced conditions. A map of the optimal phase-shift is discussed giving a fast instrument to choose for the carrier phase-shift that guarantees the lower current in the split capacitors for each operative condition.

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This manuscript reflects only the authors views and opinions, neither the European Union nor the European Commission can be considered responsible, for them.

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