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High-Energy Dynamic Avalanche to Failure by Incremental Source-Voltage Increase in Symmetric Double-Trench & Asymmetric Trench SiC MOSFETs

MANA HOSSEINZADEHLISH [1] (Graduate Student Member, IEEE), SAEED JAHDI [1] (Senior Member, IEEE), XIBO YUAN [1] (Senior Member, IEEE), JOSE ORTIZ-GONZALEZ [2] (Member, IEEE), AND OLAYIWOLA ALATISE [2] (Senior Member, IEEE)

[1]Electrical Energy Management Group, School of Electrical, Electronic and Mechanical Engineering, University of Bristol, BS8 1UB Bristol, U.K.
[2]Power Electronics Applications and Technology in Energy Research Group, School of Engineering, University of Warwick, CV4 7AL Coventry, U.K.

CORRESPONDING AUTHOR: SAEED JAHDI (e-mail: saeed.jahdi@bristol.ac.uk)

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ABSTRACT The unclamped inductive switching (UIS) measurements can be categorized as “low energy” and “high energy” avalanche. The conventional approach to these tests is to increase the stress by either increasing the pulse length, or decreasing the inductor’s size. However, for evaluation of the novel trench SiC MOSFETs, increase of electric field by voltage can be more influential to detect the degradation patterns and exact point of failure. This article, for the first time, investigates the avalanche rating to failure of the similarly rated SiC power MOSFETs in planar, symmetric double-trench and asymmetrical trench structures through incremental increase of applied voltage as the “high energy” technique to investigate the mechanisms of dynamic avalanche under elevated electric fields. Using this approach, the electrothermal stress is induced by incremental increases of voltage source on UIS at a range of temperatures between 25 °C and 175 °C. Silvaco technology computer-aided design (TCAD) simulations have been developed, validated, and analyzed to evaluate the stress mechanisms to failure. The measurements, validated by TCAD, show that some failure mechanisms when stress is elevated by increase of source voltage are different than the case of “high current” avalanche initiation by increase of pulse durations as reported in the past. In planar device, the peak electric field plays a key role in failure, as is the failure in symmetric device at low case temperatures. In asymmetric device, the critical avalanche energy of failure in both cases of 25 °C and 175 °C are very close, suggesting independence from the thermal headroom.

INDEX TERMS Avalanche breakdown, double-trench, electrothermal ruggedness, silicon carbide (SiC), MOSFET.

I. INTRODUCTION

Silicon carbide MOSFETs have ten times higher critical electric field than silicon MOSFETs, and consequently can block higher voltages with a thinner drift region resulting in lower ON-state resistance and conduction loss which can improve the efficiency of power systems [1], [2], [3], [4], [5]. Moreover, their three times higher thermal conductivity compared to the Silicon enables better thermal dissipation. Silicon-based power semiconductor devices have limitations in high voltage and high temperature applications, addressed by wide-bandgap semiconductors such as SiC, which has ameliorated the performance of the power MOSFETs. Several structures of SiC power MOSFET are developed in recent years, with Fig. 1 illustrating the cross-section of the key structures, as planar, symmetrical double trench, and asymmetrical trench gates, respectively.

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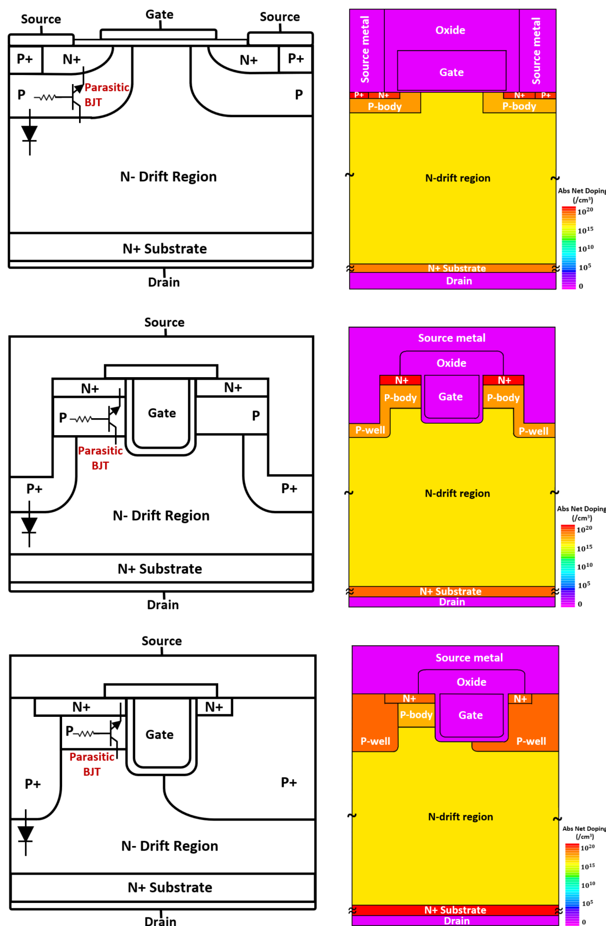

FIGURE 1. Cross-sectional schematics and TCAD model of the planar, symmetrical double-trench & asymmetrical trench SiC MOSFETs.

The representative model in technology computer-aided design (TCAD) is also shown as validated by *IV* comparisons with manufacturers' datasheets and will be used to analyse the dynamics of unclamped inductive switching (UIS) at "high energy" avalanche.

Due to the simple structure and production process, SiC planar gate have been widely used in fabrication of SiC MOSFETs to-date. However, planar gate MOSFETs suffer from high ON-state resistance as a result of low channel conductivity and presence of the FET region. The interface states between SiC and SiO_2 also impact the performance and reliability of SiC MOSFETs [6], [7]. This issue has been significantly alleviated in SiC MOSFETs with trench gate structures [8]. Trench-gated MOSFETs offer advantages, such as reduced ON-state resistance leading to decreased conduction losses, as well as high power density, fast switching speed, and lower switching loss [9], [10]. However, there are other reliability concerns with trench structures too. First, the inconsistency of the oxide thickness at different regions during fabrication is an issue, with oxide at the side trenches usually being thicker than the bottom trench. Second, the elevated concentration of high electric field across the corners and the base of the trench gate in blocking state [11], [12] can lead to rupture at the oxide insulation [2]. In an effort to address these shortcomings in normal trench gates, two novel structures are developed as symmetric double-trench and asymmetric trench, by Rohm and Infineon, respectively. The third-generation symmetric double-trench SiC MOSFETs compose of two deep P- regions within the source-body cells that suppress the density of the electric field at gate trench base to an extent [13], [14], [15]. Nevertheless, these P pillars not only reestablish an additional junction field effect transistor (JFET) section, but also restrict the downscaling of the cell pitch, while based on the previous research the asymmetrical trench SiC MOSFETs can achieve a cell pitch even as fine as 0.2 μm [16], enabling better switching and conduction performance [9], [17], [18]. The symmetric double-trench structure enables a wider more-conductive channel with a higher carrier density, and overall less ON-state resistance than planar devices [19], [20]. However, the bottom of the trench of the gate oxide region has a thinner layer of SiO_2 than the sidewalls due to uneven oxidation process [6]. Here, the gate oxide is protected by additional P^+ regions on the source trench. One other approach to address this shortcoming is extension of the P-body region to underneath the gate trench on one side to protect it from the excessive electric fields. This is the concept of the asymmetric trench. This technique, however, means only one channel formed as one of the tow sidewalls of the gate trench. The reduced current density is compensated by the trench oxide be parallel to the (11–20) crystal plane with a 4° angle [21], [22] to the vertical direction which enables doubling of the carrier mobility [21], [23].

Several papers in the past have attempted to analyze the avalanche [24], [25], [26], [27] performance of the planar SiC MOSFETs, compared with third generation asymmetric trench and symmetric double-trench SiC MOSFETs [28], [29], [30], [31], [32] during avalanche. However, all of the past research have simply increases the electrothermal stress on device, up to failure, by either increasing the pulse duration during which the inductor is charged, resulting in higher current, or by decreasing the size of the inductor which similarly leads to increase of the avalanche current until failure. In these cases, the devices are typically failed by activation of the parasitic bipolar junction transistor (BJT). This is because the BJT only activates at high displacement currents conducted through the p-body region as the base of the BJT. In these cases, the avalanche voltage is conventionally calculated [33], [34] by

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} \tag{1}$$

in which BV_{DSS} is the breakdown voltage, the V_{DD} is applied source voltage, and the I_{AS} is the single pulse avalanche current [33], [34].

However, unlike past research where the energy stored in the inductor is gradually increased by prolonging the pulse duration, in this article, the energy is increased by incremental increase of the voltage while the pulse duration and inductor are fixed. This means the device will not only experience

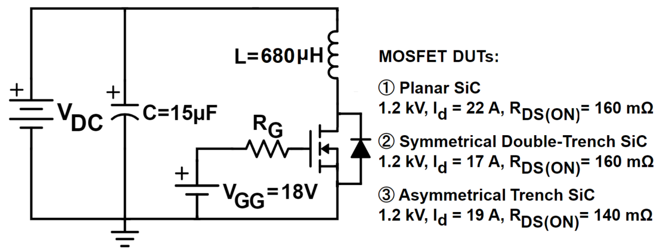

FIGURE 2. Schematic of UIS circuit and DUTs.

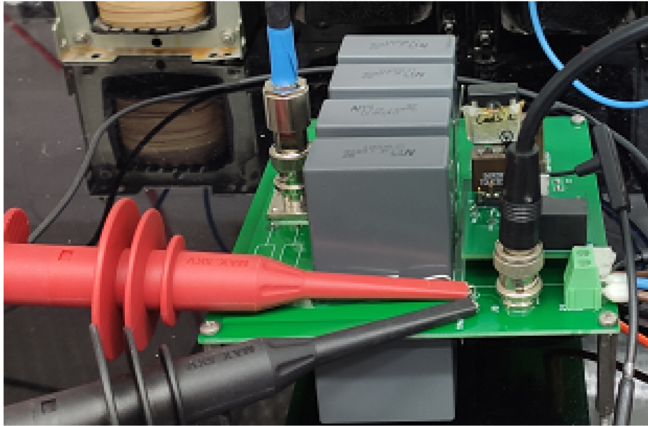

FIGURE 3. Experimental test setup of UIS test.

high current, but will experience high current and high applied electric field concurrently. This is why the first type of avalanche is typically referred to as "high current," while this is called the "high energy" avalanche.

This article aims to investigate the "high energy" type avalanche by UIS [35] with fixed inductor and fixed pulse duration, with increase of the applied source voltage to the inductor until failure. Three similarly rated SiC MOSFETs with different structures are selected to evaluate their robustness against electro-thermal stress using the "high energy" avalanche. To enable verification of the experimental results and to understand the actual failure mechanisms during avalanche breakdown, TCAD simulations of the experiment conditions have been carried out using Silvaco TCAD validated by device *IV* comparisons with manufacturers' datasheets. A comprehensive analysis and comparison of the failure mechanisms have been made between planar gate and trench MOSFETs.

II. EXPERIMENTAL MEASUREMENTS OF "HIGH ENERGY" UIS

The failure mechanisms and capability of devices under "high energy" avalanche are evaluated by utilizing an UIS test shown in Fig. 2. Fig. 3 depicts the test setup of this experiment in which a single gate pulse with the fixed duration of 40 μs across all tests is applied to the device while an inductor of 680 μH is used in series with the device under test (DUT). The UIS test has been done at both room temperature and 175 °C so as to check the impact of temperature on the avalanche mechanism with a high voltage electronic test & power systems (ETPS) power supply (HTP-HPp 40 757) rated at maximum 4 kV and 750 mA to charge the dc-link capacitors. These capacitors hold and release the electric charge at the point of UIS to enable the avalanche currents to tens of amps, although its rate of rise to very high currents can lead to a nonlinear rise profile.

According to Fig. 2, initially a gate pulse is applied to the DUT in the turn-ON mode. During this time interval, the inductor starts to be charged via the power supply through the DUT up to the point of reaching the maximum avalanche current. Avalanche current peak is specified with the size of the inductor and the width of the applied gate pulse. This is followed to the turn-OFF mode, in which a high voltage equal to the breakdown voltage is generated across the DUT. At the same time, since the power inductor current cannot be changed to zero promptly, this current will flow from drain to the source of the DUT as the shoot-through current induces the DUT into the avalanche mode. This time interval continues until all the energy stored in the power inductor releases and then avalanche mode terminates. In the following, the measured drain-source voltage, peak avalanche current as well as calculated avalanche energy are presented in order to evaluate and compare the avalanche ruggedness of the aforementioned device structures.

Figs. 4 and 5 demonstrate the drain-source voltage and load current of the three devices for incrementally increased dc-link voltages until failure at 25 °C and 175 °C. It can be seen that raising the temperature to 175 °C has resulted in failure of the devices at a lower dc-link voltage. Based on Fig. 5, the planar SiC MOSFET can stand maximum avalanche current of 25 A before failure at both room temperature and 175 °C. Symmetrical double-trench SiC MOSFET fails at $V_{DC} = 600\,V$ and $V_{DC} = 420\,V$ at 25 °C and 175 °C, respectively. According to Fig. 5, it after tolerating 34 A avalanche current at room temperature and avalanche current of 26 A at 175 °C. Asymmetrical tench SiC MOSFET fails at lower dc-link voltage compared to the other two devices at room temperature, while it fails at higher dc-link voltage as the temperature increases to 175 °C. With regard to the avalanche current, the asymmetrical trench SiC MOSFET fails after enduring avalanche current of 27 A at room temperature and 35 A at high temperature. It is clear that asymmetrical trench MOSFET has a better performance compared to symmetrical double-trench MOSFET at 175 °C.

In all three devices the avalanche failure happens at lower dc-link voltage when increasing the temperature from 25 °C to 175 °C. Based on Fig. 1, all structures are composed of a bipolar BJT structured by the N drift region, P-body along with the N^+ region of the source. When the device enters the avalanche Mode, high electric field is formed across the junction of the N drift region and the P-body, so an avalanche current flows from the drain to the source through the PN junction. During this process, if a part of the current flows

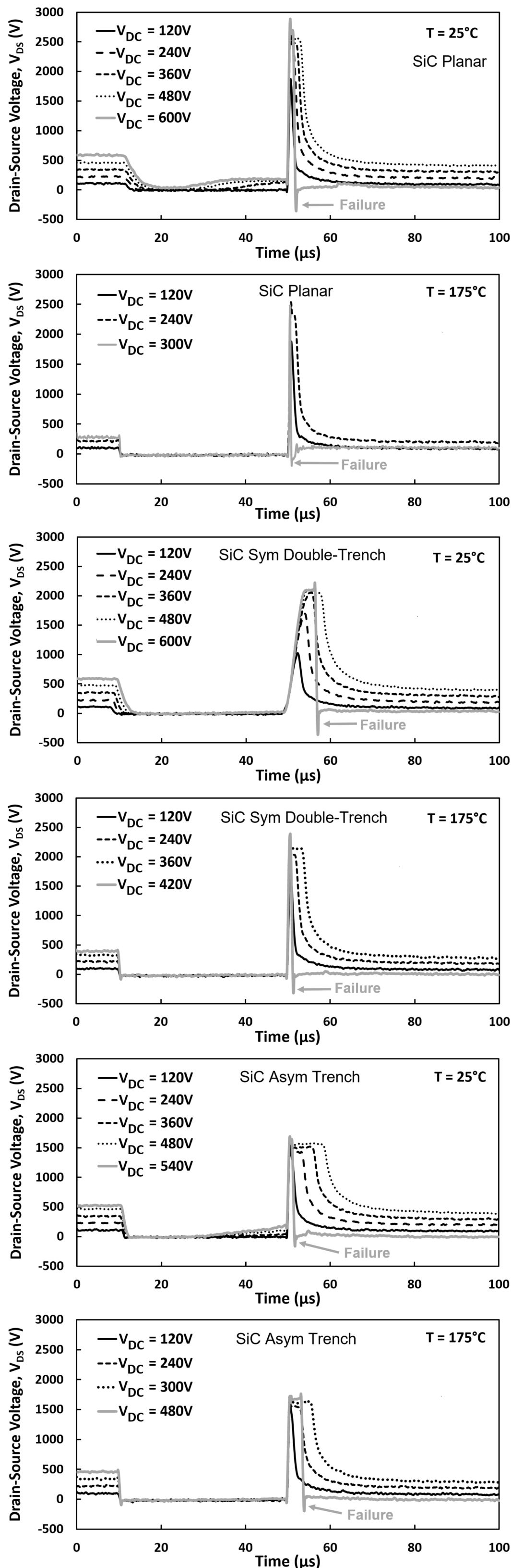

FIGURE 4. **Avalanche drain-source voltage of the three devices for various dc-link voltage until the devices failed at 25 °C and 175 °C.**

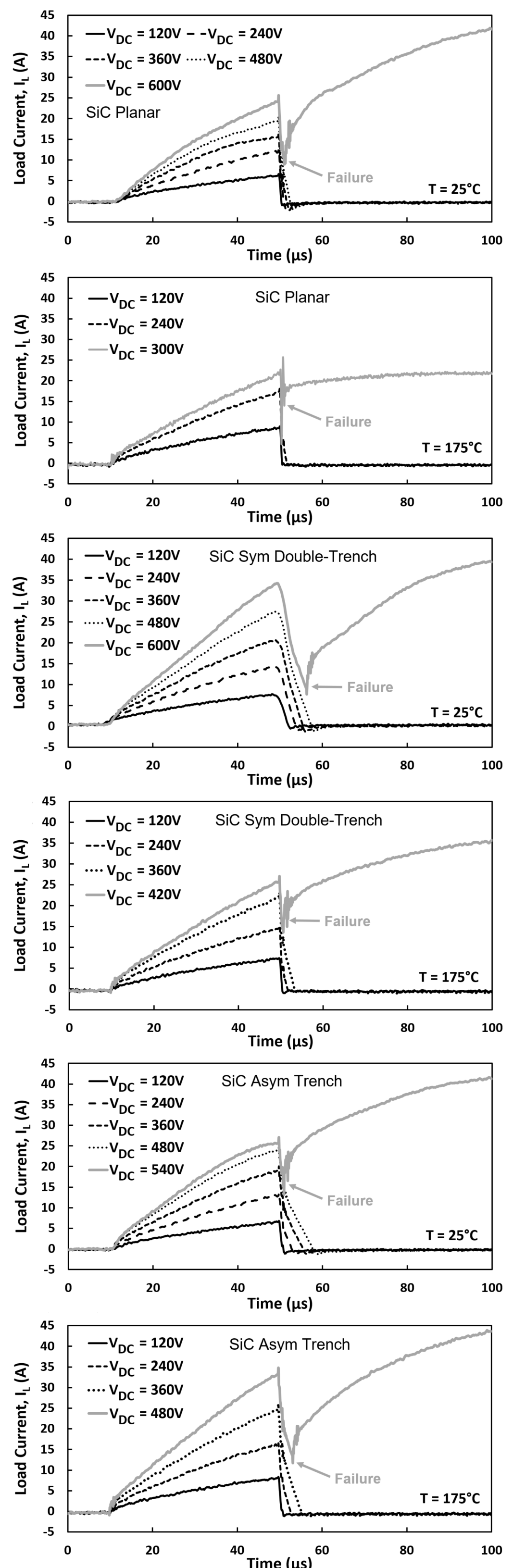

FIGURE 5. **Avalanche load current of the three devices for various dc-link voltage until the devices failed at 25 °C and 175 °C.**

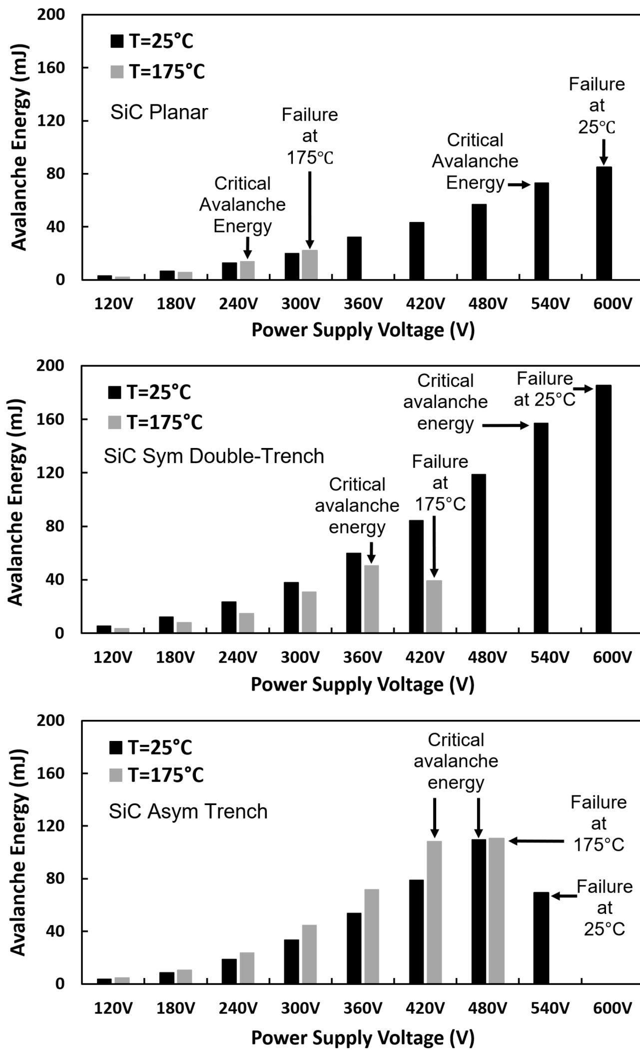

FIGURE 6. Measured UIS avalanche energy of the three DUTs for incrementally increased dc-link voltage at 25 °C and 175 °C, indicating the critical avalanche energy before failure.

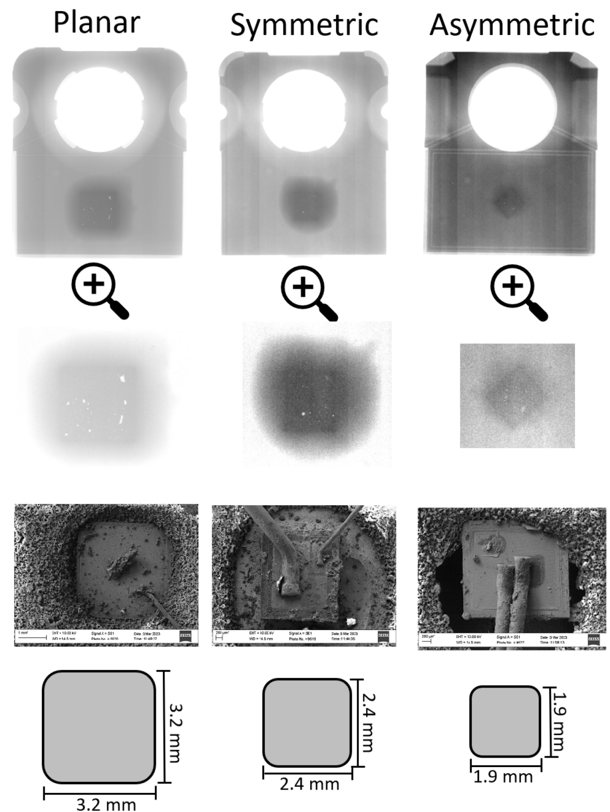

FIGURE 7. Die sizes by CT-scan and the images of the failed cell by scanning electron microscope (SEM) the three SiC power MOSFETs.

horizontally in the P-body region and passes through its resistance R_b, it may result in the voltage drop of V_b between the P-body and the N^+ regions of the source, which if exceeding the built-in voltage PN junction, could lead to latch up of the parasitic BJT with destructive consequences. Therefore, as the temperature increases, due to the positive and negative coefficients of the R_b and voltage drop of V_b, respectively, the BJT could also be triggered earlier.

In Fig. 6, avalanche energy of the three devices are calculated and compared at 25 °C and 175 °C. The avalanche energy here is direct measurements from the experiments rather than theoretical estimations by (1). In order to accurately calculate the avalanche energy, it is crucial to define the boundary time that embraces the entire duration of the avalanche process. The boundary time starts from the initiation of the avalanche event, which is indicated by the onset of the rise in drain-source voltage from almost zero and the simultaneous decrease in the avalanche load current. This boundary time ends when the avalanche load current reaches zero, while the avalanche voltage reaches the peak value. Critical avalanche energy as the maximum avalanche energy that a device can withstand before failure is about 75 and 15 mJ for the planar SiC MOSFET at room temperature and 175 °C, respectively, which is the smallest energy among all three devices. Symmetrical double-trench SiC MOSFET has the largest critical avalanche energy at room temperature which is followed by asymmetrical trench SiC mosfet. However, at high temperature, asymmetrical trench SiC MOSFET can sustain the largest critical avalanche energy.

The die sizes, as shown in Fig. 7, has been measured to determine the avalanche energy density of the devices. Planar SiC MOSFET has the largest die size which has subsequently led to the smallest avalanche energy density at both 25 °C and 175 °C. Asymmetrical trench SiC MOSFET demonstrates the highest avalanche energy density due to the smallest die size which is followed by the symmetrical double-trench SiC MOSFET. Overall, based on the experimental results, at room temperature, the symmetrical double-trench SiC MOSFET exhibits greater ruggedness compared to other devices because of its failure at higher dc-link voltage and its ability to sustain higher critical avalanche energy before failure. At elevated

temperatures, the asymmetrical trench SiC MOSFET demonstrates a higher ruggedness. The avalanche energy density of the planar device is smallest given its lower avalanche energy and largest die area, while it is highest for asymmetric trench device at both 25 °C and 175 °C compared with the symmetric double-trench device given its closer avalanche energy and 40% smaller die area.

These avalanche-induced failures are the result of "high energy" avalanche, which as oppose to the "high current" avalanche that leads to failure by hot-spotting, leads to failure by total burn-out. During the "high current" avalanche by increased pulse durations, the failure modes can be attributed to BJT latch-up of the MOSFETs, whereas in the "high energy" avalanche, the failure is either by the excessive electric field, or thermal runaway. The electric field failures are a result of punch-through in the body-region, excessive field beyond the critical electric field, or the gate oxide electric field crowding beyond [6], [30]. Failures by thermal runaway are also usually a results to thermal fatigue between the aluminum wire bonds with melting point of 933 K [36], and the source pads [6]. To investigate the exact mechanism of failure, and the differences with the "high current" avalanche, TCAD modeling are performed.

III. VALIDATION OF DEVICE TCAD MODELS

First, the device models are developed based on existing device parameters reported by manufacturers in published literature. For unknown parameters, reasonable values are selected, and the static performance of the device models in terms of the output and transfer characteristics are compared with the reposted values by their datasheets.

A. TCAD APPROACH

The failure mechanisms of each device under "high energy" UIS is studied by comprehensive simulations of the single-pulse UIS test has been performed using Silvaco TCAD software. Fig. 9 demonstrates the typical avalanche operation waveforms in which drain-source voltage is equal to V_{DD} in turn-OFF mode, then it increases to the breakdown voltage value $V_{\mathrm{BD}(eff)}$ during the UIS event. Notably, the actual breakdown voltage, $V_{\mathrm{BD(eff)}}$, during single-pulse UIS events exceed the rated breakdown voltage of the device, $V_{\mathrm{BD(DSS)}}$, by approximately 60% [37]. In order to provide an insight into the physical properties of the devices, four points have been identified to represent the operational modes of turn-ON, Avalanche mode, postavalanche, and heat dissipation, respectively. Three main parameters, electric filed, total current density, and lattice temperature have been captured in these four points both before and after failure by avalanche to aid discussion. Point 1 in Fig. 9 is at the point where current is ramping up, but the avalanche has not occurred yet. This is included to provide a baseline for the level of current distribution and electric field prior avalanche. Point 2 is immediately after the turn-OFF where the voltage rises to

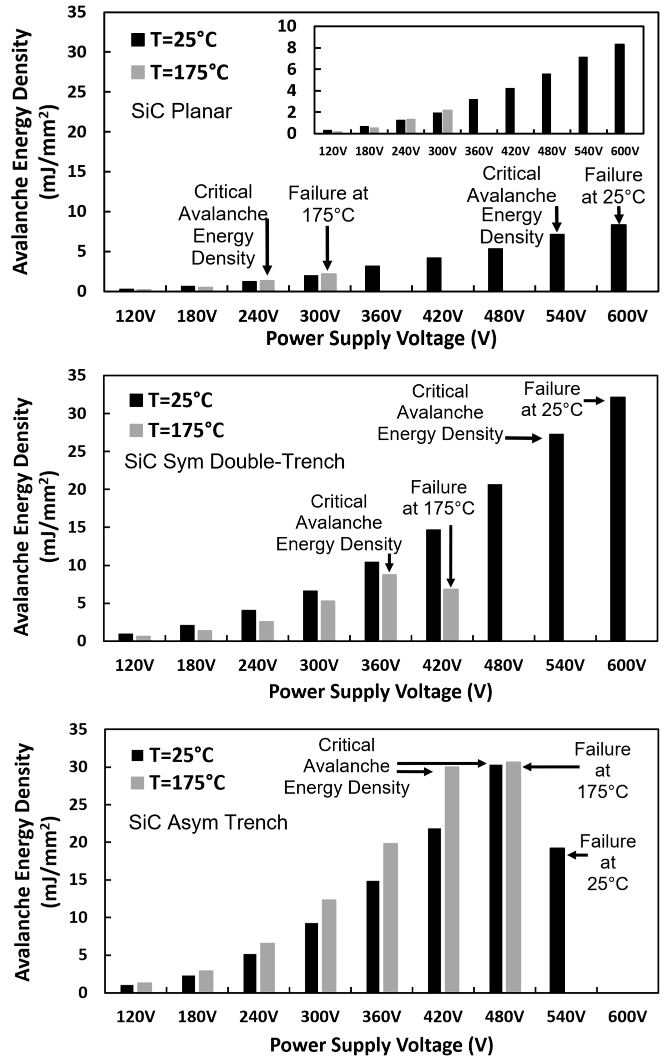

FIGURE 8. Measured UIS avalanche energy density of the three DUTs for incrementally increased dc-link voltage at 25 °C and 175 °C, indicating the critical avalanche energy density before failure.

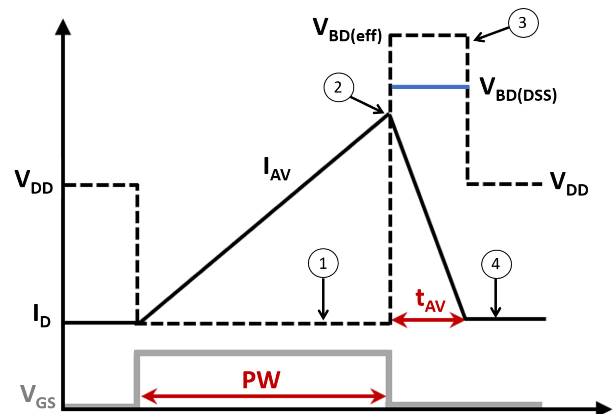

FIGURE 9. Four test points of UIS transient analysed by TCAD models.

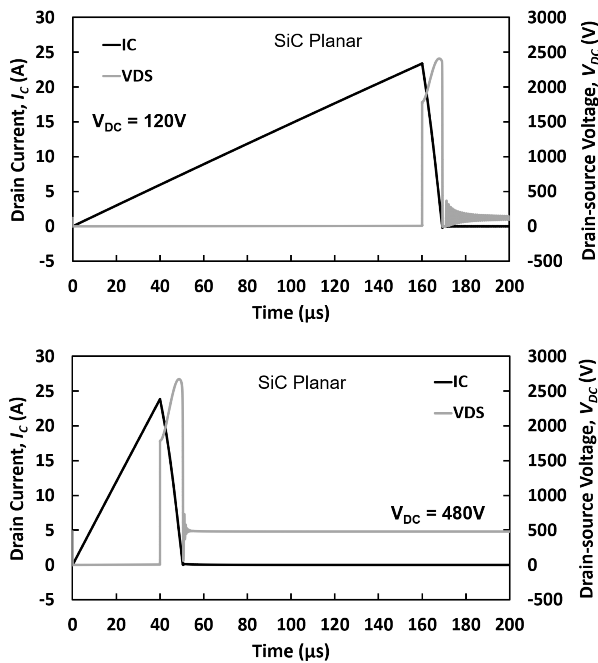

FIGURE 10. TCAD-modeled UIS voltage and current transients of SiC planar MOSFET with V_{DC} of (top) 120 V and (bottom) 480 V, with various pulse lengths and same avalanche current peak.

the avalanche peak and current in the DUT starts to drop. The DUT suffers the highest electrical stress at this point, but its temperature is still low. Point 3 is at the point where current into the transistor approaches zero, while the voltage is still at the avalanche peak. At this point, the stress is under the highest thermal stress as heat has accumulated in the DUT. Finally, point 4 is selected at a time the voltage across the device is back V_{DC}-link while current is at zero.

The avalanche rating to failure of the similarly-rated SiC power MOSFETs in Planar have been investigated through incremental increase of the dc-link voltage while the gate pulse length is kept fixed as through this approach not only a high avalanche current is induced in the device, but also a high voltage and electric field density in generated. The experimental results, depicted in Figs. 4 and 5, reveal an evident increase in both avalanche current and avalanche voltage as the dc-link voltage is raised. To further validate the impact of the dc-link voltage on these parameters, TCAD simulation has been conducted on a SiC planar MOSFET with dc-link voltages of 120 and 480 V, as illustrated in Fig. 10. Given the pulse duration in the case of $V_{DC} = 120$ V is 4 times longer than the case of 480 V, the peak of the avalanche current in both cases is 25 A, while the peak of the avalanche voltage in the case of $V_{DC} = 480$ V is about 300 V higher. These results demonstrate that even when the current is kept constant, varying the dc-link voltage increases the avalanche voltage and, subsequently, the electric field density.

TABLE 1. Key Parameters in TCAD Models of Assessed SiC MOSFETs

Device Type	Planar	Symmetric DT	Asymmetric T
Cell Width (μm)	10	4	3.1
Gate Oxide Thickness (nm)	50	75 (sidewall) 100 (bottom)	75 (sidewall) 100 (bottom)
N-Drift Thickness (μm)	14	11	10
Doping of N-Drift (cm^{-3})	7×10^{15}	8×10^{15}	5×10^{15}
Doping of N^+ (cm^{-3})	6×10^{19}	5×10^{19}	1×10^{19}
Doping of P-base (cm^{-3})	5×10^{17}	6×10^{17}	3.5×10^{17}
Doping of P-well (cm^{-3})	–	–	1×10^{19}
Doping of N^+ Substrate (cm^{-3})	1×10^{19}	1×10^{19}	5×10^{19}

B. TCAD VALIDATION

In order to validate the models used in TCAD simulations, and to confirm that the structure models can indeed represent the actual devices, comparisons are performed between the static electrical characteristics of the modelled devices and the measurements on the devices based on their datasheets. The doping density and thickness of the drift region are determined adequately in order to ensure that the devices modeled can withstand the 1.2 kV breakdown voltage stated by the datasheet.

The dimensions and doping profiles of the devices utilized in Silvaco TCAD simulation are outlined in Table 1. Although these parameters may not perfectly be identical to the real-world devices, they offer valuable insights into the internal physics of the devices. Notably, these parameters have proven reliable, resulting in model outputs that closely resemble the transfer and output characteristics depicted in the manufacturers' datasheets, as illustrated in Figs. 11–13.

Figs. 11 and 12 depict the comparison of the transfer and output characteristics of the TCAD model and actual device of planar and symmetrical double-trench MOSFET, respectively, for $V_{DS} = 10$V and $V_{GS} = 18$V as per datasheet, while Fig. 13 shows the IV characteristic comparison for Asymmetrical trench MOSFET for $V_{DS} = 20$V and $V_{GS} = 18$V. The model outputs are close enough to datasheets to warrant further analysis of device performance under the "high energy" dynamic avalanche.

The UIS test simulations are conducted in the SILVACO TCAD mixed-mode circuit simulation suite. The electrical condition in the simulation is the same as the experiment: $V_{GS} = 18$V, and $t_{PW} = 40$ μs. According to the datasheets, thermal resistance is 0.7, 1.12, and 1.2 K/W for planar, symmetrical double-trench and asymmetrical trench SiC MOSFETs, respectively. Accordingly, for all devices, the thermal boundary in the simulation is set from the top of the N-channel region to the bottom of the drain electrode with their specified junction-to-case thermal resistance. The ambient temperature is set to be 300 K for the room temperature test. Moreover, the temperature coefficients of thermal conductivity and thermal capacitance of the SiC material are considered according to [38], [39].

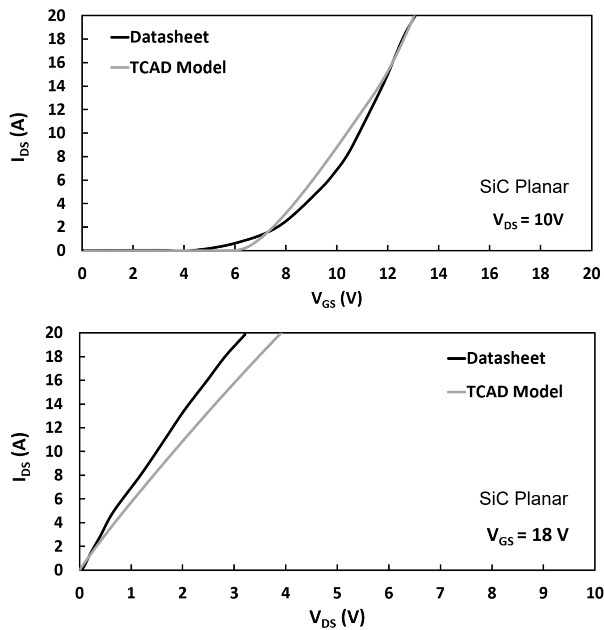

FIGURE 11. TCAD Modeling and measurement of *IV* characteristics of SiC planar MOSFET for $V_{DS} = 10$ V and $V_{GS} = 18$ V as per datasheet. The model is subsequently used for analysis of failure mechanisms.

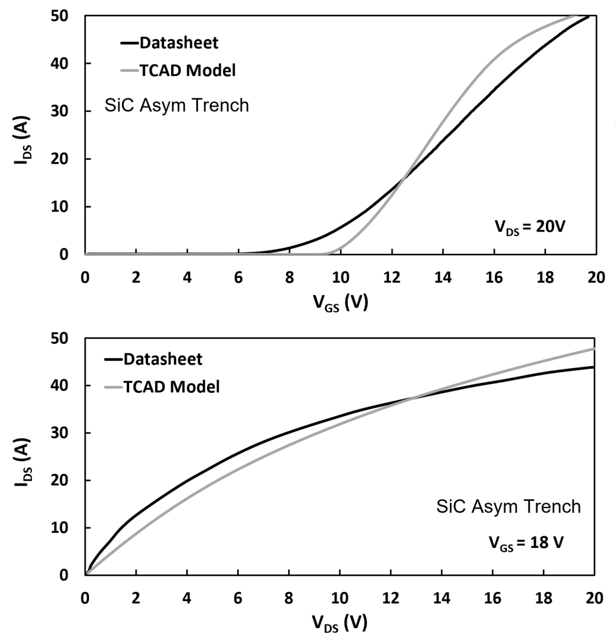

FIGURE 13. TCAD Modeling and measurement of *IV* characteristics of SiC asymmetrical trench MOSFET for $V_{DS} = 20$ V and $V_{GS} = 10$ V as per datasheet. The model is used for analysis of failure mechanisms.

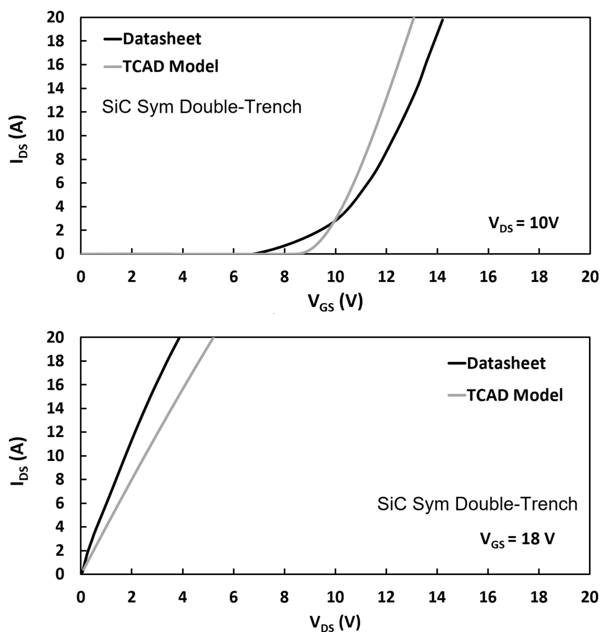

FIGURE 12. TCAD Modeling and measurement of *IV* characteristics of SiC symmetrical double-trench MOSFET for $V_{DS} = 10$ V and $V_{GS} = 18$ V as per datasheet. The model is used for analysis of failure mechanisms.

IV. TCAD ANALYSIS OF "HIGH ENERGY" AVALANCHE

The measurements are analyzed with TCAD models for the three device structures under the "high energy" avalanche in mixed-mode simulations using the validated device models discussed above. For each device, two scenarios of before failure, and at failure, are discussed, with each scenario showing the current density, electric field, and lattice temperature as indicative parameters at the four points shown in Fig. 9.

A. PLANAR SIC MOSFET PRIOR FAILURE AT CRITICAL UIS ENERGY

The TCAD modeling and measurement of the drain-source voltage and current of planar SiC MOSFET under avalanche before failure are compared as per Fig. 14. The circuit parameters used in the mixed-mode simulation are identical to that of experimental measurements. The dc voltage of $V_{dc} = 480$V has been applied to the device at room temperature. As depicted in Fig. 14, the drain-source voltage increases to up to 2300 V during avalanche, and the peak avalanche current increases to 24 A. The three important parameters, electric field, total current density, and lattice temperature have been captured. Due to the slight differences between the datasheet and the output of Silvaco TCAD models, owing to the imperfections of the models that reflected the slight errors in Figs. 11–13, there are some differences in avalanche transients with measurements as well. For example, it can be seen that the avalanche duration and voltage peak in measurements is slightly different than the model output in planar device, i.e. Fig. 14, while these will be closer in the two trench devices. These differences although are not ideal, but will not make impact the analysis of the overall mechanism of avalanche toward failure in each case.

Electric field distribution is shown Fig. 15. It must be noted that in analysis of the electric field the junction terminations is not considered in the model to focus solely on the mechanism of UIS in the active area of each single cell device. It can

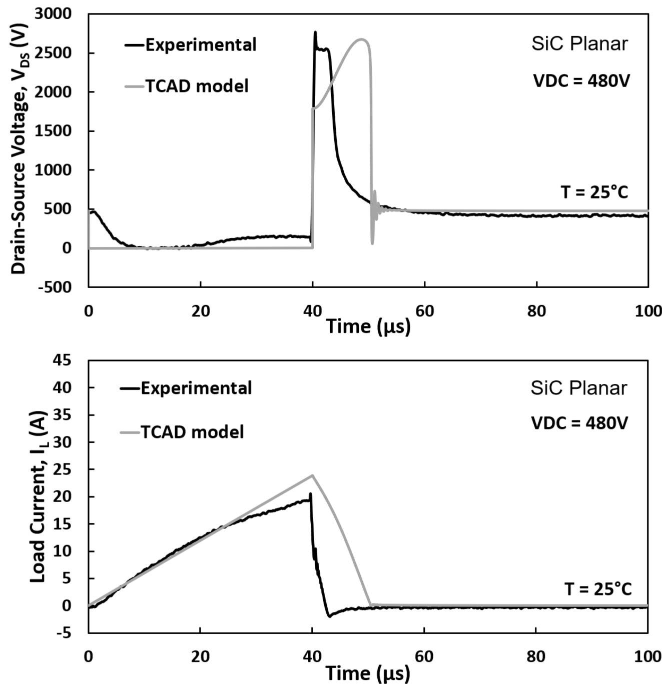

FIGURE 14. TCAD Modelling and measurement of the drain-source voltage and current of the planar SiC MOSFET under avalanche prior failure at critical UIS energy.

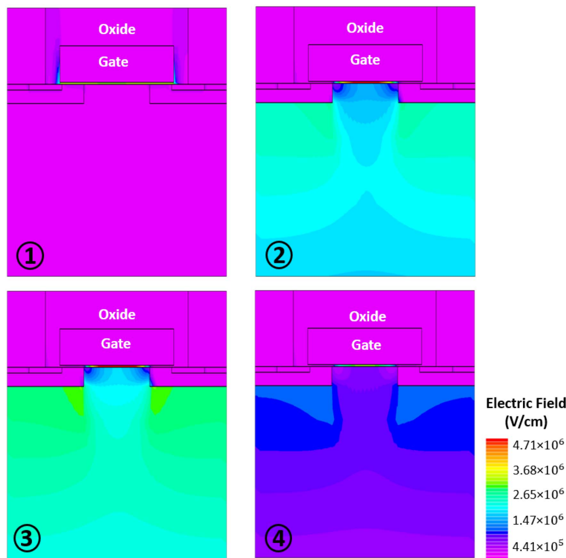

FIGURE 15. Electric field distribution of SiC planar MOSFET prior failure at critical UIS energy.

be seen that in the first point, as the gate voltage is applied, an inversion layer is formed underneath the gate oxide and electric field is distributed linearly in the gate oxide and then extended in the channel region. Then, in point 2, as the gate voltage is turned OFF the device enters the avalanche mode and a high concentration of electric field is formed under and in the corners of the P-body region, which indicates the conductivity

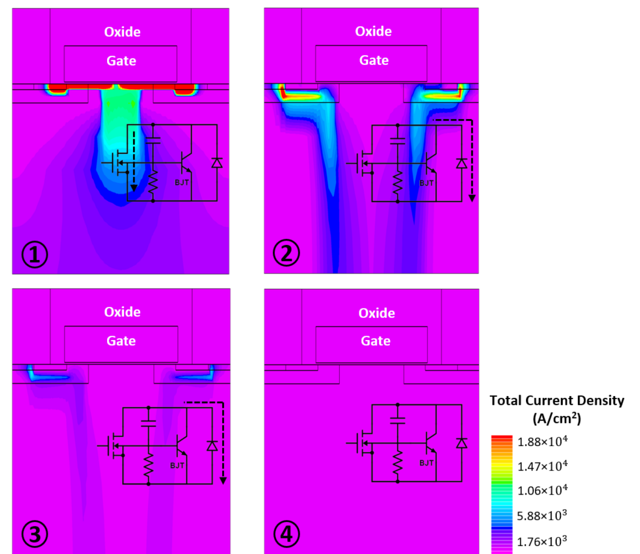

FIGURE 16. Drain Current distribution of SiC planar MOSFET prior failure at critical UIS energy.

of the body diode. Next, drain-source voltage reaches the maximum amount in point 3 while the drain current is reducing. In this point, the electric field increases to its maximum with uniform distribution throughout the device. Finally in point 4, after avalanche event has completed, the electric field reduces remarkably across the P-body and N-drift junction and the device is restored to its nominal state.

Fig. 16 demonstrates the total current density of the device before failure. As the gate voltage is applied to the device, the total current density increases in the channel, so the drain current increases gradually until the channel becomes fully conductive and the current density expands toward the drain region of the device. Following the observation in Fig. 15, as the electric field density increases sharply in point 2, a large current starts flowing vertically from drain to source region through the body diode. In a normal condition when the MOSFET is in the OFF-state mode, because the depletion region is created across the PN junction, just a small reverse leakage current passes through the body diode. However, when the applied reverse voltage across the diode exceeds its breakdown voltage as in the point 3, the reverse current increases dramatically and diode enters the avalanche breakdown. During this process, a part of the current flows horizontally in the P-body region and pass through its resistance R_b and brings about a voltage drop of V_b between the P-body and the N^+ region of the source. It is worth mentioning that this horizontal current flow path in the P-body region in phases 2 and 3 can be attributed to the combination of higher doping concentration and electric field distribution. The electric field distribution in the device depends on the applied voltage and doping density. In Fig. 15, the electric field is mainly concentrated near the edge of the depletion region and regions with higher doping density. Accordingly, the electric field is more pronounced near the edge of the p-base region resulting in horizontal current flow. In this level of the applied voltage, the voltage

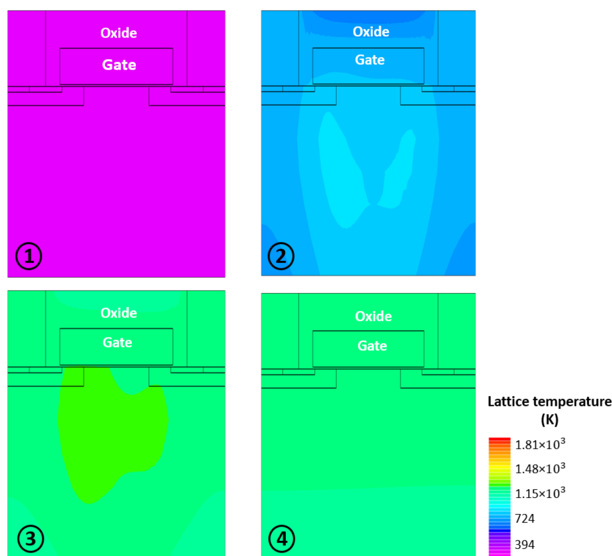

FIGURE 17. **The lattice temperature distribution of SiC planar MOSFET prior failure at critical UIS energy.**

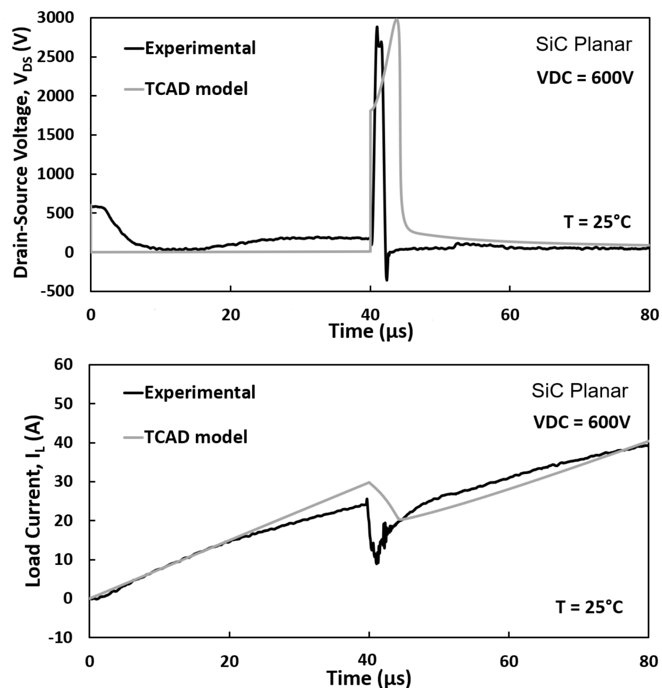

FIGURE 18. **TCAD modeling and measurement of the drain-source voltage and current of the planar SiC MOSFET under avalanche at failure.**

drop does not exceed the built-in voltage of PN-junction. In point 3, the drain current starts to reduce gradually and finally it decreases to a great point after avalanche event as in point 4.

According to Fig. 17, lattice temperature is relatively low in point 1, but in point 2, as avalanche event starts the lattice temperature increases notably that is attributed to the high concentration of electric field across the P-body N-drift junction together with a high current density flowing through the junction. In point 3, the electric field reached its maximum which results in generation of additional heat throughout the device especially across the PN junction. In the last step, the lattice temperature becomes lower and more uniform compared to the avalanche event because of heat dissipation.

B. PLANAR SIC MOSFET AT FAILURE

Fig. 18 shows a comparison between experiment and TCAD model in terms of drain-source voltage and load current of the planar device at failure by "high energy" avalanche. By applying $V_{DC} = 600$V in simulation, drain-source voltage and load current reach 2500 V and 30 A, respectively, and the device enters avalanche failure as was the case in the experiments. The electric field, total current density, and lattice temperature distribution are depicted in Figs. 19–21.

Before avalanche starts, the distribution of the three parameters are the same as that of the "before failure" case presented in previous section. As avalanche starts in point 2, a high density of electric filed is formed primarily in the junction of the P-body and N-drift regions and avalanche current starts flowing through intrinsic body diode from drain to source regions of the Planar SiC MOSFET. As this current reaches a maximum, the lattice temperature increases rapidly especially at the edges of the PN junctions. In point 3, the electric field reaches the maximum in the PN junction and current starts

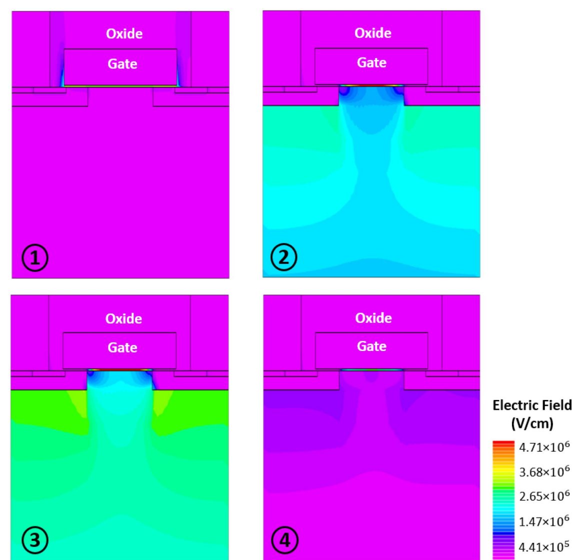

FIGURE 19. **Electric field distribution of SiC planar MOSFET at failure.**

reducing to a point and then increases again resulting in a considerable temperature rise underneath the PN junctions and device enters avalanche failure as depicted in point 4.

The failure in SiC planar device happens at the beginning of the avalanche process, when the peak electric field is at its maximum for both cases of 25 °C and 175 °C avalanche. During "high current" avalanche, the parasitic BJT latches-up together with consequences of the thermal runaway. In the case of "high current" avalanche, the high avalanche current

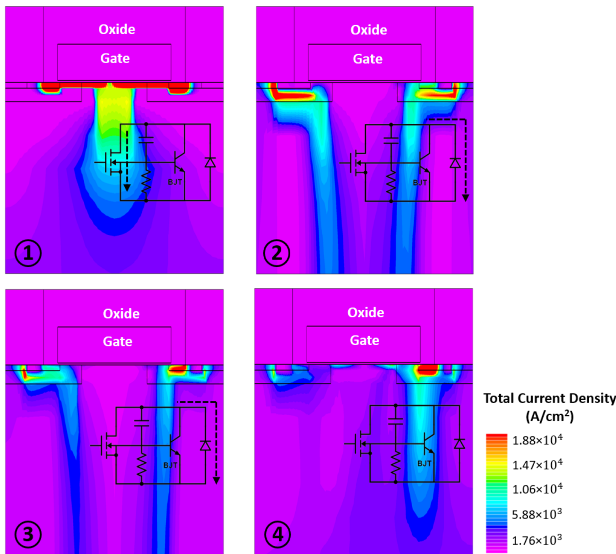

FIGURE 20. Drain current distribution of SiC planar MOSFET at failure.

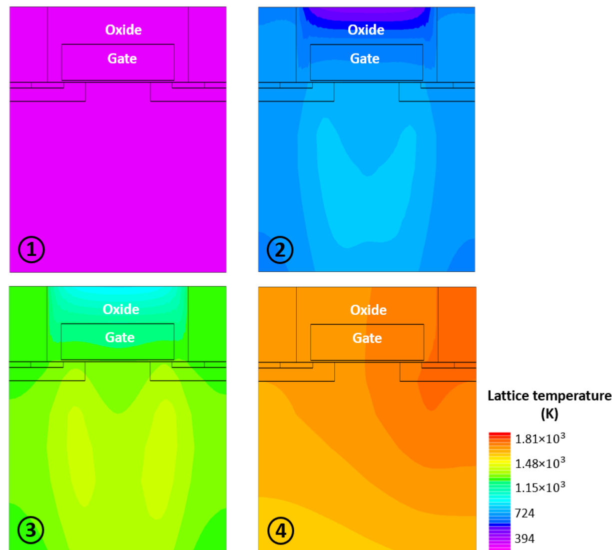

FIGURE 21. Lattice temperature distribution of SiC planar MOSFET at failure.

that flows vertically through the PN junction passes toward the source region horizontally and this can induce a voltage drop of V_b by R_b and subsequent thermal runaway. This would be followed by formation of a hot spot. However, in the "high energy" avalanche observed here, the planar device has failed before reaching such high level current. This indicates that the failure has been through high electric field concentration at the gate oxide. This is verified by the short-circuit detected on the gate and source terminals of the device. At elevated temperature, the same mechanism is observed at even lower load current. At high temperatures, the gate oxide interface traps are less likely to be occupied as the charges are released [2], which leads to a gradual change in failure mode from oxide rupture to thermal fatigue, which combined with the elevated

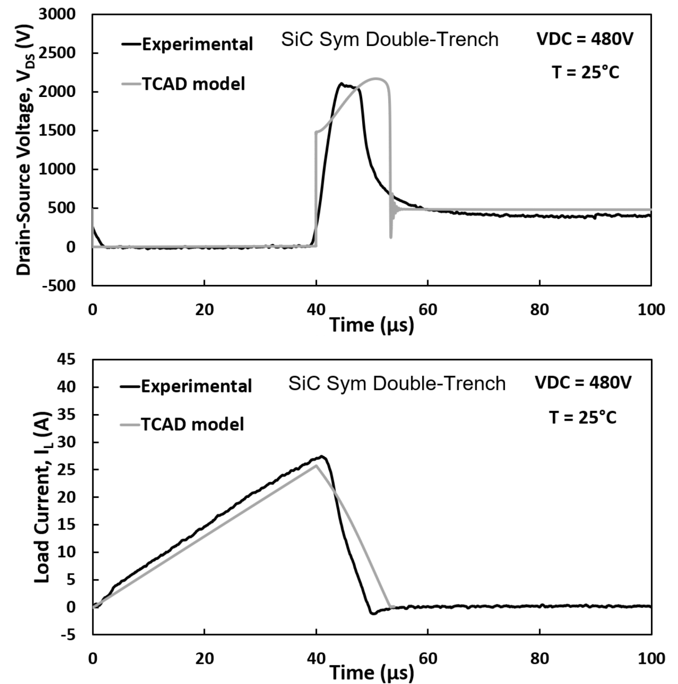

FIGURE 22. TCAD modeling and measurement of the drain-source voltage and current of the symmetric trench SiC MOSFET under avalanche prior failure at critical UIS energy.

case temperature of 450 K compared with Al wire-bond melting point of 933 K leads to thermal fatigue and failure as in Fig. 20. The postfailure asymmetry in the current path seen in point 4 in Fig. 20 can be attributed to the mechanism of BJT latch-up leading to thermal runaway in either of the two P-base regions in device cell. The visual may also slightly vary depending on exact time frame selected to capture the cross-section.

C. SYMMETRICAL DOUBLE-TRENCH SIC MOSFET PRIOR FAILURE AT CRITICAL UIS ENERGY

Fig. 22 demonstrates a comparison between the experimental and TCAD model of symmetrical double-trench SiC MOSFET before failure at room temperature. The results in terms of drain-source voltage and load current are close to each other. Figs. 23–25 show the distribution of the electric filed, total current density and lattice temperature at four different points before failure, respectively.

The distribution of electric field in point 1 is the same as the case in the planar SiC MOSFET, but in point 2 it is seen that the electric field is primarily concentrated at the bottom of the gate oxide and P-well trench region and it reaches its maximum in point 3 leading the drain-source voltage to reach its peak. After the avalanche event, electric field begins to reduce significantly in point 4.

In Fig. 24, it is evident that the distribution of the total current density is uniform explained by the symmetric structure of the device. Path of the current in point 1 is also the same as the planar MOSFET and it flows through the channel and N-drift

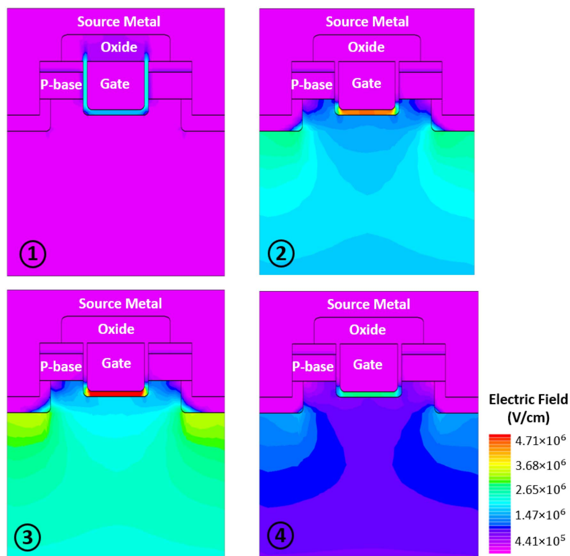

FIGURE 23. Electric field distribution of symmetrical double-trench SiC MOSFET prior failure at critical UIS energy.

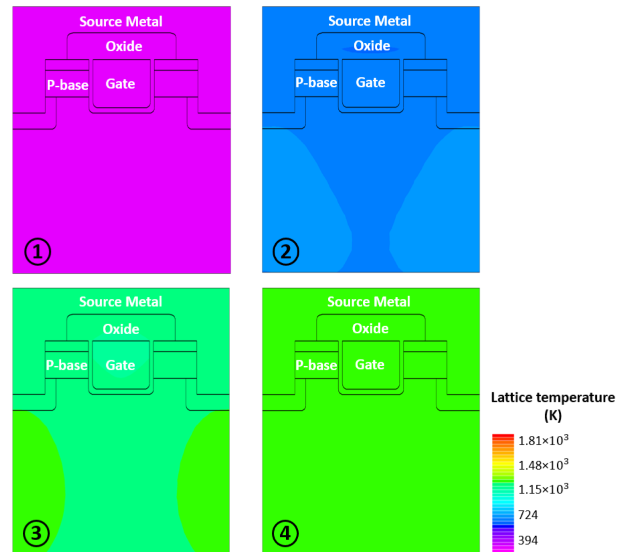

FIGURE 25. Lattice temperature distribution of symmetrical double-trench SiC MOSFET prior failure at critical UIS energy.

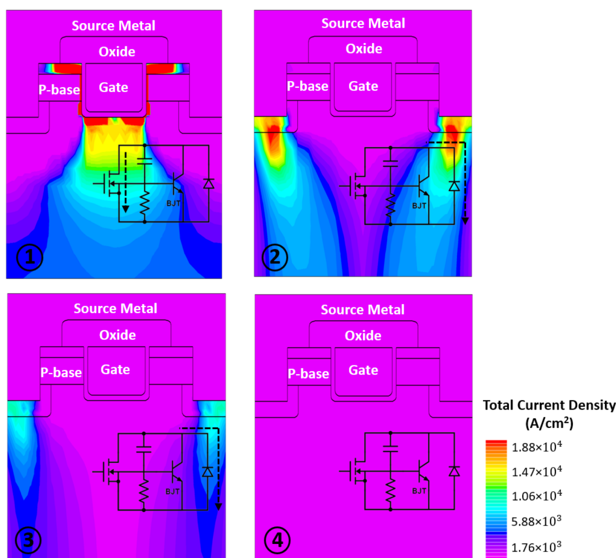

FIGURE 24. Drain Current distribution of symmetrical double-trench SiC MOSFET prior failure at critical UIS energy.

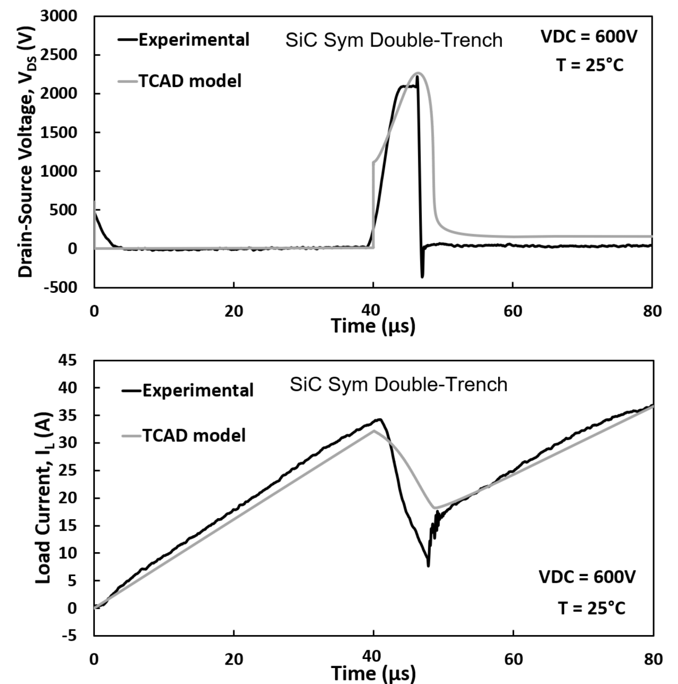

FIGURE 26. TCAD modeling and measurement of the drain-source voltage and current of the symmetric double-trench SiC MOSFET under avalanche after failure.

region. As the device enters the avalanche event by increasing the applied reverse voltage, the P-well N-drift junction of the device opens and the path of current changes from channel to the PN-junction. Then, the current starts to decrease in point 3 until finally in point 4 the drift region it will become devoid of charge carriers. According to Fig. 25, the lattice temperature distribution as well as current distribution is symmetric and the hot-spots form in the junction of P-well trench and N-drift region junctions in point 2 and 3 as the current flows through it.

D. SYMMETRICAL DOUBLE-TRENCH SIC MOSFET AT FAILURE

The drain-source voltage and load current of experimental results and TCAD model of symmetrical double-trench MOSFET in failure mode have been compared based on Fig. 26. Electric field, total current density, and lattice temperature distribution have been reflected in Figs. 27–29, respectively.

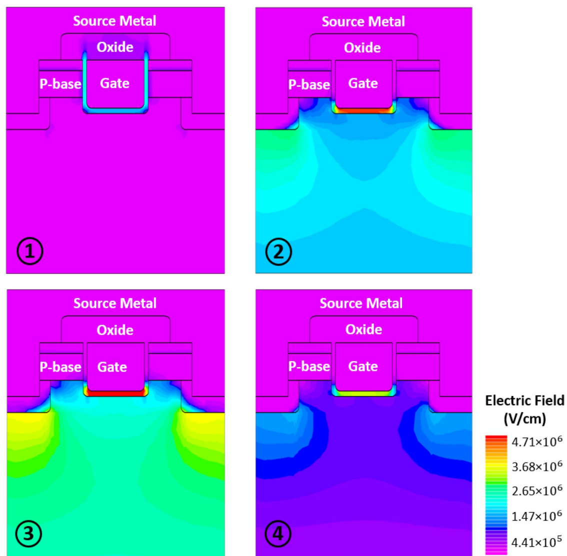

FIGURE 27. Electric field distribution of symmetrical double-trench SiC MOSFET at failure.

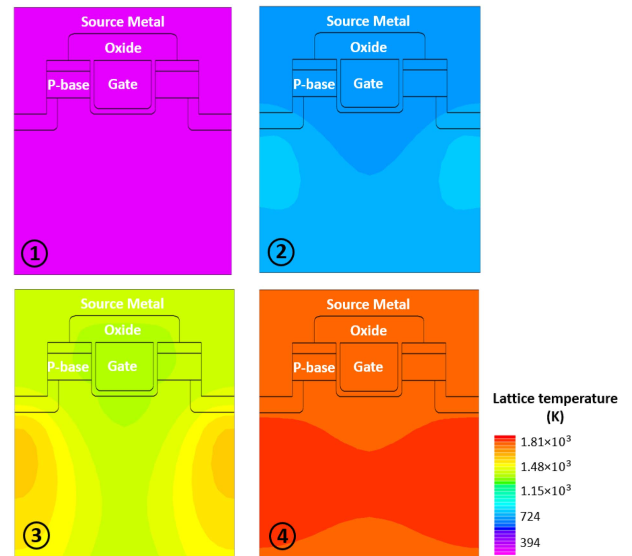

FIGURE 29. Lattice temperature distribution of symmetrical double-trench SiC MOSFET at failure.

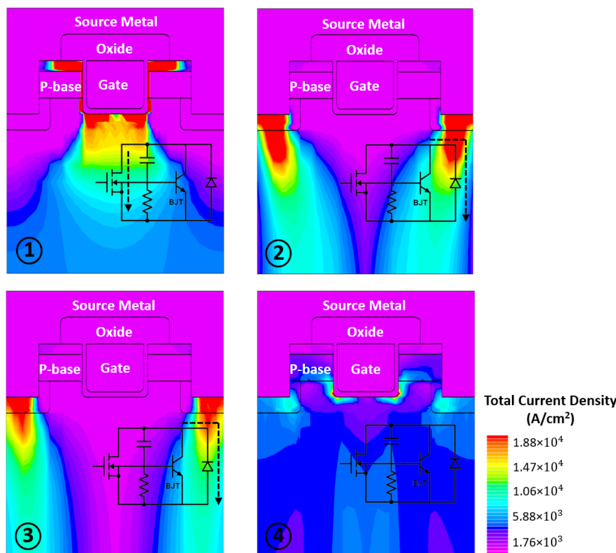

FIGURE 28. Drain Current distribution of symmetrical double-trench SiC MOSFET at failure.

In the failure mode, as higher voltage is applied to the device, the electric field concentration is increased at the base of the gate oxide and P-well trench region in point 2 and 3 of Fig. 27 compared to prefailure avalanche event. The overlap of the high density of current that flows vertically through PN-junctions and the high voltage across them results in creation of very hot spots at those regions based on Fig. 29. Eventually, in point 3 the device enters the avalanche failure mode by increasing the current abruptly until in point 4 device fails.

Majority of the current flows vertically through the PN-junction, reducing likelihood of activation of the parasitic BJT. Therefore, parasitic BJT latch-up cannot be considered as a failure mechanism in symmetrical double-trench MOSFET. Two main factors can be raised for the failure mechanism which are the gate oxide degradation and thermal runaway. Effectively, in symmetric double-trench device, failure happens toward the end of the avalanche process at 25 °C, suggesting failure by thermal runaway together gate oxide rupture, and earlier in 175 °C due to the reduced headroom at elevated temperatures. Here, the base and corners of the gate trench suffer from lack of proper protection, as those regions are subject to high concentration of electric field compared to other regions that can result in hot carrier injection generated by impact ionization into the gate oxide. This phenomenon can affect the gate by trapped charges, interface states which can cause shifts in the threshold voltage, increased gate leakage current, and degradation by early gate oxide breakdown. However, by increasing the temperature of the case of symmetrical double-trench MOSFET, the failure mode will evolve into thermal runaway as the primary destructive force with thermal fatigue on wire-bonds and source pads/electrodes. This phenomenon can be explained by the reduction of the charge in the interface states [2], [40], [41] at higher temperatures, generating enough energy for the trapped charge to be released. This is in-line with the observation that in “high energy;; avalanche, as in Fig. 4, the peak electric field was the maximum for SiC planar, reduced for SiC symmetrical double-trench, and minimum for SiC Asymmetric trench device. In contrary, the period of the avalanche process in planar structure is minimum, increased for SiC symmetrical, and maximum for SiC asymmetric. The avalanche energy of the planar device is the lowest when failure occurs as the issue if

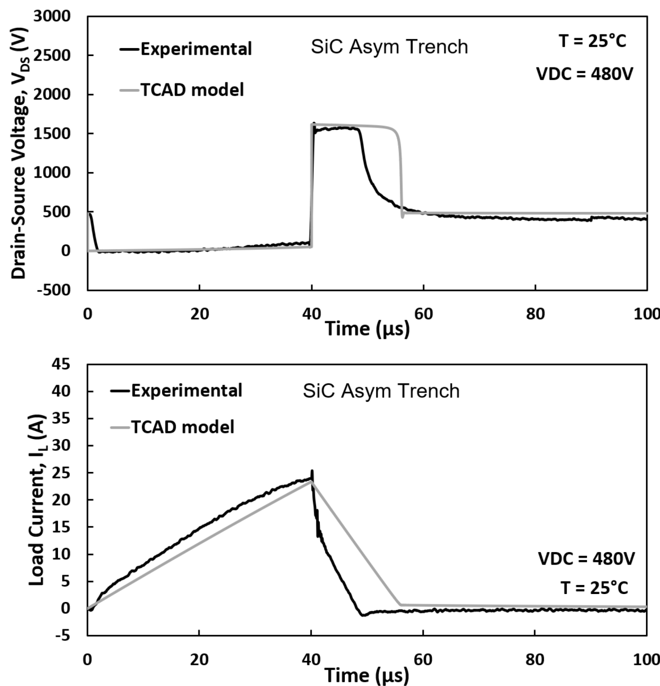

FIGURE 30. TCAD modeling and measurement of the drain-source voltage and current of the asymmetric trench SiC MOSFET under avalanche prior failure at critical UIS energy.

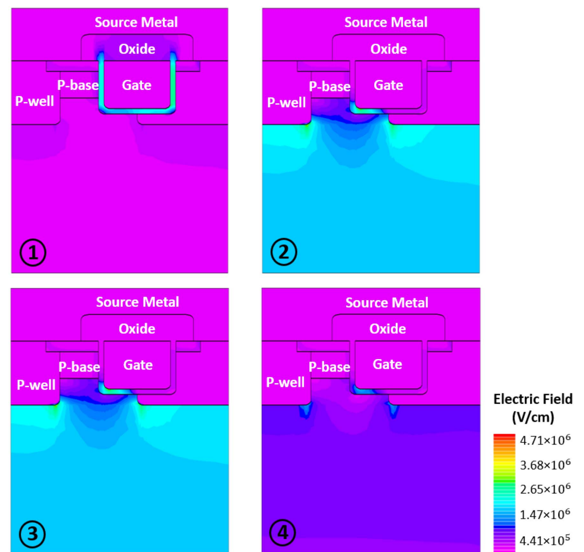

FIGURE 31. Electric field distribution of asymmetrical trench SiC MOSFET prior failure at critical UIS energy.

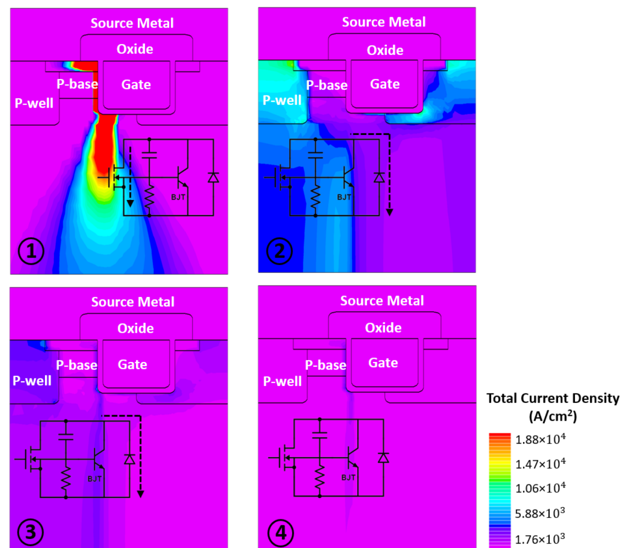

FIGURE 32. Drain current distribution of asymmetrical trench SiC MOSFET prior failure at critical UIS energy.

the gate oxide rupture. The avalanche energy at room temperature, as shown in Fig. 6 is also the highest for SiC symmetric double-trench device, while at elevated temperature of 175 °C is highest for the asymmetric trench device. This suggests that the failure mode in the symmetric double-trench device at low initial temperature is less heat-dependant and more reliant on peak electric field damaging the gate oxide, while as temperature increases the failure mode becomes thermal runaway.

E. ASYMMETRICAL TRENCH SIC MOSFET PRIOR FAILURE AT CRITICAL UIS ENERGY

Experimental results and TCAD model of asymmetrical trench MOSFET before failure have also been compared to each other in Fig. 30 and similarity of the results confirm that the model is close to the real device. Based on the distribution of electric field inside the device shown in Fig. 31, it can be seen that the electric field is concentrated mainly in the channel region and the gate oxide as the gate voltage is applied to the device in point 1.

Unlike symmetrical double-trench SiC MOSFET, in asymmetrical trench SiC MOSFET, one of the side-wall trenches is designed to be used as the field plate structure in order to increase the breakdown capability of the device by protecting the bottom of the gate oxide of excessive electric field. Moreover, in real device the left trench orientation is aligned with (11-20) crystal plane that takes advantage of higher mobility compared to other crystal planes [21]. Consequently, the current mostly flows from the left side channel of the device in conduction mode as illustrated in Fig. 32. Thereby, the loss of right channel for current conduction can be effectively compensated and asymmetrical trench MOSFET can still attain its high conduction capability [21], [42]. Under avalanche condition in points 2 and 3 of Fig. 31, the electric field is predominately dense on the corner of the P-well region compared to the base of the gate oxide which means that the gate oxide is effectively protected from high electric field by the P-well. In terms of current and temperature in avalanche mode it is evident that the current passes through the P-well N-drift region junction, so the temperature in these points will be increased as in Fig. 33.

F. ASYMMETRICAL TRENCH SIC MOSFET AT FAILURE

Fig. 34 illustrates the comparison results of experiment and TCAD model for asymmetric trench MOSFET at failure.

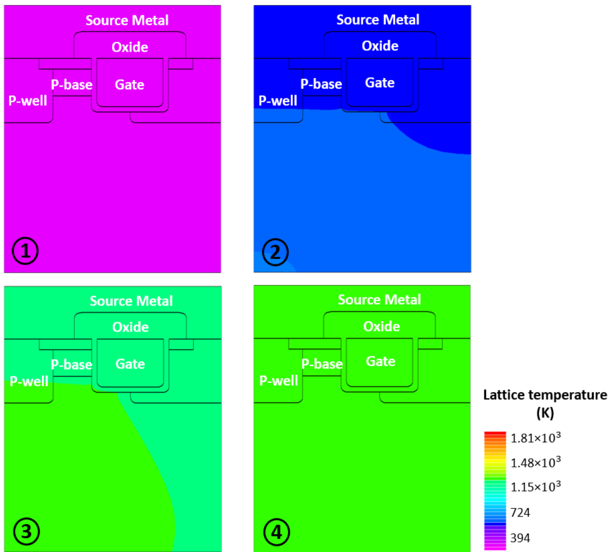

FIGURE 33. Lattice temperature distribution of asymmetrical trench SiC MOSFET prior failure at critical UIS energy.

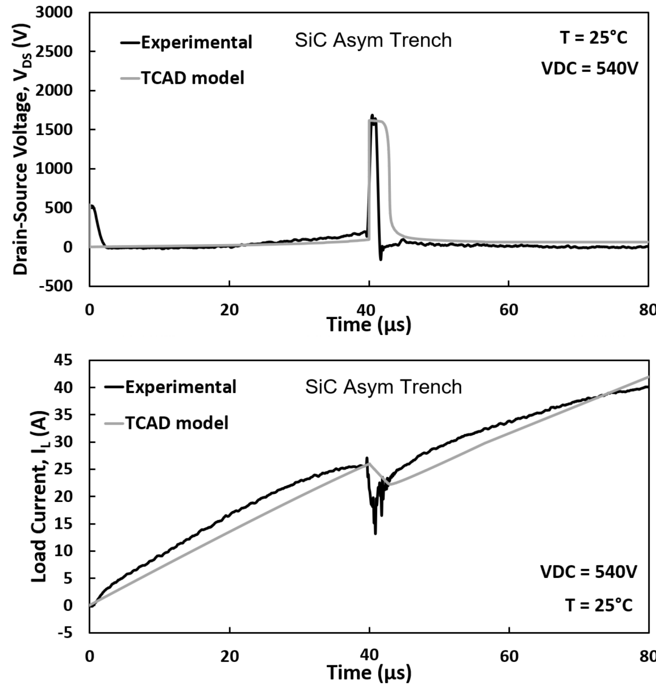

FIGURE 34. TCAD model and measurement of drain-source voltage and current of the asymmetric trench SiC MOSFET in avalanche after failure.

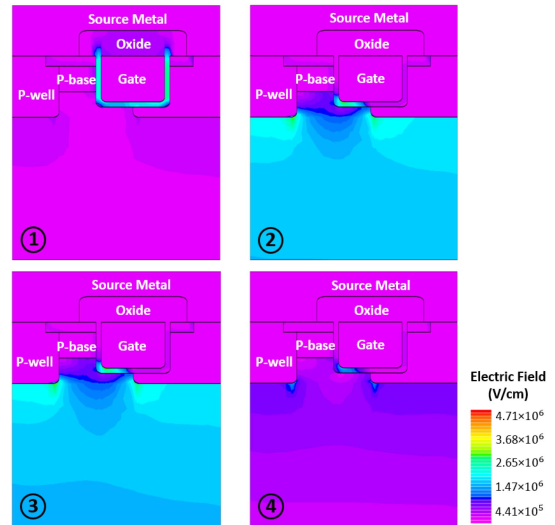

FIGURE 35. Electric field of asymmetrical trench SiC MOSFET at failure.

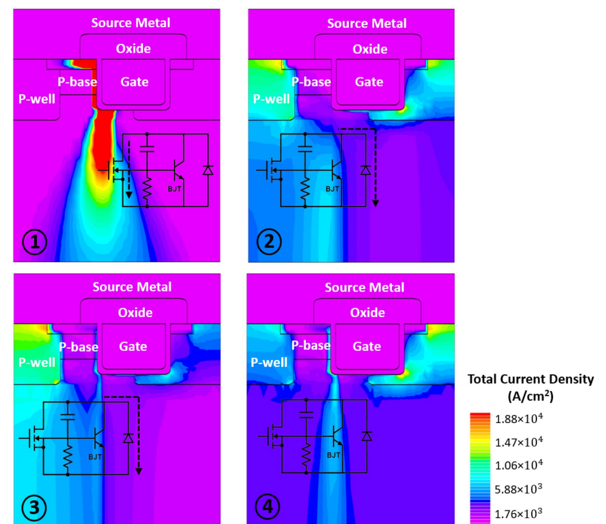

FIGURE 36. Drain current of asymmetric trench SiC MOSFET at failure.

According to point 2 and 3 of Fig. 35, the peak electric field is at the corner and bottom of the P-well region. Unlike the "high current" avalanche observed with low source voltage, and high pulse duration, in which the sole source of failure in asymmetric trench SiC MOSFET was thermal, in the case of "high energy" avalanche, we can observed that failure is after initiation of the avalanche, with a rather short process (compared with the symmetric device) before failure occurs, as in Fig. 4, for both cases of 25 °C and 175 °C. The critical avalanche energy of failure in both cases of 25 °C and 175 °C are also close, as shown in Fig. 6, suggesting independence from the thermal headroom. These combined indicate a different failure mechanism in asymmetric trench SiC MOSFET in the "high energy" avalanche compared with the "high current" avalanche, with the excess electric field (>3 MV/cm) at the gate oxide being a key contributor to the failure, reducing the effectiveness of the P-pillars in protection of the gate oxide. In addition, as depicted in point 2 of Fig. 36, current is mainly flowing through the left side P-well region toward the source region resulting in generation of high temperatures in the junction of the N-drift and P-well regions. Based on the total current density and lattice temperature at avalanche failure mode in Figs. 36 and 37, respectively, the aluminium wire-bonds and pads suffer metal fatigue, with eventual melting when the entire die temperature rises above 933 K [36], especially given its smallest die size shown in Fig. 7.

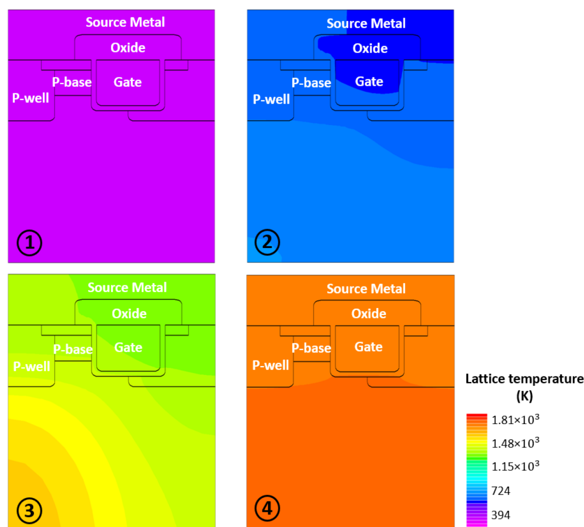

FIGURE 37. Lattice temperature of asymmetric trench SiC MOSFET at failure.

Measurements and simulations have confirmed that the dc-link voltage required for avalanche breakdown toward failure significantly reduced with the rise of temperature. To quantity this, with temperature rise from 25 °C to 175 °C, the dc-link voltage initiating the failure of the planar SiC device reduces to 300 V from 600 V, in symmetrical double-trench drops to 420 V from 600 V, and in asymmetrical trench drops to 480 V from 540 V.

V. CONCLUSION

In this article, a new mechanism for UIS measurements, namely the "high energy" avalanche, is applied to third generation planar, symmetrical double-tench, and asymmetrical trench SiC MOSFETs to evaluate the avalanche and failure mechanism when subject to UIS at high source voltage. As the measurements results indicate, confirmed by TCAD modeling, the failure mechanisms in the "high energy" avalanche by increase of source voltage differ from "high current" avalanche by increasing of load current by prolonged pulse durations. The measurements, supported by TCAD modeling, confirm that in the case of planar SiC MOSFET, the failure during "high energy" avalanche has been through the concentration of the high electric field at the gate oxide leading to leakage by carriers trapped in oxide defects, while in the case of the symmetric double-trench SiC MOSFET, the failure mode at low initial temperature is less heat-dependant and more reliant on peak electric field density damaging the gate oxide, while as the case temperature increases the failure mode moves toward thermal runaway. In the case of asymmetric trench SiC MOSFET, failure is after initiation of the avalanche, with the critical avalanche energy of failure in both cases of 25 °C and 175 °C being close, suggesting independence from the thermal headroom. This means the protection offered by the asymmetric P pillars to the gate oxide is not as effective in the case of "high energy" avalanche compared with the "high current" avalanche, and the failure mechanisms in the "high energy" UIS are in fact closer to failure mechanism in the failure by short-circuit events than "high current" avalanche cases.

DATA STATEMENT

All data supporting this study are provided in full in this article. Specific data of measurements are available with authors at request.

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MANA HOSSEINZADEHLISH (Graduate Student Member, IEEE) received the B.S. and M.Eng. degrees in electrical engineering from the University of Guilan, Rasht, Iran, in 2015, and Sahand University of Technology, Sahand, Iran, in 2019. She is currently working toward the Ph.D. degree in electrical engineering with the Electrical Energy Management Group Laboratory, School of Electrical, Electronic and Mechanical Engineering, University of Bristol, Bristol, U.K.

Her research interests include the performance and reliability analysis of wide-bandgap power semiconductor devices, including silicon carbide unipolar and bipolar power semiconductor devices in power electronics applications.

SAEED JAHDI (Senior Member, IEEE) received the Ph.D. degree in power electronics from the University of Warwick, Coventry, U.K., in 2016.

Formerly, he was with the HVDC Center of Excellence of General Electric, General Electric (GE) Grid Solutions, Stafford, U.K., as a Power Electronics Engineer and Line-Coordinator on several onshore and offshore VSC-HVDC projects in the U.K., Germany, Sweden, France, and Italy. His research interests include wide-bandgap power semiconductor devices in power electronics.

Dr. Jahdi was a recipient of the GE's Early-Career Engineering Award in 2018 for contribution to the success of GE's flagship VSC-HVDC projects. He is currently an Assistant Professor of power electronics with the Electrical Energy Management Group, University of Bristol, Bristol, U.K. He was also a recipient of the 2021 outstanding paper award for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.

XIBO YUAN (Senior Member, IEEE) received the B.S. degree from the China University of Mining and Technology, Xuzhou, China, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2005 and 2010, respectively, both in electrical engineering.

His research interests include power electronics and motor drives, wind power generation, multilevel converters, application of wide-bandgap devices, electric vehicles, and more electric aircraft technologies.

JOSE ORTIZ-GONZALEZ (Member, IEEE) received the B.Eng. degree in electrical engineering from the University of Vigo, Vigo, Spain, in 2009, and the Ph.D. degree in power electronics from the University of Warwick, Coventry, U.K., in 2017.

Since 2013, he has been with the School of Engineering, University of Warwick, Coventry, U.K. He was appointed as a Senior Research Fellow in power electronics in 2018. Since 2019, he has been an Assistant Professor in power electronics. He has authored or coauthored more than 100 publications in journals and international conferences. His current research interests include electrothermal characterization of power devices, reliability, and condition monitoring.

OLAYIWOLA ALATISE (Senior Member, IEEE) received the B.Eng. (first class Hons.) degree in electrical and electronics engineering and the Ph.D. degree in microelectronics and semiconductors from Newcastle University, Newcastle upon Tyne, U.K., in 2005 and 2008, respectively.

In 2004 and 2005, he briefly joined ATMEL North Tyneside where he worked on the process integration of the 130-nm CMOS technology node. In 2008, he joined the Innovation R&D Department, NXP Semiconductors, as Development Engineer, where he designed, processed, and qualified discrete power trench MOSFETs. In 2010, he joined the University of Warwick as Science City Research Fellow to investigate advanced power semiconductor materials and devices for improved energy conversion efficiency. Since 2019, he has been a Professor in electrical engineering with the University of Warwick, Coventry, U.K. His research interests include investigating advanced power semiconductor materials and devices for improved energy conversion efficiency.