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A Versatile Switched-Mode Large-Signal GaN-Based Low-Distortion Arbitrary Waveform Generator

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ABSTRACT In a multitude of industrial and biomedical applications, the need for arbitrary waveform generators is essential, serving the purpose of load characterization and excitation, among others. Historically, these generators have had limitations in terms of voltage, current, and frequency output, primarily related with constraints associated with the power devices and circuit topologies. However, notable advancements in semiconductor technology have introduced a new era, enabling the creation of highly versatile waveform generators capable of superior performance, and extended operational capabilities. In this article, a versatile AWG based on switched modules is proposed. In contrast to the previous ones, whose implementation was based on linear amplifiers, it enables arbitrary waveform generation, higher efficiency, and very low output impedance. In addition, it is also presented as a novelty that the voltage in each of the modules is different, following a digital to analog converter (DAC) structure, which allows us to obtain a lower total harmonic distortion (THD) in the output waveform than with conventional methods. The design will take advantage of wide band gap devices to be able to switch in the MHz range to achieve a high bandwidth. Furthermore, in addition to the design and implementation of a high-performance generator, a comparative analysis between the conventional and the proposed DAC-based modulation pattern is performed based on a comparative analysis of the THD and switching losses.

INDEX TERMS Arbitrary waveform generation (AWGs), gallium nitride power device, inverter, multilevel converter.

I. INTRODUCTION

Today, arbitrary waveform generators (AWGs) are increasingly required in multitude high voltage/high power applications, from the industrial to the biomedical range. Their versatility allows them to be used in many different operating conditions, especially for powering or characterizing loads [1]. Fig. 1 shows some application examples under excitation conditions similar to real conditions. Fig. 1(a) represents the biomedical treatment of electroporation [2], [3], [4], which consists of applying high-voltage pulses to liver tissue with the aim of eliminating cancer cells present in the tissue. Fig. 1(b) shows how the AWG can be used to characterize highly non-linear induction heating loads [5], [6], [7]. In these two applications, highly variable waveforms in large current/voltage ranges are required.

Therefore, given the growth of this type of generators in recent years, a study of the current state of the art has been carried out to be able to analyze in more detail the existing technology gap.

Classically, three approximations to obtain AWGs are considered. High-voltage AWGs can be obtained by amplifying the low-voltage waveform through power linear amplifiers, by using switched topologies such as class-D amplifiers or multi-level converters, or by using a hybrid approach between

(a) (b)

FIGURE 1. Applications of the proposed versatile generator. (a) Electroporation of liver tissue. (b) characterization of induction heating loads.

both strategies. The low efficiency and high load dependence of linear power amplifiers, which imply high losses and correspondingly complex thermal management, make conventional purely analog concepts unsuitable for future high-performance power amplifiers. In spite of this, there are still many commercial high-bandwidth analog amplifiers [8]. Also, by using linear amplifiers, in [9], arbitrary waveforms up to 200 V, 500 mA, and 5 kHz are obtained, and in [10] an AWG able to reach 60 V, 50 mA, and 1 kHz has been developed.

When considering switch-mode amplifiers, in early stages there were systems based on standard two-level [insulated gate bipolar transistor (IGBT-based)] class-D inverters, featuring switching frequencies of around 10 kHz in the range of 10 to 50 kVA, achieving fundamental output frequencies of up to 100 Hz [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]. Higher fundamental output frequencies can be achieved by moving from silicon IGBTs to WBG power semiconductors [21], [22], [23], reaching up 10 kHz output bandwidth. To reach a better performance, some authors opted for implementing interleaving techniques in order to reduce the stress in terms of current, the output current ripple, and to increase the effective switching frequency. Using this implementation, [24] reaches up to 320 V, 10 A, and 1 kHz. Similarly, [25] employs a full-bridge configuration with dual six interleaved IGBT bridge-legs to implement a 50 kVA (three-phase) amplifier with a bandwidth of 1 kHz for grid emulation applications. Parallel interleaving has also been used in industrial systems. For example, the work in [26] and [27] describe a 350 V, 480 A emulation system that achieves a large-signal bandwidth of 5 kHz using six parallel amplifier modules with six interleaved IGBT bridge-legs each. Similarly, Liebig et al. [28] describe a high-power industrial motor emulator system with an overall output current rating of up to 800 A at 50 V and a fundamental frequency of up to 5 kHz. Recent work [29] aiming lower output voltages and making use of state-of-the art 150 V gallium nitride (GaN) transistors has been able to reach 45 V, 18 A and 350 kHz bandwidth. However, all these systems still lack performance in terms of high voltage/current in the MHz range.

Later, with the growth of multi-level converters, new solutions started to appear, such as neutral point clamped (NPC), flying capacitors (FCs) and cascaded H-bridge (CHB) converters. Regarding NPC and FCs, in [30] a five-level NPC bridge-leg structure is proposed to realize a 7.5 kW (three-phase) amplifier with an output frequency of 2 kHz. Similarly, but now making use of SiC power semiconductors, Boillat et al. [31], [32], [33] propose a 10 kW three-phase ac power source that operate with a switching frequency of 48 kHz, achieving a large-signal bandwidth limited to 300 Hz. Recently, Suthar et al. [34] demonstrated an AWG with an eight-level FC bridge-leg using GaN transistors switching at 200 kHz. The prototype is rated at only 500 W and operates with a relatively low dc-bus voltage of 200 V, and it achieves a large-signal output waveforms with fundamental frequencies of up to 40 kHz. In [35], an AWG is proposed to deliver 100 kV, 100 mA with a large-signal bandwidth of 50 Hz. More recently, Schmitt et al. [36] proposed a motor emulator that consists of three parallel interleaved three-level NPC bridge-legs that provides 200V, 70 A and 2.5 kHz output bandwidth. The 400 V, 4 kW prototype described in [37] achieves a large-signal bandwidth of 10 kHz with a three-level NPC digital amplifier switching at 100 kHz.

With regard to CHB implementations, in [38] it is described a system with grid-level output voltage ranges, up to 400 V, and 5 A which could achieve a closed-loop large signal bandwidth of 5 kHz. Similar results have also been reported in [39] or, for lower output voltages, in [40]. The scalability of the CHB concept renders it suitable also for applications with higher voltages and medium-voltage grid simulation, as indicated in [41], where a 6 MVA, 50 Hz system that can provide 35 kV output voltage (with a step-up transformer) has been implemented. Recently, Petković et al. [42] and Hildebrandt et al. [43] introduced a 3 kV, 120 A and 7 kHz system with five cascaded cells. CHB converters have also been employed for special applications, with low power but high voltage for supplying plasma reactors with a 15 kV square-wave voltage at 5 kHz [44]. Similarly, in [45], a high voltage multi-level AWG for insulation testing has been developed, providing up to 14 kV, 0.1 A and 100 kHz. A similar concept is used in [46] obtaining 20 kV, 0.4 A and 5 kHz output bandwidth. In [47], a CHB has been implemented for pulsed electric field applications reaching 500 V, 2 A and 2 kHz. In [48], a bipolar modular MLC based on half-bridge and special full-bridge for electroporation applications has been employed delivering 2 kV, 10 A and a high output bandwidth of 500 kHz. Other concepts more focused on a high output bandwidth has been implemented in [49] and [50] obtaining up to 400 V, 4 A and 1 MHz output bandwidth.

Regarding hybrid topologies, which mix both, analog and digital power amplifiers there exists different works in the literature. For example, Gong et al. [39], and Gong et al. [51], [52] describe a 130 V rms, 1 kW (single-phase) system consisting of nine cascaded converter cells with equal dc voltages, which achieves a large-signal bandwidth of 10 kHz and, thanks to the linear stage, a very high small-signal bandwidth

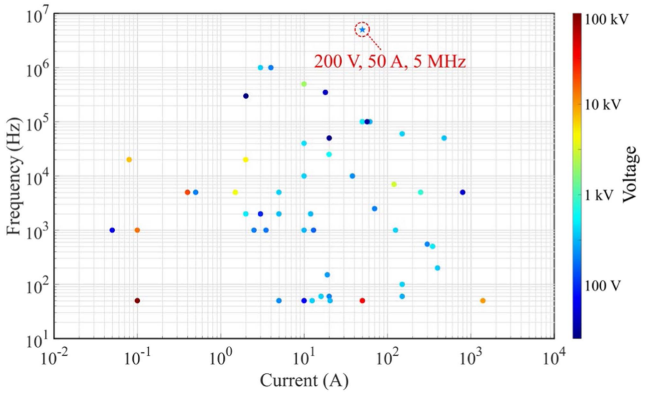

FIGURE 2. State-of-art analysis of AWGs.

of 600 kHz. The 140 Vrms, 500 W hybrid amplifier proposed in [53] achieves a similar small-signal bandwidth of 400 kHz, but uses only four cascaded cells that, however, feature unequal dc voltages and thus can realize 19 voltage levels. In [54], it is described a converter able to provide 480 V, 50 A and a large-signal bandwidth of 100 kHz.

The aim of this article is to propose, design, implement and optimize a versatile large-signal high-frequency AWG taking advantage of the new GaN devices and being able to provide a 400 Vpp, 50 Arms and 5 MHz large-signal output bandwidth. The aim of this converter is to fill the existing gap in the high voltage/current AWGs in the MHz range. All the previous state-of-art analysis and the proposed converter are represented in Fig. 2, where the clear existing gap and novelty of the proposed topology can be observed. For this purpose, a multilevel topology has been chosen and a new modulation scheme has been proposed, based on different voltage levels in each module, which allows us to obtain a significantly better total harmonic distortion (THD) than in the case of conventional implementations [55], and better performance in terms of switching losses. To demonstrate this, in this article, a detailed analysis of the THD and switching losses with this new modulation has been carried out and compared with the previous ones, and detailed experimental results are provided.

The rest of this article is organized as follows. Section II shows the proposed power converter. In Section III, a modulation strategy analysis is carried out. Section IV details the main implementation and main experimental results. Finally, Section V concludes this article.

II. PROPOSED POWER CONVERTER

The proposed converter is presented in Fig. 3. It employs a CHB multilevel structure comprising n modules. Regarding the CHB topology, it has been selected for the following reasons: First, it requires the least number of components among all alternatives. Table 1 gives the component requirements of NPC, FC, and CHB converters depending on the number of levels, m. It can be seen how, in NPC and FC topologies, the clamping diodes and balancing capacitors, respectively,

TABLE 1. Comparison of Power Component Requirements per Phase Leg Among Three Multilevel Converters

Converter type	NPC	FC	CHB
Main switching devices	$2\cdot(m\text{-}1)$	$2\cdot(m\text{-}1)$	$2\cdot(m\text{-}1)$
Main diodes	$2\cdot(m\text{-}1)$	$2\cdot(m\text{-}1)$	$2\cdot(m\text{-}1)$
Clamping diodes	$(m\text{-}1)\cdot(m\text{-}2)$	0	0
DC bus capacitor	$(m\text{-}1)$	$(m\text{-}1)$	$(m\text{-}1)/2$
Balancing capacitors	0	$(m\text{-}1)\cdot(m\text{-}2)/2$	0

increases quadratically, while for the CHB the increment of all the components is linear with the number of levels.

Secondly, the CHB topology offers a higher scalability because, related with the reduced number of components, it is easier to increment the output voltage levels in CHB with respect to NPC and FC topologies. This is due to the fact that a modularized circuit layout and packaging is possible because each level has the same structure. And, finally, in the CHB topology, there are different power supplies for each level, which allows a higher versatility in terms of voltage levels because it is the only alternative which can reach different bus voltages in each level and avoid the problem of balancing the voltage in the bus capacitors.

Each level follows a full-bridge configuration which can supply a bus voltage of $\{-V_{\text{bus},i}, 0, V_{\text{bus},i}\}$, i=1, …, n. In this design, each level's voltage is carefully chosen to optimize the resulting output voltage waveform. Consequently, the maximum attainable output voltage is

$$V_{o,\max} = \sum_{i=1}^{n} V_{\text{bus},i}, \tag{1}$$

allowing the generation of arbitrary waveforms with an amplitude resolution of $\min_{i=1\ldots n}(V_{\text{bus},i})$.

To generate the desired arbitrary waveforms, each level is activated sequentially to achieve the instantaneous output voltage

$$v_o = \sum_{i=1}^{n} v_{o,i} \tag{2}$$

being $v_{o,i} = \{-V_{\text{bus},i}, 0, V_{\text{bus},i}\}, i = 1, \ldots, n$.

In order to maximize temporal and frequency resolution, WBG devices are employed, leveraging their low Q_{oss}, minimum figure of merit, $\text{FOM}_g = Q_g \cdot R_{\text{on}}$, and negligible Q_{rr} characteristics. Consequently, WBG devices provide a rapid response, enabling the minimization of signal lag and distortion and increasing the maximum operating frequency. Different modulation strategies have been investigated and compared (see Fig. 4). On the one hand, the fixed-voltage pulsewidth modulation (PWM) where $V_{\text{bus},i} = V_{o,\max}/n$, i=1, …, n. This strategy enhances resolution by employing high-frequency PWM techniques [56], [57] capitalizing on the benefits of WBG devices. On the other hand, in this article, a DAC-based approach is proposed, employing a different bus voltage in each module to achieve similarly low harmonic

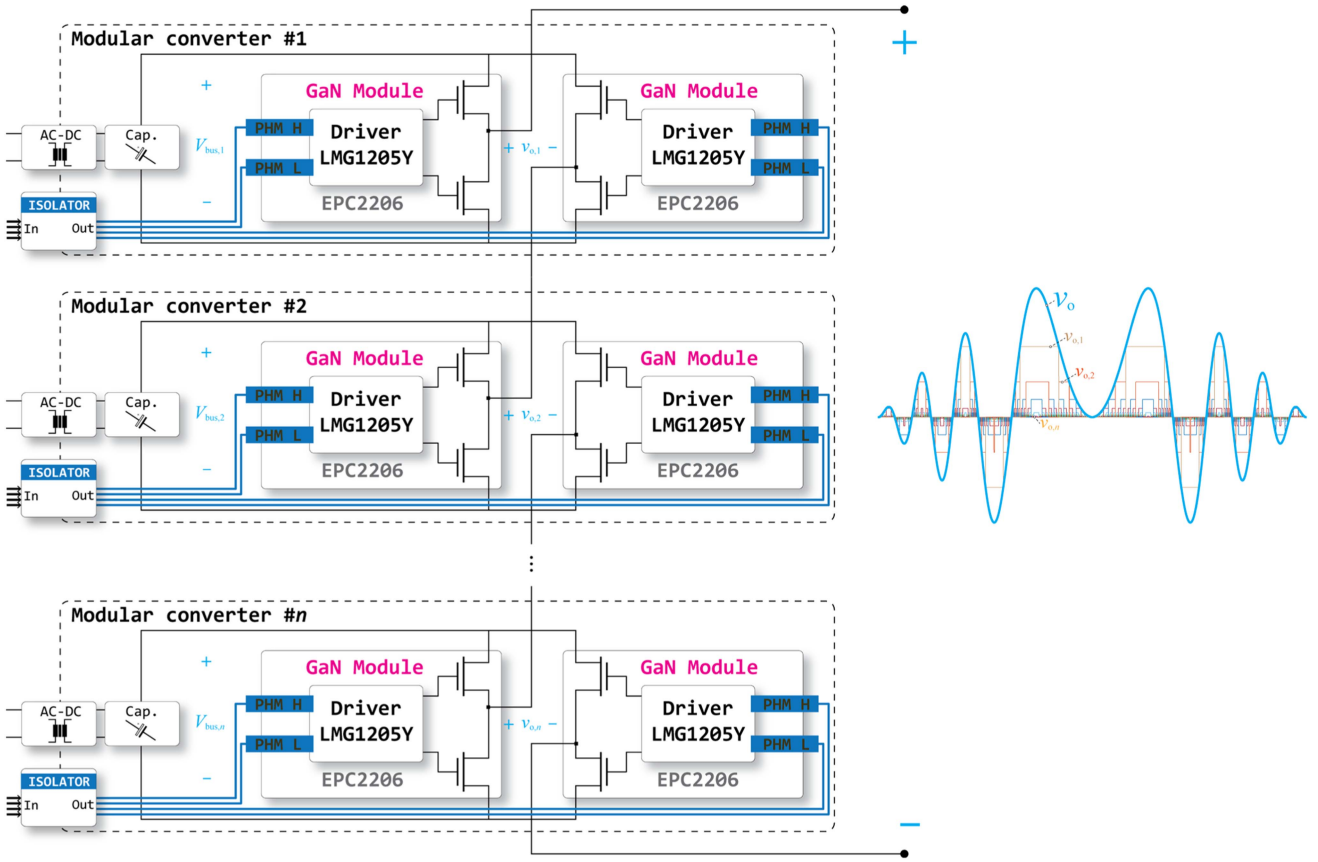

FIGURE 3. Proposed GaN-based multilevel topology.

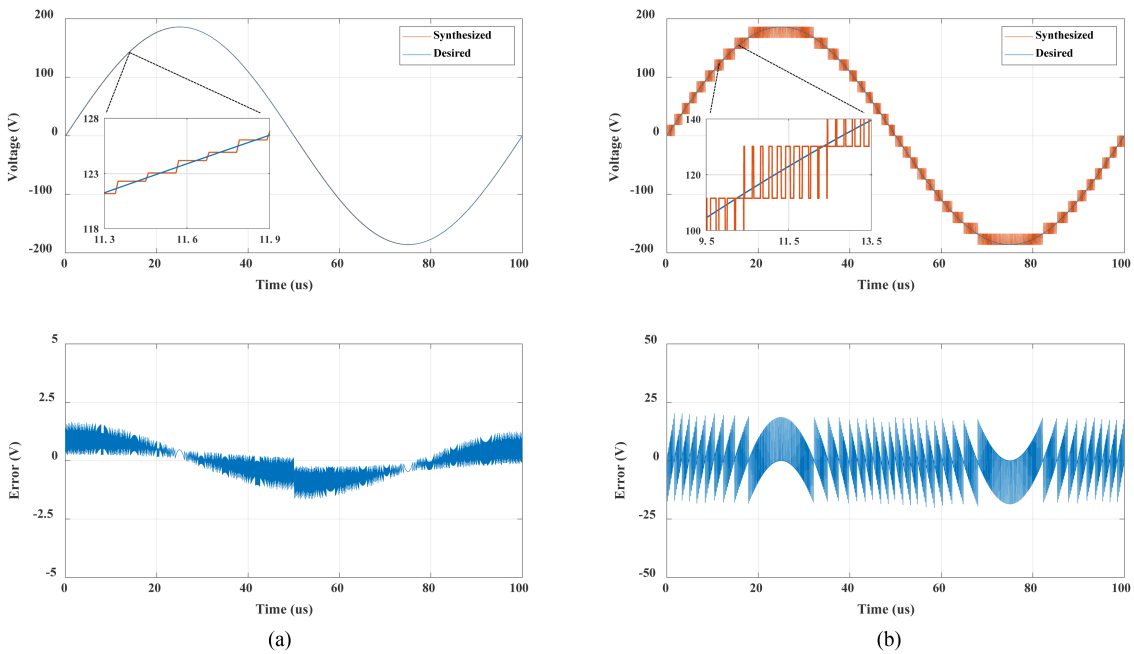

FIGURE 4. Comparative analysis of the analyzed modulation strategies. (a) DAC modulation. (b) Fixed-voltage PWM modulation.

distortion. The bus voltage of each module is defined as $V_{\text{bus},i} = V_{o,\max} \cdot 2^{(i-n-1)}$, i=1, …, n.

In this article, the latter strategy is going to be implemented in order to attain improved total harmonic distortion across a broad spectrum of operating conditions, encompassing different output voltage amplitudes and frequencies, while also requiring a limited number of levels.

III. MODULATION STRATEGY ANALYSIS

To determine the optimal implementation and modulation strategy, a comprehensive analysis has been conducted, taking into account factors, such as the number of levels, switching losses, total harmonic distortion, and system complexity.

A. DESCRIPTION

In the first approach, the fixed-voltage PWM modulation [58], [59], [60], each H-bridge level is controlled using PWM, where the duty cycle of the switching signals is adjusted to control the output voltage. The PWM strategy ensures that each H-bridge creates an average output voltage that is a fraction of the dc-bus voltage. The modulation strategy in this configuration is relatively simple, as each H-bridge operates with the same modulation scheme. The control algorithms are straightforward and easy to implement. Besides, since all H-bridges share the same dc-bus voltage, voltage balancing between the levels is less critical. Minor voltage differences can often be managed through simple control adjustments.

On the other hand, in DAC modulation, or hybrid modulation [61], [62], [63], [64], the modulation is more complex due to different voltage levels at each level, but it provides a better performance. In this case the lowest voltage module is the one that will determine the accuracy of our converter. It will act as the least significant bit of a DAC converter. Therefore, the maximum error that can be obtained when synthesizing a waveform is half of this voltage. As the voltage buses are configurable, it allows us to obtain a higher precision than PWM modulation, as it can be seen in Fig. 4. In this example, the proposed modulation achieves five times less error than the fixed-voltage counterpart. This configuration can potentially provide better efficiency because each H-bridge can operate at a voltage level close to the required output voltage, reducing voltage losses in the switching devices. Furthermore, variable voltage levels lead to lower THD in the output waveform, as it will be explained in following section.

B. HARMONIC DISTORTION ANALYSIS

In order to perform a fair comparison between both alternatives in terms of the output waveform quality, the total harmonic distortion rate has been taken as a reference figure of merit. In both cases, the maximum output voltage waveform is the same, but not the number of modules, because in order to reach the same amplitude, in the DAC implementation, it will be necessary to include more modules due to the reduced bus voltage in some of them.

The general expression for calculating the THD is as follows:

$$\text{THD} = \sqrt{\sum_{h=2}^{\infty} V_h^2} \Big/ V_1 \tag{3}$$

where V_h is the voltage amplitude of the hth harmonic.

Therefore, to calculate the THD, the value of all harmonics of the output waveform are required to be calculated in each case. The fundamental harmonic corresponds to the reference sinusoidal signal to be synthesized for both, the fixed PWM voltage and DAC approach.

In case of fixed voltage PWM approach, the shape of the output waveform is also a ladder, however this has subpulses per voltage level, because it has more than one switching angle per step, so in order to do the fast Fourier transform (FFT) over the output waveform, those switching angles are taken into account. In [65] an analytical method for calculation of multilevel pulse width modulation has been developed, obtaining the generic (4) for FFT calculation in this modulation

$$v(t) = \sum_{h=1}^{\alpha} \frac{4V_{o,\max}}{n\pi h} \left[\sum_{i=1}^{\frac{k-1}{2}} \sum_{j=1}^{L_i} (-1)^{j-1} \cos\left(h\alpha_{ij}\right) \right] \text{sen}\,(h\omega t) \tag{4}$$

where $V_{o,\max}/n$ is the bus voltage of each module, k is defined as the number of steps, L_i is a vector that indicates the number of switching angles for step i, j denotes the specific switching angle within a step i, α represents the switching angle, ω, the output frequency and h represents the harmonic number.

Therefore, combining (3) and (4) in order to calculate the THD, the following expression is obtained as

$$\text{THD}_{\text{PWM}} = \frac{\sqrt{\sum_{h=2}^{h\max} \left(\sum_{i=1}^{\frac{k-1}{2}} \sum_{j=1}^{L_i} (-1)^{j-1} \cos\left(h\alpha_{ij}\right) \right)^2}}{\sum_{i=1}^{\frac{k-1}{2}} \cos\left(h\alpha_i\right)}. \tag{5}$$

For the DAC modulation case, it is required to start from the equation that defines the step function, which is the following:

$$f(t) = \frac{V_m}{2^n} \cdot \left[\left(2^n - 1\right) \sin\left(\frac{2\pi}{M} \left[\frac{Mt}{T} \right] \right) \right] \; (0 \le t < T) \tag{6}$$

where V_m represents the amplitude of the reference voltage, M the number of discrete points in a period T, T/M the time interval for discretization, n is the number of bits and $[\cdot]$ means number rounding.

Through different mathematical manipulations and by performing the FFT over the function $f(t)$ the generic (7) shown at the bottom of the next page can be obtained [66] for the calculation of THD, which has been taken as reference

Once the procedures for the THD calculation have been defined for each case, specific operating conditions will be established to perform a representative comparison. WBG devices will enable the switching frequency to be 5 MHz,

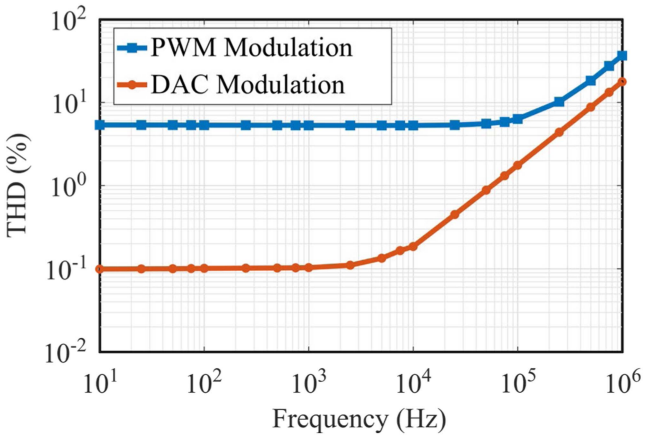

FIGURE 5. Total Harmonic Distortion comparison between the two analyzed modulation strategies.

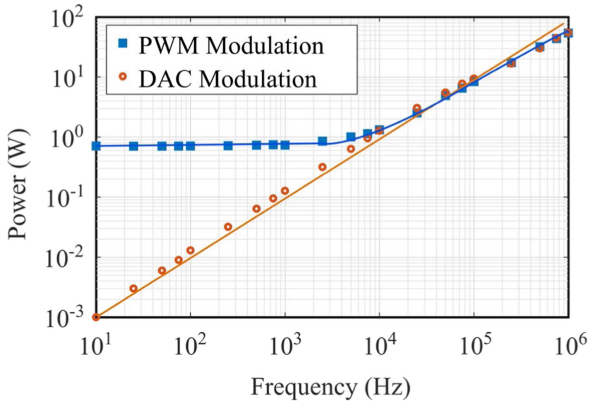

FIGURE 6. Switching losses comparison between the two analyzed modulation strategies.

which will correspond to the sampling frequency. In order to compare the two analyzed modulation strategies, the THD is going to be calculated in both cases for different output frequencies, from 10 Hz up to 1 MHz at the highest output voltage, 400 Vpp. Under these conditions, the main results are summarized in Fig. 5.

In view of the results obtained, it can be observed as the DAC modulation strategy presents a much better behavior in terms of output THD values, especially in low frequencies where the PWM modulation strategy presents more than ten times higher THD values. As the synthesized frequency is increased, this difference decreases, but better results are still obtained with the DAC modulation alternative.

As a conclusion of this analysis, although DAC modulation demands a greater quantity of switching modules to achieve an equivalent output voltage, it excels in performance, notably in terms of reducing output voltage THD.

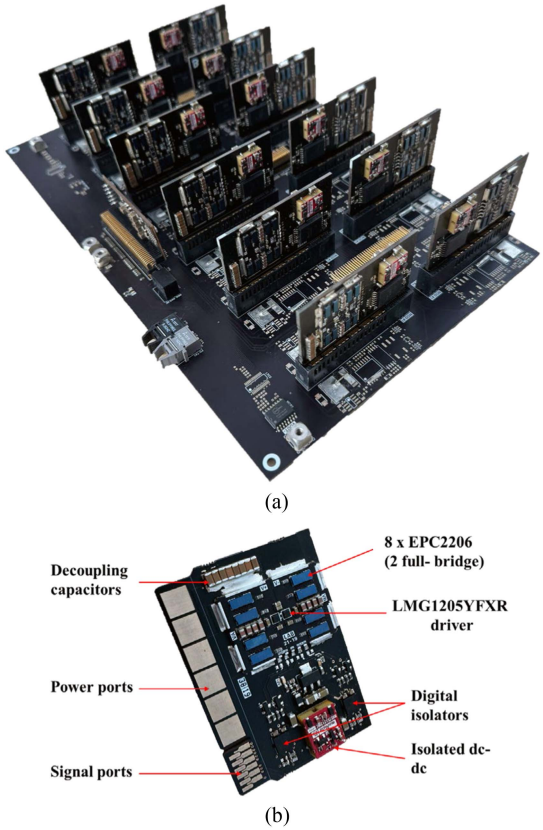

FIGURE 7. Experimental prototypes. (a) Global view. (b) Detail of one power sub-module.

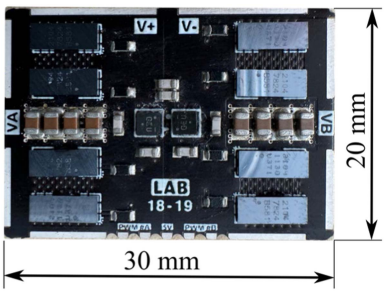

FIGURE 8. Detailed high frequency power devices layout.

C. SWITCHING LOSSES ANALYSIS

In order to make a comparison between both modulation strategies in terms of switching losses, the switching power losses in the converter have been calculated as a function of

$$\mathrm{THD}_{\mathrm{DAC}} = \sqrt{\frac{\frac{2\pi^2}{M}\sum_{i=0}^{M-1}\left[(2^n-1)\sin\left(\frac{2\pi}{M}i\right)\right]^2}{\left\{\sum_{i=0}^{M-1}\left[(2^n-1)\sin\left(\frac{2\pi}{M}i\right)\right]\left(\sin\left(\left(\frac{2\pi}{M}\right)(i+1)\right)\right)-\sin\left(\frac{2\pi}{M}i\right)\right\}^2+\left\{\sum_{i=0}^{M-1}\left[(2^n-1)\sin\left(\frac{2\pi}{M}i\right)\right]\left(\cos\left(\frac{2\pi}{M}i\right)-\cos\left(\frac{2\pi}{M}(i+1)\right)\right)\right\}^2}-1}. \quad (7)$$

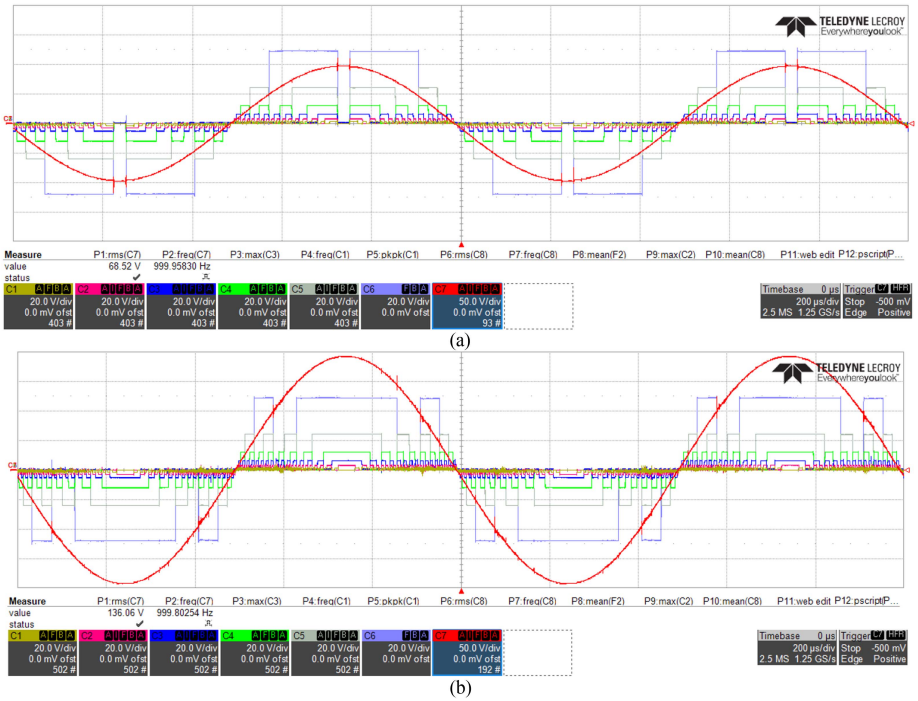

FIGURE 9. Experimental waveforms with sinusoidal operation at 1 kHz. (a) 68 Vrms output voltage. (b) 136 Vrms output voltage. Total output voltage (CH7) and single level output voltages (CH1-6).

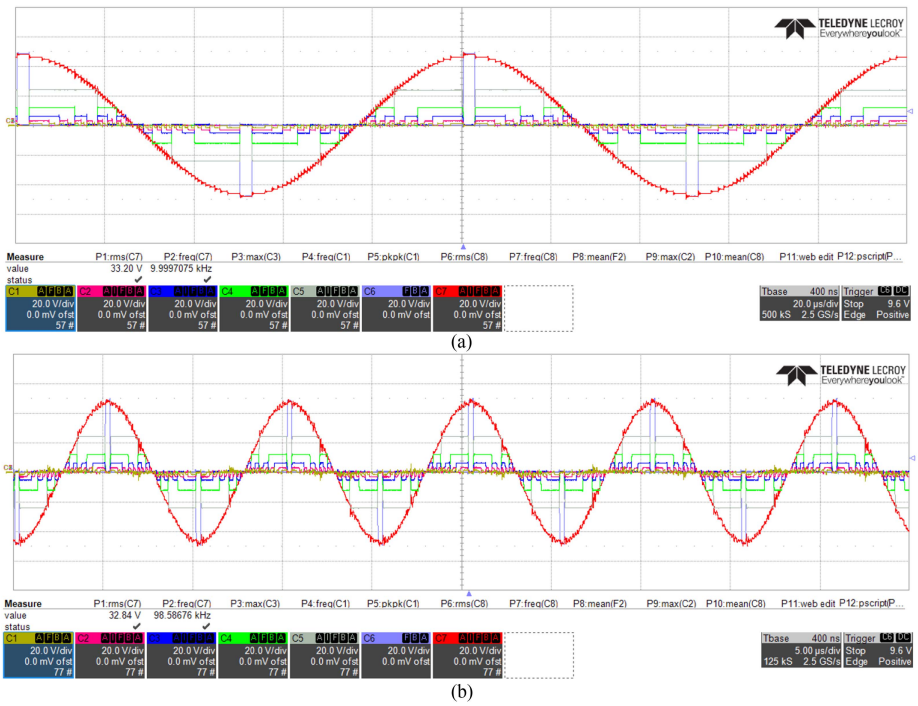

FIGURE 10. Experimental waveforms with sinusoidal operation at 1 kHz. (a) 68 Vrms output voltage. (b) 136 Vrms output voltage. Total output voltage (CH7) and single level output voltages (CH1-6).

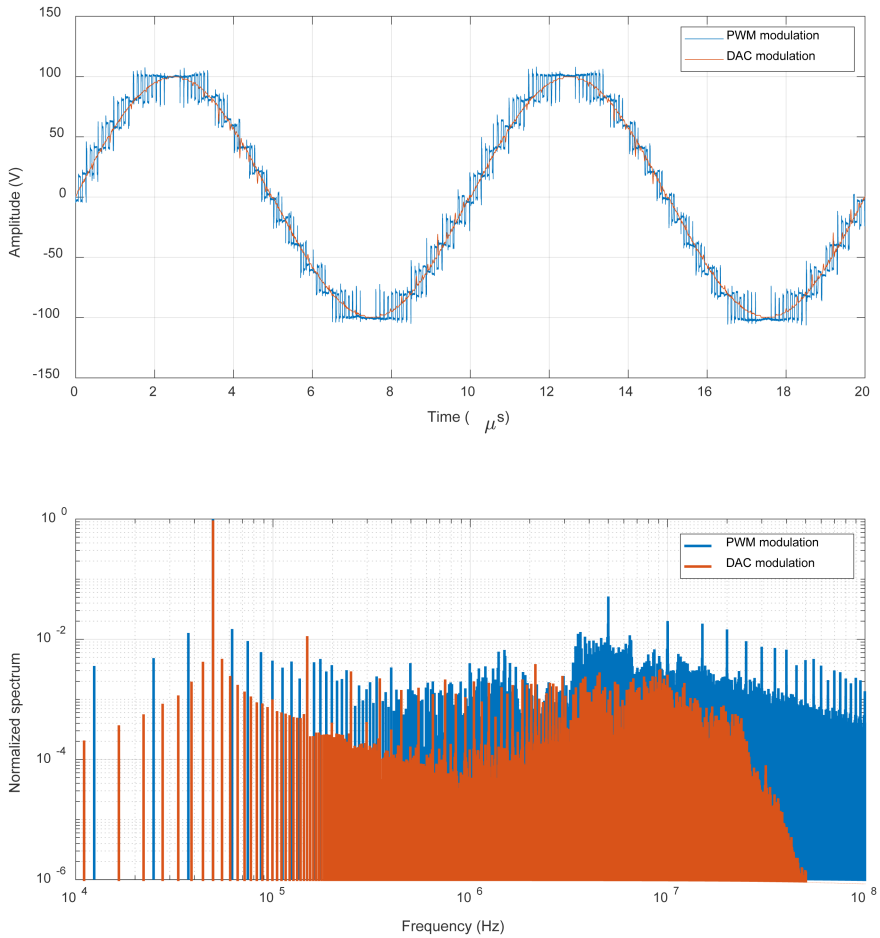

FIGURE 11. Comparison of DAC modulation and PWM modulation synthesizing a sinusoidal waveform of 100 V and 50 kHz. (a) Time domain. (b) Frequency domain.

the frequency generated at the output. For this purpose, the E_{oss} variable of the selected device, in this case the GaN device EPC2206, was used. It is important to remark that the E_{oss} variable evolves nonlinearly with the voltage to be blocked by the device. This is why, in the case of PWM modulation strategy, the E_{oss} will be constant for all modules, and for DAC modulation, its value will be changing. Second, to make a comparison between both alternatives, a 10-module CHB converter has been modeled in Matlab/Simulink, generating a sine function at the output with an amplitude of 200 V. In this simulation, different counters have been placed on each of the devices to know the exact number of times that they switch during one output waveform period. Finally, this number of switching events has been multiplied for the output waveform frequency in order to know the real switching frequency of the devices. Multiplying this switching frequency by the E_{oss} obtained in the first step, the switching power losses can be obtained as

$$P_{sw} = f_{sw} \cdot E_{oss}. \tag{8}$$

In order to obtain a comparison in a wide range of output frequencies, a frequency sweep has been made, from the Hz to the MHz range. The results of this simulations have been represented in Fig. 6. It can be observed that, at low frequencies (up to 10 kHz), there is an important dominance of the DAC modulation over PWM modulation, and from 10 kHz to the MHz range both strategies have similar power losses, in the order of 60 W. This power is shared among all the power devices of the converter and the heat produced can be easily evacuated. In summary, DAC modulation is more efficient in terms of switching frequency than PWM modulation.

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The proposed versatile large-signal AWG has been implemented to provide up to 400 Vpp output voltage with a maximum operating frequency of 5 MHz (see Fig. 7). The proposed converter features EPC2206 devices with LMG1205Y driver, providing up to 50-A RMS continuous output current. This implementation has been made using a modular approach, where each full-bridge is an surface-mount device (SMD) component. The output voltage at each level can be set to different values. In the case of DAC modulation, the voltage level of each module will

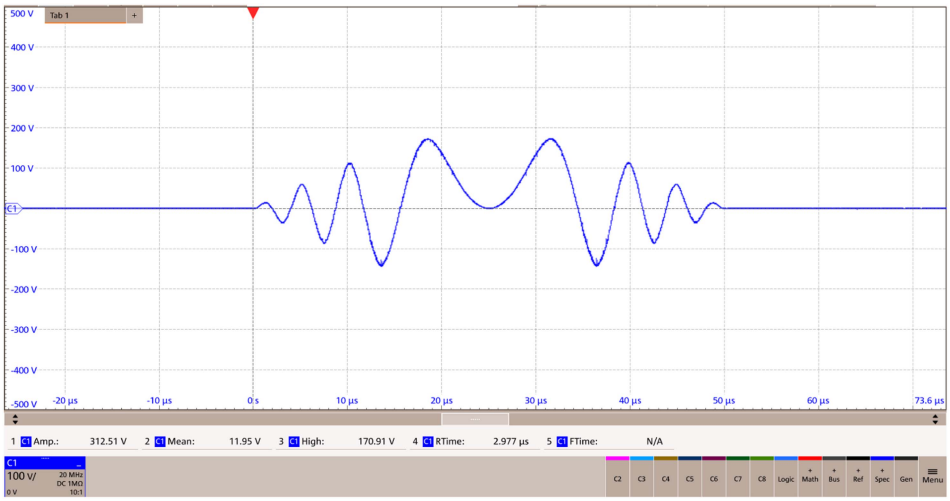

FIGURE 12. Arbitrary output waveform using DAC modulation strategy.

be configured as powers of two, but in the PWM modulation, all modules will be configured at the same voltage. Fig. 7 shows the proposed modular design implemented, including a view of the complete prototype (a) as well as de detail of one of the power sub-modules containing the GaN-based full bridge structure, decoupling capacitors and drivers (b).

For the routing and placement of the components, the manufacturer design guidelines [67] for the Gan devices has been followed, to maximize efficiency and performance at the MHz switching range. More in detail, an optimal-power-loop-implementation strategy has been selected, reducing the main parasitic power-loop-inductance below 0.5 nH and, therefore, minimizing oscillations and overvoltage during switching transitions. Additionally, gate drivers are located symmetrically and very close to the power transistors to minimize possible oscillations caused by the gating circuit. In Fig. 8, a detailed image of the high frequency board has been included to show the component placement.

Fig. 9 shows a representative example of the converter applying the DAC modulation and operating at 1 kHz with two different output voltage amplitudes. In this figure, the total output voltage, and the individual output voltage provided by each one of the levels are represented, where the different voltage, distribution can be seen. Following the same approach, Fig. 10 shows two more examples of operation at different sinusoidal output voltage frequencies: 10 and 100 kHz. These experimental results prove the ability of the converter to operate at a wide range of operating conditions.

In order to facilitate the comparison, both the temporal waveforms and the resulting FFT of two new experimental high-resolution captures using PWM and the proposed DAC modulation are included in Fig. 11. Both modulations synthesized a sinusoidal waveform with a 100 V amplitude and a 50 kHz output frequency. The temporal waveforms of both modulations result in lower THDs, with the quality of the DAC modulation appearing superior. This assumption is verified in the spectral plot, where the amplitude of the non-fundamental harmonics is much lower for the DAC modulation. Additionally, it can be observed that the 5 MHz switching frequency of the PWM modulation creates intermodulation products, worsening the spectrum. The obtained THD from the FFT analysis results in 11.21% and 2.53% for the PWM and DAC modulations, respectively, (7% and 0.88% theoretical). Differences from theoretical predictions are mainly caused by the non-ideal switching waveforms.

Finally, in order to test the flexibility of the proposed converter, Fig. 12 shows an arbitrary output waveform featuring highly variable amplitude and frequency. In this case it has been represented using the DAC modulation strategy, which has demonstrated a better performance. As a conclusion, the proposed system can be used to generate up to 400 Vpp and 50 A waveforms with a bandwidth in the MHz range defined by the 5 MHz GaN-devices switching frequency.

V. CONCLUSION

In this article, a versatile large-signal high-frequency AWG has been presented. It follows a multilevel CHB structure and takes advantage of GaN devices to achieve a low-distortion and high-bandwidth operation. Different modulation strategies have been discussed, DAC modulation and fixed-voltage PWM modulation. In order to compare both alternatives, a comprehensive analysis in terms of harmonic distortion and switching losses has been carried out, opting for DAC modulation to enhance both switching efficiency and minimize output voltage THD. The proposed converter has not only been designed but also successfully implemented, yielding a high performance design featuring a 400 Vpp voltage and a 50 A current at 5 MHz switching frequency. This achievement represents a significant stride in achieving both high voltage and remarkable temporal/amplitude resolution, effectively paving the way for future applications in the realms of industrial and biomedical fields.

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