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Review and Analysis of Voltage Clamping Circuits With Low Overvoltage Ratios for DC Circuit Breakers

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ABSTRACT Voltage clamping circuits are critical components in most direct-current circuit breakers (dcCBs) to achieve ultrafast dc fault interruptions and an extended lifetime. A key performance index of voltage clamping circuits is the overvoltage ratio, which calculates the peak switching overvoltage over the nominal voltage during fault interruption processes. A lower overvoltage ratio is beneficial to minimize the dcCB insulation voltage and reduce the total breaker cost, meanwhile alleviating the overvoltage interference to the dc bus and, thus, enhancing the stability of the dc power system. This article evaluates the overvoltage ratio of various clamping circuits reported in dcCB literature. The basic working principles, switching overvoltage magnitude, advantages, and limitations of different voltage clamping circuits are evaluated by circuit simulations. A capacitor-metal–oxide varistor (C-MOV) circuit is selected for experimental validation considering its specifically low overvoltage ratio. The C-MOV prototype is verified with high-power tests at 1 kV dc bus. The measured overvoltage ratio of the C-MOV prototype matches parametric analyses. The effects of stray inductance and fault rise rate on the overvoltage ratio are also experimentally validated. Finally, the C-MOV circuit is compared with other voltage clamping circuits in the literature to demonstrate its benefits and limitations in dcCB applications.

INDEX TERMS Metal–oxide varistor (MOV), overvoltage suppression, solid-state circuit breaker (SSCB), voltage clamping circuits.

I. INTRODUCTION

The dc power systems have been witnessing great progress recently. They offer a higher efficiency, less stages of power conversion, and a higher penetration of renewable energy [1]. The dc systems have become promising solutions for power distribution and transportation electrification applications, such as electric ships [2], renewable energy integration [3], electric vehicle charging infrastructure [4], and electric aircraft [5].

However, fault protection in dc power systems is a major technical challenge [6], [7], [8]. Due to the absence of natural zero crossing in dc systems, interrupting fast-developing dc fault current with switching arcs becomes overwhelmingly tricky and slow [9], [10]. Instead, energy absorption devices, such as metal–oxide varistors (MOVs), are added into higher voltage direct-current circuit breakers (dcCBs) (1 kV and above) to accelerate dc fault interruption processes [11], [12]. These MOVs are installed in parallel to the main switches of the dcCB and, thus, constitute a voltage clamping circuit.

A voltage clamping circuit, for its namesake, aims to clamp the switching overvoltage generated across the dcCB during fault current interruption processes. The clamping overvoltage ratio (OVR) is the key performance index to evaluate a voltage clamping circuit as defined in (1)

$$\mathrm{OVR} = V_{\mathrm{pk}}/V_{\mathrm{op}} \tag{1}$$

where V_{pk} is the peak transient overvoltage and V_{op} is the maximum dc operating voltage of the dcCB. Typically, a low-OVR value is pursued by voltage clamping circuits in dcCBs. With a lower switching overvoltage generated across

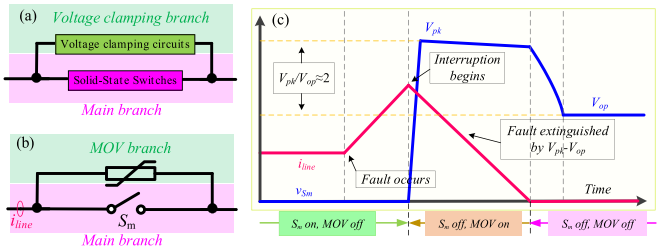

FIGURE 1. Voltage clamping circuit of SSCBs. (a) Typical configuration. (b) Classical MOV-based clamping circuit. (c) Working principles of a classical MOV-based clamping circuit in an SSCB.

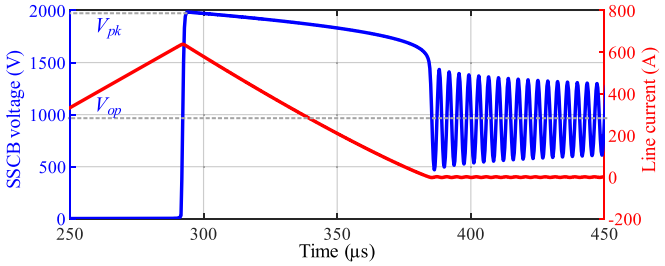

FIGURE 2. Voltage clamping waveform of a 950 V SSCB with classical MOV-based clamping circuit in which the OVR is 1985 V/950 V = 2.09.

the dcCB, there can be a lower insulation strength of the main branch switches [13]. Moreover, a lower switching overvoltage alleviates interference to the dc bus, therefore enhancing the stability of dc power system [14]. Meanwhile, with a low-OVR voltage clamping circuit, the total cost of a dcCB can be significantly reduced due to the less capital investment on the main switches with regard to particular dc voltage V_{op}, as the number of main switches in series can be reduced due to lower switching overvoltage V_{pk}.

Fig. 1(a) illustrates a configuration when the main switches are solid-state switches and the dcCB becomes a solid-state circuit breaker (SSCB) [15]. Compared with dcCBs with mechanical switches in the main path, SSCBs are more prone to overvoltage damages and more sensitive to the multiplied cost by cascading numerous semiconductors [16], [17]. Therefore, this article focuses on low-OVR designs of voltage clamping circuits in 1 kV and above SSCBs.

MOV is a key component in voltage clamping circuits. It is usually placed across the main solid-state switches for overvoltage protection. However, the OVR of this type of voltage clamping circuit is affected by the MOV characteristics [18], [19], [20]. For example, assuming peak transient overvoltage V_{pk} roughly equal to MOV maximum clamping voltage V_{clamp}, and V_{op} is selected equal to MOV dc nominal voltage rating $V_{M(\text{dc})}$ since the voltage span of typical MOVs clamping region of is relatively wide ($V_{\text{clamp}}-V_{M(\text{dc})}\approx V_{M(\text{dc})}$), it can be approximated that the OVR of this type of voltage clamping circuit is relatively high (∼2.0). Recently, advanced voltage clamping circuits have been proposed to reduce the OVR using different technical solutions, including adding dc disconnecting components [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32] or dc-blocking components [21], [33] in series with the MOV.

Therefore, this article aims to systematically compare existing state-of-the-art low-OVR circuits and innovatively categorize them into three categories: classical MOV-based circuits, dc disconnected MOV circuits, and dc-blocked MOV circuits. Two technical solutions are identified to solve the high-OVR problem of classical MOV-based clamping circuits. Among more than ten circuits under evaluation, a capacitor-metal–oxide varistor (C-MOV) circuit is selected and verified to achieve one of the lowest OVR values as compared with the literature. Moreover, the major contribution of the work includes the experimental validation of the C-MOV circuit in high-power, fast-rising dc fault scenarios of a 1 kV SSCB prototype. Last but not the least, a comprehensive comparison of this work with state-of-the-art results is performed. The comprehensive comparison targets at presenting reviews, analyses, and evaluations of various clamping circuits reported in representative dcCB literature focusing on the OVR reduction performances. Overall, it is proved that C-MOV circuits with all passive components can achieve a significantly low OVR that benefits the interruption reliability of dcCBs against ultrafast dc faults.

II. CLASSICAL MOV-BASED VOLTAGE CLAMPING CIRCUITS

A. WORKING PRINCIPLE

The MOV by itself is the most straightforward voltage clamping circuit for SSCBs. As indicated by Fig. 1(b), it is usually placed directly across protected main solid-state switches. Fig. 1(c) shows the basic working principle of a classical MOV-based clamping circuit for SSCBs. During the interruption process, the voltage overshoot $V_{\text{pk}}-V_{\text{op}}$ provided by MOVs can effectively extinguish fault current in the system. MOVs in this type of voltage clamping circuits must withstand dc bus voltage at the breaker OFF-state. To avoid significant leakage current, the maximum operating voltage V_{op} cannot exceed the dc voltage rating $V_{M(\text{dc})}$ of the MOVs, leading to relatively high clamping ratios with OVR $\geq$ 2.0.

It is noted that a lot of reported MOV voltage clamping circuits claimed a lower OVR. Basically, that is because a maximum operating voltage V_{op} much higher than $V_{M(\text{dc})}$ of the MOVs is applied, which will cause excessive leakage current at static OFF-state. For a fair comparison, the maximum operating voltage V_{op} of these works is regarded as $V_{M(\text{dc})}$ of the used MOVs in this article.

B. LIMITATIONS: HIGH TRANSIENT OVR

Fig. 2 shows a simulation case study, which demonstrates the clamping voltage of an exemplary MOV. The peak clamping voltage V_{pk} is 1985 V, while the maximum operating voltage V_{op} of the MOV is 950 V, indicating a high OVR of 2.09 at a 630 A interruption.

Adding another snubber branch with the clamping branch has been proposed in some literature to reduce *dv/dt* during

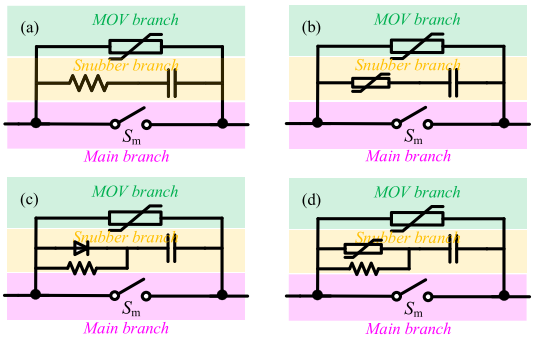

FIGURE 3. Four basic snubber configurations with MOV clamping circuit. (a) *RC* snubber [34], [35], [36]. (b) MOV-C snubber [37]. (c) RCD snubber [38], [39], [40]. (d) RCV snubber [41].

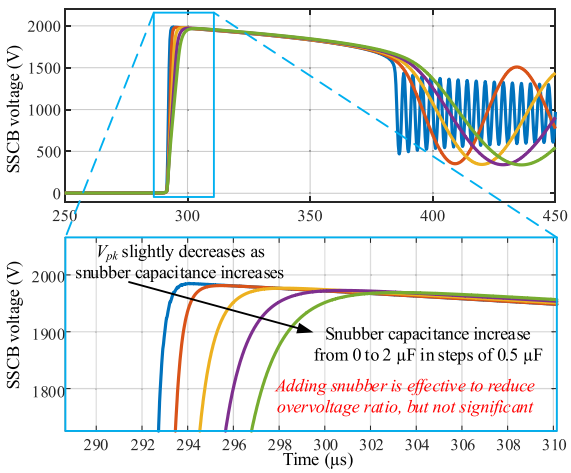

FIGURE 4. Clamping voltage investigation with *RC* snubber (snubber resistance is 0.5 Ω), showing that it is effective to reduce OVR, but not significant.

interruption. Fig. 3 shows four basic snubber configurations, including resistor–capacitor (*RC*) [34], [35], [36], varistor–capacitor (VC) [37], resistor–capacitor–diode (RCD) [38], [39], [40], and resistor–capacitor–varistor (RCV) [41]. Since the MOV current is determined by its voltage in the clamping region, reducing MOV *dv/dt* voltage ramping rate slows down the commutation and decreases *di/dt* in the MOV clamping branch. It is noted that the commutation mentioned here is from the snubber branch to the MOV branch. V_{pk} is, therefore, reduced as a lower $L_{MOV} \times di/dt$ is obtained, where L_{MOV} represents the stray inductance in the MOV commutation path. Fig. 4 shows a clamping voltage investigation with the widely used *RC* snubber. When snubber capacitance increases from 0 to 2 μF, the ratio decreases from 2.09 to 2.07. It shows that adding snubbers is viable to reduce the OVR of classical MOV-based voltage clamping circuits, but the overall effect is not significant. Another method involves paralleling multiple MOVs to reduce the OVR. The basic idea is still reducing MOV *di/dt* by distributing the total current across the MOVs, and the effectiveness is limited, while the total MOV volume and cost increase significantly.

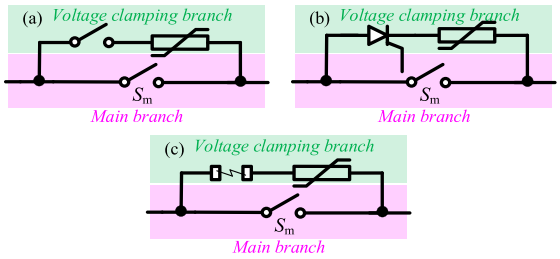

FIGURE 5. DC disconnected MOV voltage clamping circuits to increase V_{op}. (a) Full-control switch as disconnecting component [21], [22], [23], [24], [25], [26]. (b) Semicontrol switch as disconnecting component [27], [28], [29], [30]. (c) Breakable gap as disconnecting component [31], [32].

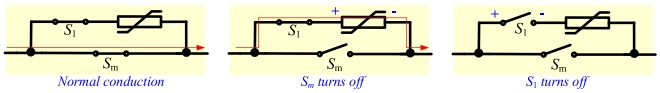

FIGURE 6. Operation sequence of full-control switch-based dc disconnecting MOV voltage clamping circuits.

III. DC DISCONNECTED MOV VOLTAGE CLAMPING CIRCUITS

It is straightforward from (1) that there are two different technical solutions to reduce the OVR:

1) increasing maximum operating voltage V_{op};
2) reducing peak clamping voltage V_{pk}.

In this section, solution 1) is first discussed, and the existing solutions are analyzed.

A. TECHNICAL SOLUTION#1: INCREASING BREAKER DC OPERATING VOLTAGE TO REDUCE OVR

Directly enhancing breaker V_{op} will increase MOV leakage current, which can lead to MOV damage due to the higher thermal dissipation. So, the prerequisite of enhancing V_{op} is to find a component that can safely disconnect the dc source from the MOVs during the OFF-state. Three dc disconnecting components will be discussed in the following sections: fully controlled switches, silicon controlled rectifiers (SCRs), and breakable gaps.

1) FULLY CONTROLLED SWITCHES FOR DC DISCONNECTION

As shown in Fig. 5(a), the most straightforward dc disconnecting components are fully controlled switches, such as MOSFETs and insulated-gate bipolar transistors (IGBTs). Operation sequences, working principles, and critical waveforms of a unidirectional dc disconnected MOV clamping circuit with fully controlled switching devices for dc disconnection, namely, switch-MOV (SW-MOV), are demonstrated in Figs. 6 and 7.

Since the maximum operating voltage V_{op} is enhanced, there will be a significant leakage current in MOV after the voltage clamping process is completed. Once this state is detected, auxiliary switch S_1 reacts to cutoff the MOV leakage current in a timely manner and withstand V_{op} while MOV

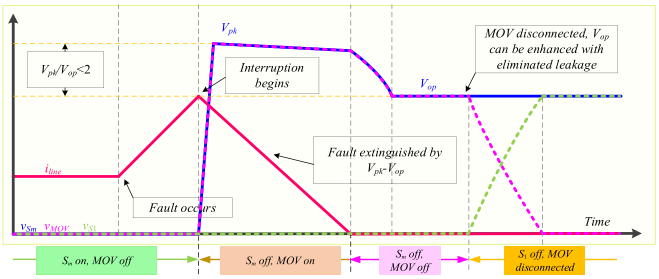

FIGURE 7. Working principles of switch-based dc disconnected MOV clamping circuits.

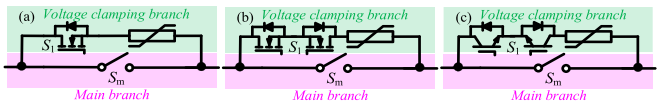

FIGURE 8. Typical full-control switch-based dc disconnecting MOV clamping circuits, as summarized in [21], [22], [23], [24], [25], and [26]. (a) Unidirectional configuration using MOSFET. (b) Bidirectional configuration using two MOSFETs. (c) Bidirectional configuration using two IGBTs.

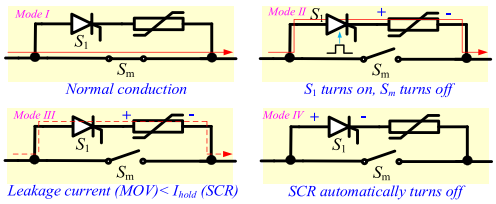

FIGURE 9. Operation sequence of SCR-based dc disconnecting MOV voltage clamping circuits.

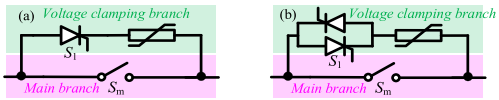

FIGURE 10. Utilizing antiparallel configuration to form bidirectional SCR-based dc disconnecting MOV voltage clamping circuits [27], [29].

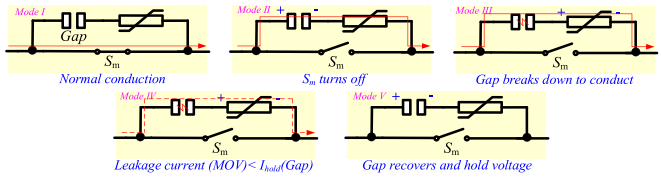

FIGURE 11. Operation sequence of gap-based dc disconnecting MOV voltage clamping circuits.

voltage stress is removed during the OFF static state. In practical engineering, since the resistance of MOV might be higher than a solid-state switch (S_1) at OFF-state, an additional large resistor R_p may be in parallel with MOV for the purpose of desired voltage distribution. It is noted that the OFF-state means the inactivity of MOV and switch after the fault current is extinguished and a significant dc voltage is blocked by the breaker. A quantifying criterion to opt for such a solution if the resistance of the MOV is close to or higher than that of S_1 in the OFF-state at V_{op} is to ensure that the equivalent resistance of MOV$\|R_p$ is much lower than the OFF-state resistance of S_1. For instance, considering S_1 as a typical SiC MOSFET with OFF-state resistance at mega-ohms range, it is recommended to select R_p at a range of tens or hundreds of kilo-ohms.

As a result, V_{op} of the voltage clamping circuit is safely enhanced and the MOV leakage current is eliminated, which reduces the OVR.

Fig. 8 shows the typical configurations of dc disconnecting, MOV-based voltage clamping circuits, as summarized in [21], [22], [23], [24], [25], and [26], in which MOSFET and IGBT are used as the fully controlled auxiliary switches. Antiseries connections of MOSFETs or reverse conductive IGBTs can be used to form bidirectional configurations.

2) SCRS FOR DC DISCONNECTION

The semicontrolled SCR is also feasible for use as a dc disconnecting component. Fig. 5(b) shows the configuration of an SCR-based MOV (SCR-MOV) clamping circuit for unidirectional fault interruptions, as summarized in [27], [28], [29], and [30].

The basic working principles of SCR-MOV clamping circuits are demonstrated in Fig. 9. Its critical waveforms are like those using fully controlled switches, as shown in Fig. 7. The only difference lies in the auxiliary switch S_1 turn-OFF mechanism. For the SCR-based dc disconnection scheme for MOV-based clamping circuits, after the voltage clamping duration, the MOV leakage current must be lower than the holding current of the SCR [27]. Then, after a period of delay, the SCR is naturally turned OFF and reobtains its voltage-blocking capability. Similarly, MOV resistance might be higher than the SCR in the OFF-state [27]. So, an additional large resistor in parallel with MOV might be necessary for the purpose of SCR dc voltage blocking in practice. Hence, V_{op} of the voltage clamping circuit is safely enhanced with an eliminated leakage current, which reduces the clamping OVR.

Since SCRs are unidirectional conducting devices, antiparallel connections are necessary to form bidirectional voltage clamping circuit configurations, as shown in Fig. 10.

3) BREAKABLE GAPS AS DC DISCONNECTING COMPONENTS

Breakable gaps are also used as dc disconnecting components for MOV clamping circuits (gap-MOV). The configuration is presented in Fig. 5(c), as summarized in [31] and [32]. It must be noted that both turn-ON and turn-OFF mechanisms of the spark gap used in this type of circuit are different.

The operation sequence, working principles, and critical waveforms of a gap-MOV voltage clamping circuit are shown in Figs. 11 and 12. During fault interruption, gap voltage ramps up first as the main switch S_m turns OFF. After it exceeds its dc sparkover voltage, the gap breaks down to conduct and MOV starts to work. After the voltage clamping duration, if the MOV leakage current is lower than the gap holding current threshold, the voltage-blocking capability of the spark gap can be recovered. Eventually, the gap will withstand the dc voltage and the high voltage stress on MOV can be removed. Hence,

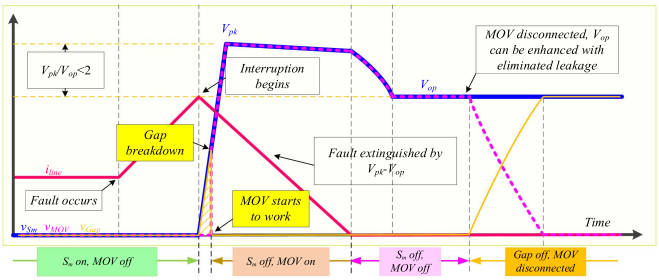

FIGURE 12. Working principles of gap-based dc disconnecting MOV voltage clamping circuits.

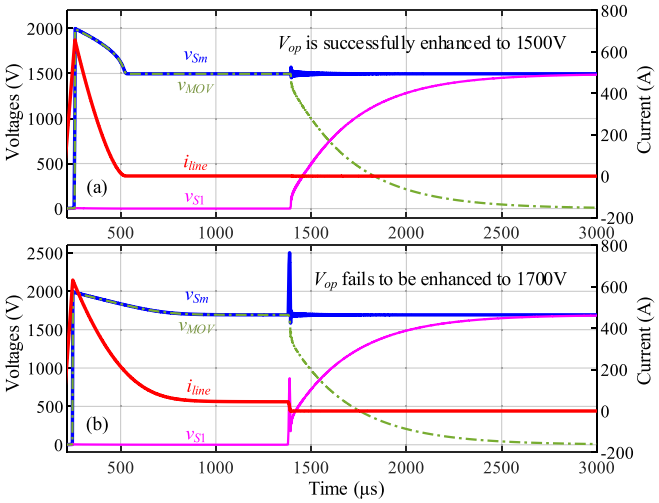

FIGURE 13. LTspice-simulated voltage clamping demonstration of a fully controlled switch-based MOV clamping circuit. (a) V_{op} is enhanced to 1500 V and the OVR is reduced to 1985 V/1500 V = 1.32 at a 630 A interruption. (b) V_{op} fails to be further enhanced to 1700 V.

V_{op} of the voltage clamping circuit is safely enhanced with an eliminated leakage current, which reduces the clamping OVR.

B. ADVANTAGES AND LIMITATIONS OF DC DISCONNECTED MOV-BASED VOLTAGE CLAMPING CIRCUITS

Different types of dc disconnected MOV voltage clamping circuits have their pros and cons. Their specific advantages and limitations are discussed as follows.

1) SW-MOV voltage clamping circuits feature a relatively low OVR. Fig. 13 shows a simulation study using the example 950-V-rated MOV, which demonstrates that the V_{op} is enhanced successfully to 1500 V by connecting a MOSFET in series with the MOV. As a result, the OVR is reduced to 1.32 with a peak clamping voltage of 1985 V. It also features the advantages of small size and fast speed.

However, there are some disadvantages that must be mentioned. First, the fully controlled switch must turn OFF after the system current decreases to the MOV leakage current level. This functionality requires separate current detection units, control feedback, and gate-drive units, which enhance the design complexity and system-level cost. Besides, its reliability is not as good as other purely passive solutions.

Meanwhile, it must be noted that the upper limit of V_{op} enhancement is determined by the overvoltage spike over the fully controlled switch when it cuts OFF the MOV leakage current. Fig. 13 also shows that the clamping circuit fails to enhance the V_{op} to 1700 V. When V_{op} exceeds its limit, a high cutting OFF current will generate a high voltage spike across the fully controlled switch. Then, the main switch voltage might be higher than the MOV peak clamping voltage and affect the total OVR of the clamping circuit. The high voltage spike is also risky as it might cause main switches breakdown. Therefore, the main design criteria for successfully establishing new V_{op} is that the total v_{Sm} spike during S_1 turn-OFF transient $V_{spike(Sm)}$ does not exceed the front maximum clamping voltage V_{clamp} of the MOV. In this case, the total V_{pk} will remain equal to V_{clamp} and will not be influenced by $V_{spike(S1)}$, which means that the OVR is effectively reduced by enhanced V_{op}.

2) Semicontrolled SCR-MOV clamping circuits can be either active or passive solutions, depending on different gate firing schemes. The above-mentioned current detection units, control feedback, and gate drive of full-control switches can also be used for active SCR-MOV solutions. Some works also propose self-firing methods by using low-voltage MOVs or breakover diodes across the gate and anode terminals to form passive SCR-MOV solutions for the purpose of reducing the cost and complexity [27]. SCRs can be automatically turned OFF if the MOV leakage current is designed to be below its holding current. This type of solution does not need separate SCR turn-OFF control. Besides, SCRs are usually much cheaper than fully controlled switches at the same ratings.

However, the V_{op} enhancement effect of this solution is limited by the SCR characteristics. Fig. 14 shows that V_{op} can be successfully enhanced to 1400 V by an auxiliary SCR in series with MOV. MOV leakage current is eliminated by SCR automatic turn-OFF as it is lower than the SCR holding current I_H. But it fails to further enhance the V_{op} to 1500 V, as MOV leakage current under this voltage exceeds SCR I_H threshold. If the SCR does not turn OFF, the MOV will be subject to high voltage stress until a thermal breakdown occurs. For the SCR-MOV circuit, the main design criteria for successfully establishing new V_{op} is that the MOV leakage current at new V_{op} is lower than the SCR holding current. In this case, the SCR S_1 can turn OFF and the MOV can be safely disconnected at the new V_{op}. The OVR is, thus, effectively reduced by the unchanged V_{clamp} and the enhanced V_{op}.

There is another concern regarding the turn-ON process of SCR in this solution. Unlike common fully controlled switches, such as MOSFETs or IGBTs, the turn-ON of an SCR is relatively slow. It takes substantial time for the gate region carriers to turn ON the remaining active region and anode–cathode voltage to drop. SCRs cannot conduct a high current

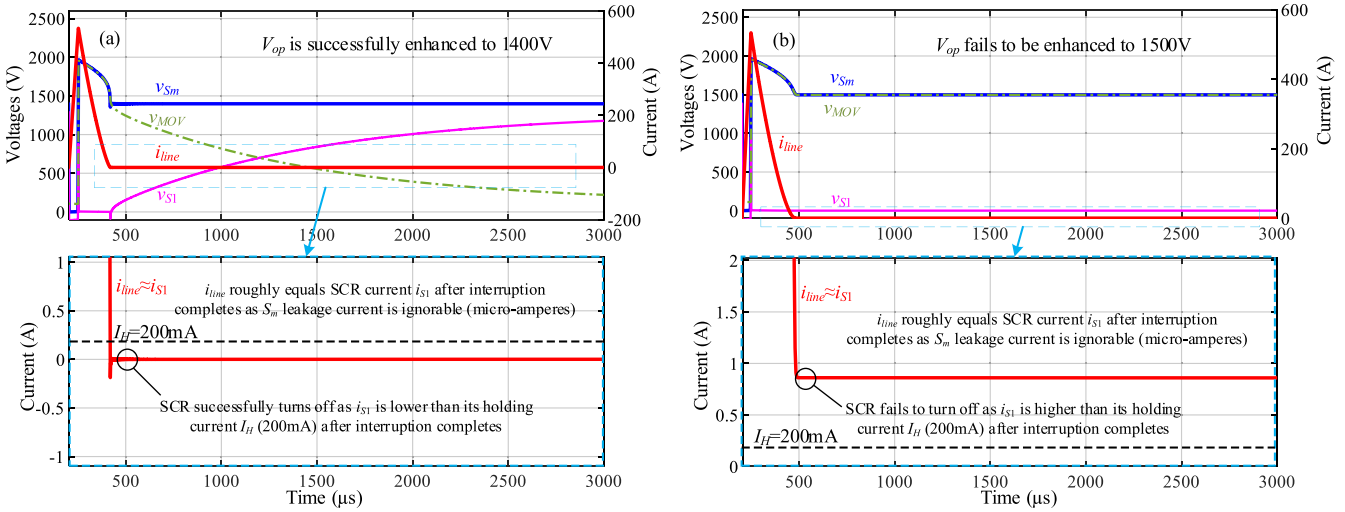

FIGURE 14. **LTspice-simulated voltage clamping demonstration of a semicontrol SCR-MOV clamping circuit. (a) V_{op} is enhanced to 1400 V, and the OVR is reduced to 1960 V/1400 V=1.4 at a 500 A interruption. (b) V_{op} fails to be further enhanced to 1500 V.**

before the carrier diffusion process is completed, which results in a limited *di/dt* capability. However, in SCR-MOV clamping circuits, the *di/dt* in the auxiliary SCR is extremely high due to the fast switching speed of the main switch and large fault magnitude. Thus, a high-SCR *di/dt* capacity is always required in this solution, which might cause overdesign in terms of device surge current ratings and increased total cost and size. It is noted that, without a properly designed *di/dt* capacity, the reliability of an SCR-MOV clamping circuit will be significantly impacted, as the MOV will be subject to a constant overvoltage if the SCR is damaged, which will eventually lead to a thermal breakdown.

3) Gap-MOV voltage clamping circuits are also passive solutions. Its sparkover during turn-ON and recovery during turn-OFF are both completely automatic, depending on the specific gap breakdown voltage threshold and holding current. It features a low-OVR, high-current handling capability, simple structure, and relatively low cost. However, the biggest problem with this solution is its lifetime, as arcing and burning occur across the gap during fault interruption operations. The gap stability issue is also a concern. It has been revealed that the breakdown voltage fluctuation of the gap device can be up to 40% with similar discharging testing condition, which might affect the practical performance of this type of clamping circuit [31], [32].

IV. DC-BLOCKED MOV VOLTAGE CLAMPING CIRCUITS

A. TECHNICAL SOLUTION#2: REDUCING PEAK CLAMPING VOLTAGE TO REDUCE OVR

Equation (1) also indicates that the OVR can be reduced by decreasing peak clamping voltage V_{pk}. Directly using a lower voltage MOV subject to the original V_{op} absolutely leads to significant leakage current. Therefore, it is necessary to use a component that can block the static dc voltage to the MOV while not affecting its transient clamping operations during the interruptions. An example is given below by adding a dc-blocking capacitor in series with a lower voltage MOV.

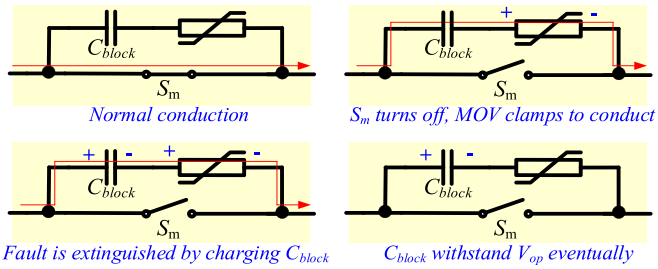

FIGURE 15. **Operation sequence of dc-blocking capacitor-based MOV voltage clamping circuits [21], [33].**

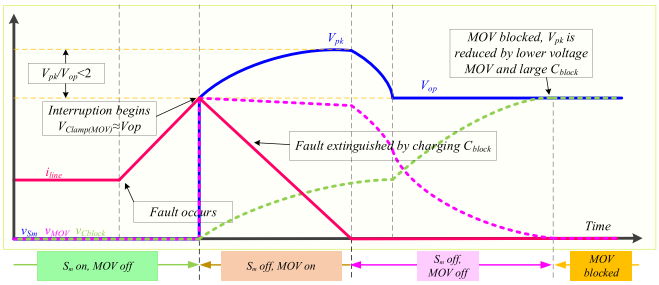

FIGURE 16. **Working principles of dc-blocking capacitor-based MOV voltage clamping circuits.**

1) ADDING DC-BLOCKING CAPACITORS WITH MOVS

Adding a large value capacitor with a lower voltage MOV (C-MOV) is effective to reduce V_{pk} of the total voltage clamping circuit. Figs. 15 and 16 show the circuit topology, operation sequence, working principles, and critical waveforms of the C-MOV voltage clamping solution, as summarized in [21] and [33].

The major difference between this solution and all the above-mentioned classical MOV and dc disconnecting MOV-based solutions is its fault extinguishing impedance nature. The voltage overshoot $V_{pk}-V_{op}$ to extinguish system fault current is provided by the MOV clamping voltage in classical solutions. Alternatively, for this specific C-MOV solution, the clamping voltage of the MOV is selected roughly equal to V_{op}. As a result, the fault current increasing trend is stopped in a timely manner by the MOV clamping; thereafter, the voltage overshoot $V_{pk}-V_{op}$ to extinguish fault current is provided by charging a series-connected dc-blocking capacitor C_{block} during the fault interruption process.

Moreover, after the fault current drops down to zero, MOV voltage will gradually decrease, while C_{block} voltage will increase within tens of milliseconds to several seconds. Eventually, the dc bus voltage will mainly drop on the capacitor C_{block} and almost no voltage drops on the MOV. In this case, the leakage current through a lower voltage MOV is effectively minimized and the clamping OVR is reduced.

B. ADVANTAGES AND LIMITATIONS OF DC-BLOCKED MOV-BASED VOLTAGE CLAMPING CIRCUITS

The major advantage of the C-MOV solution is that it is completely passive, which means the complexity or cost of an extra auxiliary switch, current detection unit, control feedback, and gate-drive unit of other solutions can all be avoided. Since only MOV and capacitor are used in this simple circuit, it will work with good robustness and reliability. In this solution, the leakage current of the total clamping circuit is determined by the blocking capacitor leakage, which is relatively low compared with the leakage current of other solutions, which depends on active switches or spark gap leakage characteristics, Besides, the OVR of this solution is decoupled from the MOV characteristics, which can be flexibly tuned by changing C_{block} value.

The disadvantage of this solution is also obvious. For classical MOV or disconnecting MOV-based solutions, the OVR at different system parameters, including line inductances (*di/dt*) and fault magnitudes, is determined by the MOV characteristics in the clamping region, which is relatively stable. However, the OVR of the C-MOV solution is greatly affected by the system parameters. For example, a higher line inductance (lower *di/dt*) or higher fault current level will lead to a higher OVR. It means that the generality of this solution to fit for different systems is relatively limited. SSCBs based on this clamping circuit are more suitable for those specific systems with clear parameters' definitions/variations.

V. EXPERIMENTAL EVALUATION

A. C-MOV VOLTAGE CLAMPING CIRCUIT

In the literature, the C-MOV circuit has been demonstrated at a very low voltage range and a relatively high OVR of around 3.69 [21]. To explore the feasibility of C-MOV circuit at a higher voltage range and a lower OVR performance, a C-MOV voltage clamping circuit-based SSCB prototype is implemented, as shown in Fig. 17. Specific dcCB prototype information, including nominal and fault ratings, and components design details of the clamping circuit are shown in Table 1. Compared with the similar C-MOV design, as presented in [21], the V_{op} in the experiment is increased to 1000 V, and the circuit parameters are optimized to reduce the OVR. A large blocking capacitor C_{block} value of 150 μF is used, and an MOV with about 1000 V fault clamping voltage is selected. The C_{block} of 150 μF is selected to satisfy our targeting OVR lower than 1.4 at fixed dc system voltage V_{DC} (roughly equal to V_{MOV}) of 1000 V, $L_{line} = 80$ μH, and $I_{line} = 630$ A. It is calculated by $C_{block} \times (V_{Cblock})^2 \approx L_{line} \times (I_{line})^2$.

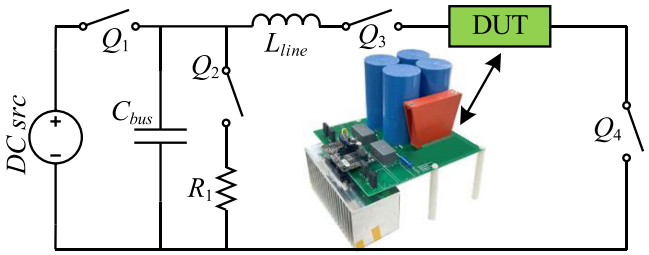

FIGURE 17. Experimental schematic of the short-circuit interruption test, showing the C-MOV voltage clamping circuit-based SSCB prototype.

TABLE 1. C-MOV-Based dcCB Prototype Design Information: System and Component Parameters

Parameter	Description	Parameter	Description
V_{DC} (V_{op})	1000V	*OVR*	<1.4
I_{rated}	100A	S_m	1.2 kV, 450 A
I_{fault}	6 × I_{rated}	C_{block}	150 μF
L_{line}	80μH (130μH)	MOV	680 V DC @ 1 mA leakage, 1060 V clamping

During the test, the fault is initialized by another controllable switch in the test loop, and the SSCB device under test (DUT) is only responsible for fault interruption. After each fault interruption and dc voltage buildup, the C_{block} needs to be discharged by resistors before the next short-circuit test.

Table 2 presents the components' details and descriptions of a short-circuit interruption testing setup, as shown in Fig. 17. A 10 kV/1 A dc source is used to charge the testing dc bus capacitor bank C_{bus} through a mechanical contactor Q_1. After each testing cycle, C_{bus} discharges through a resistor R_1 and a mechanical contactor Q_2. Q_3 is an IGBT power module used to initialize short-circuit faults during the test. Q_4 is a mechanical contactor that serves as an isolation disconnect switch for a breaker. The DUT in Fig. 17 contains the main electronic switch S_m and C-MOV voltage clamping circuit.

Fig. 18 shows the testing results of the short-circuit interruption with a line inductance $L_{line} = 80$ μH. DUT voltage bump, MOV voltage clamping, and blocking capacitor charging are all consistent with the prior analysis. The 630 A fault

TABLE 2. Short-Circuit Interruption Testing Setup Parameters

Parameter	Description	Parameter	Description
DC src	10kV/1A	R_1	100 Ω
Q_1	Mechanical contactor (charging)	Q_3	3.3 kV, 2 kA
C_{bus}	36mF	Q_4	Mechanical contactor (disconnect)
Q_2	Mechanical contactor (discharging)	DUT	C-MOV based SSCB prototype

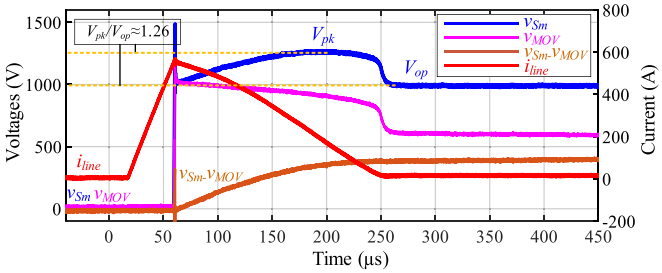

FIGURE 18. Experimental results of the C-MOV clamping circuit at 1000 V/630 A interruption test when L_{line} = 80 μH.

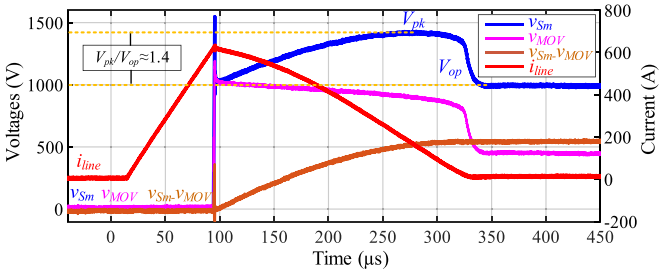

FIGURE 19. Experimental results of the C-MOV clamping circuit at 1000 V/630 A interruption test when L_{line} = 130 μH.

current is extinguished in 190 μs. The peak clamping voltage V_{pk} is only 1260 V, which successfully achieves a low OVR of 1.26. It is noted that the first DUT voltage spike is ignored, which will be explained in Section V-B.

Experimental validation with different L_{line} values is then conducted. Fig. 19 shows testing results at all same conditions except that L_{line} is increased to 130 μH. The fault interruption duration is elongated to 230 μs due to a high fault energy stored in the system line inductance, which also explains the DUT voltage bump enhanced to 1410 V. The OVR is increased to 1.41 at higher line inductances, which is consistent with the analysis in Section IV-B. It is noted that the voltage of the dc-blocking capacitor V_{Cblock} is included in $v_{Sm}-v_{MOV}$ in Figs. 18 and 19, which will be explained in Section V-B.

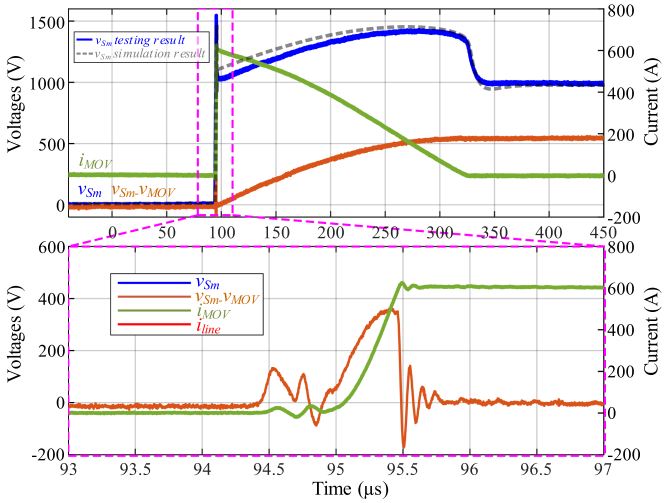

FIGURE 20. Experimental results when L_{line} = 130 μH, showing voltage spike caused by C-MOV branch parasitic inductance L_{stray} coupled high *di/dt* as compared with simulation.

B. EFFECT OF LAYOUT STRAY INDUCTANCE

Both Figs. 18 and 19 show an observation of a small voltage bump in the $v_{Sm}-v_{MOV}$ measurement, which leads to the DUT voltage spike simultaneously. This voltage spike might be higher than the following voltage bump and, thus, affecting the total OVR of the clamping circuit, which is worth further investigation.

Ideally, the voltage spike should not happen if there are only MOVs and capacitors in the clamping circuit branch. However, in reality, there is always some stray inductance L_{stray} resulting from the circuit traces/connection. Therefore, the measurement of $v_{Sm}-v_{MOV}$ can be regarded as $v_{Lstray}+v_{Cblock}$. Fig. 20 shows the detailed voltage and current waveforms. The voltage spike is synchronous with the MOV current rising. It implies that the voltage spike is caused by the high *di/dt* coupled with L_{stray} of the C-MOV clamping circuit branch.

A simulation study is conducted in LTspice to validate the above analysis. An L_{stray} = 240 nH is placed in the LTspice simulation model and the corresponding DUT voltage is demonstrated by a gray dashed line in Fig. 20 for comparison. The resulting voltage spike is consistent with experimental measurements, which validates the effect of practical circuit layout on the OVR performance. It is noted that the slight difference in the following long voltage bumping process is caused by the discrepancy of MOV models used in the simulation.

It needs to be further explained that this voltage spike is ignored in the OVR calculation as it can be effectively reduced by optimizing the C-MOV branch circuit layout. Fig. 21 shows the parametric study as L_{stray} reduces by printed circuit board (PCB) layout optimization. When L_{stray} < 200 nH, the DUT voltage spike is lower than the following voltage bump V_{pk}. In this case, its impact on the OVR estimation of the total clamping circuit can be ignored.

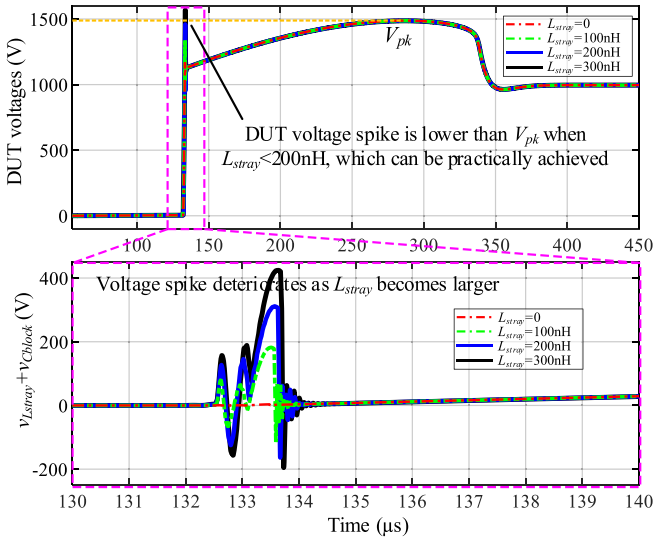

FIGURE 21. Study of DUT voltage spike variation with different L_{stray} values at 1000 V/630 A interruption condition.

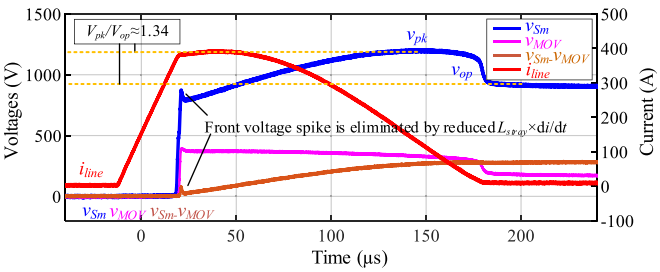

FIGURE 22. Experimental results of the C-MOV clamping circuit at 900 V/393 A interruption test with reduced *di/dt*, showing eliminated front voltage spike.

Since the voltage spike is caused by the high *di/dt* coupled with L_{stray} of the C-MOV clamping circuit branch ($L_{\text{stray}} \times di/dt$), it is expected that the front voltage spike can also be eliminated by reducing the *di/dt*, which can be realized by slowing down switching OFF the speed of the main switch.

To validate this analysis, Fig. 22 shows the experimental results of the C-MOV clamping circuit at 900 V/393 A interruption test when $L_{\text{line}} = 80$ μH with reduced *di/dt*. It is noted that the MOV used in the updated test has a total clamping voltage of around 900 V, which is selected close to the original MOV with 1000 V clamping voltage. The C_{block} value in the updated test is also reduced from 150 to 75 μF. This change is due to a lower testing current level in the updated test, which will not affect the purpose of front voltage spike validation. Fig. 22 clearly indicates that the DUT front voltage spike is successfully eliminated by reducing the $L_{\text{stray}} \times di/dt$, which is consistent with the above-mentioned analysis.

C. OVR AT DIFFERENT DI/DT FAULTS

During the fault interruption process, the energy accumulated in line inductance will be mainly transferred to charge the dc-blocking capacitor C_{block} while partially consumed by the

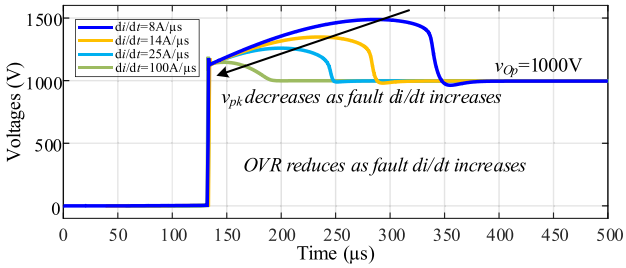

FIGURE 23. Study of OVR variation with different fault *di/dt* at 1000 V/630 A interruption condition.

ON-state MOV resistance. Therefore, the major DUT voltage bump (V_{pk}) is expected to increase (OVR also increases) at a larger L_{line} value or a higher fault magnitude, which can be observed in Figs. 18 and 19.

Fig. 23 further shows a parametric study of V_{pk} with an increased fault *di/dt*. At a fixed dc operating voltage V_{op}, *di/dt* increasing is equivalent to L_{line} reduction (lower line inductance energy). It indicates that as *di/dt* rises from 8 to 100 A/μs, V_{pk} gradually decreases from 1500 to 1130 V, meaning that the OVR decreases from 1.50 to 1.13. It implies that the C-MOV clamping circuit is preferred for those compact dc systems that feature a low line impedance and a high fault *di/dt*. To summarize, as an inductor-capacitor-MOV (LC-MOV) resonant circuit, the main factors controlling the effectiveness of the C-MOV circuit to reduce OVR are system line inductance L_{line} (fault *di/dt*), fault current magnitude I_{fault}, and C_{block} values. Considering the same fault tripping threshold I_{fault}, for a system with low L_{line} (high fault *di/dt*), it is acceptable to appropriately reduce the C_{block} while still satisfying the low-OVR requirement. Reversely, for a system with high L_{line} (low fault *di/dt*), it is necessary to use a large C_{block} value to compensate for the excessive inductive energy to satisfy the same OVR requirement.

VI. SURVEY OF EXISTING LOW-OVR CLAMPING CIRCUITS

The experimental evaluations of C-MOV clamping circuit in this study are compared with other existing SSCB clamping circuits in Table 3. There are two major categories of dc disconnecting MOV and dc-blocking MOV, respectively. A total of four configurations on SW-MOV, SCR-MOV, Gap-MOV, and C-MOV are summarized based on the analysis in this article. Different SSCB voltage clamping solutions are evaluated and compared with respect to circuit type, peak clamping voltage V_{pk}, maximum operating voltage V_{op}, OVR, cost, compactness, and reliability evaluations. Although V_{op} and V_{pk} are provided in the comparative study, these two parameters are not treated as pivotal indicators in the comparison and evaluation. Instead, the switching overvoltage ratio $\text{OVR} = V_{\text{pk}}/V_{\text{op}}$ is used as a core performance indicator. Thanks to the nondimensionalizing calculation, the effect of different V_{op} and V_{pk} values can be homogenized for a fair comparison.

TABLE 3. Survey of Existing Low Clamping Overvoltage Ratio Solutions for DC Breakers

Category	Configuration	References	Circuit Type	V_{pk}	V_{op}	Overvoltage Ratio (OVR)	Evaluations
DC Disconnecting MOV	SW-MOV	[21]	Active	45 V	32.5 V	1.38	Pros: Compact, adjustable trigger time on fault conditions Cons: Extra cost on auxiliary sensor and gate drive, fair reliability;
		[22], [23]	Active	N/A	N/A	N/A	
		[24]	Active	872 V	600 V	1.45	
		[25]	Active	1083 V	720 V	1.50	
		[26]	Active	799 V	600 V	1.33	
	SCR-MOV	[27]	Passive	2840 V	2000 V	1.42	Pros: Reduced auxiliary components, highly compact with self-firing SCR Cons: Reliability issue at high d*i*/d*t*, limited OVR reduction because of SCR current limit
		[29]	Active	1790 V	1250 V	1.43	
		[25]	Active	1134 V	720 V	1.58	
		[30]	Active	871 V	375 V	2.32	
	Gap-MOV	[31], [32]	Passive	3887 V	3240 V	1.20	Pros: lowest OVR reported Cons: unstable trigger level, arcing degradation
DC Blocking MOV	C-MOV	[21]	Passive	120 V	32.5 V	3.69	Pros: cost-saving and high reliability using only passive components Cons: large form factor with a large capacitance
		[33]	Passive	N/A	N/A	N/A	
		This work	Passive	1260 V	1000 V	1.26	

According to the comparison, all the presented SW-MOV clamping circuits presented in [21], [22], [23], [24], [25], and [26] are strictly active solutions, which means that extra cost is applied due to the additional active switch, gate drive, feedback control unit, isolated power supply, and current sensor. Their reliability is, therefore, evaluated as fair because of the complex system configuration. However, the utilization of the active switches makes this solution type free from bulky passive components, thus reducing their overall size. The OVR of the SW-MOV solutions ranges from 1.33 to 1.50, which is relatively low compared with other solution types.

Semicontrolled SCR-MOV clamping circuits are realized by active or passive method. Zhao et al. [25], [29], [30] show active solutions, which also utilize separate gate driver, feedback unit, isolated power supply, and current sensor to control the SCR ON and OFF. A self-firing circuit is featured in [27] by placing a breakover diode or a low-voltage MOV across the SCR anode and gate terminals, which reduces total cost and size. However, the *di/dt* issue of SCRs, as mentioned in Section III-E, is not addressed in existing works; thus, their reliability index is evaluated as fair. The OVR of the SCR-MOV solutions ranges from 1.42 to 1.58, which is overall higher than the SW-MOV solutions.

Gap-MOV-based dc disconnecting MOV solution is first discussed in [31] and further explored in [32] for dc breakers. It achieves the lowest OVR among all clamping circuits, claimed to be 1.20, although the phenomenon of spark gap complete recovery and eventually withstanding dc bus voltage is not fully presented in this work. Besides, high-voltage spark gaps are relatively expensive with large size, thus affecting its compactness and cost evaluation indices. The stability concern of spark gaps is also revealed in this work, which impacts its reliability evaluation.

C-MOV clamping circuits are previously presented in [21] and [32]. However, the testing condition and parameters design are not optimized in those works. Thus, this solution is reimplemented in this article for a comprehensive evaluation. Since only passive components are used in this simple configuration, the cost saving and reliability of this solution are ranked high. However, a large blocking capacitor value is required for realizing a low OVR, which affects its compactness index. By optimizing the parameter design, a low OVR of 1.26 is demonstrated in this work, which lies in between that of gap-MOV and SW-MOV solutions.

To summarize the contributions of this work, although there exists prior art that focuses on the topic of low-OVR voltage clamping circuits [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], currently, there is no such systematic survey, analysis, and experimental evaluation conducted to comprehensively review the existing low-OVR solutions.

To fill this technical gap, this article reviews and evaluates various clamping circuits reported in representative dcCB literature, focusing on the OVR reduction performances. The circuit categorization, basic working principles, peak clamping voltage, maximum operating voltage, OVR, cost, compactness, and reliability of different voltage clamping circuits are systematically evaluated, which is expected to serve as a guideline for engineers to compare and select suitable voltage clamping circuits for designing dc breakers oriented at overvoltage suppression performance.

Moreover, this article strives to provide specific technical contributions regarding the C-MOV voltage clamping circuit based on the review. In the literature [21], the C-MOV circuit has been demonstrated at a limited voltage range and a relatively high OVR of around 3.69. To explore the feasibility of C-MOV circuit at a higher voltage range and a lower

OVR performance, a C-MOV voltage clamping circuit-based SSCB prototype is implemented in this article. Through the work presented in this article, it has been validated that a significantly low-OVR performance of 1.26 can be realized at 1000 V nominal dc voltage, which greatly enhances the practicality of C-MOV-type voltage clamping circuit in real dcCB applications.

VII. CONCLUSION

This article summarizes voltage clamping circuit solutions for dcCBs, especially SSCBs, pursuing a low OVR below 2.0. The drawbacks of MOV-only voltage clamping circuits and their variants are first introduced. Their clamping OVR is usually as high as 2.0, which might inject excessive voltage interference to dc system and enhance the count of main solid-state switches required. Existing low-OVR voltage clamping circuits, including SW-MOV, SCR-MOV, gap MOV, and C-MOV, are then reviewed and categorized based on the nature of the configurations. Their basic working principles are analyzed and studied by simulations. Intrinsic advantages and limitations of different solutions are revealed and compared. A C-MOV clamping circuit is selected and prototyped in this article. A low clamping OVR of 1.26 is experimentally validated at 1000 V/630 A condition. Finally, a comparison of the existing low-OVR clamping circuits with the experimental results from this work is presented, which provides comprehensive evaluations in terms of circuit type, peak clamping voltage, maximum operating voltage, OVR, cost, compactness, and reliability evaluations. This article is expected to serve as a guideline for engineers to compare and select suitable voltage clamping circuits for designing dc breakers oriented at overvoltage suppression performance.

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