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Synthesis and Comparison of Soft-Switched Operating Modes of a Series Resonant Balancing Converter for Bipolar DC Grids

SACHIN YADAV [1] (Graduate Student Member, IEEE), PAVOL BAUER [1] (Senior Member, IEEE), AND ZIAN QIN [1] (Senior Member, IEEE)

Delft University of Technology, 2628CD Delft, The Netherlands

CORRESPONDING AUTHOR: ZIAN QIN (e-mail: z.qin-2@tudelft.nl).

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ABSTRACT This article discusses the various operating modes of a series resonant balancing converter for bipolar dc grids. It is shown that the converter can be operated in both the capacitive and inductive regions with respect to the resonant frequency of the *LC* tank. Furthermore, concerning the pulse width modulation signals to the switches, the converter can either be operated by controlling the phase shift between the converter half bridge legs or the duty cycle of the half bridges. A qualitative comparison of the different modes proves that a) the phase shift modes have better soft switching capabilities, b) the capacitive phase shift mode can show zero voltage switching at switch turn-ON in the whole operating range, c) the losses in case of capacitive phase shift mode shows best performance at low load power, d) the inductive region power modes show lower rms current for the same power flow compared with capacitive region modes which lead to lower losses at higher output power. The simulation and experimental results depict the operation of all the modes. Finally, a prototype is designed to validate all operating modes, demonstrating >99% system efficiency at 1.75 kW.

INDEX TERMS Dc–dc power conversion, dc grids, modulation, resonant power conversion, soft-switching converters, soft-switching techniques, zero current switching (ZCS), zero voltage switching (ZVS).

I. INTRODUCTION

Bipolar dc grids have many advantages over unipolar dc grids. First, in the case of solid grounding of the neutral, a line-ground fault imposes half the full pole–pole voltage on the insulators. Due to low voltage, a lower current flows through the ground fault. Second, bipolar dc grids have higher power transfer capacity than unipolar dc and three-phase ac grids at the same peak system voltage levels [1]. This advantage is vital for large distribution grids with long cable lengths. Third, more than one voltage level is available in a bipolar dc grid. However, when an asymmetric load is connected in a bipolar dc grid, the neutral voltage can shift from ground potential. According to IEC 60364 Part 5, any voltage above 50 V is potentially dangerous for direct contact [2]. To avoid this issue, balancing converters are essential to balance the voltage at the two poles dynamically.

Several topologies of balancing converter are found in literature [3], [4], [5], [6], [7], and [8]. Most topologies have limited soft-switching (ZVS turn-ON) capability. ZVS is essential in reducing the electromagnetic interference emissions from the power converters [9], [10]. The buck–boost and other derived topologies (Cuk, interleaved buck–boost, dual buck–boost) can exhibit ZVS turn-ON using the triangular current modulation scheme [10], [11]. However, this comes at the cost of bulky passive components. Furthermore, these converters exhibit asymmetrical losses in the semiconductor switches. The Cuk, dual buck–boost, and interleaved buck–boost converter has multiple inductors. Moreover, they require large dc filter capacitors because of the large current ripple [10]. Hence, designing these converters can be pretty challenging.

Resonant power topologies can be better alternatives for the challenges of the topologies mentioned previously. They

can exhibit ZVS or zero current switching (ZCS) in all the switches. Furthermore, due to the combination of inductors and capacitors as energy-storing elements, the size of the passive components can be much smaller. This is because of the high energy density of a capacitor compared to an inductor. The research in this topology is well-established, primarily within the context of switched capacitor converters. Early studies revealed that incorporating a small inductor in series with the capacitor facilitates ZCS operation of the switches and reduces current peaks during capacitor charging and discharging [12], [13], [14]. Subsequent investigations demonstrated that the converter achieves ZVS turn-ON for all switches when the two half-bridges are operated with a phase shift and the switching frequency exceeds the resonant frequency of the *LC* tank [15], [16], [17]. Despite these advancements, a comprehensive synthesis of all possible operating modes for this converter remains absent in the literature.

A series resonant converter with a series connection of an inductor and a capacitor can be a promising solution for balancing a bipolar dc grid. This topology has been utilized in the capacitor balancing in multilevel converters and battery balancing applications [15], [16], [18]. The literature shows that the topology operates in the inductive region and with phase shift control. These literature do not show the converter operation at different power flows. At low power flows, ZVS turn-ON of the switches are lost for these applications. Furthermore, Vasic et al. [19] presented this converter as a resonant switched capacitor converter. The converter operates in an inductive region with phase shift control. Furthermore, the authors demonstrate that the converter loses ZVS turn-ON at low power loads. To address this, they propose pulse skipping modes to extend the soft switching range, resulting in ZVS turn-ON for two switches and ZCS turn-ON for the other two. This mode is similar to the duty cycle modes proposed in this article. Zhuang et al. [20] utilized this topology to interface distributed photovoltaics with medium voltage dc grids, leveraging the series connection of the series resonant circuits and operating exclusively in the inductive region. Similarly, the authors in [21] and [22] employed this topology for balancing converters but did not explore its potential in the capacitive region, focusing only on inductive region operation with phase shift. This article shows that the converter can be operated in several other modes. Furthermore, all the operating modes are compared in terms of their soft switching capabilities, ZVS range, and power losses. Thus, the contributions of this article are as follows.

1) It is found that operating the series-resonant balancing converter cannot fully balance the bipolar dc grid when operating at the resonant frequency. Hence, this article proposes the switch modulation methods to solve the problem.
2) This article proposes and synthesizes the different soft-switched operating modes for the series-resonant balancing converter.

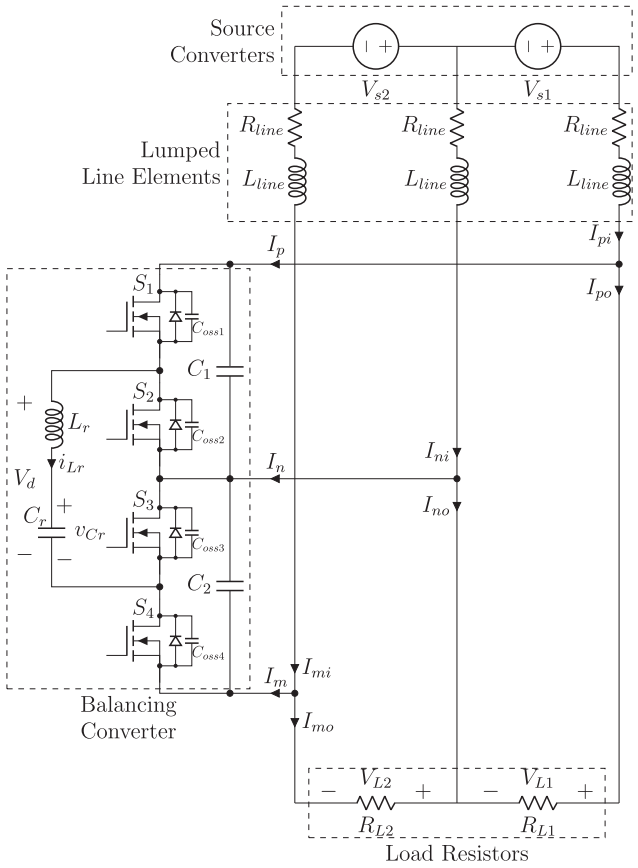


FIGURE 1. Series resonant balancing converter schematic and its application in the bipolar dc grid.

3) This article compares the converter's various operating modes and modulation schemes, which ensure soft-switching.
4) This article reveals the limitations of achieving the ZVS turn-ON when operated in inductive phase shift mode. Furthermore, it is found that ZVS turn-ON can be achieved in the whole operating range of the converter only if the converter is operating in capacitive phase shift mode.
5) The tradeoffs of using the converter in inductive and capacitive regions are also discussed.

The rest of the article is organized as follows. Section II describes the topology and its limited usage when operated at the resonant frequency. Section III provides the synthesis of various soft-switched operating modes of the converter. Section IV provides the power flow analysis of the converter under the different operating modes. Section V provides a holistic comparison of all the converter operating modes. After that, Section VI provides the simulation and experimental results of the converter operation. Finally, Section VII concludes this article.

II. SERIES-RESONANT BALANCING CONVERTER

The schematic of a series resonant balancing converter and its application in a bipolar dc grid is shown in Fig. 1. The

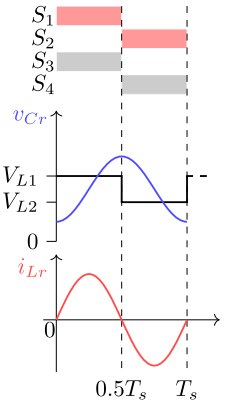


FIGURE 2. Voltage across the resonant tank when the converter operates at the resonant frequency.

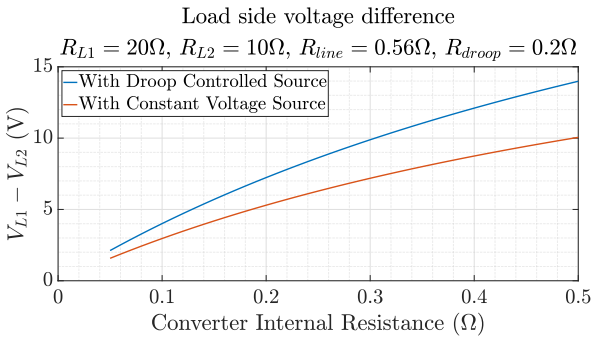


FIGURE 3. Voltage difference with varying converter voltages when the converter is operated at the resonant frequency.

converter consists of four switches $S_1 - S_4$, resonant inductor L_r, and resonant capacitor C_r. V_{s1} and V_{s2} represent the voltage sources making up the bipolar dc grid; R_{line} and L_{line} represent a distribution line; R_{L1} and R_{L2} represent the loads connected in the grid

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \tag{1}$$

In the real world, the converter would have a finite internal resistance, which can be a combination of the resistances of the switch, inductor, and capacitors. Suppose the converter is operated at the resonant frequency given by (1). In that case, the converter's internal resistance (represented by R_{conv}) limits the current flow from one pole to the other. The voltage across the resonant tank along with C_r voltage and L_r current in one switching cycle (T_s represents the switching cycle duration) is shown in Fig. 2. The first harmonic of the voltage across the resonant tank contributes to the power flow through the converter [23]. The first harmonic value of the voltage difference is given by the following:

$$V_{d,1} = \frac{\pi}{4}(V_{L1} - V_{L2}). \tag{2}$$

The resonant converter takes power from one of the poles and supplies it to the other. The current flowing from one pole to the other can be calculated using the following:

$$I_{\text{no}} = \frac{V_{L1} - V_{L2}}{2R_{\text{conv}}}. \tag{3}$$

The current output from the resonant converter decreases the voltage difference between the poles. However, a steady-state voltage difference is always required to flow the current through the resonant converter. Hence, operating the converter at the resonant frequency does not achieve the desired goal of power and voltage balancing. Fig. 3 shows this effect of voltage deviation with two kinds of voltage sources (droop-controlled and constant voltage source). Therefore, it becomes necessary to have alternative modulation schemes for the resonant converter to balance the bipolar dc grid. Furthermore, operating the converter at the resonant frequency cannot lead to the ZVS turn-ON of all the switches. However, ZCS is achieved for all the switches in one switching instant. Therefore, in the following sections, different switching patterns are synthesized, which ensure either complete or partial soft switching of the resonant converter.

TABLE 1 Possible Switching States for the Converter Ignoring the Dead Time States

S_1	S_2	S_3	S_4	Possible?	Switch state name
0	0	0	0	✗	-
0	0	0	1	✗	-
0	0	1	0	✗	-
0	0	1	1	✗	-
0	1	0	0	✗	-
0	1	0	1	✓	SP3
0	1	1	0	✓	SP2
0	1	1	1	✗	-
1	0	0	0	✗	-
1	0	0	1	✓	SP4
1	0	1	0	✓	SP1
1	0	1	1	✗	-
1	1	0	0	✗	-
1	1	0	1	✗	-
1	1	1	0	✗	-
1	1	1	1	✗	-

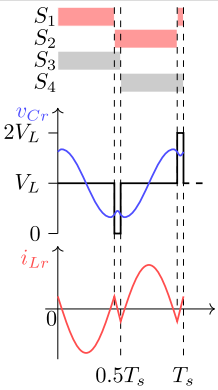
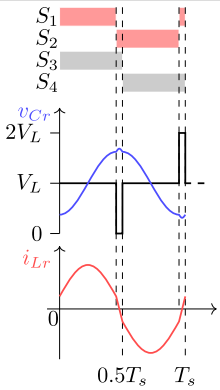
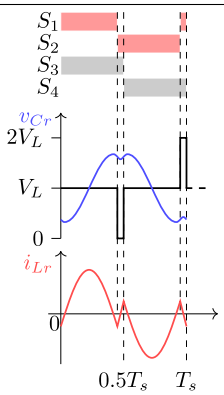
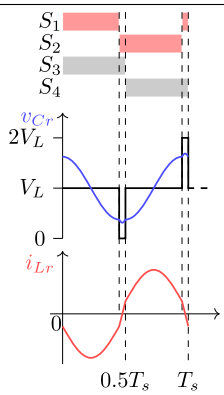
III. SWITCHING PATTERN SYNTHESIS

The switching pattern synthesis in this section only concerns the modulation schemes that can guarantee the semiconductor switches' soft switching (ZVS and ZCS). This section provides a qualitative and quantitative description of the various possible modulation schemes for the resonant balancing converter.

The resonant converter consists of four switches S_1-S_4. Switches S_1 and S_2 and S_3 and S_4 form half bridges. Hence, these pairs cannot be switched simultaneously with a dead time between them. Furthermore, at any moment, two switches must conduct L_r current either through the MOSFET channel or its body diode. Considering these constraints, Table 1 shows the possible switch combinations.

The possible states are SP1, SP2, SP3, and SP4. It should be noted that only SP1 and SP3 states allow for active power flow through the converter because the neutral is connected to poles through the converter. The operation at the resonant frequency

TABLE 2 Switching Patterns in Phase Shift Mode

Switching pattern	Capacitive region	Inductive region
SP1 → SP2 → SP3 → SP4		
SP1 → SP4 → SP3 → SP2		

of the converter elaborated in the previous section consisted of SP1 and SP3 only. Furthermore, states SP2 and SP4 contribute to the reactive power flow in the converter because the neutral is not connected to the poles.

For power flow between the + and – poles, both SP1 and SP3 should always be present. Otherwise, there is no active power flow from one pole to another. This article recognizes two distinct classes of patterns for achieving soft switching, which imparts different voltages and currents on the resonant tank. The first class is referred to as phase shift mode. This mode occurs when all the switching states are used to form the switching pattern. From the principles of permutations and combinations, 6 ($4! \div 4 = 6$) switching patterns are possible. However, there is an added constraint that switching states SP2 and SP4 cannot be adjacent.

Hence, only two patterns are eventually possible for the phase shift mode. The patterns and the resulting voltage across the resonant tank in one switching cycle are shown in Table 2 when the bipolar dc grid is balanced (when $V_{L1} = V_{L2} = V_L$). All the switches operate at 50% duty cycle. Furthermore, there is a phase shift between the switches of the upper half-bridge (consisting of S_1 and S_2) and the lower half-bridge (consisting of S_3 and S_4). In the first pattern, the upper half-bridge leads the lower half-bridge; in the second, the lower half-bridge leads the upper half-bridge.

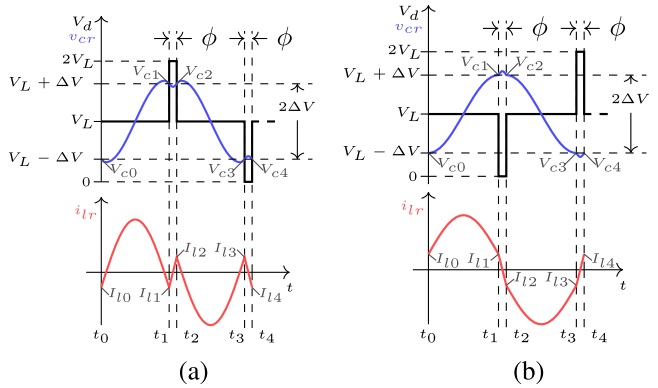


FIGURE 4. Resonant converter states for phase shift modes. (a) Converter states in capacitive phase shift mode with switching pattern SP1 → SP4 → SP3 → SP2. (b) Converter states in inductive phase shift mode with switching pattern SP1 → SP2 → SP3 → SP4.

When SP1, SP3, and either SP2 or SP4 are used, it is called duty cycle mode. This is because the upper and lower half bridges have different duty cycles. It should be noted that the duty cycles are symmetric. This means the duty cycle of S_1 and S_4 are the same. Similarly, the duty cycle of S_2 and S_3 are the same. The different possible switching patterns and the resulting resonant tank voltage waveform in one cycle are shown in Table 3.

IV. ANALYSIS OF OPERATING MODES

This section discusses the power flow through the converter with various operating modes. The analysis assumes that the converter operates at steady-state while balancing the power flow from one pole to another. Hence, the voltages V_{L1} and V_{L2} are the same. For each mode, the analysis is presented for a single switching pattern. The analysis is generic and can be extended for other switching patterns with the corresponding initial value of state variables (L_r current and C_r voltage).

A. PHASE SHIFT MODES

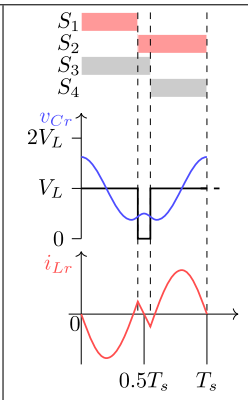
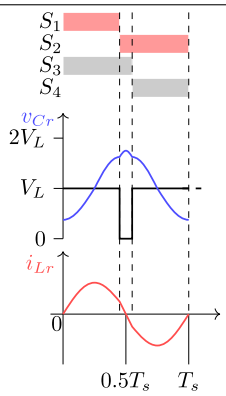
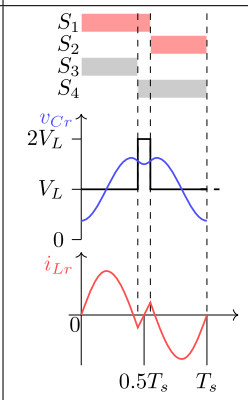
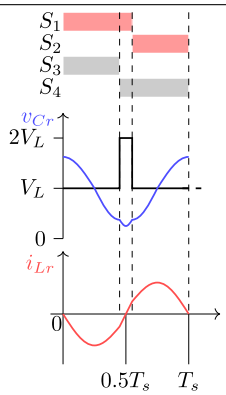
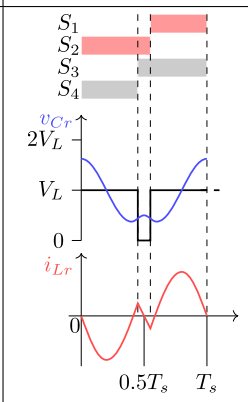
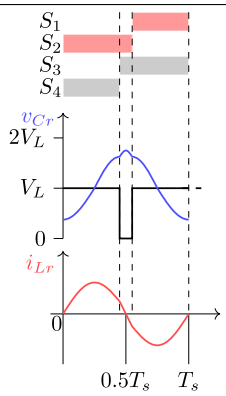
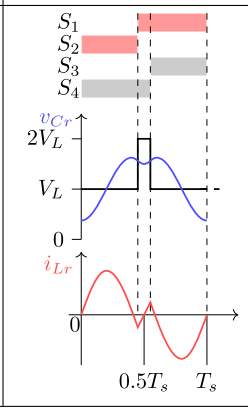
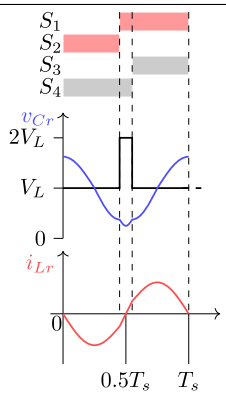
The switching pattern SP1 → SP4 → SP3 → SP2 is used for this mode. The relevant figures are shown below for the convenience of the readers. The figure also shows the initial L_r currents (I_{lx}) and initial C_r voltages (V_{cx}) at the beginning of each switching state.

Specific relationships between the initial currents in phase shift modes can be established in scenarios where the grid is balanced, as detailed in (4). A rigorous proof has been given in the appendix, delineating the underlying principles and calculations substantiating this relationship

$$I_{l0} = I_{l1} = -I_{l2} = -I_{l3} = I_{l4}. \tag{4}$$

C_r voltage is symmetrical with respect to the midpoint voltage of V_L. When the grid is balanced, the voltage of the poles is the same and can be considered equal to V_L. The various initial C_r

TABLE 3 Switching Patterns in Duty Cycle Mode

Switching pattern	Capacitive region	Inductive region
SP1 → SP2 → SP3		
SP1 → SP4 → SP3		
SP3 → SP2 → SP1		
SP3 → SP4 → SP1		

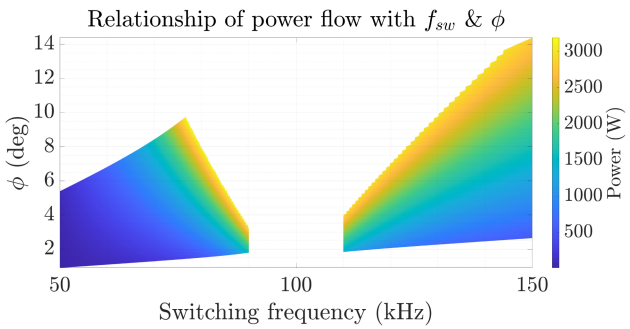


FIGURE 5. Power flow for f_{sw} and ϕ for phase shift mode for the designed converter prototype.

voltage as shown in Fig. 4 can be represented as

$$\begin{aligned} V_{c0} &= V_{c3} = V_{c4} = V_L - \Delta V \\ V_{c1} &= V_{c2} = V_L + \Delta V \end{aligned} \tag{5}$$

where ΔV is the difference between the C_r voltage at the switching instances and V_L. At switching instances, there is a difference of $2\Delta V$ between V_{c0} and V_{c1} and V_{c2} and V_{c3}. With the volt–second principle for the inductor, the duration $t_1 - t_0$ is equal to $t_3 - t_2$ and $t_2 - t_1$ is same as $t_4 - t_3$. Using the solution for the L_r current, these time durations can be found as

$$\begin{aligned} t_1 - t_0 &= \frac{2}{w_0}\left[\frac{\pi}{2} - \tan^{-1}\left(\frac{Z_0 I_{l0}}{V_L - V_{c0}}\right)\right] \\ t_2 - t_1 &= \frac{2}{w_0}\left[\frac{\pi}{2} - \tan^{-1}\left(\frac{-(2V_L - V_{c1})}{Z_0 I_{l0}}\right)\right]. \end{aligned} \tag{6}$$

Using (6), f_{sw} and ϕ can be calculated as

$$\begin{aligned} f_{\text{sw}} &= \frac{1}{2((t_2 - t_1) + (t_1 - t_0))} \\ \phi &= f_{\text{sw}}(t_2 - t_1). \end{aligned} \tag{7}$$

Using (5), (6), and (7), ΔV can be found out as

$$\Delta V = \frac{V_L}{2} \pm \sqrt{\left(\frac{V_L}{2}\right)^2 - I_{l0}^2 Z_0^2 + \tan\left(\frac{\omega_0}{4 f_{\text{sw}}}\right) I_{l0} V_L Z_0}\,. \tag{8}$$

The active power flow through the converter can be found as

$$P_o = 4 f_{\text{sw}} C_r \Delta V\, V_L. \tag{9}$$

Using, (8) and (9), the power flow is given by

$$\begin{aligned} P_o = 4 f_{\text{sw}} C_r V_L \Bigg[&\frac{V_L}{2} \\ &+ \sqrt{\left(\frac{V_L}{2}\right)^2 - I_{l0}^2 Z_0^2 + \tan\left(\frac{\omega_0}{4 f_{\text{sw}}}\right) I_{l0} V_L Z_0} \Bigg]. \end{aligned} \tag{10}$$

A map of the power flow for f_{sw} and ϕ can be created for capacitive and inductive phase shift modes. This map is shown in Fig. 5 for the converter parameters given in Table 4.

TABLE 4 Parameters of the Designed Converter Prototype

Parameter	Value
MOSFET $R_{ds,on}$	25 $m\Omega$
MOSFET C_{oss}	174 pF
MOSFET part number	C3M0025065J1
DC link capacitor (C_1 & C_2)	240 μF
DC link capacitor part number	DCP4G056007GD4KSSD
Resonant frequency (f_r)	100 kHz
Resonant capacitor (C_r)	297 nF
Resonant capacitor part number	CGA9Q1C0G3A333J280KC
Resonant inductor (L_r)	8.6 μH
Core size	PQ 5050
Core material	N95
Core area	332 mm^2
Core volume	37630 mm^3
Air gap	7 mm
Number of turns	11
Conductor area	6 mm^2

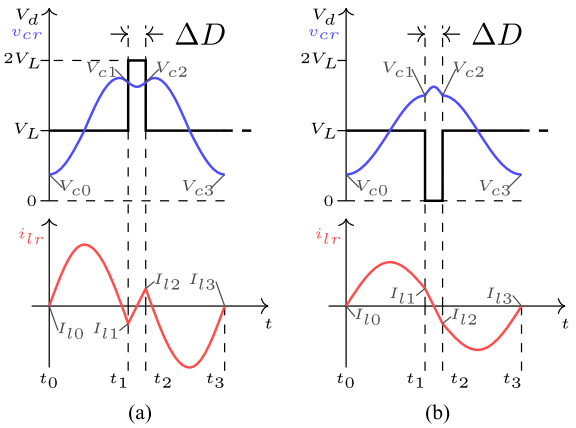


FIGURE 6. Resonant converter states for duty cycle modes. (a) Converter states in capacitive duty cycle mode with switching pattern SP1 → SP4 → SP3. (b) Converter states in inductive duty cycle region with switching pattern SP1 → SP2 → SP3.

B. DUTY CYCLE MODES

An example of the power flow in duty cycle mode is shown in Fig. 6. The switching pattern used in this example is SP1 → SP4 → SP3 for capacitive region and SP1 → SP2 → SP3 for inductive region.

Like the phase shift modes, L_r currents for the duty cycle modes are related as follows:

$$\begin{aligned} I_{l0} &= I_{l3} = 0 \\ I_{l1} &= -I_{l2} \end{aligned} \tag{11}$$

$$\begin{aligned} V_{c0} &= V_{c3} \\ V_{c1} &= V_{c2}. \end{aligned} \tag{12}$$

It should be noted that, unlike the phase shift modes, V_{c0} is not related to V_{c1} through ΔV in duty cycle modes. The time duration $t_1 - t_0$ and $t_2 - t_1$ are given by

$$t_1 - t_0 = \frac{1}{\omega_0}\sin^{-1}\left(\frac{I_{l1}Z_0}{V_d - V_{c0}}\right) \tag{13}$$

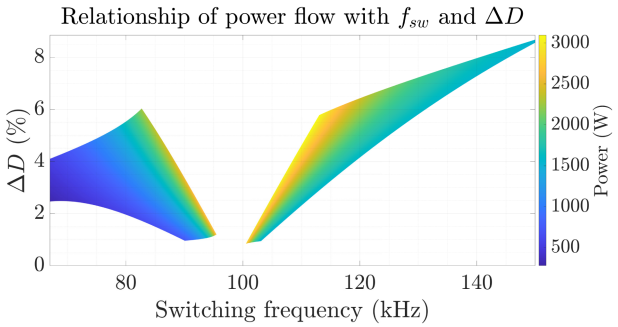


FIGURE 7. Power flow for f_{sw} and ΔD for duty cycle mode for the designed converter prototype.

$$t_2 - t_1 = \frac{1}{\omega_0}\left[\cos^{-1}\left(\frac{I_{l1}Z_0}{\sqrt{I_{l1}^2Z_0^2 + (2V_d - V_{c1})^2}}\right) - \tan^{-1}\left(\frac{-(2V_d - V_{c1})}{Z_0 I_{l1}}\right)\right] \tag{14}$$

$$f_{\text{sw}} = \frac{1}{2((t_2 - t_1) + (t_1 - t_0))}$$

$$\Delta D = f_{\text{sw}}(t_2 - t_1). \tag{15}$$

Finally, the value of V_{c1} and consequently of V_{c2} can be calculated as

$$V_{c1} = V_{c2} = V_d \pm (V_d - V_{c0})\cos(w_0(t_1 - t_0)) \tag{16}$$

where the $\pm$ sign is used to signify a generalized case.

In the duty cycle modes, the V_{c1} is an independent variable that can not be eliminated like in the case of phase shift modes. Hence, an assumption of both V_{c0} and I_{l0} needs to be taken to create a power flow map. f_{sw} and ΔD is calculated using (15). For different values of V_{c0} and I_{l0}, the power map for the capacitive duty cycle and inductive duty cycle modes using the converter parameters given in Table 4 is shown in Fig. 7.

V. COMPARISON OF DIFFERENT MODES

In this section, the various operating modes are compared. First, a qualitative comparison is given from the perspective of the converter's soft-switching capability and ZVS range. The power losses are compared for the operating modes using the analysis provided in Section IV.

A. SOFT-SWITCHING CAPABILITY

The modes discussed above have different soft-switching capabilities. First, only two of four switches have ZVS turn-ON in one switching cycle for the duty cycle modes. This happens for the switches turning on before and after the middle switching state in Table 3. When there is a change between SP1 and SP3, there is ZCS for all the switches. As an example, consider pattern SP1-SP2-SP3. At the beginning of the state, SP1, S_2 and S_4 are turned-OFF, and S_1 and S_3 are turned-ON at zero current. Hence, all the switches achieve ZCS. At the end of SP1, S_1 is turned-OFF. At this instance, L_r current discharges

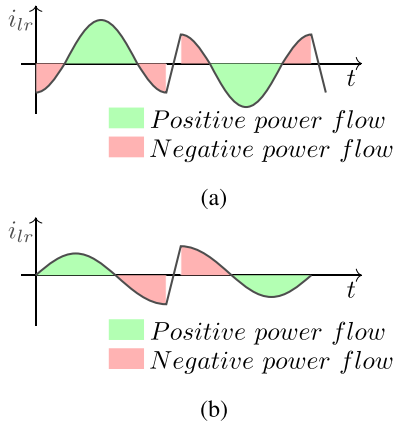


FIGURE 8. Illustration of average power flow in one switching cycle for the capacitive region. (a) Phase shift mode—capacitive region. (b) Duty cycle mode—capacitive region.

the C_{oss} of S_2; hence, S_2 turns-ON with ZVS. In this case, the middle switching state (SP2) has sufficient duration such that L_r current changes direction. At the end of this duration, S_3 is turned-OFF, and L_r current discharges the C_{oss} of S_4, thus preparing it for ZVS turn-ON.

For the phase shift modes, the ZVS turn-ON can be guaranteed for all switches when the converter operates in the capacitive region. This is because L_r current at the switching instances can be guaranteed sufficient amplitude for discharging the C_{oss}. However, if the converter is operated in the inductive region, the ZVS turn-ON capability is limited and depends upon the load current. This is discussed further in the following section.

B. ZVS RANGE

Fig. 8 shows L_r current for a switching pattern in phase shift and duty cycle modes. The area in green shows the power flow from the source to the load; the area in red shows the power flow returning to the source.

In the capacitive region for both operating modes, there are regions of positive and negative power flows in the half cycle. At higher power flow, the region of positive power flow is much larger than that of negative power flow. On the other hand, at lower power flow, the area of negative power flow increases and becomes comparable to that of positive power flow. Thus, it is possible to have zero power flow with ZVS turn-ON at suitable switching instances.

The negative power flow in Fig. 8 can be regarded as reactive power because it does not contribute to the output power flowing to the load. On the other hand, the positive power flow only contributes to the output load power. Fig. 9(a) and (b) shows the ratio of active power flow to the reactive power flow for capacitive phase shift and duty cycle modes, respectively, for the designed converter prototype. The reactive to active power ratio increases as the output power decreases (lower f_{sw}). The ratio is minimal at higher output power (at higher f_{sw}). The reactive power does not contribute

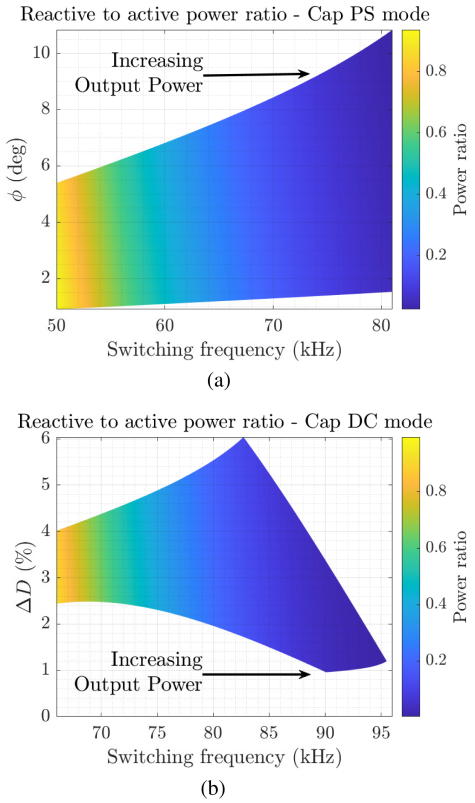


FIGURE 9. Illustration of average power flow in one switching cycle for the capacitive region. (a) Ratio of reactive to active power for capacitive phase shift mode for the converter data given in Table 4. (b) Ratio of reactive to active power for capacitive duty cycle mode for the converter data given in Table 4.

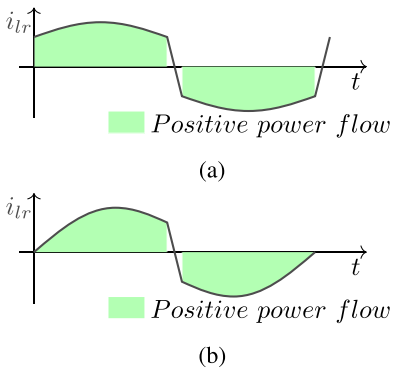


FIGURE 10. Illustration of average power flow in one switching cycle for the inductive region. (a) Phase shift mode—inductive region. (b) Duty cycle mode—inductive region.

to the output power. However, the current associated with the reactive power does contribute to the conduction losses in the semiconductor switches. Hence, the full-load ZVS range comes at the cost of higher conduction losses under light load conditions.

The average power flow for inductive region operation is shown in Fig. 10. Unlike the capacitive region, these operating modes do not have any areas of negative power flow in

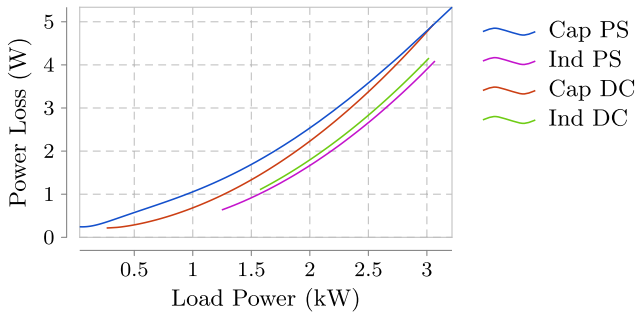


FIGURE 11. Switch conduction losses for all the modes.

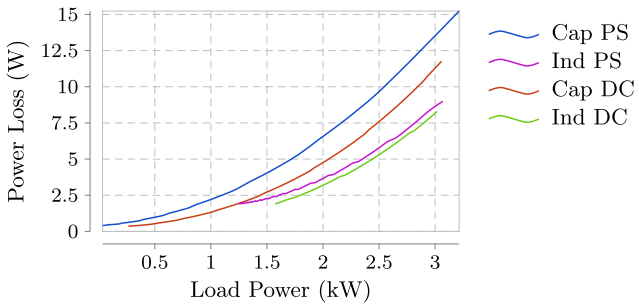


FIGURE 12. L_r losses for all the modes.

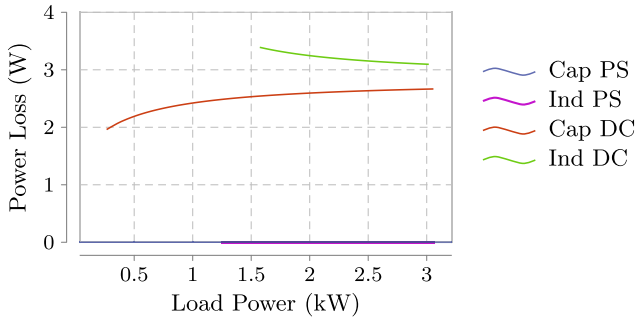


FIGURE 13. Switch turn-ON losses for all the modes.

the switching cycle. With no reverse power flow, the average output current for a particular power flow is lower than the capacitive region. Therefore, switch conduction losses are lower for the inductive region for a particular output power flow. At lower power flow, the peak of L_r current reduces. Because a certain minimum current is required for the ZVS turn-ON of switches at lower power flow, the current at switching instances will not be sufficient to achieve ZVS turn-ON for switches. Hence, achieving ZVS turn-ON for the complete operating range is impossible for inductive region modes.

C. LOSS COMPARISON

This section discusses the various converter loss components for the power flow in different operating modes. For the loss modeling, the parameters of the converters are given in Table 4. Figs. 11–14 show the losses in various components for

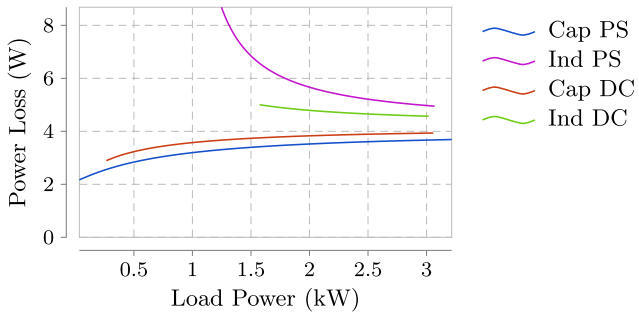


FIGURE 14. Switch turn-OFF losses for all the modes.

all the operating modes. On the x-axis is the load power in kilowatts, and on the y-axis is the losses in watts. It should be noted that for the inductive phase shift mode case, the losses are shown from 1.2 kW. This is because, as discussed in the previous subsection, the ZVS turn-ON is lost at low power flow for the inductive region. For the designed converter, this power flow is approximately 1.2 kW. The same is applicable for inductive duty cycle mode.

The root-mean-square (rms) current flowing through the switches and its $R_{ds,\text{on}}$ is used to calculate the conduction losses. At any particular power flow in a phase shift mode, the rms current in all the switches will be the same. However, the rms current in the switches for duty cycle modes will be different due to different duty cycles. Fig. 11 compares the cumulative conduction losses for four semiconductor switches in various operating modes. It can be observed that the capacitive phase shift mode shows the highest losses, and the inductive phase shift mode shows the lowest losses. This difference in the conduction losses for the same output power can be attributed to the different reactive powers in the various modes. In the capacitive phase shift modes, the reactive power ratio is higher than in other modes, contributing to the higher switch rms current, eventually leading to higher conduction losses.

Fig. 12 shows the losses in L_r for the different operating modes. A similar trend as the conduction losses can be seen in these losses. The capacitive phase shift mode shows the highest power loss due to a higher rms current. The losses in the inductive phase shift mode are marginally higher than those in the inductive duty cycle mode. This change can be attributed to the lower f_{sw} for the same power flow in the case of the inductive duty cycle compared to the inductive phase shift mode.

Fig. 13 shows the cumulative turn-ON losses for the four semiconductor switches. The losses for the capacitive and inductive phase shift modes can be neglected due to the ZVS turn-ON of the switches [24]. Due to the ZCS, turn-ON losses occur in the duty cycle modes. Furthermore, the loss trend for the two modes is different. The turn-ON loss for the capacitive duty cycle mode is reduced by reducing load power. The power output decreases with decreasing f_{sw} in capacitive modes. On the other hand, the turn-ON losses for the inductive duty cycle mode increase with decreasing f_{sw}. The power output decreases with increasing f_{sw}.

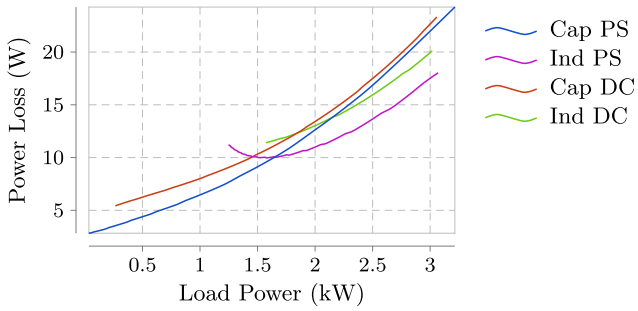


FIGURE 15. Total losses for all the modes.

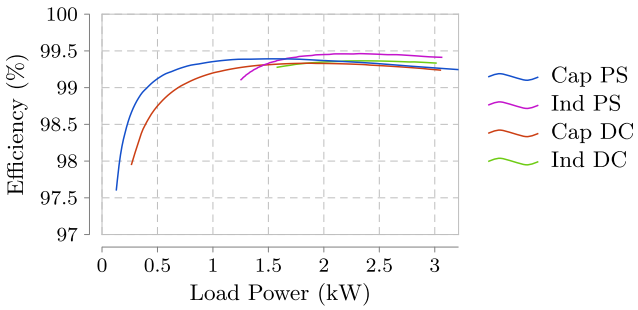


FIGURE 16. Efficiency plot for all the modes.

Fig. 14 shows the cumulative turn-OFF losses for the four semiconductor switches. The switch turn-OFF losses occur in all the modes. The loss trend in these modes is similar to switch turn-ON losses.

The sum of all the modes' losses is shown in Fig. 15. It can be seen that the losses of the duty cycle modes are generally higher than those of the phase shift modes. The higher loss occurs mainly because of the turn-ON losses in these modes. A conclusion can be drawn that the inductive phase shift mode is better for higher power operation, and the capacitive phase shift mode is more suitable for achieving ZVS turn-ON in the whole power range.

Finally, using the data in Fig. 15, the efficiency plot can be made for all the modes. The efficiency plot is shown in Fig. 16.

VI. RESULTS

The previous section discussed the operating principle and power flow characteristics. In this section, the simulation and experiment results are shown and discussed. All the tests are done with a load current of 5 A connected between the neutral and – poles. The results displayed are for the condition when the current output of both the source converters (V_{s1} and V_{s2}) is balanced.

A. CONVERTER DESIGN

The parameters for the designed converter are given in Table 4. In this section, we discuss the selection criteria for the major components of the converter for a rated voltage of

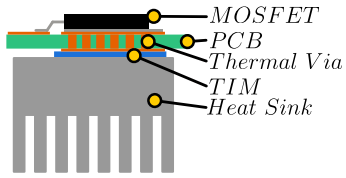


FIGURE 17. Application of heatsink in the considered designs.

+/–350 V and rated power flow of 3 kW. These are listed as follows.

1) MOSFET switch: For the MOSFET switch, surface-mount device (SMD) switches were chosen to minimize the loop area for high dv/dt and di/dt signals during switching instances. Utilizing two adjacent layers in the PCB significantly reduces the loop inductance [25], [26]. In addition, SMD components provide a compact and aesthetically pleasing design. However, a drawback of SMD switches is their limited thermal dissipation capacity. In this design, natural convection is employed for cooling, as depicted in Fig. 17. Thermal vias facilitate heat transfer from the switch case to the heatsink, which is attached to the PCB using electrically insulated thermal adhesive tape. Therefore, an SMD switch with low $R_{ds,\text{on}}$ was selected. The switch must handle at least 350 V, as only one pole-to-neutral voltage is applied when the switch is OFF. Considering these factors, the C3M0025065J1 switch from Wolfspeed was chosen.
2) Dc link capacitor: For the dc link capacitor, its primary function is to store energy from one pole during one half-cycle and deliver it to the other pole in the next half-cycle. Film capacitors were selected for their low equivalent series resistance and equivalent series inductance compared to electrolytic capacitors, resulting in lower voltage ripple, especially at high frequencies. To limit voltage ripple under all operating conditions, a total capacitance of 240 μF was installed between a pole and neutral. To maintain the aesthetic look of the converter, a dc capacitor with a height almost equal to the heatsink was used. Consequently, 4x Wima DCP4G056007GD4KSSD film capacitors were chosen.
3) Resonant capacitor: The resonant capacitors carry the load current ripple throughout the full cycle. Multilayer ceramic capacitors (MLCCs) are suitable for resonant capacitors due to their lower capacitance values compared to dc link capacitors. MLCCs with C0G dielectric were selected for their high purity and thermal stability [27], [28], [29]. For this design, TDK CGA9Q1C0G3A333J280KC capacitors were used.
4) Resonant inductor: For the resonant inductor, its low value and size are dictated by the resonant nature of the converter. Due to the unavailability of commercially suitable off-the-shelf components and the need to match the resonant frequency with the resonant capacitor, a custom design was necessary. To ensure sufficient power handling capacity with natural convection, a

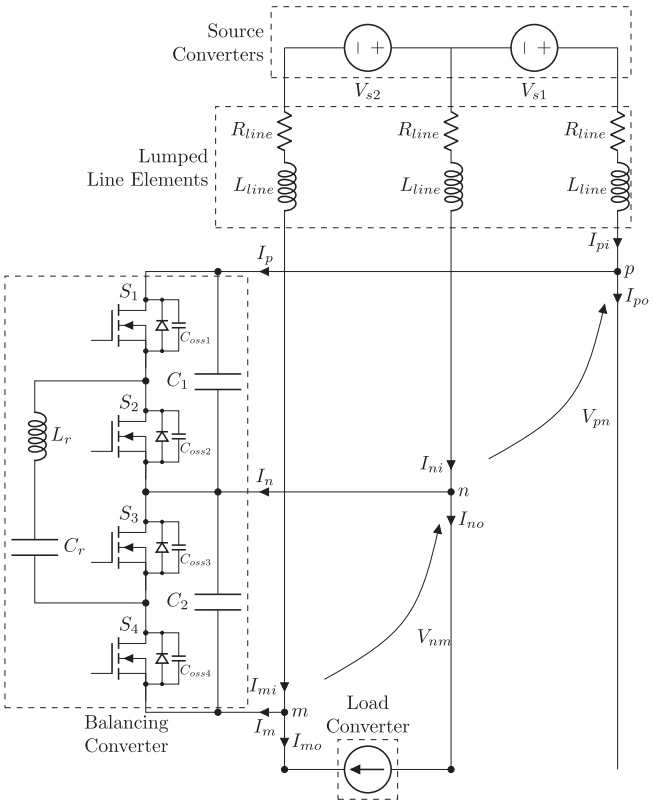


FIGURE 18. Schematic for testing the operation of series resonant balancing converter.

peak current of 40 A was considered. The frequency range was set at 120 kHz, corresponding to the maximum power flow frequency in inductive phase shift and duty cycle modes. The K_g design procedure outlined in Erickson and Maksimović's [30] work was used for designing the inductor. The final design specifications of the inductor are listed in Table 4.

B. SETUP

Fig. 18 shows the test setup schematic. The system comprises two source converters, denoted as V_{s1} and V_{s2}, and line impedances (R_{line} and L_{line}), which simulate a 100 m line. At its core is the balancing converter, connected to a load converter. Three critical nodes in this setup are p, n, and m, linking the balancing converter to the +, neutral, and – poles, respectively. Voltages across these nodes are defined as V_{pn} (between the nodes, p and n) and V_{nm} (between the nodes, n and m). Currents at these nodes are categorized into input and output currents: I_{pi} and I_{po} at node p, I_{ni} and I_{no} at node n, and I_{mi} and I_{mo} at node m. In addition, I_p, I_n, and I_m represent the currents flowing into the balancing converter from the p, n, and m nodes, respectively. It should be noted that the load converter is connected between the neutral and - pole for all the tests. The designed converter is shown in Fig. 19(a). The grid parameters are given in Table 5.

TABLE 5 Grid Parameters for Simulation and Experiments

Parameter	Value
Grid voltage (V_{s1} & V_{s2})	350 V
Line resistance (R_{line})	0.18 Ω
Line inductance (L_{line})	13 μH

C. EXPERIMENTAL VALIDATION

The experimental results for the setup above are given in Fig. 19. The load converter is set to sink 5 A current for all the results shown. This load current corresponds to a load power of 1.75 kW. The oscilloscope outputs show the converter states, the drain-to-source voltages of S_2 and S_4, and the corresponding gate-to-source voltages. Furthermore, the switching instances are magnified to show the ZVS turn-ON of the switches wherever applicable. The efficiency of the system in each operating mode is also shown. In the power analyzer results, Udc1 represents the voltage across the load converter, corresponding to V_{nm} as depicted in Fig. 18. Similarly, Udc2 refers to the voltage measured between points p and n and is equivalent to V_{pn} shown in Fig. 16. Udc3, on the other hand, denotes the voltage between points n and m, aligning with V_{nm} in the figure. Regarding the current measurements, Idc1 indicates the current flowing through the load converter, which is equivalent to I_{no} or $-I_{mo}$, as illustrated in Fig. 18. Idc2 reflects the current traveling from the positive pole of the grid to the converter, matching I_{pi} in the figure. Since there is no load between the + and neutral poles, Idc2 is also equivalent to I_p. Finally, Idc3 represents the current in the negative pole of the grid, corresponding to $-I_{mi}$, as shown in Fig. 18. Regarding the power flows, P1 is the power flowing through the load converter, calculated as the product of Udc1 and Idc1. Second, P2 quantifies the power traversing the + pole of the grid, derived from the product of Udc2 and Idc2. Finally, P3 denotes the power moving through the – pole of the grid, determined by the product of Udc3 and Idc3. The efficiency of the system is calculated using

$$\eta 1 = \frac{P1}{P2 + P3} \tag{17}$$

where P1 is the power flowing into the load converter, P2 is the power flowing from V_{s1}, and P3 is the power flowing from V_{s2}. Each of these powers is shown alongside the oscilloscope output.

The experimental result for the capacitive phase shift mode is shown in Fig. 19(b). The converter operates with f_{sw} of 72.5 kHz and ϕ of 8.35^o. The efficiency of the system at this operating point is shown in Fig. 19(c). The zoomed-in portion of the oscilloscope output in Fig. 19(b) shows the turn-OFF instant on the bottom left and turn-ON instant on the bottom right for S_2 and S_4. The turn-ON instant clearly shows the ZVS turn-ON of the switches. Furthermore, from L_r current symmetry, it can be inferred that ZVS turn-ON also occurs for S_1 and S_3.

The experimental result for the inductive phase shift mode is shown in Fig. 19(d). The converter operates with f_{sw} of

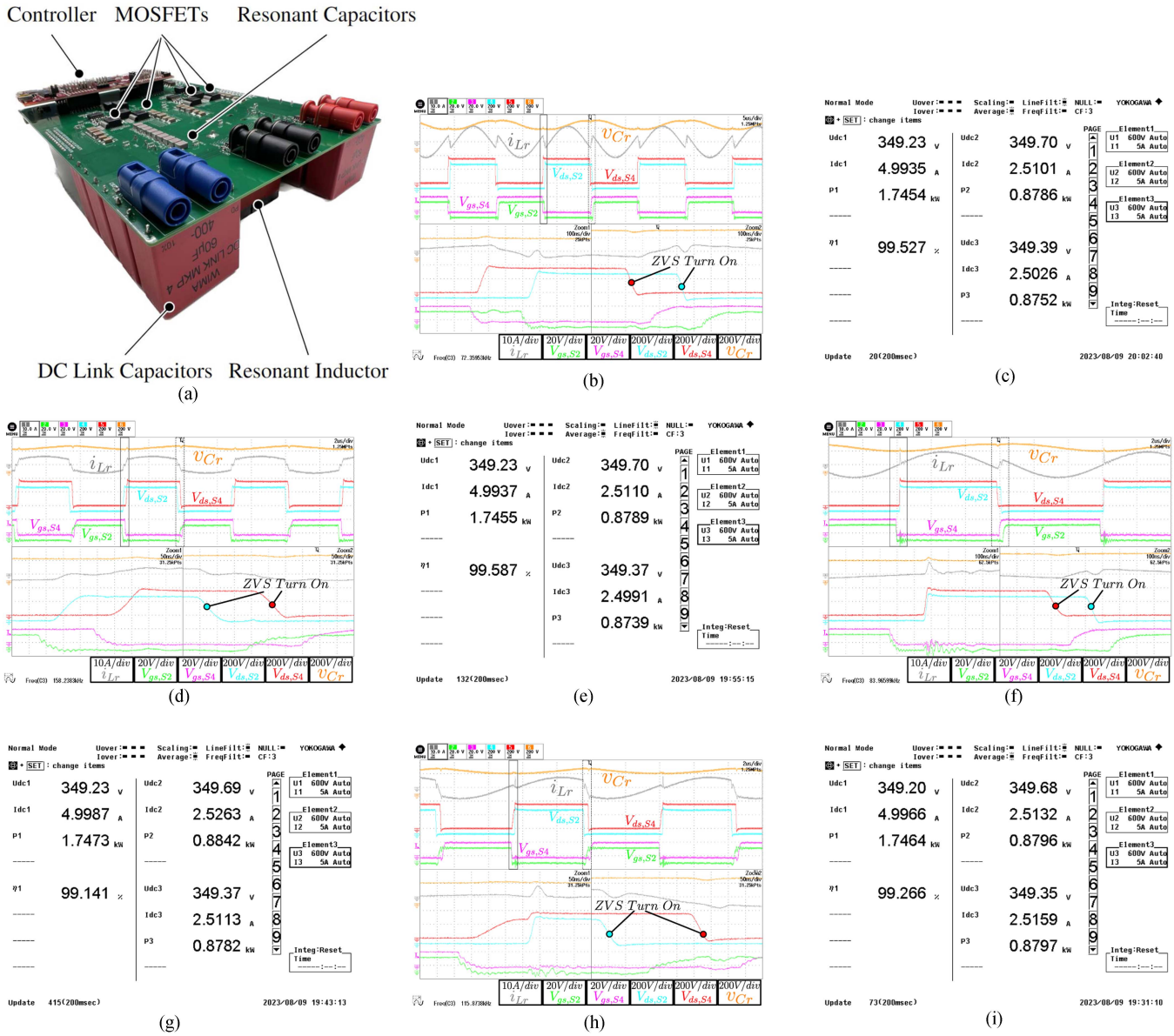


FIGURE 19. Experimental results for the different operating modes with 1.75 kW load power. (a) Designed converter prototype. (b) Experimental results for capacitive phase shift mode. (c) Power analyzer results for capacitive phase shift mode. (d) Experimental results for inductive phase shift mode. (e) Power analyzer results for inductive phase shift mode. (f) Experimental results for capacitive duty cycle mode. (g) Power analyzer results for capacitive duty cycle mode. (h) Experimental results for inductive duty cycle mode. (i) Power analyzer results for inductive duty cycle mode.

157.8 kHz and ϕ of 13.6^o. The system's efficiency at this operating point is shown in Fig. 19(e). The zoomed-in portion of the oscilloscope output in Fig. 19(d) shows the turn-OFF instant on the bottom left and turn-ON instant on the bottom right for S_2 and S_4. The turn-ON instant clearly shows the ZVS turn-ON of the switches. Furthermore, from L_r current symmetry, it can be inferred that ZVS turn-ON also occurs for S_1 and S_3.

The experimental results for the capacitive duty cycle mode are shown in Fig. 19(f). The converter operates with f_{sw} of 84 kHz and a ΔD of 0.95%. The efficiency of the system at this operating point is shown in Fig. 19(g). The zoomed-in portion of the oscilloscope output in Fig. 19(f) shows the turn-OFF instant on the bottom left and turn-ON instant on the bottom right for S_2 and S_4. The turn-ON instant clearly shows the ZVS turn-ON of the switches. However, at the turn-OFF instance, there is ZCS switching. This leads to higher overall losses in the converter.

The experimental results for the inductive duty cycle mode are shown in Fig. 19(h). The converter operates with f_{sw} of 116 kHz and a ΔD of 1.6%. The efficiency of the system at this operating point is shown in Fig. 19(i). The zoomed-in portion of the oscilloscope output in Fig. 19(h) shows the turn-OFF instant on the bottom left and turn-ON instant on the bottom right for S_2 and S_4. The turn-ON instant clearly shows the ZVS turn-ON of the switches. However, at the turn-OFF

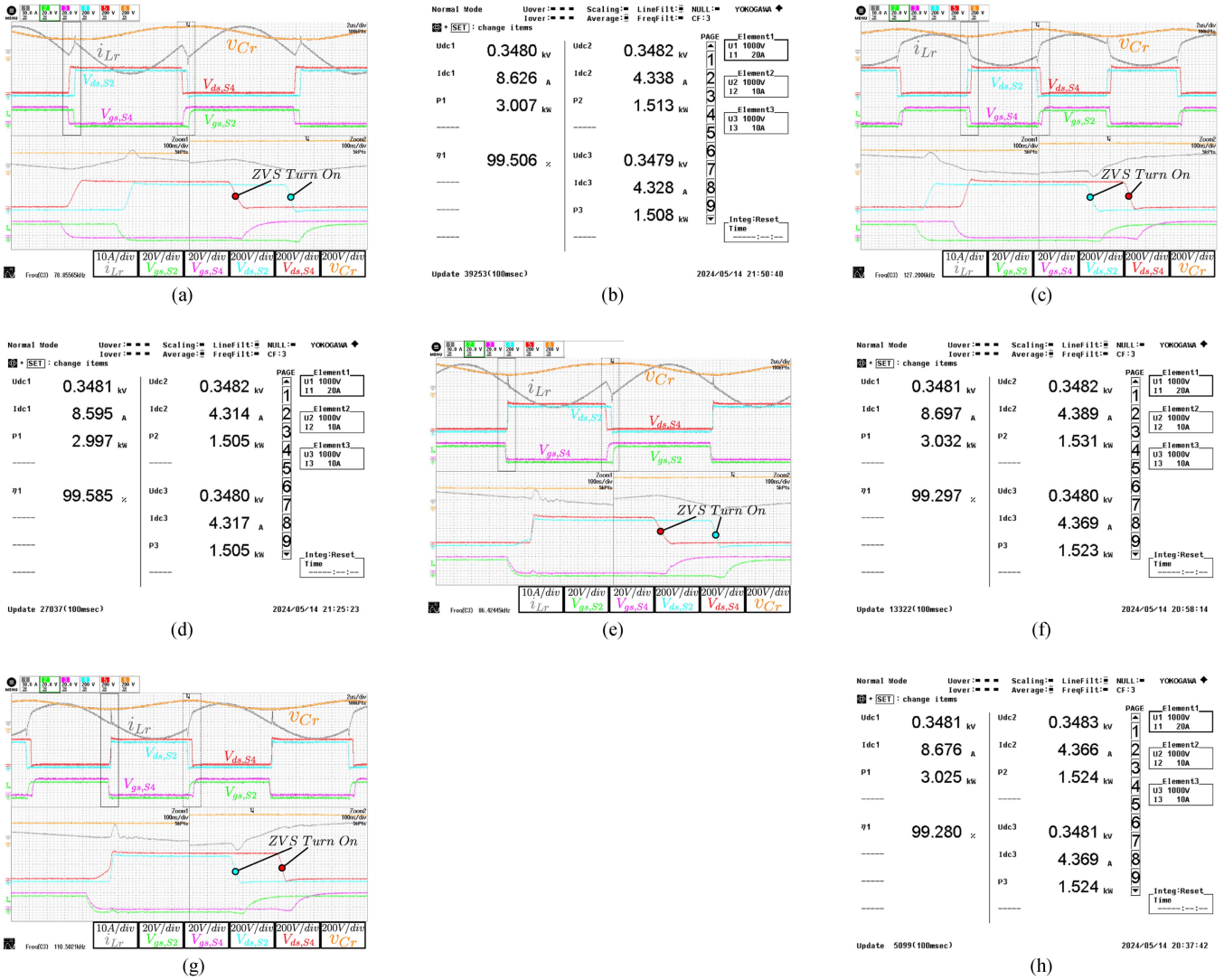


FIGURE 20. **Experimental results for the different operating modes with 3 kW load power. (a) Experimental results for capacitive phase shift mode. (b) Power analyzer results for capacitive phase shift mode. (c) Experimental results for inductive phase shift mode. (d) Power analyzer results for inductive phase shift mode. (e) Experimental results for capacitive duty cycle mode. (f) Power analyzer results for capacitive duty cycle mode. (g) Experimental results for inductive duty cycle mode. (h) Power analyzer results for inductive duty cycle mode.**

instance, there is ZCS switching. This leads to higher overall losses in the converter.

The experimental results with 3 kW load power flow are discussed as follows.

The experimental result for the capacitive phase shift mode is shown in Fig. 20(a). The converter operates with a f_{sw} of 78.8 kHz and a ϕ of 9.1^o. The system's efficiency at this operating point is illustrated in Fig. 20(b). The zoomed-in portion of the oscilloscope output in Fig. 20(a) highlights the turn-OFF instant on the bottom left and the turn-ON instant on the bottom right for switches S_2 and S_4. The turn-ON instant clearly demonstrates the ZVS turn-ON of the switches. In addition, from the symmetry of the L_r current, it can be inferred that ZVS turn-ON also occurs for switches S_1 and S_3.

The experimental result for the inductive phase shift mode is shown in Fig. 20(c). The converter operates with an f_{sw} of 127 kHz and a ϕ of 7.8^o. The system's efficiency at this operating point is depicted in Fig. 20(d). The zoomed-in portion of the oscilloscope output in Fig. 20(c) shows the turn-OFFinstant on the bottom left and the turn-ON instant on the bottom right for switches S_2 and S_4. The turn-ON instant clearly shows ZVS turn-ON of the switches. From the L_r current symmetry, it can also be inferred that ZVS turn-ON occurs for switches S_1 and S_3.

The experimental results for the capacitive duty cycle mode are shown in Fig. 20(e). The converter operates with an f_{sw} of 86.5 kHz and a duty cycle variation (ΔD) of 1.4%. The system's efficiency at this operating point is shown in Fig. 20(f). The zoomed-in portion of the oscilloscope output in Fig. 20(e) highlights the turn-OFFinstant on the bottom left and the turn-ON instant on the bottom right for switches S_2 and S_4. The turn-ON instant clearly demonstrates ZVS turn-ON of

TABLE 6 Summary of Comparison of All the Operating Modes

	Capacitive phase shift	Inductive phase shift	Capacitive duty cycle	Inductive duty cycle
Soft Switching capability	ZVS turn on possible for all switches	ZVS turn on possible for all switches	ZVS turn on for two switches, ZCS turn on for the other two	ZVS turn on for two switches, ZCS turn on for the other two
ZVS range	ZVS possible for all power flow	ZVS range is limited and possible for high power flow	Soft switching is possible for almost full load range	Similar to Ind phase shift, soft-switching range is limited
Losses	Lowest	Low	Highest	High
Loss distribution	Same in all switches	Same in all switches	Higher in two	Higher in two
L_r losses	High	Lowest	Highest	Low

the switches. However, at the turn-OFFinstance, there is ZCS. This leads to higher overall losses in the converter.

The experimental results for the inductive duty cycle mode are shown in Fig. 20(g). The converter operates with an f_{sw} of 110.5 kHz and a ΔD of 1.5%. The system's efficiency at this operating point is shown in Fig. 20(h). The zoomed-in portion of the oscilloscope output in Fig. 20(g) highlights the turn-OFFinstant on the bottom left and the turn-ON instant on the bottom right for switches S_2 and S_4. The turn-ON instant clearly shows ZVS turn-ON of the switches. However, at the turn-OFFinstance, there is ZCS switching, leading to higher overall losses in the converter.

VII. CONCLUSION

This article synthesized various operating modes exhibiting soft-switching in a series resonant balancing converter. The operating modes can be divided into phase shift and duty cycle modes. Furthermore, the converter can work either in the capacitive or inductive region with respect to the resonant frequency of the converter. The synthesis process was explained using the different possible switching patterns. The analysis can calculate the values for f_{sw} and $\phi/\Delta D$, leading to soft switching (ZVS and ZCS) in the different operating modes.

Furthermore, it is shown that the duty cycle modes show ZVS turn-ON in only two switches and ZCS in all the switches. On the other hand, the phase shift modes can show ZVS turn-ON in all the switches. Hence, the losses in all the switches for the phase shift modes are the same at a particular operating point. However, the switch losses are not the same for all the switches in the duty cycle modes. The ZVS region for the inductive phase shift mode is limited. The capacitive phase shift mode can exhibit the ZVS turn-ON of all the switches in the whole operating region. However, the increased ZVS range comes at the cost of increasing the reactive power ratio with decreasing output power. The higher reactive power leads to higher rms current, increasing switch conduction and L_r losses. A summary of the comparison of all the operating modes is given in Table 6.

With the advantage of ZVS turn-ON for all the switches, it can be concluded that phase shift modes perform better than the duty cycle modes. However, with the limited ZVS range, the inductive phase shift modes might not be suitable for low output power. However, a hybrid modulation scheme can be implemented to switch between capacitive and inductive phase shift modes depending on the power flow requirement in future work.

PROOF OF THE INITIAL L_r CURRENT RELATION FOR THE PHASE SHIFT MODES

Consider a balanced grid and ideal conditions of 50% duty cycle, as depicted in Fig. 4. Under these assumptions, if the relationship in (4) does not hold, we still observe certain constraints due to the principles governing the resonant inductor and capacitor behavior:

Resonant inductor: The volt–second balance principle dictates specific conditions for the inductor currents

$$\begin{aligned} I_{l0} &= -I_{l2} = I_{l4} \\ I_{l1} &= -I_{l3}. \end{aligned} \tag{18}$$

Resonant capacitor: The ampere–second principle imposes particular voltage relationships across the capacitor

$$\begin{aligned} V_{c0} &= V_{c4} \\ V_{c2} &= 2V_L - V_{c0} \\ V_{c1} &= 2V_L - V_{c3}. \end{aligned} \tag{19}$$

By incorporating these constraints into the state equations defining the initial resonant inductor current and capacitor voltage for the capacitive phase shift case (shown in Fig. 4), we derive certain expressions, as given in (20) and (21)

$$\begin{aligned} I_{l1} &= I_{l0}\cos(\omega_0(t_1 - t_0)) + \frac{V_L - V_{c0}}{Z_0}\sin(\omega_0(t_1 - t_0)) \\ I_{l2} &= I_{l1}\cos(\omega_0(t_2 - t_1)) + \frac{2V_L - V_{c1}}{Z_0}\sin(\omega_0(t_2 - t_1)) \\ I_{l3} &= I_{l2}\cos(\omega_0(t_3 - t_2)) + \frac{V_L - V_{c2}}{Z_0}\sin(\omega_0(t_3 - t_2)) \\ I_{l4} &= I_{l3}\cos(\omega_0(t_4 - t_3)) + \frac{0 - V_{c3}}{Z_0}\sin(\omega_0(t_4 - t_3)) \end{aligned} \tag{20}$$

$$\begin{aligned} V_{c1} &= V_L - (V_L - V_{c0})\cos(\omega_0(t_1 - t_0)) \\ &\quad + Z_0 I_{l0}\sin(\omega_0(t_1 - t_0)) \\ V_{c2} &= 2V_L - (2V_L - V_{c1})\cos(\omega_0(t_2 - t_1)) \\ &\quad + Z_0 I_{l1}\sin(\omega_0(t_2 - t_1)) \\ V_{c3} &= V_L - (V_L - V_{c2})\cos(\omega_0(t_3 - t_2)) \\ &\quad + Z_0 I_{l2}\sin(\omega_0(t_3 - t_2)) \\ V_{c4} &= 0 - (0 - V_{c3})\cos(\omega_0(t_4 - t_3)) \\ &\quad + Z_0 I_{l3}\sin(\omega_0(t_4 - t_3)) \end{aligned} \tag{21}$$

Substituting expressions in (18) and (19) into (20) and (21), respectively, it is found that the currents I_{l0} and I_{l1} turn out to be identical, as given in (22), which establishes the relationship in (4)

$$I_{l0} = -\frac{V_L\,(\sin(\omega_0(t_2-t_0))-\sin(\omega_0(t_1-t_0))+\sin(\omega_0(t_2-t_1)))}{2Z_0(\cos(\omega_0(t_2-t_0))+1)}$$

$$I_{l1} = -\frac{V_L\,(\sin(\omega_0(t_2-t_0))-\sin(\omega_0(t_1-t_0))+\sin(\omega_0(t_2-t_1)))}{2Z_0(\cos(\omega_0(t_2-t_0))+1)}$$

$$V_{c0} = \frac{V_L\,(\cos(\omega_0(t_2-t_0))+\cos(\omega_0(t_1-t_0))+\cos(\omega_0(t_2-t_1))+1)}{2(\cos(\omega_0(t_2-t_0))+1)}$$

$$V_{c1} = \frac{V_L\,(3\cos(\omega_0(t_2-t_0))-\cos(\omega_0(t_1-t_0))-\cos(\omega_0(t_2-t_1))+3)}{2(\cos(\omega_0(t_2-t_0))+1)}. \quad (22)$$

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SACHIN YADAV (Graduate Student Member, IEEE) received the bachelor's degree in electrical and electronics engineering from the Birla Institute of Technology, Mesra, India, in 2013, and the M.Sc. and Ph.D. degrees in sustainable energy technology and bipolar dc grids on ships from the Delft University of Technology, Delft, The Netherlands, in 2019 and 2020, respectively.

After the M.Sc., he joined DC Opportunities in Delft as a Power Electronics Engineer. His research focuses on the design of power electronics converters and magnetics for bipolar dc grids on ships.

PAVOL BAUER (Senior Member, IEEE) received the master's degree in electrical engineering from the Technical University of Kosice, Kosice, Slovakia, in 1985, and the Ph.D. degree in power electronics from the Delft University of Technology, Delft, The Netherlands, in 1995.

He is currently a Full Professor with the Department of Electrical Sustainable Energy, Delft University of Technology, and the Head of DC Systems, Energy Conversion, and Storage Group. He is also a Professor with the Brno University of Technology, Brno, Czech Republic, and an Honorary Professor with the Politehnica University Timisoara, Timisoara, Romania. From 2002 to 2003, he was with KEMA (DNV GL), Arnhem, The Netherlands. He has authored or coauthored eight books, more than 120 journal articles, and 500 conference papers. He holds seven international patents and has organized several tutorials at international conferences. He has worked on many projects for the industry concerning wind and wave energy, power electronic applications for power systems, such as Smarttrafo; HVdc systems, projects for smart cities, such as photovoltaic (PV) charging of electric vehicles, PV and storage integration, contactless charging; and he participated in several Leonardo da Vinci and H2020, and Electric Mobility Europe EU projects as a Project Partner (ELINA, INETELE, E-Pragmatic, Micact, Trolley 2.0, OSCD, P2P, and Progressus) and a Coordinator (PEMCWebLab.com-Edipe, SustEner, Eranet DCMICRO).

Dr. Bauer is the Former Chairman of the Benelux IEEE Joint Industry Applications Society, Power Electronics, and Power Engineering Society Chapter, the Chairman of the Power Electronics and Motion Control Council, and a Member of the Executive Committee of European Power Electronics Association and the International Steering Committee at numerous conferences.

ZIAN QIN (Senior Member, IEEE) received the B.Eng. degree from Beihang University, Beijing, China, in 2009, the M.Eng. degree from the Beijing Institute of Technology, Beijing, in 2012, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2015, all in electrical engineering.

He is currently an Assistant Professor with the Delft University of Technology, Delft, The Netherlands. In 2014, he was a Visiting Scientist with Aachen University, Aachen, Germany. He has authored or coauthored more than 100 journals/conference papers, four book chapters, and two international patents, and also worked on several European and Dutch national projects in these areas. His research interests include power quality and stability of power electronics-based grids, as well as solid-state transformers.

Dr. Qin is an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the Guest Associate Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPICS and IEEE TRANSACTIONS ON ENERGY CONVERSION. He is a Distinguished Reviewer for the 2020 IEEE TRANSACTIONS OF INDUSTRIAL ELECTRONICS. He was the Technical Program Chair of IEEE-PEDG 2023, IEEE-ISIE 2020, and IEEE-COMPEL 2020.