Received 16 May 2024; revised 15 June 2024; accepted 25 June 2024. Date of publication 3 July 2024; date of current version 24 September 2024. Digital Object Identifier 10.1109/OJAP.2024.3422426

A Proton Irradiated CMOS On-Chip Vivaldi Antenna for 300 GHz Band Slat Array Implementation

HANS HERDIAN[®]¹ (Graduate Student Member, IEEE), CHUN WANG[®]¹ (Graduate Student Member, IEEE), TAKESHI INOUE², ATSUSHI SHIRANE¹ (Member, IEEE), AND KENICHI OKADA[®]¹ (Fellow, IEEE)

¹Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Meguro City 152-8550, Japan

²Development Department, SHI-ATEX Company Ltd., Saijo City 799-1393, Japan

CORRESPONDING AUTHOR: H. HERDIAN (e-mail: hans.h@ssc.pe.titech.ac.jp)

This work was supported in part by the Ministry of Internal Affairs and Communications (MIC) under Grant JPJ000254; in part by the Support for TokyoTech Advanced Researchers (STAR); in part by the VLSI Design and Education Center (VDEC) in collaboration with Cadence Design Systems, Inc.; in part by the Mentor Graphics, Inc.; and in part by the Keysight Technologies Japan, Ltd.

ABSTRACT As the CMOS transceiver reaches the sub-millimeter wave operating frequency, its circuit area cannot keep up with the shrinkage of the $0.5\lambda_0 \times 0.5\lambda_0$ area limit for the typical 2-dimensional (2D) tile-based phased array topology. This article proposes an end-fire on-chip Vivaldi antenna on a standard 65-nm CMOS process for the 300 GHz band operation. The Vivaldi architecture was chosen for its broadband and end-fire radiation characteristics. End-fire antenna is required for slat array topology, which enables 2D array implementation for transceivers with circuit area above $0.5\lambda_0 \times 0.5\lambda_0$. The antenna length was shortened to maximize beamwidth and reduce area. Additionally, comb-shaped slots were added to suppress side lobes and back radiation pattern and reducing efficiency, the substrate was thinned to 50 μ m. A dual-layer proton irradiation process increases the substrate resistivity to 1 k Ω -cm, allowing high-efficiency on-chip antenna implementation on low-cost CMOS processes. The manufactured on-chip Vivaldi antenna has an area of $0.45\lambda_0 \times 0.45\lambda_0$, with measurement results showing 6 dBi gain with 1 dB flatness from 220 GHz to 320 GHz (37% bandwidth) and 76° E-plane beamwidth at 270 GHz with 87% efficiency. A 1 \times 4 slat array implementation using the proposed on-chip Vivaldi antenna has been demonstrated, with measurement results showing a 56° beam steering range across the E-plane.

INDEX TERMS 300 GHz, sub-millimeter wave, CMOS, on-chip antenna, end-fire antenna, slat array, wideband, proton irradiation, high-resistivity substrate.

I. INTRODUCTION

IEEE Open Journal of

I N RECENT years, research on 300 GHz band (220 GHz to 320 GHz) transceivers (TRX) has uncovered a lot of potential for applications such as imaging [1], [2], [3], radar [4], [5], [6], [7], [8], and ultra-high speed communication [9], [10], [11], [12], [13], [14]. The large available bandwidth can be utilized to improve radar spatial resolution or achieve the Tb/s data rates required for future 6G wireless communication systems [15]. The sub-millimeter wavelength reduces antenna size to the point where on-chip antenna (OCA) implementation is possible, eliminating additional losses, parasitics, and variations introduced by chip-to-PCB interconnects [16], [17]. However, the 300 GHz band has

a significant path loss [18] and cannot penetrate through obstacles. Adding a lens on top of an OCA [3], [4], [5], [6], [19] compensates for the path loss with the high lens gain. However, the narrow beamwidth and the static radiation pattern necessitate external mechanical parts for beam steering to detect or avoid obstacles. Such mechanical parts are undesirable as they increase system size and complexity. A phased array antenna implementation satisfies the high gain and electronically controlled beam steering requirement [20]. The sub-millimeter-sized antenna enables the implementation of many elements within the same area footprint typically occupied by a single sub-10 GHz antenna. Furthermore, the feasibility of TRX implementation using



FIGURE 1. Survey of TRX chip area in relation to its center frequency on CMOS and SiGe BiCMOS process.



FIGURE 2. 300 GHz band phased array implemented as (a) tile array, and (b) slat array.

a standard CMOS process has been demonstrated [8], [9], [10], [11], [12], [13], promising low cost, high yield, and large production capacity needed to manufacture the required high number of elements.

The implementation of a phased array below 60 GHz is typically done in tile configuration [21], [22], [23] using broadside antenna due to the ease of assembly, simplicity, and lower cost [24]. However, the TRX chip area survey in Fig. 1 shows that as the frequency increases above 60 GHz, the TRX chip area stays roughly the same [25], [26], [27], [28], [29], [30], [31], [32], while the $0.5\lambda_0 \times 0.5\lambda_0$ tile area limit keeps shrinking until it becomes smaller than the TRX area (λ_0 is the wavelength in free space). The TRX shape can be modified to only maintain less than $0.5\lambda_0$ length at one side [8], [28], forming a tile array depicted in Fig. 2(a). However, the array scalability is decreased from $M \times N$ into $2 \times N$, which reduces array density and area efficiency. The slat array implementation using endfire OCAs, shown in Fig. 2(b), eliminates the TRX area limitation by introducing a third dimension to expand the array, restoring the array scalability to M×N. However, endfire OCA performance on sub-terahertz frequency suffers from the surface wave effect and resistive loss induced by the high relative permittivity ($\epsilon_r = 11.9$) and low resistivity (around 3 to 15 Ω ·cm) of the silicon substrate used in the standard CMOS process [33], [34]. Furthermore, simple substrate isolation methods commonly implemented in broadside

OCAs, such as bottom metal shielding [35], [36], [37], [38], [39], [40] and artificial magnetic conductors (AMC) [41], cannot be applied to the end-fire antenna. Therefore, most end-fire OCAs were either implemented on a separate lowloss substrate like quartz [42] and glass [43] or utilized a special etching technique to remove the silicon substrate below the antenna [44], [45], resulting in more complex design fabrication and integration. A fully in-process endfire OCA implementation has been demonstrated in the SiGe BiCMOS process [46]. However, the silicon substrate in the SiGe BiCMOS process has a higher substrate resistivity (around 50 Ω ·cm) compared to the standard CMOS process, which significantly reduces degradations due to the substrate resistive loss.

IEEE Open Jo

This article proposes an end-fire 300 GHz band Vivaldi OCA fabricated on the standard 65-nm CMOS process for the slat array implementation. The Vivaldi architecture was chosen for being a wideband end-fire antenna that can cover 220 GHz to 320 GHz frequency. Because singleelement gain becomes less important for large-scale arrays, the Vivaldi OCA was optimized for wide 3-dB beamwidth and high efficiency, leading to shorter antenna length, smaller area, and lower gain in exchange for wider beamwidth than the typical gain-optimized Vivaldi antenna. Combshaped slots were added to prevent back radiation from happening due to the short length. To improve efficiency, the substrate was thinned to 50 μ m to prevent the excitation of higher mode surface waves, and the dual-layer proton irradiation was applied to raise the substrate resistivity. The dual-layer proton irradiation was developed as a postprocess and can be performed separately after the chip is manufactured [47], [48], allowing a high-resistivity substrate implementation while keeping the low-cost and high-volume production capacity of the standard CMOS process. Further details on antenna structure, working principle, and parametric analysis are described in Section II. A 1×4 slat array with the Vivaldi OCA as the element was designed as a proof of concept, with design details described in Section III. Section IV describes the verification of single-element and array design through measurement. Section V concludes the article.

II. ON-CHIP VIVALDI ANTENNA

A. ANTENNA STRUCTURE AND OPERATING PRINCIPLE Fig. 3 shows the overall implementation of the proposed Vivaldi OCA. The chip size, the antenna placement on the chip, and the chip placement on the PCB were made to closely replicate a single 300 GHz band TRX implementation. Fig. 4 shows the cross-section of the standard 65-nm CMOS process used to implement the Vivaldi OCA, consisting of nine copper metal layers enclosed with 8.75 μ m silicon dioxide inter-metal dielectric (IMD) and 2.5 μ m passivation layer formed above the silicon substrate with permittivity and resistivity of 11.9 and 3 Ω -cm, respectively.

The Vivaldi OCA was implemented at the top metal (M9), with the detailed structure shown in Fig. 5. The antenna



FIGURE 3. Overall single-element Vivaldi OCA implementation structure for simulation and measurement purpose. ($L_{CHIP} = 3 \text{ mm}$, $W_{CHIP} = 0.75 \text{ mm}$, $D_{EDGE} = 0.4 \text{ mm}$, $H_{PCB} = 3 \text{ mm}$).



FIGURE 4. Process cross-section of the standard 65-nm CMOS process used for antenna implementation.



FIGURE 5. Structure and parameters of the proposed Vivaldi OCA. (R = 3, $W_{M} = 450$ μm , $W_{F} = 25 \mu m$, $W_{T} = 5 \mu m$, $L_{A} = 300 \mu m$, $L_{B} = 200 \mu m$, $L_{E} = 150 \mu m$, $L_{S} = 80 \mu m$, $S = 5 \mu m$, $D_{S} = 10 \mu m$, $N_{S} = 28$).

radiates through the traveling-wave mechanism formed by the exponential-tapered slot [49]. Theoretically, the feeding structure limits the upper-frequency cutoff, while the aperture width W_M determines the lower frequency cutoff [50], [51]. The taper length L_A is proportional to the gain and inversely proportional to the beamwidth [51], [52]. Therefore, optimizing for maximum beamwidth leads to lower gain and shorter L_A , with area reduction as an added benefit. However, there



FIGURE 6. Comparison of simulated Vivaldi OCA E-field at 320 GHz between smooth flare edge (a) without reflector, (b) with reflector, and comb-shaped slots flare edge (c) without reflector, (d) with reflector.



FIGURE 7. Comparison of simulated (a) E-plane realized gain pattern at 320 GHz and (b) reflection coefficient between smooth and comb-shaped flare edge, both with and without reflector.

is a limit on how short the L_A is before the antenna deviates from the typical traveling-wave antenna behavior [51]. This anomalous behavior can be attributed to the increasing nonradiated energy flowing backward through the outer side of the flare as the L_A becomes shorter and a high permittivity substrate is used. This excess energy can interact with structures outside the antenna and cause problems such as unwanted side lobes, resonance, and circuit interference. The antenna characteristics also become more sensitive to structural change outside the antenna, as illustrated by the significant changes of the radiation pattern in Fig. 7(a) and reflection coefficient in Fig. 7(b) due to additional reflector placed at the back of the antenna (Fig. 6(a) and 6(b)). Therefore, comb-shaped slots were added to the outer side of both antenna flares to increase the path impedance at those locations, forcing more energy to radiate forward and preventing further flow to the back of the antenna, as shown in Fig. 6(c) and 6(d). Consequently, the antenna characteristics become more resistant to structure variations outside the antenna, as shown in Fig. 7. The slot length L_S was set approximately by $0.25\lambda_0/\sqrt{\epsilon_r}$ [53], with λ_0 denoting the wavelength at the center frequency. The slots



FIGURE 8. (a) Slotline radial stub feeding structure, and (b) the simulation results of the feeding structure in a back-to-back configuration. ($L_R = 100 \ \mu m$, $W_T = 5 \ \mu m$, $W_L = 2.5 \ \mu m$, $D_L = 7.25 \ \mu m$).

should cover the whole flare's outer sides to maximize the suppression of the energy backflow.

Fig. 8(a) shows the slot line radial stub feeding structure used to convert the grounded co-planar waveguide (GCPW) transmission line to the slot line mode of the Vivaldi OCA. This architecture was chosen because it provides the largest bandwidth compared to other planar CPW-to-slot line transitions [54]. The back-to-back structure simulation in Fig. 8(b) shows that the coverage of this feeding structure exceeded the target design frequency (220 GHz to 320 GHz), ensuring that the feeding structure does not limit the antenna bandwidth.

At the 300 GHz band, the 300 μ m thick silicon substrate used in the 65-nm CMOS process enables the excitation of higher transverse electric (TE) and transverse magnetic (TM) modes within the substrate, reducing radiation efficiency and distorting the radiation pattern. The relationship between substrate thickness (*d*) and the cutoff frequency (f_c) of the TE and TM modes *n* for both grounded (*g*) and ungrounded (*ug*) substrates are given as follows [33]:

$$d_g = \frac{nc}{4f_c\sqrt{\epsilon_r\mu_r - \epsilon_0\mu_0}}, \begin{cases} n = 1, 3, 5, \dots, \text{ for TE} \\ n = 0, 2, 4, \dots, \text{ for TM} \end{cases}$$
(1)

$$d_{ug} = \frac{nc}{2f_c\sqrt{\epsilon_r\mu_r - \epsilon_0\mu_0}}, \begin{cases} n = 0, 1, 2, \dots, \text{ for TE} \\ n = 0, 1, 2, \dots, \text{ for TM} \end{cases}$$
(2)

where c, ϵ_r , and μ_r are the speed of light, substrate dielectric permittivity, and substrate dielectric permeability, respectively. Therefore, the substrate thickness must be reduced until the cutoff frequency of TE₁ and TM₁ mode is higher than the maximum operating frequency of the antenna. Because the Vivaldi OCA metal structure behaves like a large ground cover, (1) was used to determine the suitable substrate thickness. The substrate thickness value of 50 μ m was chosen to ensure that the higher order modes above 320 GHz are suppressed while the chip maintains enough structural integrity for further post-processing. Fig. 9(a) shows how reducing the substrate thickness to 50 μ m eliminates distortion on the radiation pattern. Fig. 9(b) also shows how the efficiency decreases as more TE modes get excited with increasing thickness.

The 3 Ω -cm resistivity of the substrate used in the 65-nm CMOS process causes additional loss due to thermal



IEEE Open Journal of

FIGURE 9. The simulated effect of substrate thickness at 270 GHz on (a) E-plane realized gain pattern and (b) efficiency of the Vivaldi OCA.



FIGURE 10. The simulated effect of substrate resistivity at 270 GHz on (a) E-plane realized gain pattern and (b) efficiency of the Vivaldi OCA.



FIGURE 11. The (a) top view and (b) cross-section view of the dual-layer proton irradiation process.

dissipation and eddy current, which degrades antenna efficiency. Fig. 10 shows how increasing the substrate resistivity improves the antenna efficiency and gain, with the maximum improvement achieved at 1 k Ω ·cm. Therefore, dual-layer proton irradiation was used to increase the substrate resistivity above 1 k Ω ·cm [55], with process details shown in Fig. 11. A 100 μ m thick nickel mask was used to localize the high-resistivity region formation around the OCA and protect the active circuit from radiation damage, eliminating the need for active device remodeling. A dual-layer profile was used instead of the typical single profile [47], [48] to reduce the total proton fluence requirement, shortening



FIGURE 12. The SRP measurement results of the substrate resistivity after irradiation and annealing process.



FIGURE 13. The realized gain simulation for different L_s.

the irradiation time [55]. For this implementation, the duallayer profile consists of a main irradiation at 60 μ m depth with 2×10¹⁴ cm⁻² fluence, and an interface irradiation at 10 μ m depth with 2×10¹⁴ cm⁻² fluence. Fig. 12 shows the substrate resistivity after irradiation measured with the spread resistance profiling (SRP) method. The resistivity after 1 minute of 260° C annealing was also measured to ensure the formed high-resistivity region can withstand hightemperature post-processing.

B. DESIGN PROCESS AND PARAMETRIC ANALYSIS

The Vivaldi OCA design process began with the initialization of all design parameters. First, the substrate thickness and resistivity were set to 50 μ m and 1k Ω ·cm, in accordance with the discussion in the previous subsection. Then, the feeding structure was designed and optimized on the initialized substrate, resulting in optimized design parameters in Fig. 8, where the value of $W_T = 5 \mu$ m was determined. Finally, the rest of the OCA was built and initialized as follows (all units in μ m, except *R*): $W_M = 450$, $W_F = 25$, $L_A = 300$, $L_B = 200$, $L_E = 150$, $L_S = 80$, S = 5, $D_S = 10$, and R= 3. W_F and L_B were kept constant. The optimization and parametric analysis were performed within the 200 GHz to 340 GHz frequency range, with a target operating frequency of 220 GHz to 320 GHz.

The first parametric analysis was performed on the combshaped slots parameters L_S , S, and D_S . A back reflector similar to Fig. 6(d) was added to see the impact of the combshaped slots better. Fig. 13 shows how the slots suppress gain dips at 220 GHz and 312 GHz induced by the energy reflected from the reflector. Shorter L_S provides better dip suppression at a higher frequency, while longer L_S has better



FIGURE 14. The realized gain simulation for various (a) D_S and (b) S.



FIGURE 15. The simulation of efficiency, E-plane 3-dB beamwidth, and H-plane 3-dB beamwidth at 270 GHz for different L_A .

low-frequency dip suppression. Therefore, L_S was adjusted to around 80 μ m to achieve balanced dip suppression performance centered around 270 GHz, which also shows good agreement with the slot design equation in [53]. Fig. 14 shows the optimum value for both D_S and S is between 5 μ m to 10 μ m, or around $L_S/10$. The deviation of D_S value from $L_S/10$ has a minor effect, while the S value must be kept larger than 5 μ m to prevent degradation at upperfrequency cutoff. After the optimization of comb-shaped slots, the reflector will not affect the antenna characteristics and can be removed during subsequent optimizations.

The rest of the design parameter, L_A , W_M , R, and L_E , was investigated and optimized through parametric analysis. The results in Fig. 15 confirm that shorter L_A leads to the wider E-plane and H-plane 3-dB beamwidth. However, there is a point where efficiency starts to degrade because the taper is too short to perform the traveling-wave radiation mechanism properly. Therefore, L_A should be set at the minimum value where it still operates above 80% efficiency, which was 300 μ m in this case. The impact of W_M shown in Fig. 16 indicates that the overall reflection coefficient increases as W_M decreases. This fits with the Vivaldi antenna design equation in [50], [51], where smaller W_M moves the lower cutoff frequency closer to the operating frequency, causing the reflection coefficient to increase. To keep the antenna area small, W_M was reduced to the minimum size where the overall reflection coefficient is still below -10 dB, which is around 450 μ m. The parametric analysis results of R shown in Fig. 17 are mainly a trade-off between gain and reflection coefficient, where the gain and the reflection coefficient are



FIGURE 16. The simulation of reflection coefficient for different W_{M} .



FIGURE 17. The simulation of (a) realized gain and (b) reflection coefficient for different *R*.



FIGURE 18. The simulation of (a) realized gain and (b) reflection coefficient for different L_{E} .

inversely proportional to *R*. Therefore, *R* was also reduced to the point where the overall reflection coefficient is still below -10 dB, which is around 3. Finally, the analysis of the L_E variation summarized in Fig. 18 shows how it behaves as a dielectric load [46] that can be tuned to boost the gain or to adjust the reflection coefficient of the antenna. In this design, L_E is tuned to achieve a balance between both gain and reflection coefficient, resulting in L_E value set to 150 μ m.

The post-optimization design parameters for the OCA main structure can be found in Fig. 5. For the chip implementation, the area around the OCA was filled with metal dummies to fulfill the metal density requirement. Fig. 19 shows the final simulation results of the non-irradiated and irradiated OCA gain, reflection coefficient, and efficiency after dummy placement. After irradiation, the designed onchip Vivaldi antenna can achieve 6 dBi realized gain and around 80% efficiency across 220 GHz to 320 GHz. The



FIGURE 19. The post-optimization Vivaldi OCA simulation results of (a) realized gain, reflection coefficient, and (b) efficiency before and after irradiation.

reflection coefficient stays below -10 dB, and the gain never decreases below 3 dB of the peak gain across the operating frequency, indicating more than 37% impedance and 3-dB gain bandwidth. Fig. 20 shows the Vivaldi OCA simulated radiation pattern from 220 GHz to 320 GHz, with detailed E and H plane 3-dB beamwidth values shown in Fig. 21. From 220 GHz to 280 GHz, the 3-dB beamwidth for the E-plane and H-plane is constant at around 76° and 100°, respectively. As the operating frequency increases to 320 GHz, the beamwidth of both E-plane and H-plane gradually decreases to 58° and 92°, respectively.

III. 1X4 ON-CHIP SLAT ARRAY

To demonstrate the application of the proposed Vivaldi OCA as a slat array element, a fully-active 1×4 slat array prototype was designed with antenna configuration shown in Fig. 22. The phase control required to perform beam steering was achieved using an on-chip 300 GHz band TRX on each element, with TRX circuit details can be found in [9]. The inter-element pitch D_A was limited to 650 μ m (0.58 λ_0 at 270 GHz) due to the TRX area constraint.

Fig. 23 shows how placing the previously optimized single element Vivaldi OCA, with $W_M = 450 \ \mu m$, in array configuration causes the reflection coefficient to degrade above the $-10 \ dB$ limit. Therefore, the W_M value was reduced to 400 μm to increase inter-element distance, which reduce the active reflection coefficient to below $-10 \ dB$ across the operating frequency and reduce the mutual coupling. This indicates different optimum parameters between stand-alone and array implementation, requiring additional re-optimization. Fig. 24 shows the simulated mutual coupling between ports and the impact of inter-element phase



FIGURE 20. The simulated radiation pattern of the irradiated post-optimization Vivaldi OCA from 220 GHz to 320 GHz.



FIGURE 21. The simulated E-plane and H-plane 3-dB beamwidth of the irradiated post-optimization Vivaldi OCA.



FIGURE 22. The top view of the 4-element on-chip Vivaldi slat array. ($D_A = 650 \ \mu m$, $W_{MA} = 400 \ \mu m$).

shift $\Delta\theta$ to the active reflection coefficient using the new W_M value. The active reflection coefficient stays below -10 dB from 220 to 320 GHz for 0° to 90° $\Delta\theta$ input, maintaining



FIGURE 23. The comparison of the simulated (a) active reflection coefficient and (b) mutual coupling of the 1x4 on-chip slat array with different W_M .



FIGURE 24. The simulated (a) active reflection coefficient with different phase shift input, and (b) mutual coupling of the 1x4 on-chip slat array with $W_M = 400 \ \mu m$.



FIGURE 25. The simulated realized gain and radiation efficiency of the 1x4 on-chip slat array with $W_{\rm M}$ = 400 $\mu m.$

the 37% impedance bandwidth. The low mutual coupling of around -20 dB keeps the change of the reflection coefficient to the minimum when $\Delta\theta$ is changed.

Fig. 25 shows the simulated gains and efficiencies of the array. The array maintained realized gain above 10 dBi and efficiency above 80% from 220 GHz to 320 GHz, maintaining the 37% 3-dB bandwidth of the single element Vivaldi OCA.

Fig. 26 shows the beam steering pattern from various $\Delta\theta$ inputs at 260 GHz. The 3-dB steering range was found at $\Delta\theta$ input of $\pm 132^{\circ}$, which corresponds to -40° and 34° steering angle, or 74° steering range. The steering range is close to the value predicted from the E-plane 3-dB beamwidth of the Vivaldi OCA, which is 76°.



FIGURE 26. The simulated E-plane beam steering pattern of the 1x4 on-chip slat array at 260 GHz.



FIGURE 27. Die micrograph of the single element Vivaldi OCA.

IV. MEASUREMENTS AND DISCUSSIONS

A. ON-CHIP VIVALDI ANTENNA MEASUREMENT

Fig. 27 shows the die micrograph of the Vivaldi OCA manufactured using the TSMC 65-nm CMOS process. The antenna occupies 0.5 mm \times 0.5 mm area on the chip. The fabricated chips were diced to 0.75 mm \times 3 mm, and the substrates were thinned to 50 μ m thick. The antenna gain and reflection coefficient were measured before and after irradiation. Another measurement was performed after 260° C annealing for 1 minute to investigate the ability of the irradiated substrate to withstand high-temperature postprocessing (e.g., flip-chip, reflow soldering).

Fig. 28 shows the measurement setup to measure the reflection coefficient, gain, and radiation pattern of the single-element Vivaldi OCA as a device-under-test (DUT). The setup consisted of two VDI WR-3.4 extenders connected to the Keysight PNA-X to perform S-parameter measurements from 220 GHz to 320 GHz frequency. The extender port-1 was connected to the DUT via a 325-GHz RF probe (Cascade Microtech i325-S-GSG), and the extender port-2 was connected to the VDI WR-3.4 diagonal horn antenna. The DUT was placed on the edge of the 3 mm thick MEGTRON6 board with a 300 μ m distance between the antenna tip and the board edge to replicate the antenna implementation on the PCB. The minimum distance *R* between the horn and the DUT was determined using the far-field equation [50]:

$$R = \frac{2D^2}{\lambda} \tag{3}$$



FIGURE 28. Measurement setup for reflection coefficient, gain, and radiation pattern.

with *D* as the aperture size. Since the horn has a significantly larger aperture than the DUT, the horn aperture diameter of 5.6 mm was used to calculate the minimum distance. The distance of 7 cm was chosen because it meets the far-field requirement at 320 GHz with some margins. The extender with the horn antenna can be swept within $\pm 60^{\circ}$ around the E-plane for radiation pattern measurements. The metal parts of the measurement setup, including the extender and the GSG probe near DUT, were covered with absorbers during the measurement session to reduce interference. The extender WR-3.4 ports were calibrated using the 2-port thru-reflect-line (TRL) calibration. Then, after attaching the GSG probe to port-1 to move the measurement plane to the probe tip, an additional 1-port short-open-load (SOL) calibration was performed.

The measured DUT reflection coefficient includes both the antenna and the pad. The pad S-parameters were characterized through separate measurements, which were used to de-embed the pad from the antenna. The simulated and measured reflection coefficients for all irradiation conditions are compared in Fig. 29. The measured reflection coefficient was below -10 dB within the measurement frequency range



FIGURE 29. Simulated and measured reflection coefficient of the fabricated Vivaldi OCA.



FIGURE 30. Simulated and measured gain of the fabricated Vivaldi OCA.

of 220 GHz to 320 GHz, or more than 37% impedance bandwidth for all sample groups. The reflection coefficients of the irradiated DUT were around 5 dB to 10 dB higher than the non-irradiated DUT because the increase in substrate resistivity reduced the substrate loss, resulting in more energy available to be transmitted or reflected.

The antenna gain can be extracted from the S_{21} measurement using the following equation:

$$G_{DUT} = S_{21} - G_{horn} + L_{pad} + L_{wg} + 20\log_{10}\left(\frac{\lambda}{4\pi R}\right)$$
(4)

where G_{horn} is the gain of the horn antenna, L_{pad} is the loss of the pad, L_{wg} is the interconnect loss from the horn to the extender, and R is the distance between the horn and the DUT. All terms are in dB. The values of G_{horn} , L_{pad} , R, and L_{wg} were known from the datasheet or separate measurements. The gain measurement and simulation results for all sample groups are compared in Fig. 30. The peak measured gain for the non-irradiated DUT was 2 dBi at 270 GHz with 2 dB variation across the measurement frequency range, which improved by 4 dB to 6 dBi peak gain at 270 GHz with 1dB variation after irradiation. The 3-dB gain bandwidth was measured to be at least 100 GHz (>37%) for all irradiation cases. No significant gain variation was observed between the irradiated and the annealed DUTs, indicating that the gain enhancement provided by the irradiation process can withstand the high-temperature post-processing.

Fig. 31 shows the measured and simulated effect of irradiation on the E-plane co-polarized radiation pattern at



FIGURE 31. Simulated and measured E-plane radiation pattern of the fabricated Vivaldi OCA at 270 GHz.



FIGURE 32. Simulated and measured E-plane radiation pattern of the irradiated Vivaldi OCA across the measurement frequency.

270 GHz. The irradiation caused similar gain improvement at pattern within $\pm 48^{\circ}$ angle and slowly diminished above that limit. The measured E-plane 3-dB beamwidth was around 76° at 270 GHz both before and after irradiation because the beamwidth was within the $\pm 46^{\circ}$ limit. The E-plane radiation pattern of the irradiated Vivaldi OCA across the measurement frequency is shown in Fig. 32. The measured E-plane 3-dB beamwidths were around 76° from 220 GHz to 280 GHz, which slowly decreases to 72° at 300 GHz and 54° at 320 GHz.

Overall, the measurement results generally match the simulation results, with a discrepancy of more than 5 dB in some parts of the reflection coefficient and cross-polarization values. The possible causes of these discrepancies include the difference between actual and simulated substrate resistivity value, the rough chip edge after the dicing process, the probe affecting the antenna characteristics, and the adhesive used to fix the DUT. Due to the limitation of the measurement setup, the antenna efficiency and H-plane 3-dB beamwidth were determined from the simulation after the model was verified with measurement results. The simulated efficiency

IEEE Open Jo

Ref.	Process	Туре	Rad.	Freq.	BW (%)	Peak Gain	Efficiency	Beamwidth (°)		
			Direction	(GHz)		(dBi)	(%)	Е	Н	Dimension
[8]	65-nm CMOS	SIW Slot	Broadside	270	15*	0*	22*	60#	60#	$0.40\lambda_0 imes 0.40\lambda_0$
[37]	65-nm CMOS	Patch	Broadside	300	14	3.1	40.3*	38#	68#	$0.23\lambda_0 imes 0.42\lambda_0$
[56]	65-nm CMOS	DRA	Broadside	325	34.5*	8.6	44	60*#	43#	$0.87\lambda_0 imes 0.87\lambda_0$
[57]	65-nm CMOS	DRA	Broadside	298	22*#	6.5*	58*	_	-	$0.50\lambda_0 imes 0.33\lambda_0$
[35]	130-nm SiGe BiCMOS	Microbump	Broadside	283	7	9.87	54.4*	37	55	$0.85\lambda_0 imes 0.85\lambda_0$
[36]	130-nm SiGe BiCMOS	Patch	Broadside	295	9	1.7	_	_	45*#	$0.25\lambda_0 imes 0.36\lambda_0$
[39]	130-nm SiGe BiCMOS	Ring	Broadside	324	13*	1.4*	41*	75*#	80*#	$0.54\lambda_0 imes 0.54\lambda_0$
[40]	130-nm SiGe BiCMOS	SIW Slot	Broadside	340	7	3.3	45*	88	76	$0.58\lambda_0 imes 0.58\lambda_0$
[46]	130-nm SiGe BiCMOS	Dipole	End-Fire	320	12.5	3.9	80*	63*#	105*#	$0.50\lambda_0 imes 0.64\lambda_0$
This Work	65-nm CMOS	Vivaldi	End-Fire	270	37	6	87*	76	96*	$0.45\lambda_0 imes 0.45\lambda_0$

TABLE 1. Comparison with state-of-the-art 300GHz band on-chip antennas.

[#] Estimated from paper * Simulated value λ_0 = Wavelength in vacuum at center frequency

Bandwidth (BW) is the worst case between 3-dB gain BW or 3-dB impedance BW. Efficiency and beamwidth measured at center frequency.

at 270 GHz is 32% for the non-irradiated DUT and 87% after irradiation. The simulated 3-dB H-plane beamwidth is 96° before and after irradiation.

Table 1 shows the comparison with other published silicon on-chip antennas operating at the 300 GHz band. The proposed antenna offers the widest bandwidth, the highest radiation efficiency, and a relatively large 3-dB beamwidth compared to previous works. This work is the only end-fire on-chip antenna implemented using a standard CMOS process with less than $0.5\lambda_0 \times 0.5\lambda_0$ dimension, making it suitable for slat array implementation.

B. 1X4 ON-CHIP SLAT ARRAY MEASUREMENT

Fig. 33 shows the die micrograph of the 1×4 slat array manufactured using the TSMC 65-nm CMOS process together with the TRX circuit [9] for phase control and beam steering demonstration. The array covers 0.65 mm \times 2.6 mm area. The chip was thinned to 50 μ m thick and attached to the PCB through a flip-chip process. The array part was irradiated with dual-layer proton irradiation, while the circuits were covered with a nickel mask to protect them from radiation damage. The DUT was measured with the setup shown in Fig. 34. The required phase shift for each element to perform beam steering was adjusted by an external computer through a serial peripheral interface (SPI) controller. The measured E-plane beam steering pattern for various phase shift $(\Delta \theta)$ input is presented in Fig. 35, which shows good agreement with simulation results at $\pm 45^{\circ}$ phase shift input. The discrepancy at the -90° phase shift might be caused by the inaccuracy of the phase shifter, as the pattern appears to have phase shift input above -90° . Other possible causes of discrepancy include rough chip edge after the dicing



FIGURE 33. The micrograph of the 1x4 slat array and the photo of the PCB implementation.

process, minor phase shifter inaccuracy, and imperfect gain calibration of each TRX element. The beam steering range of 56° across E-plane has been demonstrated. However, the 3dB steering range limit cannot be verified due to the limited TRX phase shifter range.

V. CONCLUSION

This article presented the design process, optimization, and parametric analysis of a 300 GHz band on-chip Vivaldi





FIGURE 34. The setup for the 1x4 slat array beam steering pattern measurement.



FIGURE 35. The measurement results of the E-plane beam steering pattern at 260 GHz.

antenna for implementation on a standard 65nm CMOS process with a proton-irradiated substrate. The designed OCA was fabricated, irradiated, and measured to verify the proposed design. The measurement results show 3-4 dB gain improvement across the operating frequency after irradiation, achieving 6 dBi peak gain and 87% efficiency at 270 GHz. The Vivaldi OCA achieved 76° E-plane beamwidth at 270 GHz and fully covers the 300 GHz band (220 GHz to 320 GHz), which corresponds to 37% impedance and 3-dB gain bandwidth. The implementation of the Vivaldi OCA in 1×4 slat array was performed, which demonstrates 56° beam steering range. The wide bandwidth, large beamwidth,

and high efficiency demonstrated by the Vivaldi OCA make it suitable for future on-chip slat array implementation to achieve full 2-dimensional array scaling.

REFERENCES

- S. X. Huang et al., "Terahertz Mueller matrix polarimetry and polar decomposition," *IEEE Trans. THz Sci. Technol.*, vol. 10, no. 1, pp. 74–84, Jan. 2020, doi: 10.1109/TTHZ.2019.2947234.
- [2] J. Grajal et al., "Compact radar front-end for an imaging radar at 300 GHz," *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 3, pp. 268–273, May 2017, doi: 10.1109/TTHZ.2017.2673544.
- [3] A. Mostajeran et al., "A high-resolution 220-GHz ultrawideband fully integrated ISAR imaging system," *IEEE Trans. Microw. Theory Tech.*, vol. 67, no. 1, pp. 429–442, Jan. 2019, doi: 10.1109/TMTT.2018.2874666.
- [4] S. Thomas, C. Bredendiek, and N. Pohl, "A SiGe-based 240-GHz FMCW radar system for high-resolution measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 67, no. 11, pp. 4599–4609, Nov. 2019, doi: 10.1109/TMTT.2019.2916851.
- [5] E. Turkmen et al., "A 223-276-GHz cascadable FMCW transceiver in 130-nm SiGe BiCMOS for scalable MIMO radar arrays," *IEEE Trans. Microw. Theory Tech.*, vol. 71, no. 12, pp. 5393–5412, Dec. 2023, doi: 10.1109/TMTT.2023.3279872.
- [6] J. Grzyb, K. Statnikov, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 210–270-GHz circularly polarized FMCW radar with a singlelens-coupled SiGe HBT chip," *IEEE Trans. THz Sci. Technol.*, vol. 6, no. 6, pp. 771–783, Nov. 2016, doi: 10.1109/TTHZ.2016.2602539.
- [7] R. Hasan, M. H. Eissa, W. A. Ahmad, H. J. Ng, and D. Kissinger, "Wideband and efficient 256-GHz subharmonic-based FMCW radar transceiver in 130-nm SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 71, no. 1, pp. 59–70, Jan. 2023, doi: 10.1109/TMTT.2022.3207995.
- [8] X. Yi, C. Wang, X. Chen, J. Wang, J. Grajal, and R. Han, "A 220to-320-GHz FMCW radar in 65-nm CMOS using a frequency-comb architecture," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 327–339, Feb. 2021, doi: 10.1109/JSSC.2020.3020291.
- [9] C. Wang et al., "A 236-to-266GHz 4-element amplifier-last phased-array transmitter in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Tech. Dig.*, 2024, pp. 415–417, doi: 10.1109/ISSCC49657.2024.10454273.
- [10] I. Abdo et al., "A bi-directional 300-GHz-band phased-array transceiver in 65-nm CMOS with outphasing transmitting mode and LO emission cancellation," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2292–2308, Aug. 2022, doi: 10.1109/JSSC.2022.3179166.
- [11] S. Lee et al., "An 80-Gb/s 300-GHz-band single-chip CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3577–3588, Dec. 2019, doi: 10.1109/JSSC.2019.2944855.
- [12] S. Hara et al., "A 76-Gbit/s 265-GHz CMOS receiver with WR-3.4 waveguide interface," *IEEE J. Solid-State Circuits*, vol. 57, no. 10, pp. 2988–2998, Oct. 2022, doi: 10.1109/JSSC.2022.3179560.
- [13] K. Katayama et al., "A 300 GHz CMOS transmitter with 32-QAM 17.5 Gb/s/ch capability over six channels," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3037–3048, Dec. 2016, doi: 10.1109/JSSC.2016.2602223.
- [14] H. Hamada et al., "300-GHz-band 120-Gb/s wireless front-end based on InP-HEMT PAs and mixers," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2316–2335, Sep. 2020, doi: 10.1109/JSSC.2016.2602223.
- [15] H. Tataria, M. Shafi, A. F. Molisch, M. Dohler, H. Sjoland, and F. Tufvesson, "6G wireless systems: Vision, requirements, challenges, insights, and opportunities," *Proc. IEEE*, vol. 109, no. 7, pp. 1166–1199, Jul. 2021, doi: 10.1109/JPROC.2021.3061701.
- [16] P. V. Testa, C. Carta, and F. Ellinger, "Novel high-performance bondwire chip-to-chip interconnections for applications up to 220 GHz," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 2, pp. 102–104, Feb. 2018, doi: 10.1109/LMWC.2018.2792695.
- [17] C. H. Li and T. Y. Chiu, "Low-loss single-band, dual-band, and broadband mm-wave and (sub-)THz interconnects for THz SoP heterogeneous system integration," *IEEE Trans. THz Sci. Technol.*, vol. 12, no. 2, pp. 130–143, Mar. 2022, doi: 10.1109/TTHZ.2021.3128596.
- [18] A. Saeed, H. E. Yaldiz, and F. Alagoz, "GHz-to-THz broadband communications for 6G non-terrestrial networks," *ITU J. Future Evol. Tech.*, vol. 4, no. 1, pp. 241–250, Mar. 2023, doi: 10.52953/AOKY1032.

- [19] S. van Berkel et al., "Wideband double leaky slot lens antennas in CMOS technology at submillimeter wavelengths," *IEEE Trans. THz Sci. Technol.*, vol. 10, no. 5, pp. 540–553, Sep. 2020, doi: 10.1109/TTHZ.2020.3006750.
- [20] K. Sarabandi, A. Jam, M. Vahidpour, and J. East, "A novel frequency beam-steering antenna array for submillimeter-wave applications," *IEEE Trans. THz Sci. Technol.*, vol. 8, no. 6, pp. 654–665, Nov. 2018, doi: 10.1109/TTHZ.2018.2866019.
- [21] T. Sowlati et al., "A 60GHz 144-element phased-array transceiver with 51dBm maximum EIRP and $\pm 60^{\circ}$ beam steering for backhaul application," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Tech. Dig.*, 2018, pp. 66–68, doi: 10.1109/ISSCC.2018.8310186.
- [22] H.-C. Park et al., "A 39GHz-band CMOS 16-channel phasedarray transceiver IC with a companion dual-stream IF transceiver IC for 5G NR base-station applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Tech. Dig.*, 2020, pp. 76–78, doi: 10.1109/ISSCC19947.2020.9063006.
- [23] Y. Wang et al., "A 39-GHz 64-element phased-array transceiver with built-in phase and amplitude calibrations for large-array 5G NR in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1249–1269, May 2020, doi: 10.1109/JSSC.2020.2980509.
- [24] J. S. Herd and M. D. Conway, "The evolution to modern phased array architectures," *Proc. IEEE*, vol. 104, no. 3, pp. 519–529, Mar. 2016, doi: 10.1109/JPROC.2015.2494879.
- [25] C. Wang et al., "A sub-THz full-duplex phased-array transceiver with self-interference cancellation and LO Feedthrough suppression," *IEEE J. Solid-State Circuits*, vol. 59, no. 4, pp. 978–992, Apr. 2024, doi: 10.1109/JSSC.2024.3353067.
- [26] K. K. Tokgoz et al., "A 120Gb/s 16QAM CMOS millimeter-wave wireless transceiver," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Tech. Dig.*, 2018, pp. 168–170, doi: 10.1109/ISSCC.2018.8310237.
- [27] W. Deng et al., "A D-band joint radar-communication CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 411–427, Feb. 2023, doi: 10.1109/JSSC.2022.3185160.
- [28] A. Karakuzulu, W. A. Ahmad, D. Kissinger, and A. Malignaggi, "A four-channel bidirectional D-band phased-array transceiver for 200 Gb/s 6G wireless communications in a 130-nm BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1310–1322, May 2023, doi: 10.1109/JSSC.2022.3232948.
- [29] M. Elkhouly et al., "Fully integrated 2D scalable TX/RX Chipset for D-band phased-array-on-glass modules," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Tech. Dig.*, 2022, pp. 76–78, doi: 10.1109/ISSCC42614.2022.9731626.
- [30] J. Pang et al., "A 50.1-Gb/s 60-GHz CMOS transceiver for IEEE 802.11ay with calibration of LO feedthrough and I/Q imbaLance," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1375–1390, May 2019, doi: 10.1109/JSSC.2018.2886338.
- [31] K. Dasgupta et al., "A 60-GHz transceiver and baseband with polarization MIMO in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3613–3627, Dec. 2018, doi: 10.1109/JSSC.2018.2876473.
- [32] P. Zhou et al., "A -28.5-dB EVM 64-QAM 45-GHz transceiver for IEEE 802.11aj," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 3077–3093, Oct. 2021, doi: 10.1109/JSSC.2021.3057077.
- [33] B. B. Adela, P. T. M. van Zeijl, U. Johannsen, and A. B. Smolders, "On-chip antenna integration for millimeter-wave single-chip FMCW radar, providing high efficiency and isolation," *IEEE Trans. Antennas Propag.*, vol. 64, no. 8, pp. 3281–3291, Aug. 2016, doi: 10.1109/TAP.2016.2570228.
- [34] H. M. Cheema and A. Shamim, "The last barrier: On-chip antennas," *IEEE Microw. Mag.*, vol. 14, no. 1, pp. 79–91, Jan. 2013, doi: 10.1109/MMM.2012.2226542.
- [35] T. Deng, Y. Zhang, Z. Zheng, Q. Yan, and J.-F. Mao, "High-gain and high-efficiency sub-terahertz antenna-on-chip with microbumps for highly-integrated systems," *IEEE Trans. Antennas Propag.*, vol. 72, no. 5, pp. 4107–4115, May 2024, doi: 10.1109/TAP.2024.3381444.
- [36] T. Pfahler, M. Vossiek, and J. Schür, "Compact and broadband 300 GHz three-element on-chip patch antenna," in *Proc. Radio Wireless Symp. (RWS)*, 2023, pp. 139–142, doi: 10.1109/RWS55624.2023.10046297.
- [37] C. Lee and J. Jeong, "THz CMOS on-chip antenna array using defected ground structure," *Electronics*, vol. 9, no. 7, p. 1137, Jul. 2020, doi: 10.3390/electronics9071137.

[38] L. J. Xu, F. C. Tong, X. Bai, and Q. Li, "Design of miniaturised on-chip slot antenna for THz detector in CMOS," *IET Microw. Antennas Propag.*, vol. 12, no. 8, pp. 1324–1331, Mar. 2018, doi: 10.1049/iet-map.2017.0833.

IEEE Open Journal of

- [39] H. Zhu, X. Li, Z. Qi, and J. Xiao, "A 320 GHz octagonal shorted annular ring on-chip antenna array," *IEEE Access*, vol. 8, pp. 84282–84289, 2020, doi: 10.1109/ACCESS.2020.2991868.
- [40] X. D. Deng, Y. Li, W. Wu, and Y. Z. Xiong, "340-GHz SIW cavity-backed magnetic rectangular slot loop antennas and arrays in silicon technology," *IEEE Trans. Antennas Propag.*, vol. 63, no. 12, pp. 5272–5279, Dec. 2015, doi: 10.1109/TAP.2015.2490248.
- [41] H. Zhu, X. Li, W. Feng, J. Xiao, and J. Zhang, "235 GHz onchip antenna with miniaturised AMC loading in 65 nm CMOS," *IET Microw. Antennas Propag.*, vol. 12, no. 5, pp. 727–733, Mar. 2018, doi: 10.1049/iet-map.2017.0710.
- [42] Q. Le Zhang, X. G. Shi, B. J. Chen, K. F. Chan, K. M. Shum, and C. H. Chan, "325 GHz to 500 GHz single-layer planar Goubauline antenna with endfire radiation based on substrate mode," *IEEE Trans. Antennas Propag.*, vol. 70, no. 9, pp. 7755–7765, Sep. 2022, doi: 10.1109/TAP.2022.3164180.
- [43] S. Erdogan and M. Swaminathan, "D-band quasi-Yagi antenna in glass-based package," in *Proc. Int. Microw. RF Conf. (IMARC)*, 2021, pp. 1–4, doi: 10.1109/IMARC49196.2021.9714564.
- [44] W. T. Khan et al., "A D-band micromachined end-fire antenna in 130-nm SiGe BiCMOS technology," *IEEE Trans. Antennas Propag.*, vol. 63, no. 6, pp. 2449–2459, Jun. 2015, doi: 10.1109/TAP.2015.2416751.
- [45] S. Gearhart, H. Ekstrom, P. Acharya, E. Kollberg, S. Jacobsson, and G. Rebeiz, "Submillimeter-wave endfire slotline antennas," in *Proc. Antennas Propag. Soc. Int. Symp. (APS)*, 1992, pp. 1898–1901, doi: 10.1109/APS.1992.221702.
- [46] X.-D. Deng, Y. Li, H. Tang, W. Wu, and Y.-Z. Xiong, "Dielectric loaded endfire antennas using standard silicon technology," *IEEE Trans. Antennas Propag.*, vol. 65, no. 6, pp. 2797–2807, Jun. 2017, doi: 10.1109/TAP.2017.2673800.
- [47] D. Tang et al., "The integration of proton bombardment process into the manufacturing of mixed-signal/RF chips," in *IEDM Tech. Dig.*, 2003, pp. 28.6.1–28.6.4, doi: 10.1109/IEDM.2003.1269370.
- [48] L. S. Lee et al., "Isolation on Si wafers by MeV proton bombardment for RF integrated circuits," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 928–934, May 2001, doi: 10.1109/16.918241.
- [49] P. Gibson, "The Vivaldi aerial," in Proc. Eur. Microw. Conf., 1979, pp. 101–105, doi: 10.1109/EUMA.1979.332681.
- [50] C. A. Balanis, Antenna Theory: Analysis and Design, 4th ed. Hoboken, NJ, USA: Wiley, 2016.
- [51] D. Schaubert, E. Kollberg, T. Korzeniowski, T. Thungren, J. Johansson, and K. Yngvesson, "Endfire tapered slot antennas on dielectric substrates," *IEEE Trans. Antennas Propag.*, vol. 33, no. 12, pp. 1392–1400, Dec. 1985, doi: 10.1109/TAP.1985.1143542.
- [52] F. J. Zucker, "Surface-wave antennas," in Antenna Engineering Handbook, 4th ed. New York, NY, USA: McGraw-Hill, 2007, p. 10.
- [53] M. Moosazadeh, S. Kharkovsky, J. T. Case, and B. Samali, "Antipodal Vivaldi antenna with improved radiation characteristics for civil engineering applications," *IET Microw. Antennas Propag.*, vol. 11, no. 6, pp. 796–803, Mar. 2017, doi: 10.1049/iet-map.2016.0720.
- [54] C. H. Ho, L. Fan, and K. Chang, "New uniplanar coplanar waveguide hybrid-ring couplers and magic-T's," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 12, pp. 2440–2448, Dec. 1994, doi: 10.1109/22.339779.
- [55] H. Herdian, T. Inoue, T. Hirano, M. Sogabe, A. Shirane, and K. Okada, "Dual-layer proton irradiation for creating thermallystable high-resistivity region in Si CMOS substrate," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2021, pp. 191–194, doi: 10.1109/ESSDERC53440.2021.9631800.
- [56] S. Kong, K. M. Shum, C. Yang, L. Gao, and C. H. Chan, "Wide impedance-bandwidth and gain-bandwidth Terahertz on-chip antenna with chip-integrated dielectric resonator," *IEEE Trans. Antennas Propag.*, vol. 69, no. 8, pp. 4269–4278, Aug. 2021, doi: 10.1109/TAP.2021.3060060.
- [57] E. Shaulov, S. Jameson, and E. Socher, "A zero bias J-band antenna-coupled detector in 65-nm CMOS," *IEEE Trans. THz Sci. Technol.*, vol. 11, no. 1, pp. 62–69, Jan. 2021, doi: 10.1109/TTHZ.2020.3038026.



HANS HERDIAN (Graduate Student Member, IEEE) received the B.Sc. degree from the Bandung Institute of Technology, Bandung, Indonesia, in 2016, and the M.S. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 2018, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering.

His research interests include millimeter and sub-millimeter wave wireless transceiver systems, device modeling, and on-chip passive components modeling and performance enhancement.



ATSUSHI SHIRANE (Member, IEEE) received the B.E. degree in electrical and electronic engineering and the M.E. and Ph.D. degrees in electronics and applied physics from the Tokyo Institute of Technology, Tokyo, Japan, in 2010, 2012, and 2015, respectively.

From 2015 to 2017, he was with Toshiba Corporation, Kawasaki, Japan, where he developed an 802.11ax wireless LAN RF transceiver. From 2017 to 2018, he was with Nidec Corporation, Kawasaki, where he researched intelligent motors

with wireless communication. He is currently an Associate Professor with the Laboratory for Future Interdisciplinary Research of Science and Technology, Institute of Innovative Research, Tokyo Institute of Technology. His current research interests include RF CMOS transceivers for the IoT, 5G, satellite communication, and wireless power transfer.

Dr. Shirane has been a member of Technical Program Committee of the IEEE International Solid-State Circuits Conference Student Research Preview since 2019. He is a member of the IEEE Solid-State Circuits Society and the Institute of Electronics, Information, and Communication Engineers (IEICE).



CHUN WANG (Graduate Student Member, IEEE) received the B.E. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2015, and the M.E. degree from Zhejiang University, Hangzhou, China, in 2018. He is currently pursuing the Ph.D. degree in electrical and electronic engineering focusing on millimeter-wave front end and system design with the Tokyo Institute of Technology, Tokyo, Japan. His research interests include CMOS RF/sub-

THZ/THZ transceivers, phased-array transceivers, device modeling, and wireless communication systems.



KENICHI OKADA (Fellow, IEEE) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively.

From 2000 to 2003, he was a Research Fellow with the Japan Society for the Promotion of Science, Kyoto University. In 2003, he joined the Tokyo Institute of Technology, Tokyo, Japan, as an Assistant Professor, where he is currently a Professor of electrical and electronic engineering.

He has authored or coauthored more than 500 journal and conference papers. His current research interests include millimeter-wave and terahertz CMOS wireless transceivers for 20/28/39/60/77/79/100/300 GHz for 5G, WiGig, satellite and future wireless systems, digital PLL, synthesizable PLL, atomic clock, and ultra-low-power wireless transceivers for Bluetooth low-energy, and sub-GHz applications.

Prof. Okada was a recipient or co-recipient of the Ericsson Young Scientist Award, in 2004, the A-SSCC Outstanding Design Award, in 2006 and 2011, the ASP-DAC Special Feature Award, in 2011, the Best Design Award, in 2014 and 2015, the MEXT Young Scientists' Prize in 2011, the JSPS Prize in 2014, the Suematsu Yasuharu Award, in 2015, the MEXT Prizes for Science and Technology, in 2017, the RFIT Best Paper Award, in 2017, the IEICE Best Paper Award, in 2018, the RFIC Symposium Best Student Paper Award, in 2019, the IEICE Achievement Award, in 2019, the DOCOMO Mobile Science Award, in 2019, the IEEE/ACM ASP-DAC Prolific Author Award, in 2020, the Kenjiro Takayanagi Achievement Award, in 2020, the KDDI Foundation Award, in 2020, the IEEE CICC Best Paper Award, in 2020, the IEEE ISSCC Author-Recognition Award, in 2023, and more than 50 other international and domestic awards. He is a member of the Institute of Electronics, Information, and Communication Engineers (IEICE), the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP). He is/was a member of Technical Program Committees of the IEEE International Solid-State Circuits Conference, the VLSI Circuits Symposium, the European Solid-State Circuits Conference. the Radio Frequency Integrated Circuits Symposium, and the Asian Solid-State Circuits Conference. He is/was also a Guest Editor and an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUIT, an Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and a Distinguished Lecturer of IEEE SOLID-STATE CIRCUITS SOCIETY.



TAKESHI INOUE received the B.S., M.S., and Ph.D. degrees in solid-state physics from the Okayama University of Science, Okayama, Japan, in 2000, 2002, and 2006, respectively.

From 2006 to 2008, he was a Postdoctoral Fellow with the Okayama University of Science. He is currently with SHI-ATEX Company Ltd., Japan.