Coordinated Capacitor Voltage Balancing Method for Cascaded H-bridge Inverter with Supercapacitor and DC-DC Stage

Ye Zhang, Zixin Li, *Senior Member, IEEE*, Fanqiang Gao, *Member, IEEE*,
Cong Zhao, *Member, IEEE*, and Yaohua Li

***Abstract*—Cascaded H-bridge inverter (CHBI) with supercapacitors (SCs) and dc-dc stage shows significant promise for medium to high voltage energy storage applications. This paper investigates the voltage balance of capacitors within the CHBI, including both the dc-link capacitors and SCs. Balance control over the dc-link capacitor voltages is realized by the dc-dc stage in each submodule (SM), while a hybrid modulation strategy (HMS) is implemented in the H-bridge to balance the SC voltages among the SMs. Meanwhile, the dc-link voltage fluctuations are analyzed under the HMS. A virtual voltage variable is introduced to coordinate the balancing of dc-link capacitor voltages and SC voltages. Compared to the balancing method that solely considers the SC voltages, the presented method reduces the dc-link voltage fluctuations without affecting the voltage balance of SCs. Finally, both simulation and experimental results verify the effectiveness of the presented method.**

***Index Terms*—Cascaded H-bridge inverter (CHBI), Hybrid modulation strategy (HMS), Capacitor voltage balancing, DC-link voltage fluctuation, Supercapacitor (SC).**

I. Introduction

OVER the past few decades, cascaded H-bridge inverters (CHBIs) have found widespread applications in various medium and high voltage scenarios [1]-[3]. In addition, supercapacitors (SCs) are recognized for their fast discharge rate and high power density. Integrating SCs into the CHBI presents a promising energy storage solution for short-time high power and fast-changing load demands [4]-[5]. Equipped with a dc-dc stage within each submodule (SM), such as a bi-directional dc-dc converter (BDC), as depicted in Fig. 1, this CHBI ensures a distributed control over each SM, concurrently enhancing the discharging range of SCs [6]-[7].

The CHBI, as shown in Fig. 1, incorporates numerous SCs and dc-link capacitors. Balancing these capacitor voltages is of great importance, as it directly impacts the stability of the CHBI [8]-[9]. The imbalance and large fluctuations in the voltages of dc-link capacitors can affect the waveform quality of the output voltage for the CHBI and even cause capacitor overvoltage. In terms of SC voltage balancing, it aims to prevent some SMs with lower SC voltages from experiencing higher current stress through the BDC, thereby avoiding overcurrent in the power semiconductor devices. The stored SC energies across all SMs can also be fully utilized, preventing individual SCs from being over-charged or over-discharged and ensuring approximately consistent lifespans. To this end, with BDC control in each SM, the dc-link capacitor voltages can be regulated around the same reference value to achieve balance. The modulation strategy of the H-bridge, serving as another control degree of freedom for the SM, significantly affects the voltage balance of SCs [10].

In [10]-[12], a hybrid modulation strategy (HMS) is employed for both the half-bridges in the multilevel modular converter (MMC) and the H-bridges in the CHBI. This strategy combines low frequency nearest level modulation (NLM) with high frequency pulse width modulation (PWM). Therefore, the HMS inherits the benefit of simple capacitor voltage balancing from the NLM, where the capacitor voltage balancing can be achieved by rotating the order of inserted SMs without the need for extra proportional-integral (PI)-based closed-loop control for each SM [13]. According to SM voltage sorting and the sign of instantaneous ac power, the switching modes of the H-bridge are determined, which enables charging or discharging of the inserted SMs within different control cycles. Thus, the voltage balance of SCs is facilitated under the HMS. Additionally, by introducing a PWM SM, the desired sine modulation wave can be approximated. In [14], the HMS is further categorized into two types based on the flexible allocation of switching modes among the H-bridges: HMS containing zero mode (HMSCZM) and HMS without zero mode (HMSWZM).

Although the HMS offers advantages in capacitor voltage balancing, differences in the switching modes of the H-bridge between the inserted and bypassed SMs result in inconsistent voltage fluctuations in the dc-link among the SMs [15]. These

Manuscript received March 05, 2024; revised April 22, 2024; accepted April 29, 2024. Date of publication June 25, 2024; Date of current version May 05, 2024.

This work was supported in part by the CAS Project for Young Scientists in Basic Research under Grant No. YSBR-045, in part by the Youth Innovation Promotion Association CAS under Grant 2022137, and in part by the Institute of Electrical Engineering, CAS under Grant E155320101. (*Corresponding Author*: *Fanqiang Gao*.)

The authors are with the Key Laboratory of High Density Electromagnetic Power and Systems (Chinese Academy of Sciences), Institute of Electrical Engineering, Chinese Academy of Sciences, Haidian District, Beijing 100190, China, and also with the University of Chinese Academy of Sciences, Shijingshan District, Beijing 100049, China (e-mail: zhangye@mail.iee.ac.cn; lzx@mail.iee.ac.cn; gao-fanqiang@mail.iee.ac.cn; zhaocong@mail.iee.ac.cn; yhli@mail.iee.ac.cn).

Digital Object Identifier 10.30941/CESTEMS.2024.00019

significant voltage fluctuations can lead to heating and aging of the dc-link capacitors, affecting the safety and reliability of the SMs. As depicted in [16], paralleling an LC resonant branch on the dc-link can suppress voltage fluctuations with a specific frequency component. Increasing the dc-link capacitance can indeed reduce voltage fluctuations [17]-[18]. However, these hardware measures inevitably increase the volume and cost of SMs. In [5], Li *et al.* presented a hybrid voltage sorting method to bypass SMs with higher dc-link voltage fluctuations, but this method lacks theoretical analysis. In [15], Mao pointed out that, due to the necessity of zero mode, the voltage fluctuations in the dc-link under the HMSCZM can exhibit lower compared to those under the HMSWZM. Then, the traditional HMSWZM was modified in [19] by introducing some SMs running in zero mode when their dc-link voltages reached the reference value. However, the switching modes of the H-bridge for some SMs still have opposite polarity, indicating that the dc-link voltage fluctuations under the modified HMSWZM are greater than those under the HMSCZM. In [20], an improved NLM was presented for the MMC by specifically inserting and bypassing a fixed number of SMs within each control cycle, realizing low switching frequency and reduced capacitor voltage fluctuations. However, each SM in this MMC possesses only one capacitor, which differs from the SM depicted in Fig. 1. What is more, the waveform quality of the ac output voltage under this NLM is not as high as that under the HMS for the CHBI with fewer SMs. It is noteworthy that the BDC controller with feed-forward of the load current on the dc-link in [9] contributed to eliminating the voltage fluctuation in the dc-link, but the total second-order harmonic power is burdened by the BDC, increasing the BDC current stress. Similarly, in [18], to suppress the dc-link voltage fluctuations with various frequency components, the harmonic current from the H-bridge was calculated and injected into the dc-link voltage control loop. Although the dc-link capacitors are not required to give the fluctuating power, the current stress of the front converter is increased. In [21], an optimal control trajectory method was presented to minimize the current stress of DC-DC stage under any certain dc-link voltage fluctuations. However, this method does not involve the voltage fluctuations difference in the dc-link among the several SMs caused by the HMS for the H-bridges. Hence, building upon the HMSCZM, this paper aims to coordinately address the reduction of dc-link voltage fluctuations while ensuring the voltage balance of SCs.

The rest of this paper is structured as follows: In Section II, the principles of capacitor voltage balancing are outlined, and the dc-link voltage fluctuations among the SMs under the HMS are analyzed. Section III presents a capacitor voltage balancing method that reduces dc-link voltage fluctuations by introducing a virtual SM voltage sorting variable, along with details on its implementation. The simulations in MATLAB/ Simulink with fifteen SMs and experiments on a prototype with four SMs are performed to demonstrate the validity of the presented method in Section IV. Finally, Section V concludes this paper.

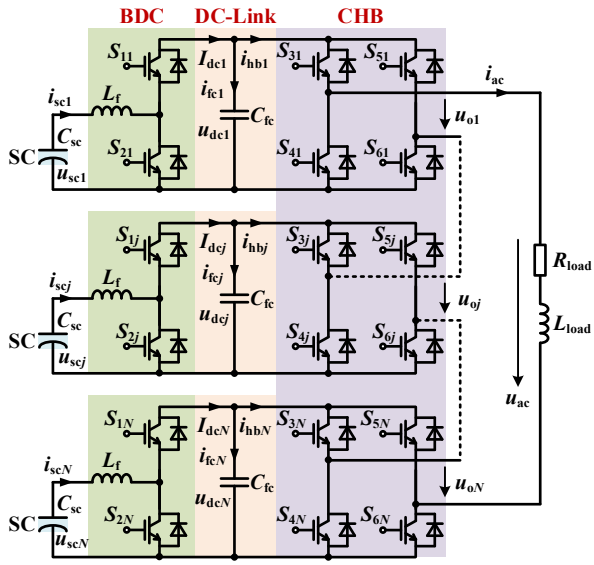


Fig. 1. Circuit topology of the CHBI with SC and BDC.

II. Operation Principles

A. Circuit Topology

The circuit topology of the single-phase CHBI with SC and BDC is depicted in Fig. 1. This phase cluster comprises N SMs, each with identical parameters. The ac output terminals of each SM are connected in series to the load. The ac output voltage of the jth SM is denoted as u_{oj}, where $j = 1, 2, \dots, N$, and u_{ac} is their sum. The ac current is represented as i_{ac}, with the sign defined as positive when it flows out of the H-bridge. Each SM is equipped with six insulated gate bipolar transistors (IGBTs, S_1-S_6). The dc-link capacitor is denoted as C_{fc}, where u_{dc} and i_{fc} represent its voltage and current, respectively. The filtering inductor of the BDC is denoted as L_f. The SC voltage and current are denoted as u_{sc} and i_{sc}, respectively.

B. DC-Link Voltage Balancing Control

As shown in Fig. 2, the dc-link voltage of each SM, u_{dcj}, can be independently stabilized around the same reference value U_{dc}^* through a double closed-loop PI controller. The inner loop is responsible for controlling the SC current i_{scj}. Consequently, the dc-link voltages are regulated around U_{dc}^* and balanced.

Nevertheless, accurate control of u_{dcj} at U_{dc}^* is challenging, particularly when considering the current stress of the BDC. This challenge arises from the reason that zero dc-link voltage fluctuation means that the dc-link capacitor does not consume any second-order harmonic power $\tilde{p}_{sm}$ within the SM, as shown in Fig. 3. At this moment, further analysis is conducted on the maximum of BDC current.

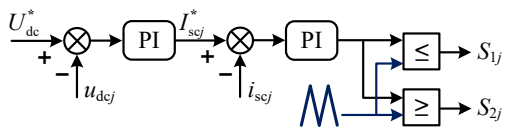


Fig. 2. Block diagram of the BDC controller.

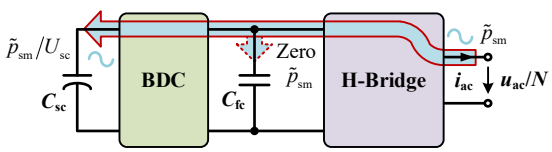


Fig. 3. Scenario when all second-order harmonic power flows into the BDC.

When ignoring the high-order harmonics in the ac voltage u_{ac} and current i_{ac}, the instantaneous ac power p_{ac} flowing through the CHBI can be derived as:

$$p_{ac} = u_{ac}i_{ac} = \underbrace{0.5U_{ac}I_{ac}\cos\varphi}_{P_{ac}} + \underbrace{\left[-0.5U_{ac}I_{ac}\cos\left(2\omega t-\varphi\right)\right]}_{\tilde{p}_{ac}} \quad (1)$$

where $u_{ac} = U_{ac}\sin(\omega t)$, $i_{ac} = I_{ac}\sin(\omega t\text{-}\varphi)$, U_{ac} and I_{ac} represents the peaks of u_{ac} and i_{ac}, ω is the ac angular frequency, φ denotes the load power factor angle, P_{ac} and $\tilde{p}_{ac}$ are the active power and second-order harmonic power, respectively. Assuming that the ac power through each SM, p_{sm}, is shared evenly within one fundamental cycle when the CHBI operates steadily, i.e.:

$$p_{sm} = P_{sm} + \tilde{p}_{sm} = \left(P_{ac} + \tilde{p}_{ac}\right)/N \quad (2)$$

When the whole p_{sm} is provided by the BDC, the maximum of SC current can be calculated as:

$$I_{sc\text{-}max} = \max\left(p_{sm}/U_{sc}\right) = 0.5U_{ac}I_{ac}\left(\cos\varphi+1\right)/\left(NU_{sc}\right) \quad (3)$$

As a result, $I_{sc\text{-}max}$ can be at least doubled compared to P_{ac}/NU_{sc}. However, especially for a small φ, this scenario in Fig. 3 is not advisable as it will significantly increase the current stress of the BDC. Therefore, this paper allows the presence of double frequency ripple in the dc-link voltages, rather than attempting to eliminate them through the BDC controller.

C. SC Voltage Balancing Control

The HMS combines low-frequency square-wave modulation with high-frequency PWM to approximate the desired sine wave $u_{ac\text{-}ref}$, while also being responsible for balancing the SC voltages, as depicted in Fig. 4. The normal switching modes of the H-bridge in the HMS are listed in Table I, corresponding to various switching functions of the H-bridge S_{hb}s. The inserted SMs can operate in the "+1", "–1" and PWM modes, while the remaining bypassed SMs run in the "0" mode. The sign of the instantaneous ac power p_{ac} will determine whether the inserted SMs will charge or discharge the SCs. The main steps of the conventional HMS-based SC voltage balancing are below:

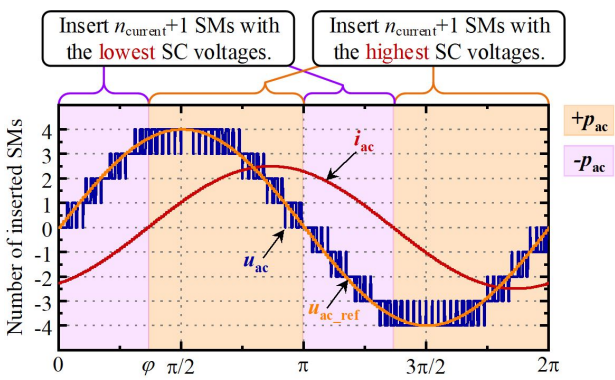


Fig. 4. HMS-based SC voltage balancing control.

TABLE I
SWITCHING MODES OF THE H-BRIDGE

Mode	+1	–1	PWM	0
S_{hbj}	+1	–1	PWM reference	0
$+p_{ac}$	discharging		similar to "±1" mode	bypassing
$-p_{ac}$	charging			

1) The sampled SC voltages are selected as the SM voltage sorting variable and arranged in descending order at a specific sorting frequency f_{sort}.

2) To approximate the desired sine wave $u_{ac\text{-}ref}$ under the HMS, a certain number of SMs needs to be inserted while the remaining SMs are bypassed within each control cycle. Note that the polarities of the switching modes for the inserted SMs always remain consistent in this paper, i.e., the "+1" mode and "–1" mode do not appear at the same control cycle. Based on the desired $u_{ac\text{-}ref}$ and the average dc-link voltage $u_{dc\text{-}ave}$, the number of inserted SMs with "+1" mode or "–1" mode within the current control cycle, $n_{current}$, can be calculated as:

$$n_{current} = \text{floor}\left(\left|u_{ac\text{-}ref}\right|/u_{dc\text{-}ave}\right) \quad (4)$$

where floor(x) is the function rounding x to the nearest integer toward zero, and $u_{dc\text{-}ave}$ is expressed as:

$$u_{dc\text{-}ave} = \sum_{j=1}^{N} u_{dcj}/N \quad (5)$$

According to the sign of $u_{ac\text{-}ref}$, determine whether the inserted SM will operate in the "+1" or "–1" modes. Meanwhile, the PWM reference of the PWM mode SM can be given by:

$$u_{ac\text{-}pwm} = u_{ac\text{-}ref} - \text{sign}\left(u_{ac\text{-}ref}\right)\cdot n_{current}u_{dc\text{-}ave} \quad (6)$$

where the function sign(x) returns the sign of x, yielding 1 when x is positive, 0 when x is zero, and –1 when x is negative.

3) The selection of inserted SMs depends on the SM voltage sorting order within each sorting cycle and the sign of the instantaneous ac power p_{ac}. When p_{ac}> 0, i.e., the CHBI is discharging, it will insert the $n_{current}$+1 SMs with the highest SC voltages while bypassing the rest with the lowest SC voltages. Whereas, for p_{ac}< 0, i.e., the CHBI is charging, the SMs with the lowest SC voltages are inserted, while those with the highest SC voltages are bypassed.

In brief, based on the HMS, the voltage balance of SCs is realized by alternately charging or discharging the inserted SMs. However, a difference exists in the switching modes of the H-bridge between the inserted and bypassed SMs. The influence of this difference on the dc-link voltage fluctuation is further investigated.

D. Analysis of DC-link Voltage Fluctuations

According to Kirchhoff's current law, the dc-link capacitor current i_{fc} in Fig. 1 can be expressed as:

$$i_{fcj} = I_{dcj} - i_{hbj} \quad (7)$$

where I_{dcj} represents the average output current of the BDC when ignoring the switching effect of the BDC, and the load current on the dc-link is represented as i_{hbj}. By introducing the switching function of the H-bridge S_{hb}, the dc-link capacitor

current i_{fc} is further obtained:

$$i_{fcj} = I_{dcj} - i_{hbj} = I_{dcj} - S_{hbj} i_{ac} \tag{8}$$

The relationship between the average SC current I_{sc} and the active power P_{ac} can be expressed as:

$$P_{ac} = 0.5 U_{ac} I_{ac} \cos\varphi = \sum_{j=1}^{N} U_{scj} I_{scj} \tag{9}$$

Assuming that the average SC voltages of N SMs, U_{sc}s, are balanced when the CHBI works steadily, the average SC currents among the N SMs, I_{sc}s, can be considered equal based on (9), i.e., $I_{sc1} = I_{sc2} =$, … , $= I_{scN}$. When invoking the power conservation theorem and neglecting the operation loss of BDC, the average output current of the BDC, I_{dcj}, can be derived as:

$$I_{dcj} = \left(U_{scj} I_{scj}\right) \Big/ U_{dcj} \tag{10}$$

At this point, I_{dc}s of the N SMs can also be considered as the same, i.e., $I_{dc1} = I_{dc2} =$, … , $= I_{dcN}$. Furthermore, I_{dc}s will remain approximately constant when the ac voltage u_{ac} and current i_{ac} are unchanged by combining (9) and (10).

According to (8), the dc-link voltage fluctuation of the jth SM within a sorting cycle $1/f_{sort}$, Δu_{dcj}, can be derived as:

$$\begin{aligned} \Delta u_{dcj} &= \int_0^{1/f_{sort}} \left(I_{dcj} - S_{hbj} i_{ac}\right) \mathrm{d}t \Big/ C_{fc} \\ &= I_{dcj} \Big/ \left(f_{sort} C_{fc}\right) - \int_0^{1/f_{sort}} \left(S_{hbj} i_{ac}\right) \mathrm{d}t \Big/ C_{fc} \\ &= \Delta u_{dc1j} + \Delta u_{dc2j} \end{aligned} \tag{11}$$

where

$$\Delta u_{dc1j} = I_{dcj} \Big/ \left(f_{sort} C_{fc}\right) \tag{12}$$

$$\Delta u_{dc2j} = -\int_0^{1/f_{sort}} \left(S_{hbj} i_{ac}\right) \mathrm{d}t \Big/ C_{fc} \tag{13}$$

It can be seen that dc-link voltage fluctuation Δu_{dc} is divided into two parts. A larger dc-link capacitance C_{fc} or a higher sorting frequency f_{sort} can indeed reduce the values of Δu_{dc1} and Δu_{dc2}. However, these will involve upgrading the hardware and software setup. The first fluctuation, Δu_{dc1}, cannot be decreased due to the same I_{dc} across all SMs. Therefore, reducing the total dc-link fluctuation Δu_{dc} relies on suppressing Δu_{dc2}.

Since the ac current i_{ac} is determined by the ac voltage u_{ac} and load, the switching function of the H-bridge, S_{hb}, is the key term to reduce Δu_{dc2}. According to Table I, the values of four S_{hb}s, including "+1", "–1", "0" and PWM, correspond to the possible values of Δu_{dc2} within a sorting cycle $1/f_{sort}$, calculated as:

$$\Delta u_{dc2j} = \begin{cases} \Delta u_{dc2j}^{P/N} = \mp \dfrac{1}{C_{fc}} \displaystyle\int_0^{1/f_{sort}} i_{ac} \mathrm{d}t, \; S_{hbj} = \pm 1 \\ \Delta u_{dc2j}^{Zero} = 0, \; S_{hbj} = 0 \\ \Delta u_{dc2j}^{PWM} = \mp \dfrac{m}{C_{fc}} \displaystyle\int_0^{1/f_{sort}} i_{ac} \mathrm{d}t, \; S_{hbj} = \mathrm{PWM} \end{cases} \tag{14}$$

where m is modulation index of the H-bridge with PWM mode, defined by $m = u_{ac\text{-}pwm}/u_{dc\text{-}ave}$. As seen, the absolute values of Δu_{dc2} for these inserted SMs with "+1" or "–1" modes, $\left|\Delta u_{dc2}^{P/N}\right|$, are larger compared to Δu_{dc2}^{Zero}. In addition, according to (6), the output voltage polarity of the SM with PWM mode is always consistent with that of the SMs with "+1" or "–1" modes. Since m is less than one, the voltage fluctuation term Δu_{dc2} of the SM with PWM mode, Δu_{dc2}^{PWM} is lower than $\Delta u_{dc2}^{P/N}$. Consequently, different switching modes of the H-bridge lead to inconsistent trends in Δu_{dc}s among the N SMs within the same sorting cycle, which could even aggravate such fluctuations. The number of SMs with "+1" or "–1" modes is zero only when the ac output voltage u_{ac} is near zero crossings. At this point, the maximum voltage fluctuation can be obtained between the SMs with "0" mode and PWM mode. However, in most cases, the maximum fluctuation yields between the SMs of "±1" mode and "0" mode. Therefore, from the perspective of (14), allowing more SMs to operate with the "0" mode is advantageous for reducing Δu_{dc2}. Nevertheless, according to (4), the number of the inserted SMs with "+1" or "–1" modes can be determined within each sorting cycle, and thus the number of SMs with "0" mode is certain. It is essential to explore the reduction of the voltage fluctuations in the dc-link for the HMS, although those fluctuations cannot be completely eliminated.

III. Presented Capacitor Voltage Balancing Method

The HMS of the presented method for the CHBI in this paper builds upon the NLM proposed in [20]. In addition, this method further employs a virtual SM voltage variable to reduce dc-link voltage fluctuations among the SMs under the HMS.

A. DC-link Voltage Fluctuations Reduction

The NLM, as proposed in [20], involves alternating the switching modes of a fixed number of SMs within each control cycle, which leads to reduce the SM capacitor fluctuations and maintain a low switching frequency of IGBTs in the MMC. This alternation mechanism is retained and integrated into this paper. As the NLM does not include a PWM mode, the HMS is incorporated to approximate the desired sine modulation wave for the CHBI with fewer SMs and to balance capacitor voltages among the SMs.

When determining the order of inserted SMs in the HMS, the conventional SM voltage sorting variable in Section II.C, only considers the SC voltages. However, based on (14), the inserted SMs exhibit higher dc-link voltage fluctuations compared to the bypassed SM. Therefore, it lacks an essential mechanism to bypass some SMs with significant dc-link voltage fluctuations, leading to a considerable fluctuation difference among the SMs. To address this limitation, a virtual SM voltage variable, $u_{virtual}$, is proposed. This variable combines the SC voltage u_{sc} and the dc-link voltage u_{dc} of each SM and is expressed as

$$u_{virtual} = k_v u_{sc} + \left(1 - k_v\right) u_{dc} \tag{15}$$

where k_v represents the weight coefficient of u_{sc} in the $u_{virtual}$, and its range is 0-1. After sorting $u_{virtual}$ for one round, the SMs with larger dc-link voltage fluctuations can be positioned at the front of the SM sorting sequence, which allows for their

timely insertion or bypassing. The mechanism behind the reduction of dc-link voltage fluctuations under (15) is further explained.

Taking the example of the instantaneous ac power p_{ac} from φ to π in Fig. 4, where the switching function S_{hb} of the inserted SMs is "+1", and the sign of the ac current i_{ac} is positive, let's assume a positive difference of SC voltages Δu_{sc} between an inserted SM and a bypassed SM. When sorting only the SC voltages, the positive Δu_{sc} causes that both SMs will persist in their previous switching modes in the next sorting cycle, i.e., they remain the "+1" and "0" modes, respectively. Based on (11)-(14), within two sorting cycles $2f_{sort}$, their dc-link voltage fluctuations can be calculated as:

$$\Delta u_{dc}^{+1\to+1} = 2\Delta u_{dc1} - \int_{t_0}^{t_0+2/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc} \tag{16}$$

$$\Delta u_{dc}^{0\to0} = 2\Delta u_{dc1} \tag{17}$$

Note that the value of the switching function S_{hb} is substituted with "+1". By subtracting (16) from (17), the absolute value of the difference in dc-link voltage fluctuations, Δu_{dc}^{con}, under the conventional voltage sorting method can be obtained:

$$\Delta u_{dc}^{con.} = \left|\Delta u_{dc}^{0\to0} - \Delta u_{dc}^{+1\to+1}\right| = \int_{t_0}^{t_0+2/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc} \tag{18}$$

By using (15), the discrepancy of $u_{virtual}$ between the inserted and bypassed SMs is expressed as:

$$\begin{aligned}\Delta u_{virtual} &= u_{virtual}^{+1} - u_{virtual}^{0} = k_v\Delta u_{sc} + (1-k_v)\Delta u_{dc2}^{P} = \\ & k_v\Delta u_{sc} - (1-k_v)\int_{t_0}^{t_0+1/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc}.\end{aligned} \tag{19}$$

A value for k_v can be found to make (19) negative, given the same positive Δu_{sc} and positive i_{ac} in the range $[\varphi, \pi]$. Then, the switching modes of the H-bridge can be alternated between the inserted and bypassed SMs in the next sorting cycle. In other words, the inserted SM with "+1" mode experiencing larger dc-link voltage fluctuations can timely switch to the "0" mode, and the previously bypassed SM can switch to the "+1" mode. The dc-link voltage fluctuations with different switching modes within two sorting cycles can be calculated as:

$$\Delta u_{dc}^{+1\to0} = 2\Delta u_{dc1} - \int_{t_0}^{t_0+1/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc} \tag{20}$$

$$\Delta u_{dc}^{0\to+1} = 2\Delta u_{dc1} - \int_{t_0+1/f_{sort}}^{t_0+2/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc} \tag{21}$$

By (20) and (21), the absolute value of difference in the dc-link voltage fluctuations under the presented method is given by:

$$\begin{aligned}\Delta u_{dc}^{pre.} &= \left|\Delta u_{dc}^{0\to+1} - \Delta u_{dc}^{+1\to0}\right| \\ &= \left|\int_{t_0}^{t_0+1/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc} - \int_{t_0+1/f_{sort}}^{t_0+2/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc}\right| \le \\ & \max\left\{\int_{t_0}^{t_0+1/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc},\ \int_{t_0+1/f_{sort}}^{t_0+2/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc}\right\} \le \Delta u_{dc}^{con.}\end{aligned} \tag{22}$$

By comparing (22) and (18), it can be seen that the reduction in the dc-link voltage fluctuations could occur. This presents an interesting idea to mitigate the dc-link voltage fluctuations by introducing $u_{virtual}$ in the HMS.

A case is studied to illustrate the impact of k_v, with the case parameters outlined in Table II. By rewriting (19) when it is less than zero, it can be obtained that:

$$\frac{k_v}{1-k_v}\Delta u_{sc} < \int_{t_0}^{t_0+1/f_{sort}} i_{ac}\mathrm{d}t \Big/ C_{fc} \tag{23}$$

In Fig. 5(a), each colored interval denotes the integral range of $1/f_{sort}$ for the ac current i_{ac}. The relationships between Δu_{sc} and k_v are shown in Fig. 5(b) when the inequality (23) holds true in four intervals, respectively. Firstly, a lower value of k_v attributes less importance to the SC voltage in the SM voltage sorting, which allows for greater reliance on the dc-link voltage to alternate the switching modes of the H-bridge between the inserted and bypassed SMs. However, as k_v decreases, e.g., k_v ranges from 0.5 to 0.25, the effect of reducing dc-link voltage fluctuations will become less significant, since these values can easily satisfy inequality (23) under the same Δu_{sc} and i_{ac}. For k_v = 0.5, the reduction of dc-link voltage fluctuations can be seen, compared to the conventional balancing method that only sorts the SC voltages, i.e., k_v = 1. Moreover, the steady-state voltage balance of SCs remains unaffected. This is attributed to the consistency of the total voltage among the SMs under (15). The dc-link voltage of each SM can be stabilized around the same reference by the independent BDC controller, further ensuring balanced SC voltages across all SMs. Therefore, the presented method in this paper can coordinately consider both SC voltage balancing and reduced dc-link voltage fluctuations.

TABLE II
CASE PARAMETERS FOR ANALYZING K_v

Parameter	Value
AC angular frequency, ω/(rad/s)	300
AC current amplitude, I_{ac}/ kA	10
DC-link capacitance, C_{fc}/ mF	105.6
Sorting frequency, f_{sort}/ kHz	2
Power factor angle, φ/(°)	60

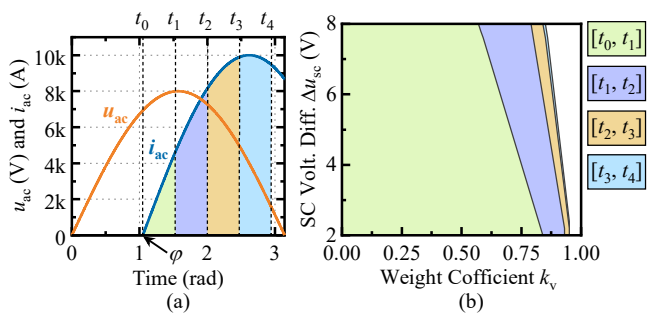


Fig. 5. Solution area when satisfying (23). (a) AC current integral intervals. (b) Relationship between Δu_{sc} and k_v.

B. *Implementation of the Presented Method*

In Section II.C, to implement the HMS for the CHBI, the number of inserted SMs within each control cycle $n_{current}$ and the PWM reference $u_{ac\text{-}pwm}$ are calculated. As shown in (15), the order of the inserted SMs is further determined by sorting the virtual SM voltage variable $u_{virtual}$. In addition, building upon [20], a fixed number (N_{fix}) of SMs are specified to exchange the switching modes of the H-bridge among several SMs. The "+1" and "–1" modes are combined into the "I"

mode, while the "0" mode is renamed as the "O" mode. The next implementation of the presented method involving the HMS, as illustrated in Fig. 6, can be summarized as follows:

1) When considering a potential change in the value of $n_{current}$ between the current and last control cycles, calculate the incremental number of the inserted SMs, Δn_{incre}, as given by:

$$\Delta n_{incre} = n_{current} - n_{last} \tag{24}$$

Note that the value of Δn_{incre} may be zero, positive, or negative. Then, add Δn_{incre} to the total number of the switched SMs, n_{switch}, within the current control cycle, including a fixed number (N_{fix}) of SMs, as shown in:

$$n_{switch} = |\Delta n_{incre}| + N_{fix} \tag{25}$$

2) By incorporating the sign of the instantaneous ac power p_{ac}, which determines whether the inserted SMs will be charged or discharged, along with the value of Δn_{incre}, the switching modes of the H-bridge among the inserted and bypassed SMs are reallocated between the last and current control cycles.

1) If $p_{ac} \geq 0$ and $\Delta n_{incre} > 0$, then switch OUT the N_{fix} SMs with the lowest voltage among the previously inserted SMs, and switch IN the n_{switch} SMs with the highest voltage among the previously bypassed SMs.

2) If $p_{ac} \geq 0$ and $\Delta n_{incre} = 0$, then switch OUT the N_{fix} SMs with the lowest voltage among the previously inserted SMs, and switch IN the N_{fix} SMs with the highest voltage among the previously bypassed SMs.

3) If $p_{ac} \geq 0$ and $\Delta n_{incre} < 0$, then switch OUT the n_{switch} SMs with the lowest voltage among the previously inserted SMs, and switch IN the N_{fix} SMs with the highest voltage among the previously bypassed SMs.

4) If $p_{ac} < 0$ and $\Delta n_{incre} > 0$, then switch OUT the N_{fix} SMs with the highest voltage among the previously inserted SMs, and switch IN the n_{switch} SMs with the lowest voltage among the previously bypassed SMs.

5) If $p_{ac} < 0$ and $\Delta n_{incre} = 0$, then switch OUT the N_{fix} SMs with the highest voltage among the previously inserted SMs, and switch IN the N_{fix} SMs with the lowest voltage among the previously bypassed SMs.

6) If $p_{ac} < 0$ and $\Delta n_{incre} < 0$, then switch OUT the n_{switch} SMs with the highest voltage among the previously inserted SMs, and switch IN the N_{fix} SMs with the lowest voltage among the previously bypassed SMs.

IV. Simulation and Experimental Results

To verify the performance of the presented capacitor voltage balancing method, a CHBI model with fifteen SMs is simulated in Matlab/Simulink. The simulation parameters are detailed in Table III. In the first simulation, with an ac voltage reference $u_{ac\text{-}ref}$ of 10 kV (peak) and an 800-V dc-link voltage reference U_{dc}^{*}, determined by (4), the maximum number of inserted SMs with "+1" or "–1" mode is twelve. Moreover, one extra SM is required to run with the PWM mode to approximate the desired $u_{ac\text{-}ref}$. For an ac frequency of 150 Hz, the load impedance and the peak of the ac current I_{ac} are calculated as 1 Ω and 10 kA, respectively.

TABLE III
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Value	
	Simulation	Prototype
Capacitance of SC, C_{sc}/F	25.38	
Filtering inductance of BDC, L_f/μH	150	
DC-link capacitance, C_{fc}/ mF	105.6	
Sorting frequency, f_{sort}/ kHz	2	
Control frequency, $f_{control}$/ kHz	10	
PWM carrier frequency, f_{pwm}/ kHz	5	
Fixed number in (25), N_{fix}	1	
Number of SMs, N	15	4
DC-link voltage ref., U_{dc}^{*} /V	800	200
Load impedance, R_{load}/ Ω,	$R_{load} = 0.5$	0.0393+j0.167
L_{load}/ mH	$L_{load} = 0.917$	@150 Hz

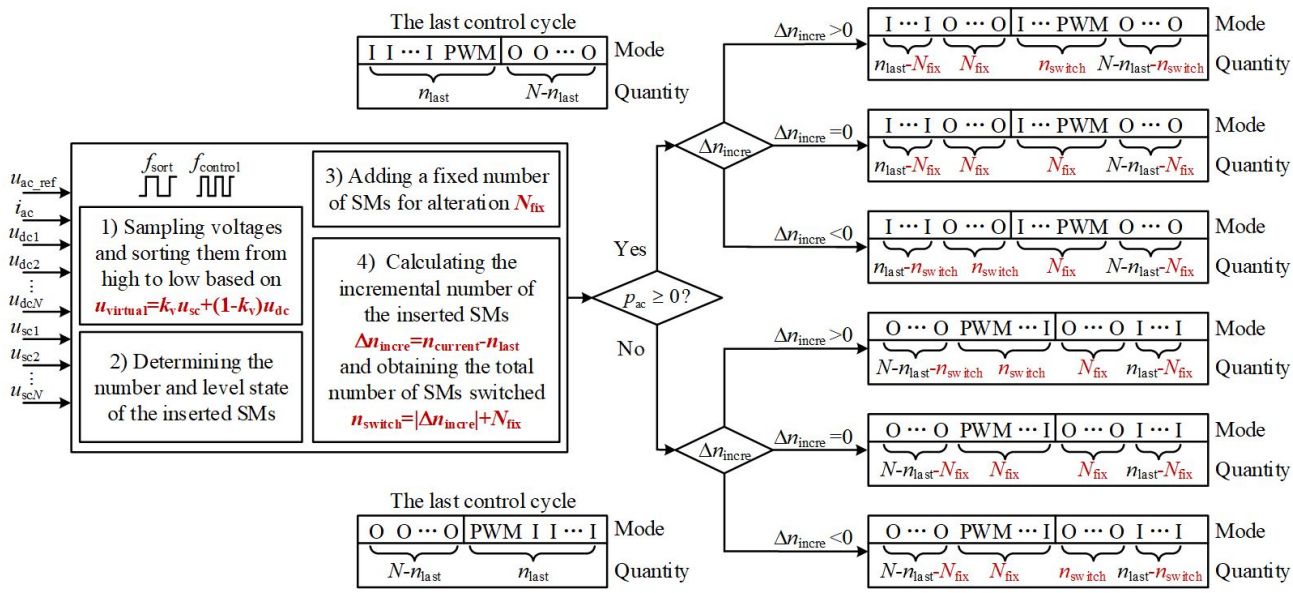


Fig. 6. Block diagram for implementing the presented capacitor voltage balancing method.

The simulation results are depicted in Fig. 7 under different weight coefficient of SC voltage k_v in (15). The SC voltages of fifteen SMs, u_{sc1}-u_{sc15}, are always balanced throughout each discharging process. When k_v is set to 1, indicating that the SM voltage sorting only considers the SC voltages, a 115-V voltage fluctuation in the dc-link is seen, which also brings significant fluctuations to u_{sc1}-u_{sc15}. However, as the value of k_v decreases, placing more emphasis on the dc-link voltage when sorting SM voltages and determining the inserted SMs can lead to a gradual reduction in the dc-link voltage fluctuations. For example, for k_v = 0.5, an 80-V dc-link voltage fluctuation can be observed, representing a 30% decrease compared to k_v = 1. When k_v is less than 0.5, there is no further significant reduction in the dc-link voltage fluctuations. Furthermore, the average dc-link voltage $u_{dc\text{-}ave}$ and the peak of the ac current i_{ac} remain unaffected when the SM voltage sorting variable only considers the SC voltages or adopts (15); just the envelope of the fifteen dc-link voltages u_{dc1}-u_{dc15} is reduced. In brief, the simulation results validate the correctness of the theoretical analysis and the effectiveness of the presented method.

Fig. 8 shows the simulation results under different peaks and frequencies of ac current i_{ac} to highlight the performance of the presented method. For an ac current i_{ac} of 8 kA (peak) and 100 Hz, the dc-link voltage fluctuations among the fifteen SMs are 64 V employing the presented method with k_v = 0.5, compared to those of 83 V when only sorting the SC voltages.

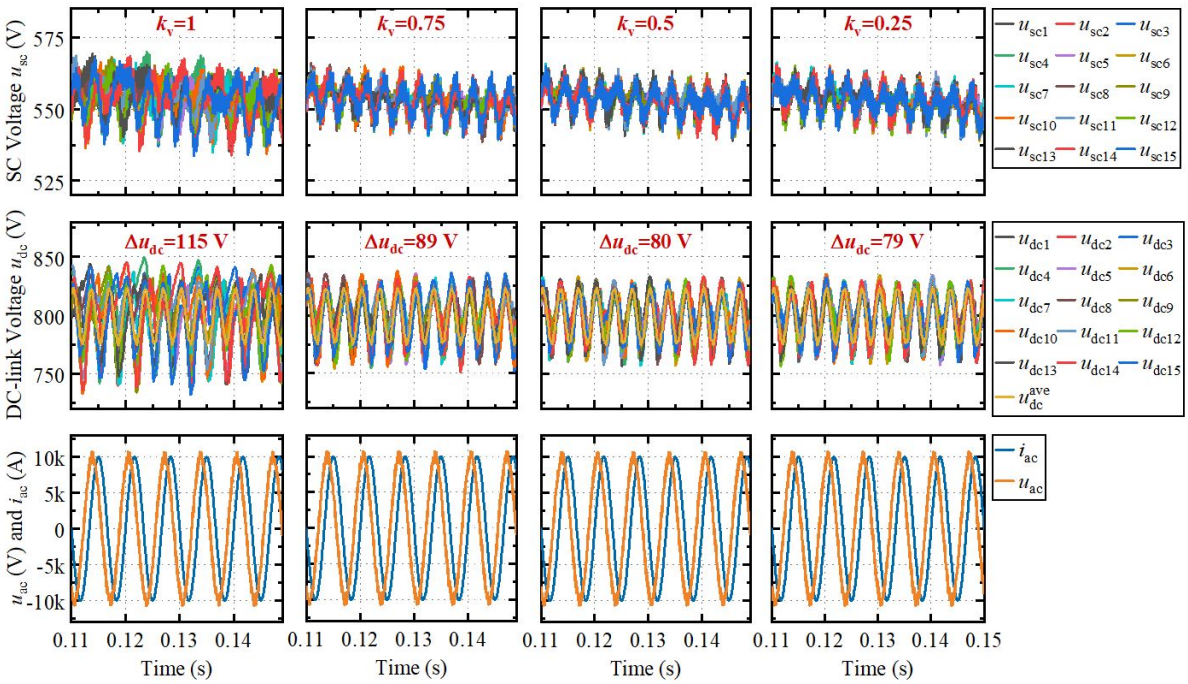


Fig. 7. Simulation results of fifteen SMs under different weight coefficient k_v.

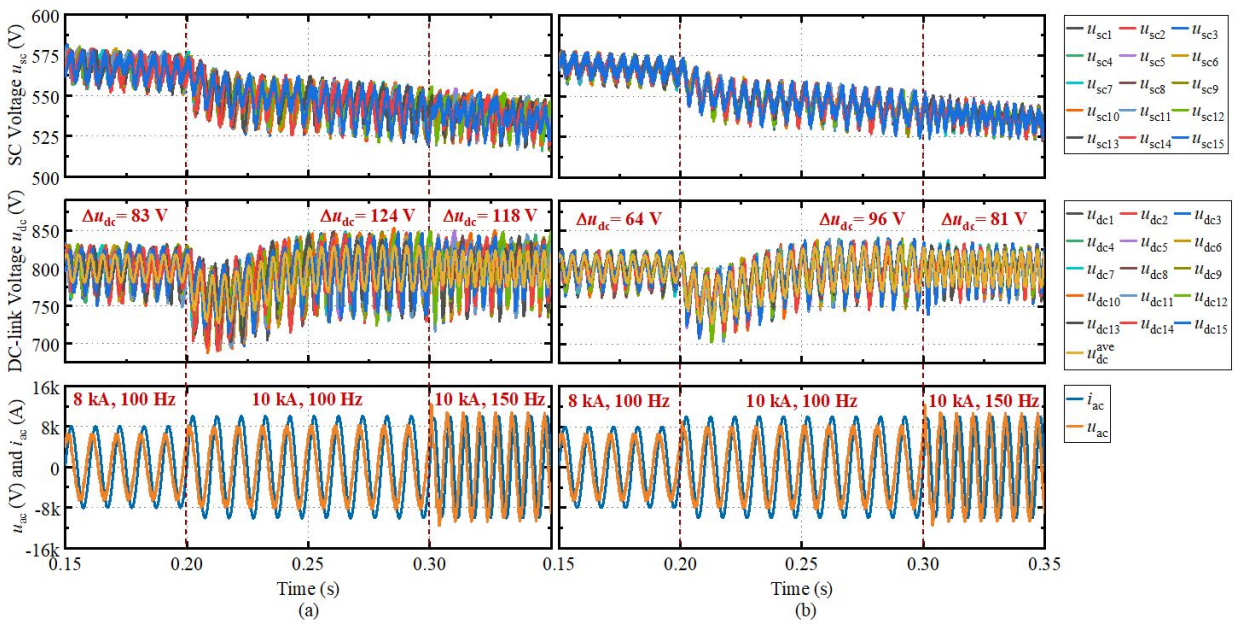


Fig. 8. Simulation results of fifteen SMs under different conditions. (a) Conventional method of only sorting the SC voltages. (b) Presented method when k_v = 0.5.

As the peak of the ac current i_{ac} increases to 10 kA, the 96-V dc-link voltage fluctuations in the presented method remain lower than the 124-V fluctuations observed under the conventional method. When the frequency of the ac current i_{ac} changes to 150 Hz, the results of 0.30-0.35 s in Fig. 8 basically align with those in Fig. 7. In these scenarios, the presented method can consistently ensure the voltage balance of SCs and reduce the voltage fluctuations in the dc-link, further highlighting its effectiveness.

A prototype with four SMs is built to validate the presented method, as illustrated in Fig. 9. The experimental load is several resistors and inductors connected in series and parallel, where the load impedance is calculated as 0.0393+j0.167 Ω under an ac frequency of 150 Hz. The experimental waveforms are captured through an oscilloscope and a digital wave recording software developed by the Shenzhen Hopewind Electric Co., Ltd. Before each discharging experiment, the SCs need to be recharged by connecting the CHBI to the grid. The simplified charging circuit is shown in Fig. 10, and the charging process is detailed in [7]. During the charging process, KM1 is closed and KM2 is opened, and low grid-connected current is employed. For each discharging experiments, open KM1 and close KM2, and the ac voltage reference remains unchanged with a peak of 450 V and a frequency of 150 Hz. The dc-link voltage reference is set to 200 V. By using (4), it is determined that at most two SMs with "+1" or "–1" mode and one SM with PWM mode run concurrently. As shown in Fig. 11, seven levels of ac voltage u_{ac} are seen, indicating the insertion of three SMs at the peak of u_{ac}, with the peak of the ac current i_{ac} approximately 2600 A.

Fig. 9. Photograph of the experimental prototype.

In the first experiment, as depicted in Fig. 12, the SCs of the four SMs begin discharging with initial voltages of about 143 V. The weight coefficient of SC voltage k_v in (15) is selected as 0.5. Throughout the 0.5-s discharging process, the four SC voltages, u_{sc1}-u_{sc4}, remain balanced. The four dc-link voltages, u_{dc1}-u_{dc4}, are stabilized at 200 V, with fluctuation ranges of 191.5-206 V. As seen in this scenario, the capacitor voltage balancing can be achieved based on the presented method in this paper.

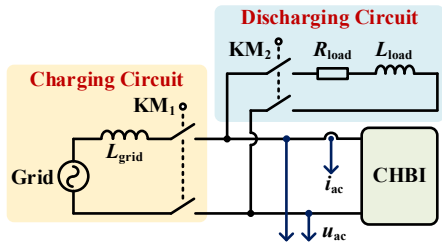


Fig. 10. Simplified experimental setup.

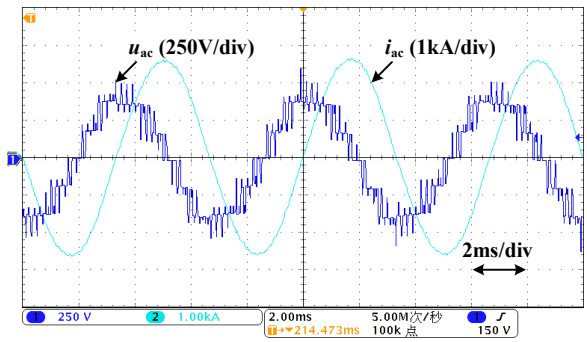
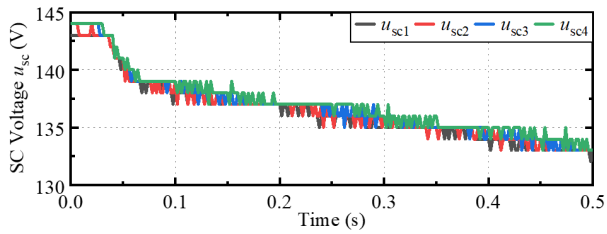
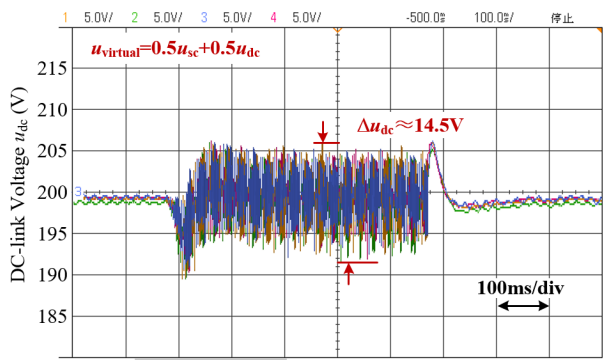


Fig. 11. Experimental waveforms of ac voltage and ac current.



(a)



(b)

Fig. 12. Experimental waveforms under same initial SC voltages across four SMs when k_v = 0.5. (a) SC voltages. (b) DC-link voltages.

Fig. 13 depicts the experimental results with initial unequal values of the four SC voltages, where k_v = 0.5. Specifically, the initial voltages of SC in the first two SMs, u_{sc1}-u_{sc2}, are set at 170 V, while those in the remaining SMs are at 150 V. During the first 0.5-s discharging process, the SC voltages in the last two SMs, u_{sc3}-u_{sc4}, exhibit a slight decrease, facilitating a trend towards balance with u_{sc1}-u_{sc2}. Meanwhile,

the dc-link voltages, u_{dc1}-u_{dc4}, are stabilized near 200 V. The steady-state fluctuation ranges of u_{dc1}-u_{dc4} align with those depicted in Fig. 12(b). This scenario indicates that the performance of the presented method in balancing inconsistent SC voltages.

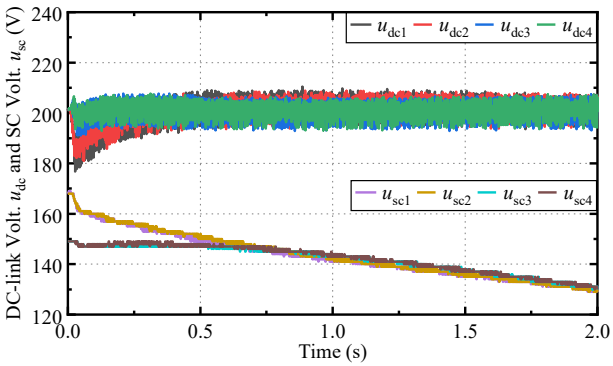
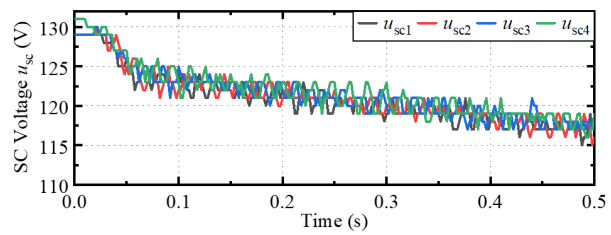
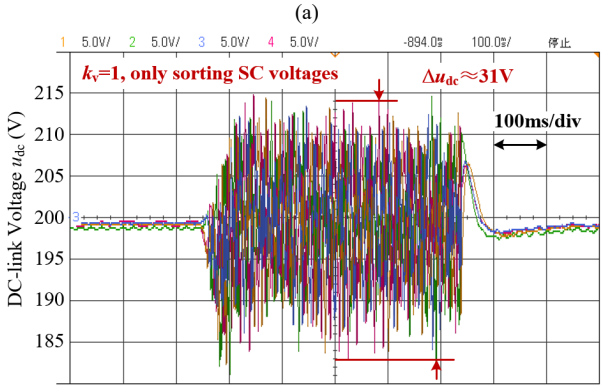


Fig. 13. Experimental waveforms with higher initial voltage in the first two SMs' SCs when employing $u_{virtual}$=0.5u_{sc}+0.5u_{dc}.

To emphasize the effectiveness of the presented method in mitigating the voltage fluctuations in the dc-link, an experiment is conducted with the weight coefficient of SC voltages k_v set to 1 in (15). With a focus on solely sorting the SC voltages, the voltage balance of SCs is ensured during the 0.5-s discharging process, as u_{sc1}-u_{sc4} shown in Fig. 14(a). However, Fig. 14(b) shows the dc-link voltage fluctuations of approximately 31 V, increasing by 53% compared to the those of 14.5 V seen in Fig. 12(b). This highlights the validity of reducing dc-link voltage fluctuations by introducing the weighted virtual SM voltage sorting variable presented in this paper.



(a)



(b)

Fig. 14. Experimental waveforms when only sorting the SC voltages. (a) SC voltages. (b) DC-link voltages.

V. Conclusion

Based on the HMS, capacitor voltage balancing of the CHBI is realized by voltage sorting to determine the order in which SMs are inserted within each control cycle. However, large differences in dc-link voltage fluctuations among the SMs are observed when the conventional balancing method considers only sorting the SC voltages. To address this issue, this paper presents a coordinated capacitor voltage balancing method with reduced dc-link voltage fluctuations for the CHBI. A virtual SM voltage sorting variable is obtained by combining the SC voltage and dc-link voltage in a weighted manner. This enables the timely bypassing of currently inserted SMs with significant dc-link voltage fluctuations. Importantly, the presented method preserves the voltage balance of SCs while mitigating dc-link voltage fluctuations. Both simulation and experimental results validate the effectiveness of the presented method.

Acknowledgment

Sincere thanks to Ziqiang Li from the State Grid Corporation of China, as well as Lei Xie, Xiuyi Wei, Zebin Wu, Tongchang Han, Jinsong Ye, Jinda Li and other staff from the Shenzhen Hopewind Electric Co., Ltd., for their help in the experiments, and to Ms. Ruochen Li for her encouragement.

References

[1] S. Kouro, M. Malinowski, and K. Gopakumar *et al*, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. on Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel Converters: Control and Modulation Techniques for Their Operation and Industrial Applications," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2066–2081, Nov. 2017.

[3] X. Zhang, M. D. Wang, and T. Zhao *et al*, "Topological Comparison and Analysis of Medium-voltage and High-power Direct-linked PV Inverter," *CES Trans. on Electr. Mach. and Sys.*, vol. 3, no. 4, pp. 327–334, Dec. 2019.

[4] M. Hamzeh, A. Ghazanfari, and H. Mokhtari *et al*, "Integrating Hybrid Power Source Into an Islanded MV Microgrid Using CHB Multilevel Inverter Under Unbalanced and Nonlinear Load Conditions," *IEEE Trans. on Energy Conversion*, vol. 28, no. 3, pp. 643–651, Sept. 2013.

[5] Z. Q. Li, F. Q. Gao, and C. Zhao *et al*, "A Novel Voltage Balancing Method of Cascaded H-bridge Multilevel Converter with Supercapacitors Energy Storage System for Capacitor Voltage Ripple Reduction," in *Proc. of IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society*, Brussels, Belgium, Oct. 2022, pp. 1–5.

[6] H. Mhiesan, J. Umuhoza, and K. Mordi *et al*, "Evaluation of 1.2 kV SiC MOSFETs in Multilevel Cascaded H-bridge Three-phase Inverter for Medium-voltage Grid Applications," *Chinese Journal of Electrical Engineering*, vol. 5, no. 2, pp. 1–13, Jun. 2019.

[7] Y. Zhang, Z. X. Li, and F. Q. Gao *et al*, "Coordinated Balancing Charging Strategy for Cascaded H-bridge Inverter with Supercapacitor and DC–DC stage," *IEEE Trans. on Ind. Electron.*, vol. 71, no. 7, pp. 7262–7272, July 2024.

[8] A. Lewicki, C. Odeh, and M. Morawiec, "Space Vector Pulsewidth Modulation Strategy for Multilevel Cascaded H-bridge Inverter with DC-link Voltage Balancing Ability," *IEEE Trans. on Ind. Electron.*, vol. 70, no. 2, pp. 1161–1170, Feb. 2023.

[9] T. Lahlou, D. Wittmann, and M. Abdelrahem *et al*, "Stabilization of the DC-link Voltage in a Two Stage Cascaded H-bridge Multilevel Converter for Battery Energy Storage Systems," in *Proc. of 2016 IEEE International Energy Conference (ENERGYCON)*, Leuven, Belgium, Apr. 2016, pp. 1–6.

[10] Y. Wang, C. Hu, and R. Y. Ding *et al*, "A Nearest Level PWM Method for the MMC in DC Distribution Grids," *IEEE Trans. on Power Electron.*, vol. 33, no. 11, pp. 9209–9218, Nov. 2018.

[11] A. Hussain, K. Raj, and K. Rajashekara *et al*, "Current Controlled Operation of Cascaded H-bridge Converter for Fast SoC Balancing in Grid Energy Storage," in *Proc. of 2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, Sept. 2019, pp. 5373–5379.

[12] M. Moosavi, G. Farivar, and H. Iman-Eini *et al*, "A Voltage Balancing Strategy with Extended Operating Region for Cascaded H-bridge Converters," *IEEE Trans. on Power Electron.*, vol. 29, no. 9, pp. 5044–5053, Sept. 2014.

[13] G. W. Liang, E. Rodriguez, and G. G. Farivar *et al*, "A Constrained Intersubmodule State-of-charge Balancing Method for Battery Energy Storage Systems Based on the Cascaded H-bridge Converter," *IEEE Trans. on Power Electron.*, vol. 37, no. 10, pp. 12669–12678, Oct. 2022.

[14] S. W. Yang, X. Zhang, and W Mao *et al*, "Quantitative Comparison and Analysis of Different Power Routing Methods for Single-phase Cascaded H-bridge Photovoltaic Grid-connected Inverter," *IEEE Trans. on Power Electron.*, vol. 36, no. 4, pp. 4134–4152, Apr. 2021.

[15] W. Mao, "Research on Key Technologies of Cascaded Photovoltaic Grid-Connected Inverter System," Ph.D. dissertation, Hefei University of Technology, Hefei, China, 2020.

[16] S. L. Wang, N. Jiao, and J. P. Ma *et al*, "Analysis and Optimization of Voltage Balancing Control Limits for Cascaded H-bridge Rectifiers," *IEEE Trans. on Ind. Electron.*, vol. 68, no. 11, pp. 10677–10687, Nov. 2021.

[17] K. G. Wang, D. R. Kong, and Z. C. Zhong *et al.*, "Suppression of Low-frequency Voltage Ripple in Cascaded H-bridge Multilevel Converters-based Large-scale PV Systems," in *Proc. of 2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Kiel, Germany, Jun. 2022, pp. 1–5.

[18] J. Sheng, C. M. Li, and X. Xiang *et al*, "Dc-link ripple Suppression of Cascaded H-bridge Based MV Grid Emulator Apparatus for Analysis and Testing of Grid-tied Converters in Distribution System," *IEEE Trans. on Power Delivery*, vol. 39, no. 1, pp. 622–634, Feb. 2024.

[19] T. Zhao, X. Zhang, and W. Mao *et al*, "A Modified Hybrid Modulation Strategy for Suppressing DC Voltage Fluctuation of Cascaded H-bridge Photovoltaic Inverter," *IEEE Trans. on Ind. Electron.*, vol. 65, no. 5, pp. 3932–3941, May 2018.

[20] Z. X. Li, F. Q. Gao, and X. Ma *et al*., "Power Module Capacitor Voltage Balancing Method for a ± 350-kV/1000-MW Modular Multilevel Converter," *IEEE Trans. on Power Electron.*, vol. 31, no. 6, pp. 3977–3984, Jun. 2016.

[21] F. Xiong, P. Wu, and H. Yang *et al*, "Optimization and Tradeoff of DC Bus Voltage Ripple and DAB Current Stress in Two-stage Single-phase Converter by Double-line-frequency Power Control," *IEEE Trans. on Power Electron.*, vol. 38, no. 11, pp. 13877–13894, Nov. 2023.

Ye Zhang received the B.Eng. degree in electrical engineering and its automation from the Hebei University of Technology, Tianjin, China, in 2019. He is currently working towards his Ph.D. degree in electrical engineering with the Institute of Electrical Engineering, Chinese Academy of Sciences and the University of Chinese Academy of Sciences, Beijing, China.

His research interests mainly include analysis and control of cascaded H-bridge inverter with energy storage.

Zixin Li received the B.Eng. degree in industry automation from the North China University of Technology, Beijing, China, in 2005, and the Ph.D. degree in power electronics and power drives from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2010.

Since 2010, he has been with the Institute of Electrical Engineering, Chinese Academy of Sciences, where he is currently a Professor and Deputy Director. He has authored or coauthored more than one hundred academic papers and holds more than twenty invention patents in China. His research interests include power electronics and electromagnetic drive technologies and their applications in power grid, transportation, energy, and other fields.

Dr. Li is an Associate Editor for IEEE Transactions on Power Electronics, IET High Voltage, and Chinese Journal of Electrical Engineering. He was the recipient of the IEEE Power Electronics Society Richard M. Bass Outstanding Young Power Electronics Engineer Award of 2015 for his contributions to multilevel and HVDC converters. He was elected as a Fellow of the Institution of Engineering and Technology (IET) in 2019.

Fanqiang Gao received the B.Eng. degree in automation control from the Huazhong University of Science and Technology, Wuhan, China, in 2006, and the Ph.D. degree in power electronics and power drives from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2012.

In 2012, he joined the Institute of Electrical Engineering, Chinese Academy of Sciences, where he is currently an Associate Professor. His research interests include analysis and control of power electronic converter in high power fields.

Cong Zhao received the B.Eng. degree in electrical engineering from the Tsinghua University, Beijing, China, in 2012, and the Ph.D. degree in power electronics and power drives from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2017.

Since 2017, he has been with the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, where he is currently an Associate Professor. His research interests include topology, analysis, and control of modular multilevel converter and power electronic transformer.

Yaohua Li received the Ph.D. degree in power electronics and power drives from the Tsinghua University, Beijing, China, in 1994.

From 1995 to 1997, he was a Postdoctoral Research Fellow with the Institute of Electrical Machine, Technical University of Berlin, Germany. In 1997, he joined the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, and is currently a Professor and Director. His research fields include analysis and control of electrical machines and power electronics.