Design and Manufacture of Dual-gate DDSCR with High Failure Current and Holding Voltage*

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Abstract: High-voltage controller area network (CAN) buses have a harsh working environment and require a robust electrostatic discharge (ESD) design window. Thus, ordinary silicon-controlled rectifier (SCR) devices do not satisfy these design requirements. To streamline the design and manufacturing of SCRs, this study proposes a novel dual-gate dual-direction SCR (DG-DDSCR) with a high failure current and holding voltage. First, four polysilicon gates, $Gate_{A1}$, $Gate_{A2}$, $Gate_{C1}$, and $Gate_{C2}$, were introduced to the N+ and P+ middle regions of the anode and cathode. When the voltage acts on the anode, the electric field generated by the polysilicon gate strengthens the SCR current path while promoting the release of ESD current in the substrate path. Specifically, the holding voltage of the DG-DDSCR and failure current derived from the test results of a transmission line pulse (TLP) are 29.4 V and 16.7 A, respectively. When the clamping voltage was 40 V, the transient current release of the structure can reach 11.61 A, which met the specifications of the CAN bus ESD window and was suitable for the ESD protection of the target application.

Keywords: High failure current, high holding voltage, CMOS technology, dual-direction SCR, gate controlled device

1 Introduction

With the continuous development of integrated circuit technology, engineers have preferred to choose devices with the highest electrostatic discharge efficiency per unit area to improve the efficiency of integrated circuits [1-3]. Basic electrostatic discharge (ESD) protection devices include PN diodes, ground-gate NMOS (GGNMOS), and silicon-controlled rectifiers (SCRs). Both the trigger voltage of the PN diodes and the on-resistance under a forward bias were low. According to the heat generation formula $P = IV$, the diode can withstand a large ESD current.

According to the heat generation formula $P = IV$, the diode can withstand a large ESD current. However, the breakdown voltage of the minimum gate oxide layer of the chip core is lower than the reverse breakdown voltage of the diode. When an electrostatic pulse is generated, the diode may not be triggered in time; thus, the internal circuit of the chip may be broken down by static electricity. Currently, on-chip-integrated GGNMOSs are employed to increase discharge current by increasing the number of interdigital fingers. However, this solution releases current unevenly among the interdigitated fingers. Consequently, when employing this solution, the die area must be magnified by several times for the same ESD window specifications. SCRs have the highest electrostatic discharge efficiency per unit area, which makes them the first choice on-chip ESD protection device for many applications [4-6]. However, the holding voltage (V_{t2}) of traditional SCRs is low. Such a low holding voltage is likely to result in a latch-up effect in the core circuit [7-10]. Current research in the field of high-voltage ESD has focused on the design of SCR structures with high holding voltages, high failure currents, and fast turn-on speeds [11]. Wang et al. [12] proposed a single gate-controlled SCR structure based on the 0.18-μm Bipolar-CMOS-DMOS(BCD) process, which increases the failure current of SCRs to beyond traditional levels, enhancing the high-voltage electrostatic discharge protection of communication buses. Do et al. [13] proposed an innovative structure

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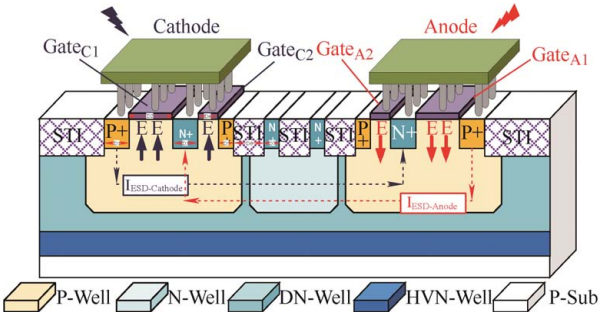
for dual-direction SCRs (DDSCRs). In this structure, the SCR positive feedback gain was reduced by adding a gate that reduces the emitter injection efficiency of the p-n-p parasitic bipolar transistor formed at the bottom of the gate. Liang et al. [14] developed a gate diode triggered SCR (GDTSCR) that splits the polygate into two and inserts a highly doped p-type region between the drain and source of a MOS triggered SCR (MTSCR). The underlying concept of his proposal was to extend the SCR path and improve the holding voltage, which represents an outstanding achievement in high-voltage ESD protection research. Sahoo et al. [15] proposed a novel LDMOS transistor with two virtual gates that improved the breakdown characteristics of the device and satisfied the protection requirements of high-voltage ESD applications. However, it appears that none of the aforementioned solutions is sufficiently sophisticated to achieve higher fault currents while maintaining a high holding voltage [16-21]. Moreover, they do not satisfy the Controller Area Network (CAN) bus window [22-25].

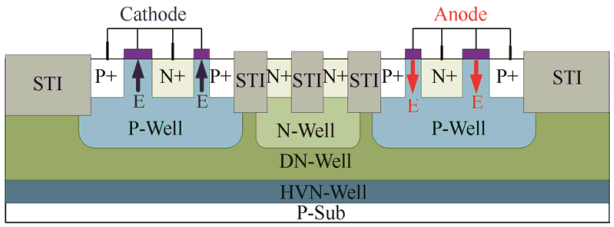
To obtain a better solution for the issue above, this study proposes a dual gate-DDSCR (DG-DDSCR) structure with a high failure current and a high holding voltage. This structure effectively overcomes the low holding voltage of traditional SCRs and increases their failure current. Furthermore, it is well-suited for providing ESD protection to the target bus.

2 Design concept of the DG-DDSCR

The three-dimensional structure of the DG-DDSCR is shown in Fig. 1a. A cross-section of the DG-DDSCR structure is shown in Fig. 1b. $Gate_{A1}$ and $Gate_{A2}$ represent the gates of the anode, and $Gate_{C1}$ and $Gate_{C2}$ represent the gates of the cathode. The arrow below the anode gate indicates the downward electric-field effect created by the gate. The arrows below the cathode gate indicate the vertical upward electric-field effect created by the gate. The dashed line pointed out from the anode represents forward ESD current path and the dashed line pointed out from the cathode indicates the reverse ESD current path. Because the voltage is between −7 V and 12 V, the CAN bus can operate normally. Therefore, when designing a chip, it must have an ESD device that copes with electrostatic pulses in both the positive and negative directions. Hence, DG-DDSCR with a bidirectional release capability offers a new option. An equivalent circuit of the DG-DDSCR is shown in Fig. 2. Owing to the symmetrical characteristics of the structure, the equivalent circuit is the same regardless of whether an ESD forward pulse is applied to the cathode or anode.



(a) 3D schematic



(b) Cross-sectional views

Fig. 1 Schematic diagram of DG-DDSCR structure

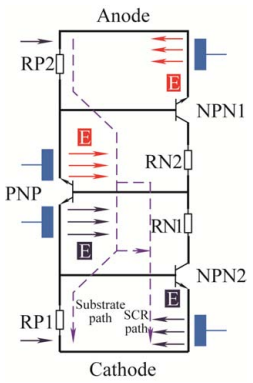


Fig. 2 Equivalent circuit of the DG-DDSCR

Taking the device exposed to a forward ESD pulse as an example: when an ESD event occurs, a device's anode is affected by ESD forward stress, which increases the voltage difference between the anode and cathode to the trigger voltage V_{t1}. This leads to an avalanche breakdown of the reverse-biased PN junction formed by the N-Well and cathode P-Well trigger surfaces, resulting in a multiplication current. As shown in Fig. 3, the avalanche breakdown produced numerous electrons and holes flowing through the N-Well under electrode suction.

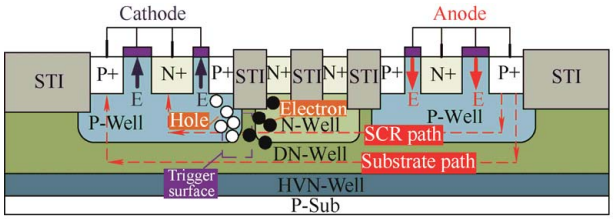


Fig. 3 Triggering mechanism of DG-DDSCR

When the voltage drop in RN1 reaches the PNP1 BE junction opening voltage, the parasitic PNP begins to discharge the ESD current. As the current slowly increases, the parasitic resistance of the cathode P-Well RP1 produces a voltage drop until it reaches the NPN1 BE junction opening voltage, causing the parasitic NPN1 transistor to turn on and finally form a positive feedback loop. When the parasitic PNP and parasitic NPN1 of the DG-DDSCR device are initially turned on, the device is in the low-impedance region and begins to gradually transition from the triggering-point state to the holding-point state, with a slight increase in the current flow. The SCR current path of the device was fully turned on as a result of the positive feedback, forming the main path (SCR path) of the PNPN.

Because there are polysilicon gates, $Gate_{A1}$ and $Gate_{A2}$ on the left and right sides of the anode, respectively, the above gates generate a vertical downward electric force. Meanwhile, because there are also polysilicon gates $Gate_{C1}$ and $Gate_{C2}$ on the left and right sides of cathode N+, $Gate_{C1}$ and $Gate_{C2}$ generate a vertical upward electric force. The electric force generated by the polysilicon gates on the right side of the anode N+ ($Gate_{A1}$) and right side of the cathode N+ ($Gate_{C2}$) acts on the main path (SCR path), which enhances the ESD current. The electric force of the polysilicon gate on the right side of the anode N+ ($Gate_{A1}$) and left side of the cathode N+ ($Gate_{C1}$) acts on the diode path, helping to activate the SCR pathway. The current travels through the SCR and diode paths simultaneously, further improving the ESD protection capability of the DG-DDSCR. When an ESD pulse arrives from another direction, the reverse SCR and diode paths are activated because the device is completely symmetrical. Owing to the electric-field effect at the gate of the DG-DDSCR, the ESD current is directed to a deeper diode path, strengthening the current and extending the length of the current path. In addition, the electric field generated by the polysilicon gate is can encourage carrier movement, resulting in the rapid turn-on of both the parasitic PNP and parasitic NPN. These conditions enable rapid recovery, along with maintaining high failure current and holding voltage.

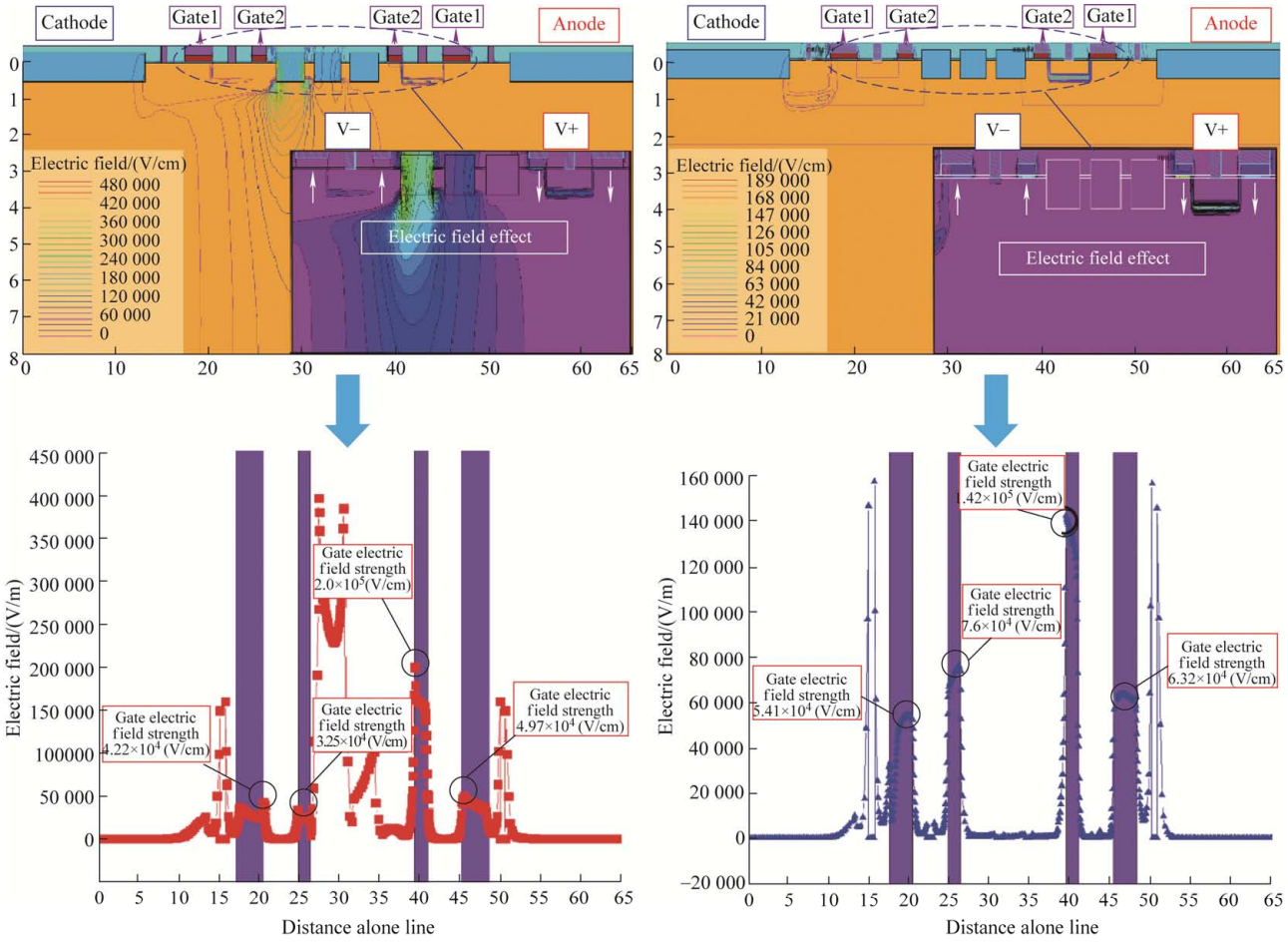
3 Discussion in two-dimensional simulation

In this study, the SILVACO TCAD simulation platform ATLAS was used to perform DC and transient simulations. Part A involves performing a DC simulation to verify the characteristics of the DG-DDSCR structure at the triggering and holding points. Part B involves transient simulations in ATLAS to observe the electrical characteristics of the DG-DDSCR structure at the trigger and holding points when the transmission line pulse (TLP) pulse passes 100 ns.

3.1 DC scanning simulation

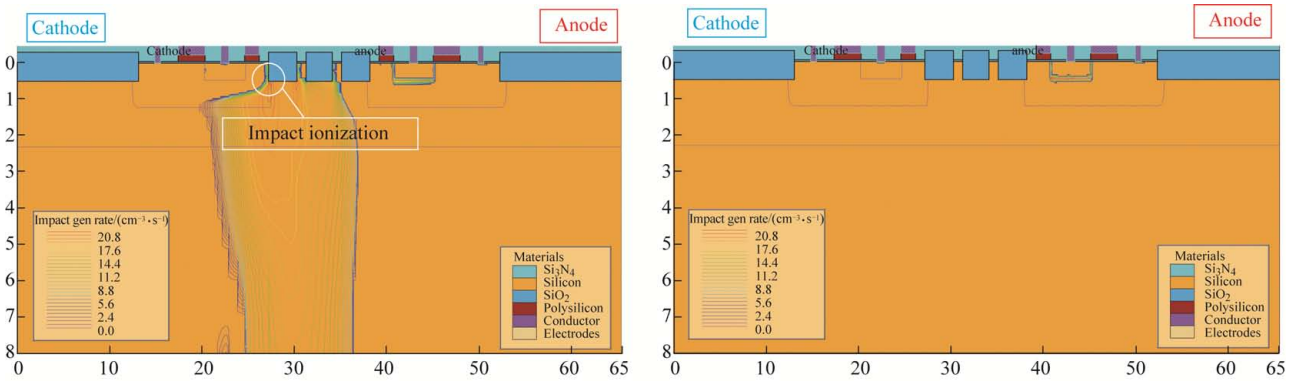
In this study, the triggering (initial opening point) and holding (full opening point) points of the DC sweep curve were selected for discussion and analysis. The electric field distribution and corresponding electric field intensity curve of the DG-DDSR at the trigger point in the DC simulation are shown in Fig. 4a. The electric-field distribution and corresponding electric-field intensity curve of the DG-DDSR at the holding point are shown in Fig. 4b. The electric field distribution at the initial turn-on proves that the voltage drops at the cathode P-Well/N-Well reverse PN junction; thus, avalanche breakdown occurs. The electric field distribution in the fully turned-on state exhibited a clear electric field distribution under the polysilicon gate. It shows that the polysilicon gate can significantly enhance the electric-field strength, which is consistent with the theoretical deduction. The impact ionization distribution of the DG-DDSCR device at the triggering point is shown in Fig. 5a, and that at the holding point is shown in Fig. 5b. The peak

area of the impact ionization distribution was located near the cathode N-Well and P-Well reverse-biased PN junctions. This indicates that the turn-on of the device depends on the avalanche breakdown of the P-Well and N-Well reverse-biased PN junctions. The impact ionization profile in the fully turned-on state shows that a voltage drop occurs in the anode N+ region and P-Well region. The current path and intensity curves of the DG-DDSCR device at the trigger point are shown in Fig. 6a. The current path and intensity curves at the holding point are shown in Fig. 6b. When the device was in the triggering-point state, the current was primarily discharged through the diode path. When the device was in the holding-point state, the current was discharged through the SCR path, and a small amount of current was discharged through the diode path. At this point, the device was fully turned on.



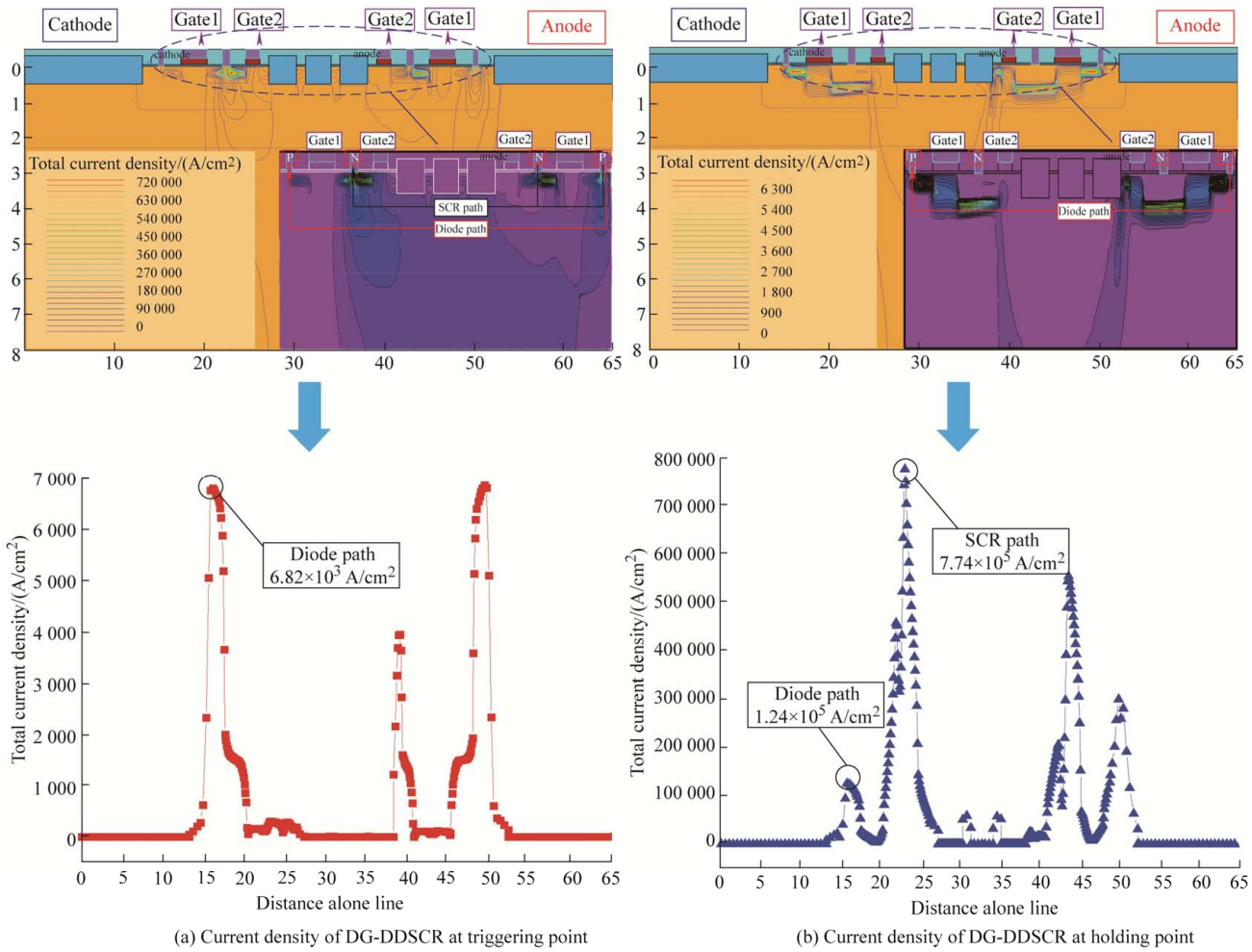
(a) Electric field of DG-DDSCR at triggering point (b) Electric field of DG-DDSCR at holding point

Fig. 4 TCAD simulation of the electric field of the DG-DDSCR



(a) Impact ionization of DG-DDSCR at triggering point (b) Impact ionization of DG-DDSCR at holding point

Fig. 5 TCAD simulation of the impact ionization of DG-DDSCR



(a) Current density of DG-DDSCR at triggering point

(b) Current density of DG-DDSCR at holding point

Fig. 6 TCAD simulation of the total current density of the DG-DDSCR

3.2 Transient simulation

To further verify the working principle of the device, the relationship between the characteristics of the DG-DDSCR device and time was studied using a TLP transient simulation. The principle was to let a pulse with a rising edge of 10 ns, falling edge of 10 ns, pulse width of 100 ns, and amplitude of 1 mA enter the DG-DDSCCR anode to observe its transient characteristics. Data at 100 ns were selected as the full turn-on feature of the DG-DDSCR under transient TLP pulses. The global temperature curve simulation of the DG-DDSCR device is shown in Fig. 7 and indicates that the device is not prone to thermal breakdown or chip damage. The simulation results also revealed that the triggering-point selection time of the DG-DDSCR device was 4.51×10^{-9} s, and the holding-point selection time was 6.29×10^{-9} s. The transient electric-field distribution of the DG-DDSCR device at the holding point is shown in Fig. 8. Clear electric field distributions were observed under the four polysilicon gates of the device, proving that the polysilicon gates can significantly improve the electric field strength and enhance the current path. The transient impact ionization distribution of the DG-DDSCR system at the holding point is shown in Fig. 9. At this point, the device no longer experienced an avalanche breakdown. The transient current path distribution of the DG-DDSCR system at the holding point is shown in Fig. 10. The DG-DDSCR device forms an SCR path consisting of P+ at the anode, P-Well- and N-Wells at the anode, P-Well at the cathode, and N+ at the cathode. The lattice temperature of the DG-DDSCR at the holding point is shown in Fig. 11. The DG-DDSCR device

shows a peak in the lattice temperature distribution of its N+ region, which is not on the surface of the device, indicating that the device is not prone to thermal breakdown on the surface that can damage the device.

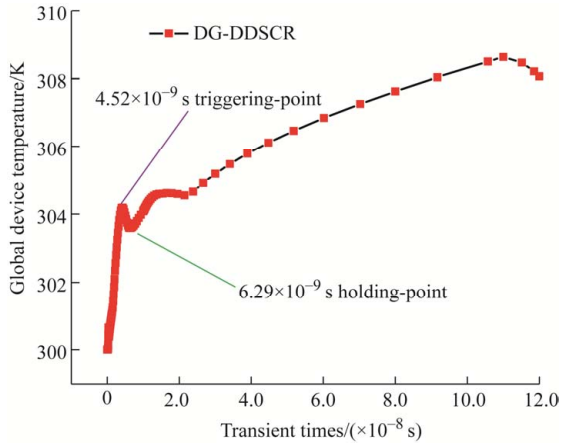


Fig. 7 Simulation of global device temperature curves for DG-DDSCR as a function of the ESD discharge current

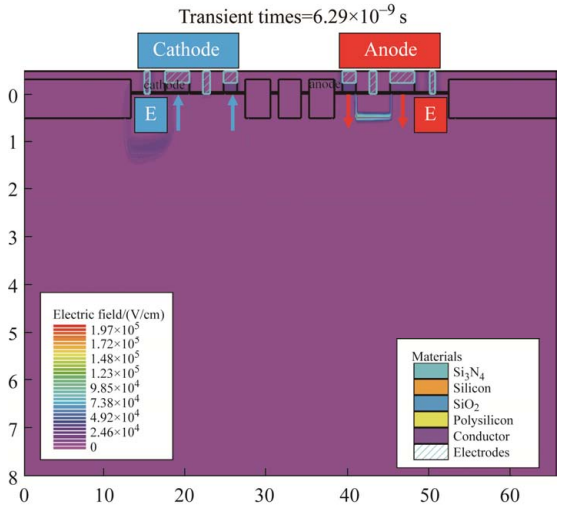


Fig. 8 Transient electric field intensity distribution of the DG-DDSCR at the holding point

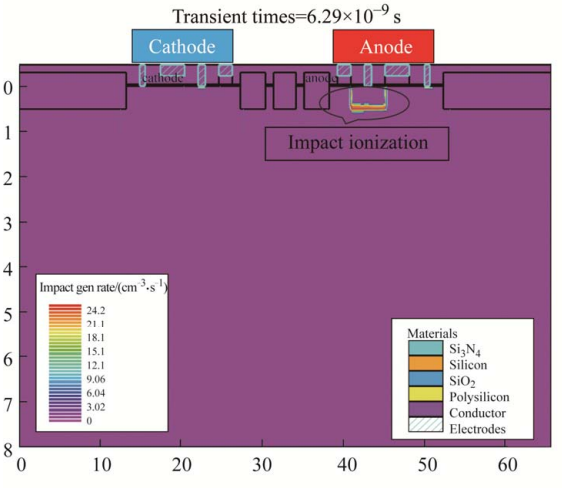


Fig. 9 Transient impact ionization distribution of the DG-DDSCR at the holding point

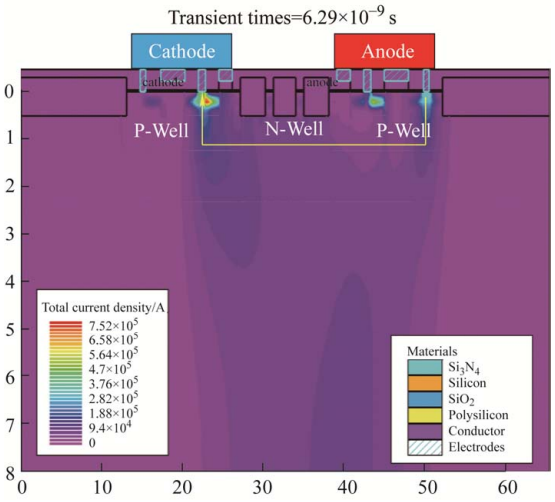


Fig. 10 Transient current density distribution of the DG-DDSCR at the holding point

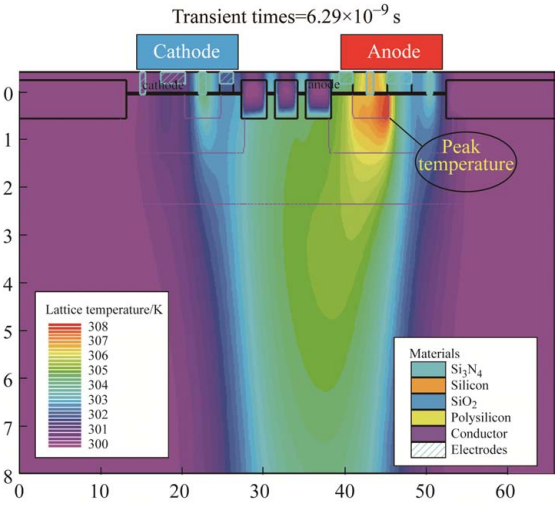


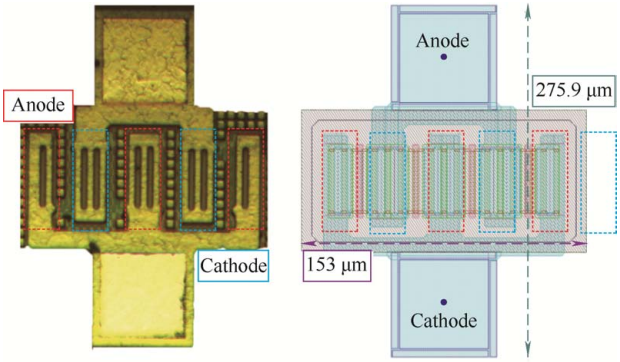
Fig. 11 Lattice temperature distribution of DG-DDSCR at the holding point

4 Experimental analysis and discussion

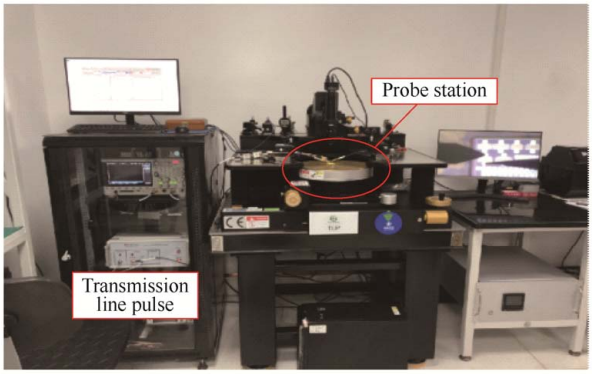
This study introduces a four-finger DG-DDSCR device with a double-gate structure using a 0.18-μm BCD process. A microscopic image and the layout of the DG-DDSCR device are shown in Fig. 12a. The total layout size of the flow sheet was 5 000 μm× 5 000 μm. The length and width of the device were 275.9 and 153 μm, respectively. The DG-DDSCR experimental platform is illustrated in Fig. 12b.

The DC curves of the DG-DDSCR device are presented in Fig. 13. The transparency of the ESD devices was observed from the DC curve. DC assessed the chip under the normal operating voltage (–7-12 V) of the target chip. At the same time, a safety margin of 20% was considered; hence, the device must not have leakage current drift when the operating voltage is

–8.4-14.4 V. When the device's voltage is –32-32 V, no leakage current drift occurred. This shows that the device can work normally in the harsh environment of the CAN bus and that the transparency of the DG-DDSCR is ideal.



(a) Microscope image and layout of the DG-DDSCR



(b) Experimental platform for DG-DDSCR

Fig. 12 Microscope image, layout, and experimental platform of the DG-DDSCR

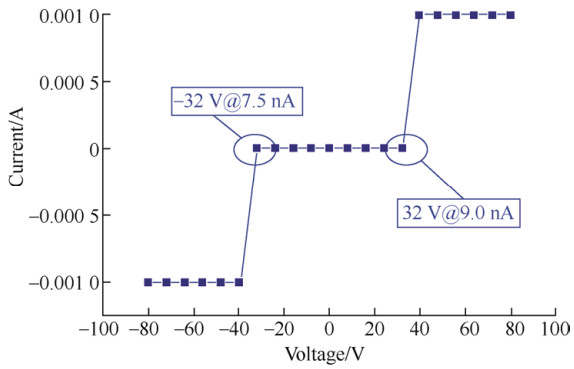


Fig. 13 DC curve of the DG-DDSCR device

The IV curves of the DG-DDSCR device under a TLP are shown in Fig. 14. When the forward and reverse currents were 16.7 A and 17.0 A, respectively, the current curve drifted, indicating that the failure current of the DG-DDSCR device was 16.7 A (17.0 A) in the fault state.

The human body model (HBM) calculation result for the device was 25.1 kV (25.5 kV), indicating that the DG-DDSCR has good ESD robustness. As indicated by the TLP test results, the forward trigger voltage of the DG-DDSCR device was 40.2 V, and the forward holding voltage was 29.4 V. The reverse trigger and holding voltages were 43.2 V and 28.8 V, respectively. Hence, the test results of the DG-DDSCR device under forward and reverse ESD stresses are essentially the same, indicating that the DG-DDSCR is symmetric. The discharge of electrostatic pulse currents close to the interior of the device is enhanced by adding four polysilicon gates. The current strength is increased, and the length of the current path is extended; furthermore, the positive feedback loop of the thyristor is strengthened. According to the CAN bus requirements, the trigger voltage of the device should be less than 52 V, the holding voltage should be more than 14.4 V, and the failure current should be more than 10.67 A. When the clamping voltage was 40 V, the release current of the device reached 11.61 A at 40 V, and the DG-DDSCR was in both the positive and negative directions; all the requirements of the target bus were met. The IV curve of the DG-DDSCR device under the action of an extremely fast TLP (VFTLP) is shown in Fig. 15. The rising edge of the pulse was 0.1 ns, pulse width was 5 ns, and limited current was 2 A. The test results showed that the trigger and holding voltages of the device were 45.1 V and 43.9 V, respectively. The magnitude of leakage current was maintained between 10^{-7} and 10^{-6}. The device can be used to protect against CDM events. Based on the TLP test conducted on the DG-DDSCR device at room temperature, additional tests were performed at elevated temperatures of 50 ℃, 75 ℃, and 100 ℃. The TLP test current was limited to 2 A in all cases. TLP test results at different temperatures are shown in Fig. 16. At 25 ℃, the trigger and holding voltages of the device were 43.3 V and 28.4 V, respectively;. at 50 ℃, they were 44.1 V and 27.5 V, respectively; at 75 ℃, they were 44.7 V and 26.7 V, respectively; and at 100 ℃, they were 45.3 V and 26.2 V, respectively. As the temperature increased, the holding voltage of the device decreased. Among the measured voltages, the minimum holding voltage of 26.2 V measured at 100 ℃ was greater than 120% of the working voltage of the CAN bus, indicating that

there is no latch-up. With increasing temperature, the trigger voltage of the device also increases, and among the measured voltages, a maximum trigger voltage of 44.7 V was observed at 100 ℃. This trigger voltage meets the requirements of the CAN bus ESD protection window for the trigger voltage.

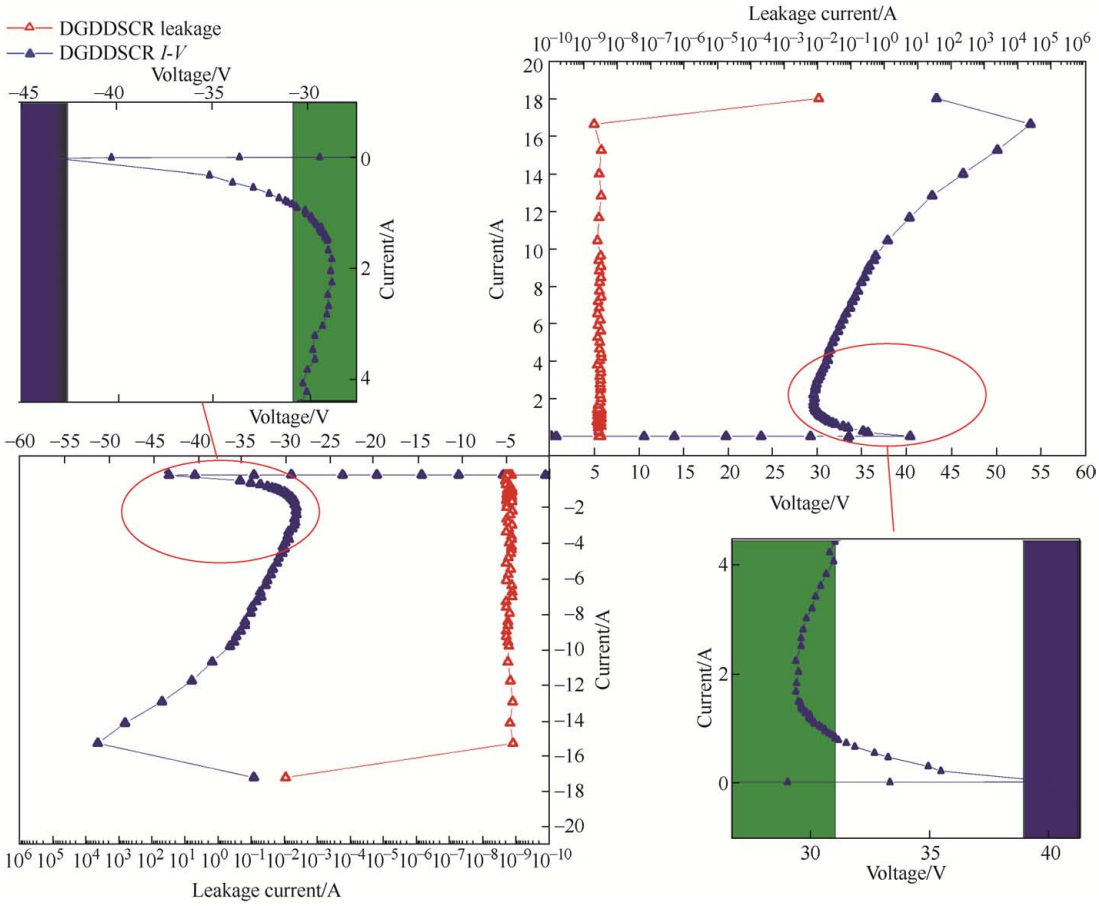


Fig. 14 TLP IV curve of DG-DDSCR device

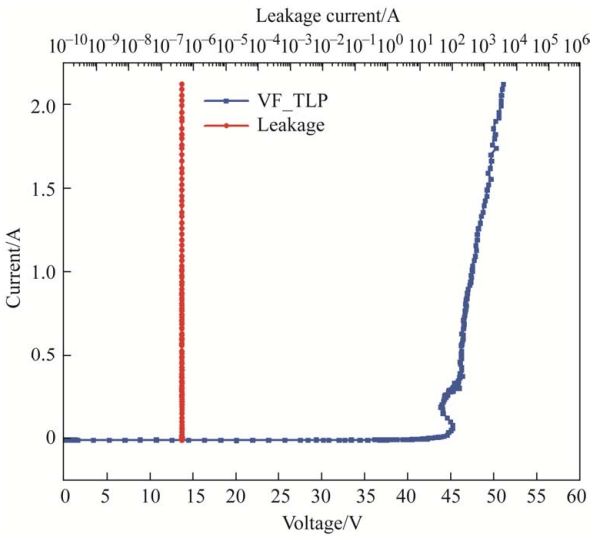


Fig. 15 VFTLP IV curve of DG-DDSCR device

The TLP test results of the DG-DDSCR and reference device are shown in Tab. 1. The comparison shows that only the DG-DDSCR device can simultaneously fulfill the criteria for both high holding voltage and a high failure current exceeding 14.4 V.

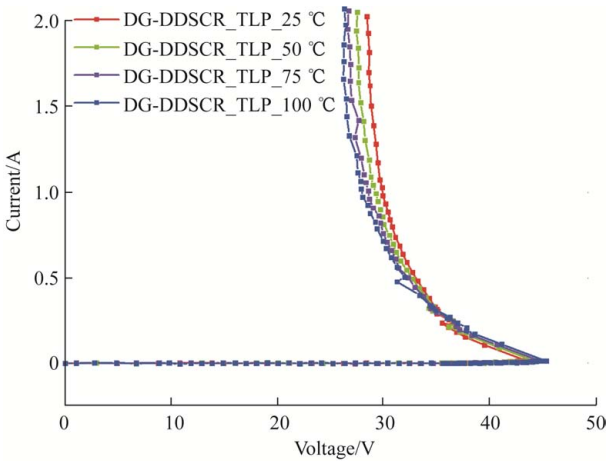


Fig. 16 TLP-IV curves of DG-DDSCR devices at different temperatures

Tab. 1 TLP data for deep well structure, improved LDMOS-DDSCR, GDTSCR, LRSCR and DG-DDSCR

Device name	Ref. [9]	Ref. [10]	Ref. [11]	DG-DDSCR
Trigger voltage V_{t1}/V	23.75	18.26	16.5	43.2
Holding voltage V_h/V	20.20	14.34	13.6	28.8
Failure current I_{t2}/A	14.27	3.41	3.8	17.0
Human body model HBM/kV	21.405	5.12	5.7	25.5
Figure of merit FOM/(mA/μm)	8	10.9	2	26.8

5 Conclusions

In this paper, a dual-gate DG-DDSCR structure with bidirectional conduction characteristics is proposed for the on-chip ESD protection of industrial-grade CAN buses. Based on the 0.18-μm standard BCD process design rules, the device structure was verified by Silvaco TCAD. The test results show that the DG-DDSCR has a high holding voltage of 29.4 V and a high failure current of 16.7 A. The HBM rating was 25 kV, which fully conforms to the target bus ESD design window. In summary, DG-DDSCR devices provide a valuable option for the ESD protection of CAN buses.

References

[1] F Hou, J Liu, Z Liu, et al. New diode-triggered silicon-controlled rectifier for robust electrostatic discharge protection at high temperatures. *IEEE Transactions on Electron Devices*, 2019, 66(4): 2044-2048.

[2] Z Qi, M Qiao, L Liang, et al. Novel silicon-controlled rectifier with snapback-free performance for high-voltage and robust ESD protection. *IEEE Electron Device Letters*, 2019, 40(3): 435-438.

[3] C Y Lin, C Y Chen. Resistor-triggered SCR device for ESD protection in high-speed I/O interface circuits. *IEEE Electron Device Letters*, 2017, 38(6): 712-715.

[4] F Du, G Jiang, M Huang, et al. Investigation and suppression of holding-voltage deterioration in multifinger SCR for robust high-voltage ESD engineering. *IEEE Transactions on Electron Devices*, 2021, 68(12): 6338-6343.

[5] J H Jung, K I Do, S H Jin, et al. An ESD protection circuit with a bidirectional structure and latch-up immunity due to a high holding voltage was studied. *Journal of IKEEE*, 2021, 25(2): 376-380.

[6] J H Kim, S M Lee, C H Park. Accurate modeling methodology of laterally diffused metal-oxide semiconductor leakage current for electrostatic discharge protection circuit design. *Journal of Nanoscience and Nanotechnology*, 2021, 21(8): 4230-4234.

[7] M D Ker, K C Hsu. Latchup-free ESD protection design with complementary substrate-triggered SCR devices. *IEEE Journal of Solid-State Circuits*, 2003, 38(8): 1380-1392.

[8] K I Do, J W Jung, J Song, et al. Design of a dual-directional SCR structure with high holding voltage and low dynamic resistance for high-voltage ESD protection. *IEEE Transactions on Electron Devices*, 2023, 70(9): 4509-4517.

[9] J Liu, L Qian, R Tian, et al. Self-triggered stacked silicon-controlled rectifier structure (STSSCR) for on-chip electrostatic discharge (ESD) protection. *Microelectronics Reliability*, 2017, 71: 1-5.

[10] S S Yen, C H Cheng, C C Fan, et al. Investigation of double-snapback characteristics in resistor-triggered SCRs stacking structure. *IEEE Transactions on Electron Devices*, 2017, 64(10): 4200-4205.

[11] N K Kranthi, S J Di, R Sankaralingam, et al. System-level IEC ESD failures in high-voltage DeNMOS-SCR: Physical insights and design guidelines. *IEEE Transactions on Electron Devices*, 2021, 68(9): 4242-4250.

[12] Y Wang, X Jin, Y Peng, et al. A high failure-current gate-controlled dual-direction SCR for high-voltage ESD protection in 0.18-μm BCD technology. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019, 9(1): 994-1001.

[13] K I Do, B B Song, Y S Koo. A novel dual-directional SCR structure with high holding voltage for 12-V applications in 0.13-μm BCD process. *IEEE Transactions on Electron Devices*, 2020, 67(11): 5020-5027.

[14] H Liang, Q Xu, L Zhu, et al. Design of gate-diode-triggered SCR for dual-direction high-voltage ESD protection. *IEEE Electron Device Letters*, 2018, 40(2): 163-166.

[15] J Sahoo, R Mahapatra, A B Bhattacharayya. Electronically programmable off-state breakdown voltage in an LDMOS transistor with a dual-dummy gate for high-voltage ESD protection. *Microelectronics Journal*, 2021, 108: 104968.

[16] C Y Lin, C Y Chen. Low-C ESD protection design with dual-resistor-triggered SCRs in CMOS technology. *IEEE*

Transactions on Device and Materials Reliability, 2018, 18(2): 197-204.

[17] C T Dai, M D Ker. Comparison of high-holding-voltage SCR and stacked low-voltage devices for ESD protection in high-voltage applications. *IEEE Transactions on Electron Devices*, 2018, 65(2): 798-802.

[18] X Huang, Z Liu, F Liu, et al. High-holding-voltage SCRs with segmented layouts for highly robust ESD protection. *Electronics Letters*, 2017, 53(18): 1274-1275.

[19] X Huang, J J Liou, Z Liu, et al. New high-holding-voltage dual-direction SCR with an optimized segmented topology. *IEEE Electron Device Letters*, 2016, 37(10): 1311-1313.

[20] R K Chang, B Peng, M Ker. Schottky-embedded silicon-controlled rectifier with high holding voltage realized in a 0.18-μm low-voltage CMOS process. *IEEE Transactions on Electron Devices*, 2021, 68(4): 1764-1771.

[21] J A Salcedo, J J Liou, J C Bernier. Design and integration of novel SCR-based devices for ESD protection using CMOS/BiCMOS technology. *IEEE Transactions on Electron Devices*, 2005, 52(12): 2682-2689.

[22] H Liang, L Zhu, X Gu. Dual-MOS-triggered silicon-controlled rectifiers for high-voltage ESD protection. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020, 9(5): 6293-6299.

[23] F Du, Z Liu, J Liu, et al. Novel symmetrical dual-directional SCR with p-type guard ring for high-voltage ESD protection. *IEEE Transactions on Electron Devices*, 2021, 68(8): 4164-4167.

[24] L Lou, J J Liou. Unassisted, low-trigger, high-holding-voltage SCR (uSCR) for on-chip ESD protection applications. *IEEE Electron Device Letters*, 2007, 28(12): 1120-1122.

[25] Q Cui, Han Y, S R Dong, et al. Robust polysilicon-assisted SCR for ESD protection applications. *Journal of Zhejiang University-Science A*, 2007, 8: 1879-1883.

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