# A High Voltage Signal Conditioner for the Quench Detection System of the ITER Superconducting Magnet

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***Abstract*—A Quench Detection System (QDS) will be installed for the ITER superconducting coils and feeder system. The objective of the QDS is to detect a quench in a superconducting device to protect the superconducting devices. This paper aims to provide a functional specification and qualification method for the QDS. In the baseline of I/O, the protection of magnet investment is defined to be carried out through electrical signal processing. Therefore, the primary function of the QDS is to detect the voltage drop across the unrecoverable normal zone in the superconducting system and send a trigger signal to the Central Interlock System to activate the protection circuit. Due to their pulsed operation, the superconducting systems of ITER will experience significant voltage variations, presenting a real challenge for quench detection. Detecting a quench, which typically produces around 0.1 V, among inductive signals in the range of several kilovolts, requires the implementation of digital techniques. Therefore, it is necessary to develop a system that can reliably detect quenches under high-voltage conditions. Over 56 kV electrical isolation will be needed to develop the High Voltage Signal Conditioners (HVSC). This paper provides a summary of the status of HVSC.**

***Index Terms*—Fault diagnostics, high voltage, optic link, quench, quench detection, signal conditioning, signal process, superconducting magnet, superconductor.**

## I. Introduction

A QUENCH Detection System (QDS) will be installed in order to protect the ITER superconducting magnets and feeder systems [1]. The purpose of the QDS is to detect quenches in superconducting elements in order to activate the appropriate protection systems. The baseline design required for the ITER Magnet QDS consists of a primary QDS and a secondary QDS that acts as a backup of the primary. The primary QDS is based on electrical measurements while the secondary QDS is based on thermo-hydraulic measurements. This primary QDS will be composed of High-Voltage (HV) measurements chains linked to an Electronic Quench Detection Device (EQDD). This paper outlines the design of the primary QDS by focusing on the most critical part of it: the High Voltage Signal Conditioner and Remote IO (HVSC&RIO).

The basic function of the QDS is to measure the voltage drop signals across the superconducting elements, compensate the inductive signal to extract the resistive signal, filter the noise, distinguish the quench, and transmit a protecting action trigger signal to the right actuator through the ITER Central Interlock System (CIS) to avoid the permanent damage of the magnet systems. Additionally, the QDS transmits a copy of all data (signal values, state, and health monitoring data) involved in the functions of the Electronic Quench Detection Devices (EQDD) to Control and Data Acquisitions (CODAC) for further post-event analysis.

The High Voltage Signal Conditioning & Remote Input Output (HVSC&RIO) is the signal front end and link to the EQDD. It converts & transmits the voltage signals in the HV potential to voltage digital data by the optic link to enable the digital signal processing in the EQDD which will be located in a low voltage control building.

## II. EQDD Concept Circuits for ITER Magnets

The basic parameters for the design of the primary QDS are the generated resistance and its voltage drop before the hot spot temperature reaches a critical or damage limit, typically set at 150 K [2]. The Fig. 1 shows the voltage generation after a quench has occurred. The fast discharge was initiated 5 s after the quench event. The detection criteria are assumed to be 200 mV with a holding time of 2 s. The Fig. 2 shows the hot spot temperature at the maximum magnetic field position according to this detection and fast discharge profile [3]. In the Fig. 2, $T_{adia}$ $T_{co}$, and $T_{ja}$ mean the hotspot temperature of the coil under the adiabatic condition, conductor, and jacket of conductor, respectively. From the Fig. 2, the time limit of quench detection is 3 s to avoid damage of the magnet. The detection threshold 300 mV and 2 s are confirmed as an example analysis. ITER has several type of magnets. The QDS is designed to meet specified threshold voltage requirements in a given time. The EQDD design needs to provide a high flexibility and threshold and hold time can be adjusted 0.01V $\sim$ 5V and 0 s $\sim$ 100 s.

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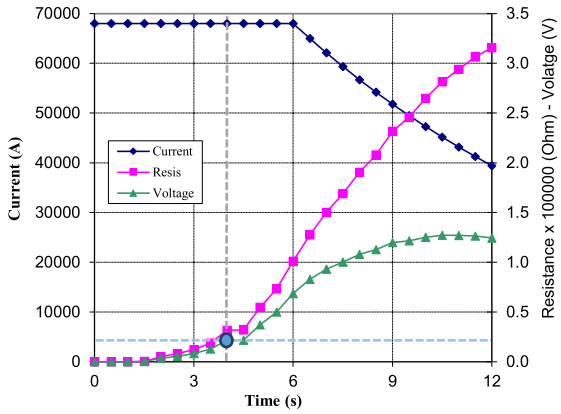



Fig. 1. Profile of current, voltage, and resistance when a quench occurs, and the protection circuit activated. The gray lines indicate the threshold and timing.

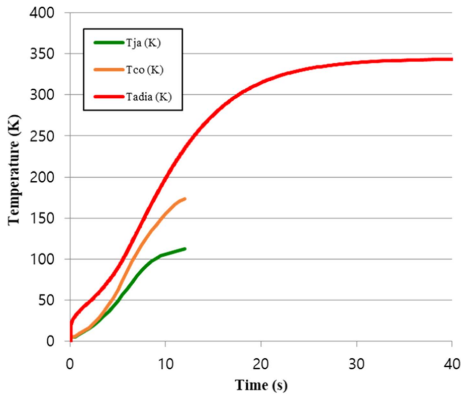



Fig. 2. Hot spot temperature according to the detection and fast discharge profiles in Fig. 1.

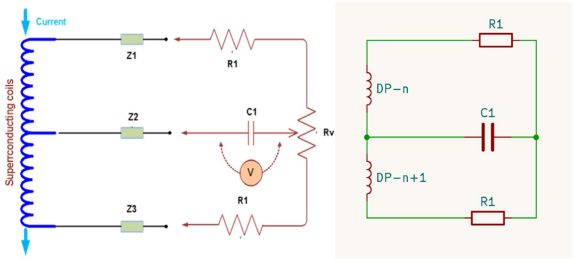



Fig. 3. Basic concept of the balanced bridge circuit. General concept (left), Fixed value balanced bridge (right).

## III. Basic Quench Signal Processing

### A. Balanced Bridge(BB) Compensation

The balanced bridge, as illustrated in Fig. 3, will be adopted for quench detection in the Poloidal Field (PF) coils due to the application of a special winding scheme known as the two-in-hand winding method [4].

In two-in-hand windings, both windings have the exact same shape [4], resulting in an expected reduction of the inductive signal by approximately 1/5000 [5] through the use of the balanced bridge (BB).

However, unlike the approach in [5], [6], it will not utilize a tuning potentiometer; instead, fixed resistors of 50.00% each, as depicted on the left side of Fig. 3, will be employed. This

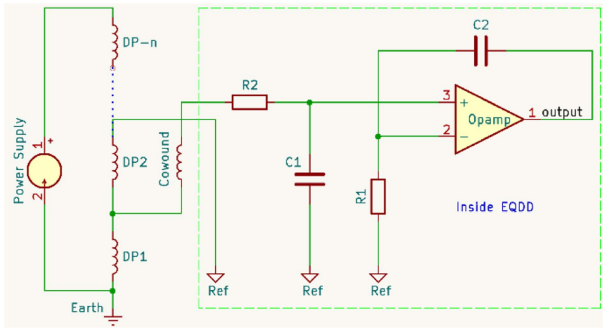



Fig. 4. Co-wound voltage tap and its analogue front end circuit connection.

configuration necessitates a second compensation by the nearby DPs. The second compensation will be carried out in the digital signal processing unit of the low-voltage EQDD.

In addition, it may be used for Double Pancake (DP) 4 to DP 3 (or 5) in Toroidal Field (TF) coils and the Correction Coils. However, it is implemented not in a hardware resistor bridge as shown in Fig. 3 right side, but rather in the digital signal processing unit of the low-voltage EQDD too.

In the Fig. 3, C1 will be installed as a 1st order low pass filter to reject the high voltage ripple first. R1 value in Fig. 3 is decided to avoid the cable impedance effect. If the value of R1 is not large enough compared to the cable impedance, the bridge circuit becomes dependent on the cable impedance variation.

### B. Co-Wound Voltage Tap Receiver

Most coils, such as TF, CS, Bus-bar, and Current Leads, will predominantly adopt a co-wound voltage tap due to its exceptional compensation performance [11]. The signal from a co-wound voltage tap exhibits distinct properties compared to a normal voltage tap, as compensation is already performed by the co-wound wire. Integrated during the coil impregnation process, the co-wound wire has a resistance range from 0.1 to 17 kΩ. To extract maximum power from the co-wound voltage,tap, it is crucial to match the input impedance with the resistance of the co-wound voltage tap. Fig. 4 illustrates the input front-end circuit. The input preamplifier utilizes a non-inverting configuration where $R_2$ is set equal to the co-wound resistance, while $R_1$, $C_1$, and $C_2$ act as a second-order low-pass filter.

The voltage tap directly from the winding pack should be connected with a reference of the circuit, and the co-wound tap will be connected to a signal input resistor $R_2$ port. Consequently, the entire circuit will function, floating from earth ground. This necessitates optic signal transfer and an isolated power supply, as depicted in Fig. 9.

### C. Central Difference Average (CDA) Circuit

The Fig. 5 illustrates a circuit designed to implement CDA in the high voltage domain, a configuration adopted for the CS coil. The input voltage is approximately 1 kV per double pancake, and the desired output voltage is set to be below 10 V. In consideration of the QD circuit, the current in the middle coil exhibits a slight difference. In cases other than a perfect match, an inductive component persists, as depicted in Fig. 5(b) and (1).

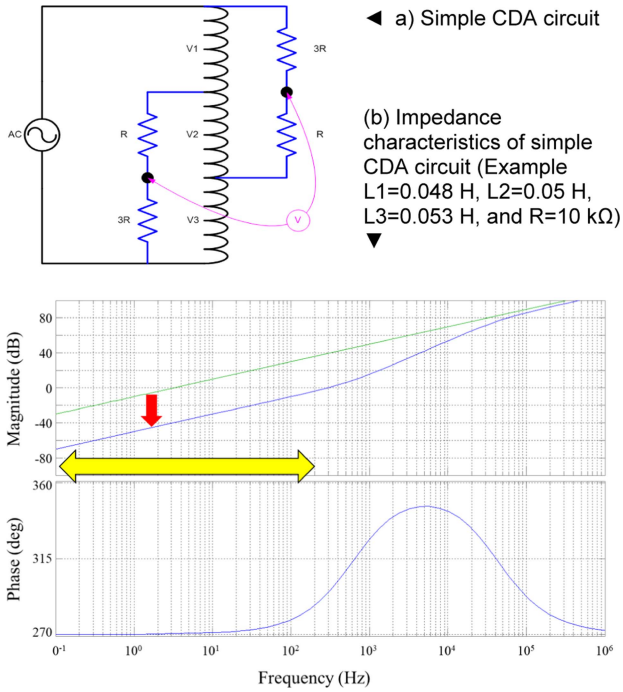



Fig. 5. CDA circuit concept and its impedance transfer function.

In the upper graph of Fig. 5(b), the green line represents the signal magnitude when only the resistance component is taken into account, while the blue line represents the signal magnitude when the inductance component is also considered. This outcome is contingent upon the system impedance Z(s).

$$Z(s) = \frac{\left[-12L_1L_2L_3s^2 - R(L_1L_2+2L_1L_3+2L_2L_3)s + R^2(2L_2-L_1-L_3)\right]s}{2\left[(L_1L_2+L_1L_3+2L_2L_3)s^2 + R(L_1+2L_2+L_3)s + R^2\right]}. \quad (1)$$

where, *Z(s)* is the impedance to calculate the impedance characteristics of the CDA circuit, and other parametric variables are expressed in Fig. 5(a).

Thus, this circuit intrinsically needs a post-compensation for high frequency application. It may be used for DP3, DP4, and DP5 in TF coil. The center DP4 can be effectively compensated by adjacent coils.

## VI. Development of High Voltage Signal Conditioners

### A. ITER Quench Detector Configuration & Components

HVSC&RIO may operate under harsh conditions such as high magnetic field, high voltages, and exposure to nuclear radiation. Since the HVSC&RIO performs the function of machine interlocking, the most important feature might be the reliability. Although lots of modern and leading-edge technologies have been invented in the electronics industrial field thank to mobile and computer science, most of them are not suitable because they are not sufficiently qualified for protection in the harsh condition described above.

Concerning the QDS architecture presented in Fig. 6, the scope of development on the HVSC&RIO and EQDD data transceiver are detailed design, prototyping, and prototype qualification [4]. For HVSC&RIO, the boundary is indicated by the red dashed line in Fig. 6.

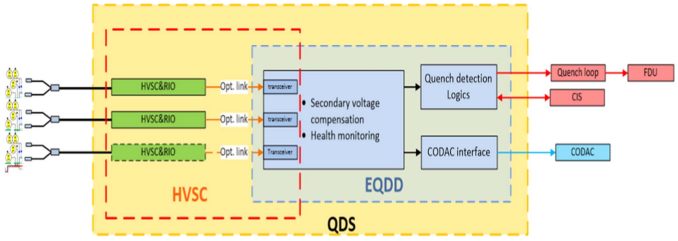



Fig. 6. ITER quench detection system full architecture.

TABLE I
Voltage Signal Measurement Specification

| Range | Low limit [V] | High limit [V] | Resolution [bit] | Accuracy [mV] |
|---|---|---|---|---|
| 1 | -600 | 600 | 24 | 10 |
| 2 | -30 | 30 | 24 | 0.5 |
| 3 | -10 | 10 | 24 | 0.1 |
| 4 | -2.028 | 2.048 | 24 | 0.01 |

### B. Mixed Signal Processing in HVSC&RIO

The fundamental principle involves converting all analog signals to digital within a high electric potential and transferring them to the low voltage side without any data loss. An Analog-to-Digital Converter (ADC) plays a pivotal role as one of the most critical components, adhering to the specifications outlined in Table I. The ADC selection focused on factors such as accuracy, reliability, and sampling speed, leading to the choice of a commercially available ADC in the market with proven performance [8].To satisfy the minimum criteria established by the selected ADC, an active type of filter was designed. The microcontroller (MCU) interfaces with the ADC via SPI at a rate of 1 MHz and utilizes UART at 230 kbps for communication with the low voltage controllers [10]. The physical layer of digital communication was implemented using an optical fiber link to withstand the high voltage environment. It's noteworthy that the MCU operates at 5 V, ensuring reliability, rather than 3.3 V or lower [10].

### C. Analog Front End in HVSC

Following configuration requirements have applied on all HVSC&RIO analogue front end.

- High-voltage protection.
- Passive compensation such as circuit balanced bridge and voltage attenuator.
- One wire among the HV cable can be selected or erused as a reference (local circuit) HV shield for the HVSC&RIO circuit.
- Active Low Pass filter with 10 Hz ~30 Hz cut-off frequency.

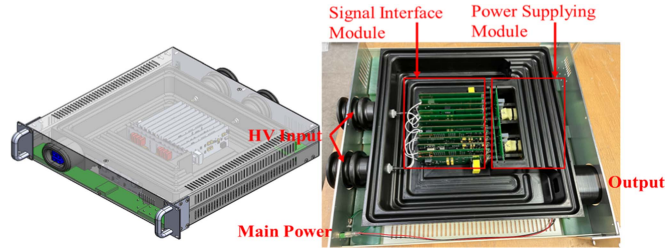
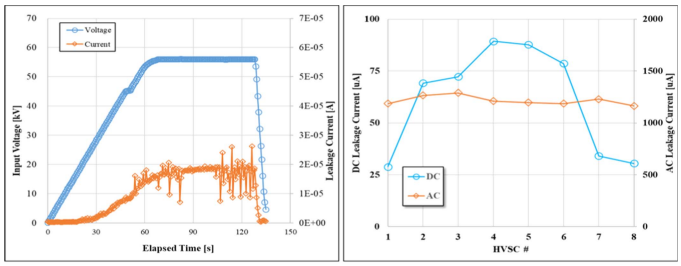



Fig. 7. Fabricated insulation case of HVSC&RIO.




(a) (b)

Fig. 8. HVSC&RIO Hipot test results under DC 56 kV and AC 20 kV: (a) DC and (b) test results for 8 HVSC&RIO.

- The HVSC&RIO circuit shall be fully surrounded by an electrical ground for electrostatic discharge.

This reference shall be electrically insulated from the Power grid earth or to the cubicle ground.

### *D. High Voltage Insulation in HVSC*

The input part in the HVSC&RIO will be electrically connected to the magnet conductor through a protection system. It shall be fully insulated from any electrical ground including chassis ground as it will be set at the same potential as the superconducting magnet.

The insulation case for the HVSC&RIO was implemented by Bakelite Polymer plate. The dielectric strength of Bakelite material has 33 kV/mm [7]. The minimum thickness of insulation case between main circuit board and system ground is set to 10 mm. Designed and fabricated HVSC&RIO case is shown in Fig. 7.

A signal interface and power supplying interface were installed inside the insulated case. The required IO criterion voltage is 56 kV DC and 20 kV AC under 50 Hz [1]. To ensure insulation stability, High Potential (Hipot) tests were conducted on 8 HVSC&RIO case. Fig. 8 shows the Hipot test results of the fabricated HVSC&RIO. The HVSC&RIO has sufficient dielectric strength for design conditions.

### *E. Insulated Remote Power Supply*

In general, an electrical transformer can be the best candidate for powering HVSC&RIO, provided that the magnetic field generated by Tokamak coils is not a critical concern. The magnetic core is prone to saturation, especially at 300 G conditions, which may cause mechanical forces as well as low power transfer rates. Another way to mitigate is capacitive coupling power transfer or air coupling inductive power transfer. Recently, the mobile phone market has been growing by introducing plenty of products to implement these technologies. These techniques make it easier to avoid uncertainties that arise during development. Fig. 9 shows the simple circuit diagram. One HVSC has dual supplying unit to separate the operating electrical potential within the circuits.

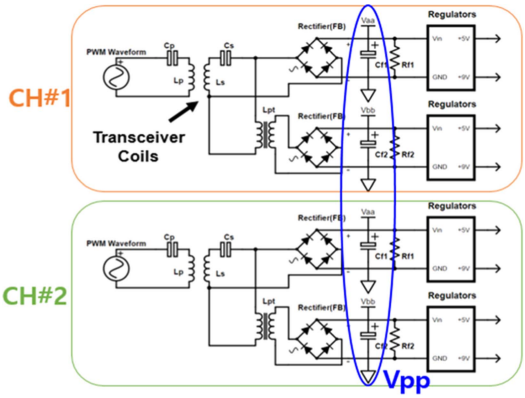



Fig. 9. Inductive remote power supply circuit.

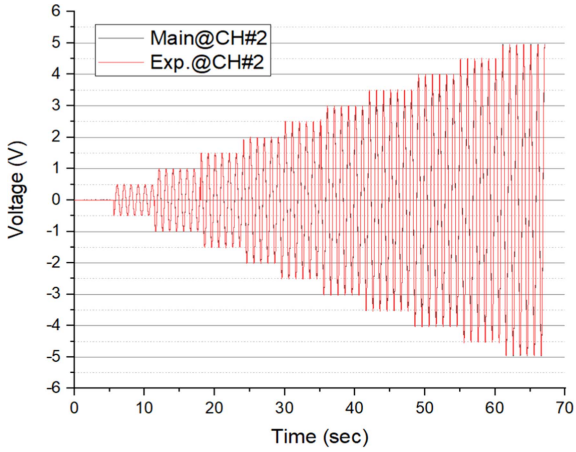



Fig. 10. Measured signal (gray) by developed prototype HVSC. The red line is the applied signal. The gray line is overlapped by red line because of very little measurement error.

### *F. Prototype Development*

Applying all technical specifications, a prototype HVSC and optical interface were developed. Fig. 10 shows the measured signals by a developed HVSC compared to applied input signal. The input and output have less than 0.1% error in 10 kV AC common mode voltage applied thus they are overlapped. For the reliability, an automobile microcontroller was adapted for embedded control [9]. Fig. 11 shows the PCB for the HVSC, with an example of a voltage attenuator on the left and the MCU control and mix signal circuit on the right. This is a prototype circuit board, and all elements are surface mounted (some components were removed after functional testing) and coated with silicone insulator to prevent corona discharge. For the long-time reliability test, A few HVSC&RIO are installed in KSTAR Tokamak measuring the PF voltages.

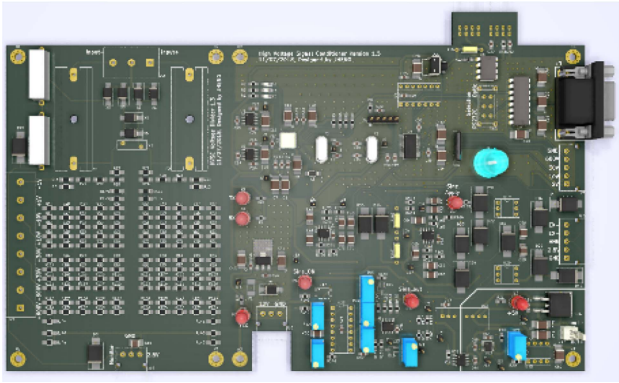


Fig. 11. HVSC PCB for the HVSC, with a voltage attenuator on the left and the MCU control and mix signal circuit on the right.

## V. Conclusion

As part of the ongoing development of a Quench Detection system for the ITER Superconducting Magnet, High Voltage Signal Conditioners have been successfully developed, marking the transition to the series production phase. The fundamental concept involves converting all analog signals to digital within a High Voltage potential and transmitting them through digital communication to prevent any signal losses. This approach requires robust electronics and an isolated power supply in a high voltage environment.

The concept was validated during the prototype development and underwent qualification through operational testing on a superconducting Tokamak machine. ITER has scheduled a Manufacture Readiness Review in November 2023, signaling the initiation of series production starting from 2024.

## VI. Disclaimer

The views and opinions expressed herein do not necessarily reflect those of the ITER Organization.

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