Experimental and Numerical Analysis of Off-State Bias Induced Instabilities in Vertical GaN-on-Si Trench MOSFETs

Nicolò Zagni, *Member, IEEE*, Manuel Fregolent, Giovanni Verzellesi, *Senior Member, IEEE*, Francesco Bergamin, Davide Favero, Carlo De Santi, *Member, IEEE*, Gaudenzio Meneghesso, *Fellow, IEEE*, Enrico Zanoni, *Life Fellow, IEEE*, Christian Huber, Matteo Meneghini, *Senior Member, IEEE*, and Paolo Pavan, *Senior Member, IEEE*

***Abstract*—We analyzed the threshold-voltage dynamic instabilities induced by OFF-state stress in pseudo-vertical GaN-on-Si Trench MOSFETs (TMOS). Extensive measurements revealed that OFF-state stress experiments induce a progressive increase of threshold voltage (V_T), that is fully recoverable only after high-temperature cycles, so that it can appear as permanent degradation at room temperature. V_T increase is found to be strongly affected by drain bias and negligibly influenced by gate bias (below threshold). Activation energy (E_A) extracted from high-temperature V_T recovery experiments was determined to be ≈1 eV. We further characterized pseudo-vertical *p–n* junction diodes fabricated onto the same wafer as the TMOS's by means of capacitance isothermal spectroscopy. This experiment revealed depletion capacitance (C_{DEP}) instabilities with the same E_A as that characterizing the V_T instability, leading to the conclusion that trap states present in the epitaxy are the cause of both observations. Numerical device simulations guided the physical interpretation of the observed phenomena, i.e., donor traps at 1 eV from the conduction band and localized in the *p*-layer lead to both V_T and C_{DEP} instabilities in the TMOS and in the *p–n* diode, respectively, by dynamically modulating the effective *p*-type doping density in the former and the effective depletion layer width in the latter.**

***Index Terms*—OFF-state stress, reliability, stability, trapping, trench MOSFET (TMOS), vertical GaN.**

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Nicolò Zagni and Paolo Pavan are with the Department of Engineering "Enzo Ferrari", University of Modena and Reggio Emilia, 41125 Modena, Italy (e-mail: nicolo.zagni@unimore.it; manuel.fregolent@unipd.it).

Manuel Fregolent, Francesco Bergamin, Davide Favero, Carlo De Santi, Gaudenzio Meneghesso, Enrico Zanoni, and Matteo Meneghini are with the Department of Information Engineering, University of Padova, 35131 Padova, Italy (e-mail: manuel.fregolent@dei.unipd.it).

Giovanni Verzellesi is with the Department of Sciences and Methods for Engineering (DISMI) and also with the EN&TECH Center, University of Modena and Reggio Emilia, 42122 Reggio Emilia, Italy.

Christian Huber is with the Advanced Technologies and Micro Systems Department, Robert Bosch GmbH, 71272 Renningen, Germany.

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I. Introduction

VERTICAL GaN-on-Si devices are a potential cost-effective alternative compared to Si and SiC counterparts for high power switching applications [1], [2]. While GaN-on-Si pseudo-vertical diodes with breakdown voltage (V_{BR}) in the 800–900 V range [3], [4] and with avalanche capability [5] have already been proven in research labs, the challenge of delivering high performance and reliability on large-scale wafers (>200 mm) is yet to be overcome [6]. Moreover, vertical transistors, such as trench MOSFETs (TMOS's) present further hurdles compared to diodes related to the gate stack such as mobility degradation, threshold voltage (V_T) instability and oxide breakdown [7], [8], [9], [10]. These issues need to be characterized under bias conditions relevant for power switching applications, so that their significance for practical applications can be readily assessed.

In this article, we extensively characterize V_T instabilities during OFF-state stress experiments. Instability refers to any recoverable parametric change in device characteristics during operation as a consequence of dynamic effects associated with traps present in the device structure. The stress experiments carried out in this article allow quantifying the cumulative effect on device V_T of OFF-state operating conditions applied, for instance, in switching converters. Interestingly, the observed V_T increase was found to be positively correlated with increasing drain bias while not being significantly influenced by gate bias, suggesting that the mechanism is related with device epitaxy rather than gate stack. V_T recovery was assessed at zero bias at different temperatures and a ≈1-eV activation energy (E_A) was extracted from the Arrhenius plot of the process. Further characterization was carried out on pseudo-vertical *p–n* junction diodes – with the same epitaxy as that of the TMOS's—by means of capacitance isothermal spectroscopy (C-ITS). These experiments revealed an increase of the depletion capacitance (C_{DEP}) under reverse bias conditions, accelerated by temperature with the same E_A as that extracted from the V_T recovery. This correlation points to trapping effects occurring in the device epitaxy as the mechanism behind both observations.

Particularly, V_T increase during OFF-state stress experiments is attributed to the charging of donor traps in the *p*-body region by

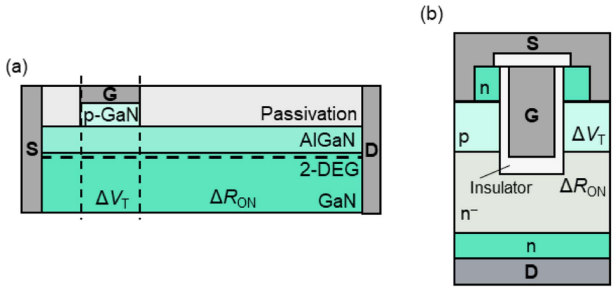

Fig. 1. Schematic representation of (a) lateral p-GaN HEMT and (b) vertical GaN TMOS.

electrons leaking from source to drain under subthreshold conditions. The observations drawn from experiments were supported by calibrated numerical simulations that reproduced well both V_T instability and C_{DEP} increase when including deep donor traps in the p-type body region with 1-eV ionization energy (with respect to GaN conduction band). Finally, we discuss the possible origin of these epitaxy trap states and quantify their impact on the efficiency of a 36-12 V buck converter.

The rest of the article is organized as follows. Section II gives an overview of reliability aspects of GaN devices, particularly focusing on the comparison between lateral and vertical normally-off transistors. In Section III the devices characterized in this article are described. Section IV presents the experimental results. Section V discusses the model proposed to interpret the experiments and the results of the numerical simulations that confirm the interpretation. Finally, Section VI concludes this article.

II. Lateral p-GaN HEMTs Versus Vertical Trench MOSFETs

While lateral GaN devices have already reached commercial maturity [2], [12], [13], [14], vertical counterparts have started only recently to gather attention from the industry [2]. Fig. 1 schematically depicts a lateral, normally-OFF, p-GaN/AlGaN/GaN high-electron mobility transistor (HEMT) and a vertical GaN TMOS.

The promises of the TMOS are: achieving high breakdown voltages (>1 kV) without increasing chip area, high V_T values thanks to the inversion-mode operation, lower impact of trapping issues on R_{ON} compared to lateral GaN devices. The latter point is true provided that the electric field in the OFF-state peaks in the drift region, away from the device surface and gate stack [2]. Nevertheless, owing also to their lower maturity, vertical GaN devices are expected to suffer from charge-trapping related issues. These issues critically affect both conduction and switching losses because of the degradation of key electrical parameters (i.e., V_T [7], R_{ON} [15], as well as device capacitances [16]).

In general, trapping mechanisms can be classified depending on: the specific trap parameters determining their dynamics; the location of the traps within the complex device structure; the type of carriers being captured/emitted; and the charging/discharging path of the trap [2].

TABLE I
Summary of Most Relevant V_{T} and R_{ON} Instability Sources for Lateral and Vertical GaN Devices

	Lateral p-GaN HEMT	Vertical GaN TMOS
ΔV_{T}	Hole depletion (p-GaN) [18] Electron/hole trapping (barrier) [19]	Electron trapping (gate insulator, insulator/GaN interface) [7] Electron trapping (donor traps in p-type body) [this article]
ΔR_{ON}	Hole emission (C-doped buffer) [20] Hole virtual gate (barrier) [21] Hot electron trapping (buffer/barrier) [22], [23]	Electron trapping (along trench sidewall) [15]

In practical terms, these aspects need to be considered either for technology optimization or for determining the proper device for the desired application.

Owing to their different topology, GaN lateral and vertical devices are generally affected by different trapping mechanisms, which in turn determine the drift of V_T, and/or R_{ON}. Table I summarizes the most relevant trapping mechanism in both lateral p-GaN HEMT's (i.e., the most common option in commercial applications) and vertical GaN TMOS's (under investigation in this article).

V_T instability (ΔV_T) is determined by dynamic charge trapping occurring under the gate terminal in lateral devices (p-GaN, AlGaN barrier, GaN buffer) or in either the p-type body region or in the gate insulator in TMOS devices. This occurs because trapped charge affects the capability of the gate terminal to populate the channel—either formed thanks to the two-dimensional electron gas in HEMT's or to the inversion channel in TMOS's.

Depending on the electrical nature of the traps and bias applied to the gate, V_T can shift both negatively and positively [7], [16], [17], [18], [19].

Dynamic R_{ON} (ΔR_{ON}) is determined by trapping occurring in the gate-to-drain access region or drift region in lateral and vertical devices, respectively. The two regions in fact are the largest ones in the structure and as such dominate R_{ON}. Both dynamic R_{ON} increase and decrease can be observed depending on the operating conditions [20], [21], [22], [23]. In TMOS's, dynamic R_{ON} can adversely be affected by traps located along the trench sidewalls [15].

III. Device Description

Devices under test consist of pseudo-vertical GaN TMOS's on a silicon substrate. The epitaxial stack, obtained by metalorganic chemical vapor deposition consists of a strain relief buffer layer, an n^+ drain layer (1 μm), an n^- drift layer (1 μm), a p^+ body channel layer (500 nm), and a n^+-GaN source layer (300 nm). The gate trench was formed with a Cl-based inductive coupled plasma reactive ion etching followed by a Tetramethylammonium hydroxide (TMAH) wet etching to achieve a vertical sidewall free of the plasma damage. Then, 70 nm silicon di-oxide gate dielectric was deposited by low-pressure chemical vapor deposition at a temperature of 880 °C, followed by a

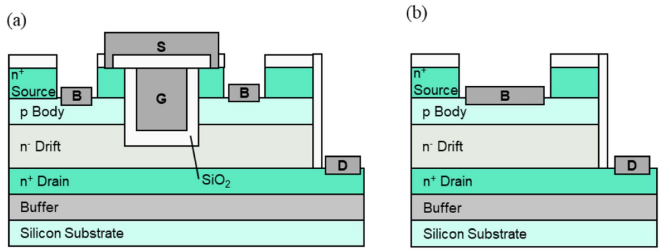

Fig. 2. Schematic cross-section of the (pseudo) vertical GaN devices under study in this article. (a) Trench MOSFET. (b) *p–n* diode. Devices share the same epitaxy.

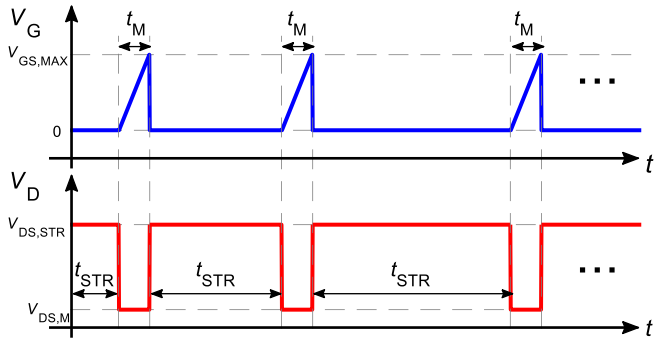

Fig. 3. Sketch of voltage waveforms applied at gate and drain terminals during OFF-state stress experiments (source was kept grounded). $V_{\mathrm{GS,MAX}} = 15$ V, $V_{\mathrm{DS,STR}}$ varied between 0 and 40 V $\Delta V = 10$ V, $V_{\mathrm{DS},M} = 5$ V. $t_M = 10\ \mu$s, t_{STR} was increased logarithmically from 10^{-5} to 10^{2} s.

post-deposition annealing at 900 °C, to improve the mobility in the channel [24]. The gate electrode was made out of polysilicon.

Drain contacts to the $n+$ layer were made from the frontside, laterally displaced with respect to the TMOS mesa structure, creating a pseudo-vertical device.

The structure is a simplified vesion of the classical TMOS that can nominally operate at low voltages, because of the relatively thin drift layer and the lack of thick bottom dielectric [25], [26], [27], or the *p*-type shielding [28] usually implemented in other technologies such as Si and SiC to optimize the breakdown voltage. The structure of the TMOS's under study is schematically reported in Fig. 2(a). As far as V_T instability is concerned, performing the analysis on pseudo- or fully-vertical TMOS's does not affect the conclusions of this article, as the device region responsible for the parametric instability is not the drift region but the *p*-type body region which is the same in both structures.

IV. Degradation Characterization

We characterized V_T instability after OFF-state stress conditions at different bias and temperatures. We also characterized the deep levels in the semiconductor layers of a *p–n* diode (fabricated on the same wafer as that of the TMOS's) by means of capacitance C-ITS under reverse bias conditions. The latter experiments allowed gaining deeper insights into the mechanism underlying V_T instability.

V_T instability characterization was performed under moderate OFF-state stress conditions (i.e., $V_{\mathrm{DS,STR}} = 0$–40 V and $\Delta V_{\mathrm{DS}} = 10$ V) [29]. Fast V_T transient were acquired as follows: device was stressed at a constant bias ($V_{\mathrm{DS,STR}}$) which was periodically interrupted to sample V_T by acquiring I_D-V_{GS} with a fast 10-μs gate voltage ramp, while keeping the drain bias at 5 V.

V_T was defined as the necessary V_{GS} to have $I_D = 1$ mA. Fig. 3 shows a sketch of the voltage waveforms applied on the gate and drain terminals during these experiments. The same setup was also used to assess recovery, for which $V_{\mathrm{DS,REC}} = 0$ V. Stress and recovery maximum duration was 100 s. All these experiments were carried out at room temperature. To avoid any trapped charge accumulation, devices were exposed to 365 nm (3.4 eV) ultraviolet illumination for a few minutes between each stress measurement.

The I_D-V_{GS} acquired during stress with $V_{\mathrm{DS,STR}} = 30$ V are reported in Fig. 4(a), from which it can be observed how the stressed devices are subject to a V_T increase, with negligible changes in terms of subthreshold slope and saturation current. The noisy off-state current for $V_{\mathrm{GS}} < 2.5$ V is limited by the inaccuracy of the autozero procedure applied to compensate the current probe offset. Fig. 4(b) shows instead I_D-V_{GS} acquired during recovery after 100-s stress at $V_{\mathrm{DS,STR}} = 30$ V, showing negligible ΔV_T during the duration of the experiment. The features of V_T instability can be further assessed with the aid Fig. 4(c) and (d), showing ΔV_T (calculated with respect to the pre-stress value) during stress and recovery, respectively, acquired after different $V_{\mathrm{DS,STR}}$.

ΔV_T during stress increases in magnitude (up to saturation) as well as accelerates with increasing $V_{\mathrm{DS,STR}}$, whereas ΔV_T during recovery remains flat regardless of $V_{\mathrm{DS,STR}}$. These results are different from those obtained with gate-stress experiments [29], in which V_T did not show saturation during 1000-s stress and partially recovered in 1000 s. V_T instability during gate-stress experiments were attributed to traps located in the gate oxide near the semiconductor/insulator interface [7], [29]. The different features of V_T instability during OFF-state stress compared to gate stress lead to conclude that it is likely influenced by other mechanisms than oxide traps.

To identify the driving force of the mechanism underlying V_{T} instability, we performed another set of transient characterization also by applying different $V_{\mathrm{GS,STR}} < 0$ V.

This effectively increases V_{DG} during OFF-state stress. The results of this characterization, along with the different combinations of ($V_{\mathrm{DS,STR}}$, $V_{\mathrm{GS,STR}}$) are reported in Fig. 5. From Fig. 5 one can observe how V_T increase is strongly affected by drain bias while it is negligibly influenced by gate bias. To understand why this is the case, we acquired drain and gate leakage currents during constant OFF-state stress experiments. These were carried out starting with $V_{\mathrm{DS}} = 0$ V with $V_{\mathrm{GS}} = 0$ V (i.e., below V_T) for 120 s. After the 120-s period elapsed, V_{DS} was increased by 5 V and kept constant for another 120 s.

The process was repeated in a bias range for which catastrophic failure did not occur, i.e., up to $V_{\mathrm{DS}} = 60$ V. The results of this characterization are reported in Fig. 6, which shows that the drain leakage starts to increase at $V_{\mathrm{DS}} = 15$ V, and keeps increasing progressively up to $V_{\mathrm{DS}} = 60$ V. Instead, during the whole bias range gate leakage current stayed approximately

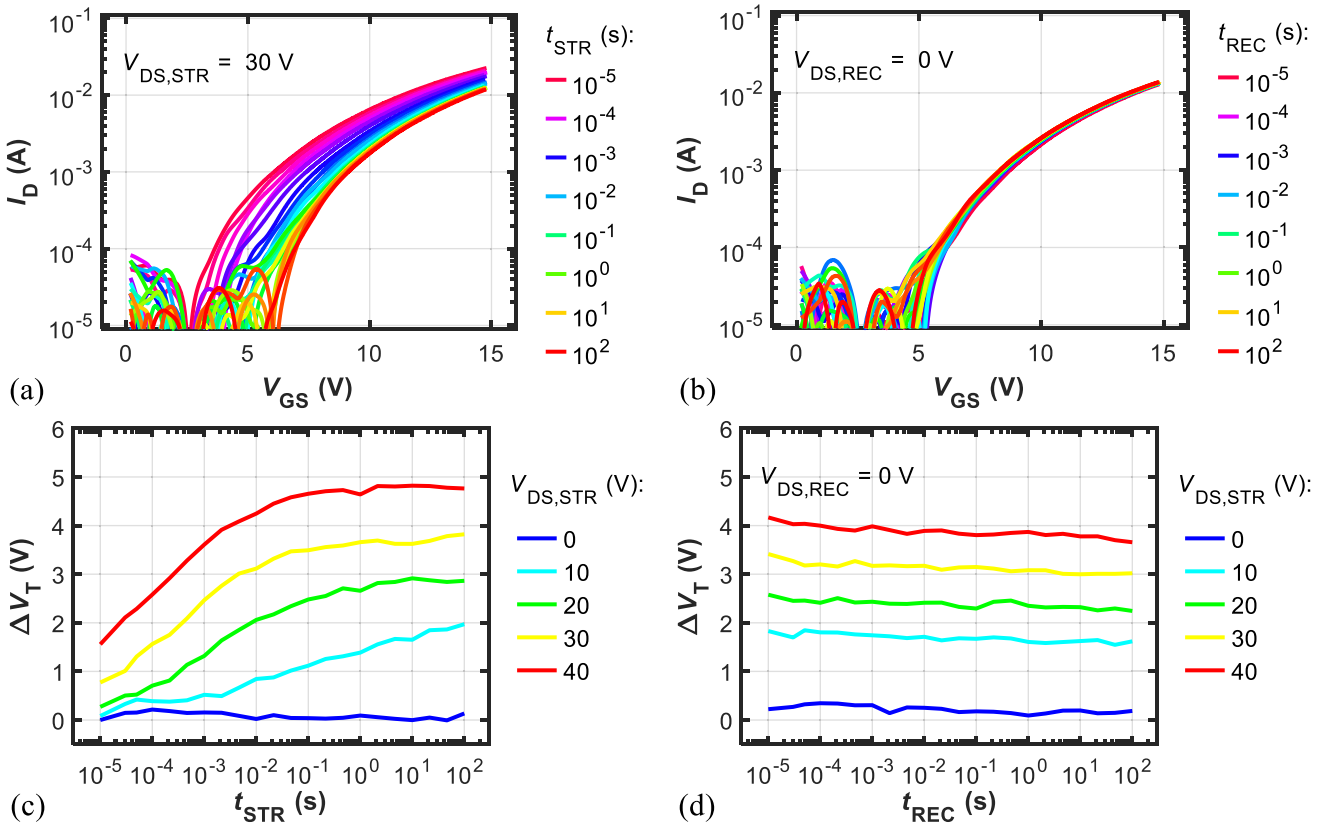

Fig. 4. Analysis of V_T instability during OFF-state stress by means of fast V_T transient characterization. Typical I_D-V_{GS} curves in (a) stress ($V_{DS,STR} = 30$ V) and (b) recovery ($V_{DS,REC} = 0$ V) conditions. (c) and (d) ΔV_T transients extracted during stress and recovery, at different $V_{DS,STR}$ (see legend).

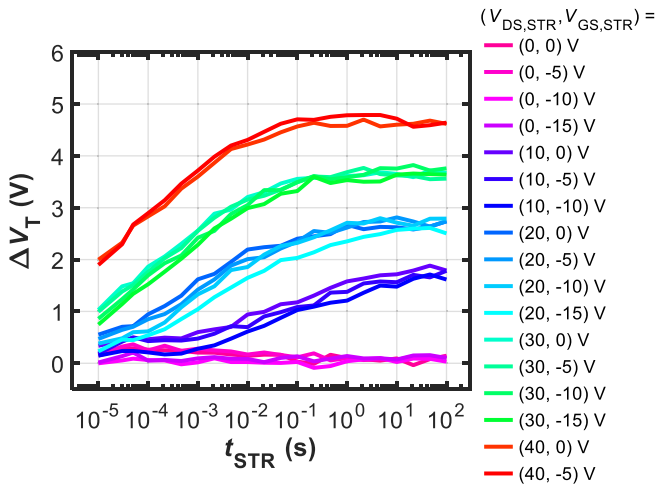

Fig. 5. Analysis of the OFF-state V_T transients as a function of different $V_{DS,STR}$ and $V_{GS,STR}$ (see legend). The increase of V_T is strongly dependent on $V_{DS,STR}$ and negligibly affected by $V_{GS,STR}$.

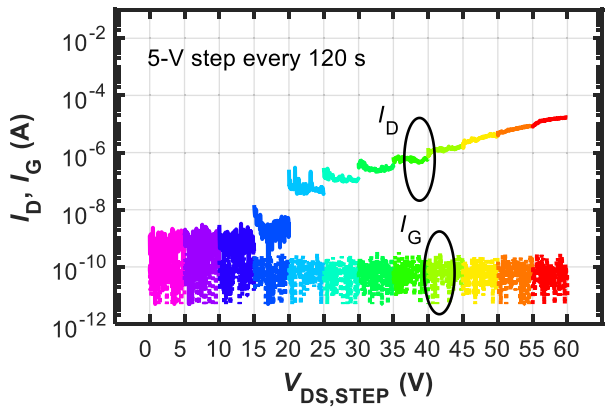

Fig. 6. Drain and gate leakage current during the step-stress experiment.

constant and below ≈0.1 nA, indicating good stability of the gate stack.

From all the experimental findings hitherto reported, one then concludes that V_T instability is influenced by electron trapping occurring within deep levels located in the epitaxial structure (rather than in the gate oxide), that get filled by the source-drain leakage current.

The dynamic properties of the traps responsible for V_T instability were determined by extracting V_T transients at different temperatures. Stress at $V_{DS,STR} = 30$ V was applied for 100 s, and then V_T evolution was monitored at $V_{DS} = 0$ V for 1000 s. The results reported in Fig. 7 show that to induce a significant V_T decrease, high temperature (>150 °C) is required. Furthermore, by fitting V_T decrease with a stretched exponential function following the procedure described in [30], the Arrhenius plot

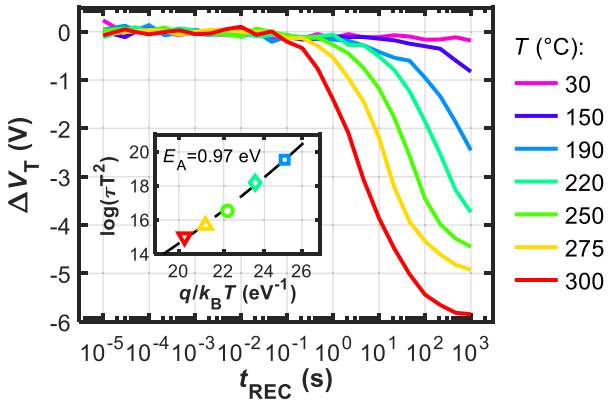

Fig. 7. V_T transients acquired while applying $V_{\rm DS} = 0$ V after 100-s stress at $V_{\rm DS,STR} = 30$ V. (Inset) Arrhenius plot extracted from the data.

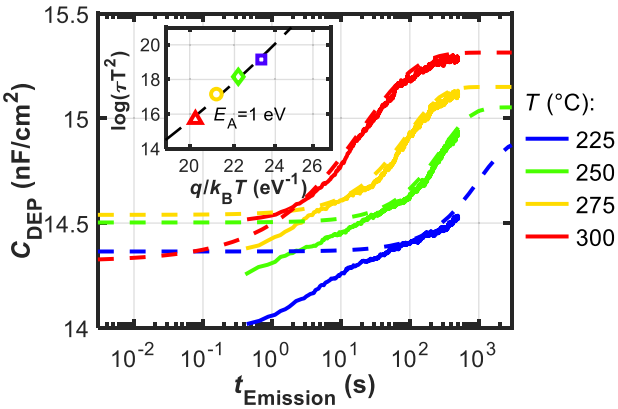

Fig. 8. C-ITS capacitance transients detected on p–n diodes at different temperatures, while keeping $V_R = -30$ V. Dashed lines are $C_{\rm DEP}$ fitting curves with stretched exponentials from which the time constants (τ's) are obtained. (Inset) Arrhenius plot extracted from the τ's.

of the process can be built, see inset in Fig. 7. The extracted activation energy (E_A) is ≈ 0.97 eV.

Finally, to confirm that the traps responsible for the V_T instability are related to the epitaxial structure, we performed an analysis of the deep levels on p–n diodes [on the same wafer as the TMOS's, see Fig. 2(b)] by means of capacitance C-ITS [31]. In these structures the absence of the n-type source layer, and thus of the leakage current observed instead in TMOS's, allows us to single out the effect of electron emission from traps.

The experimental procedure consisted of two phases. First, the diode was biased at a filling voltage $V_F = 0$ V for 100 s, such that any deep levels present in the junction are in a steady-state occupation condition. Then, the diode was reversely biased at $V_R = -30$ V (i.e., the same used to monitor V_T transients) for up to 1000 s and the depletion capacitance ($C_{\rm DEP}$) transient was acquired. In this phase, trapped carriers emitted from traps can be assessed by looking at the variation of $C_{\rm DEP}$. Different temperatures were employed to accelerate carrier emission and to obtain an Arrhenius plot as previously. Results are shown in Fig. 8. The data were fitted with stretched exponential curves in the range attributed to carrier emission; the fitting curves are shown in Fig. 8 as dashed lines. The fitting curves were used to extract the time constants (τ's) to build the Arrhenius plot of the process. The activation energy of the process, obtained from the Arrhenius plot shown in the inset of Fig. 8 is $\approx$1 eV, in very close agreement with that obtained from the V_T transients of Fig. 7. This agreement confirms the hypothesis of traps being located in the epitaxy of the device to be the cause for V_T instability in TMOS's and $C_{\rm DEP}$ increase in p–n diodes.

V. Numerical Simulations

Two-dimensional numerical device simulations were performed with the device simulator included in the Synopsys technology CAD suite [32]. Simulations were devoted to further elucidate the physical mechanism behind both V_T instability and $C_{\rm DEP}$ increase in TMOS's and p–n diodes, respectively. Simulated device cross sections resemble those of the actual devices, see Fig. 2. The simulation setup for the TMOS is based on the one employed in our previous work [7] where we investigated the role of interface and oxide traps on the subthreshold slope and the I–V hysteresis, respectively, in similar devices to the ones considered in this article. Drift-diffusion formalism was employed to simulate charge transport. Incomplete ionization of magnesium (Mg) acceptors was taken into account in the p-doped body region. The Mg ionization energy was set to 0.2 eV from the GaN valence band edge. The trap-occupation dynamics was accounted through the Shockley–Read–Hall (SRH) trap-balance equation without any quasi-static approximation. We included deep donor traps in the p-doped body region with 1-eV ionization energy with respect to GaN conduction band edge. The particular choice for location within the epitaxy stems from the modeling of $C_{\rm DEP}$ increase in the p–n diodes, explained in the following.

The ionization energy of these traps is set equal to the E_A extracted from the experiments. Concentration of traps was set to $N_D = 10^{17}$ cm^{-3}. The same bias conditions and timing that were used during characterization (see Section IV-C) were replicated in the simulation setup. Fig. 9 shows the relative $C_{\rm DEP}$ increase when considering donor traps either in the p-type body, in the n-type drift, and in both regions. As it can be observed, in all cases $C_{\rm DEP}$ increases over emission time. This happens as a result of the reduction of the depletion layer width on the n-side by the emitted electrons. $C_{\rm DEP}$ increase is accelerated by temperature, as expected from SRH theory. The E_A extracted from the Arrhenius plot (not shown) in all cases was 1 eV as expected. However, Fig. 9(a) is the only case for which $\Delta C_{\rm DEP}$ quantitatively agrees with experimental observations. For the sake of comparison, the inset in Fig. 9(a) reports $\Delta C_{\rm DEP}$ obtained from the fitting curves of experimental data. We assume from now on that traps are located only in the p-type body region.

Then, we simulated the V_T recovery transients in TMOS's corresponding to experiments in Fig. 6, starting from an initial condition with filled donor traps. This condition corresponds to the end of the stress period, during which donor traps are filled by source-drain leakage electrons. In this simulation, $N_D = 3 \times 10^{17}$ cm^{-3} to get a quantitative agreement with experiments in terms of magnitude of ΔV_T. Fig. 10 shows

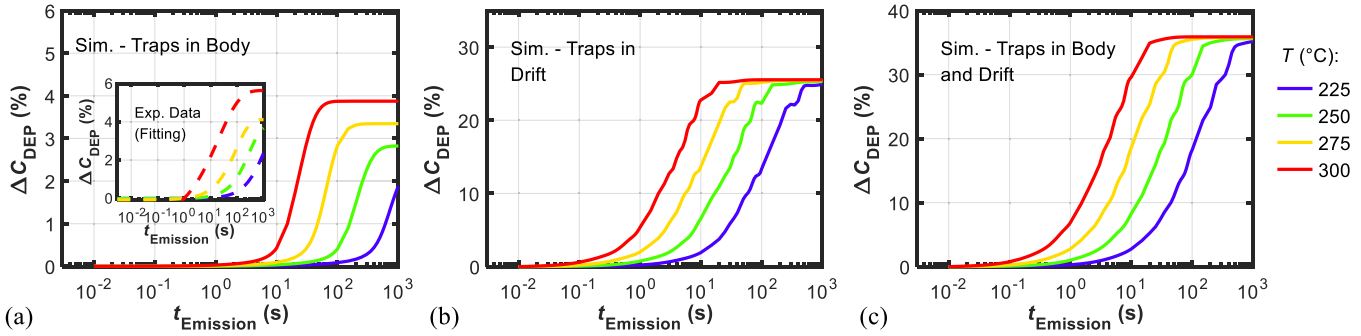

Fig. 9. Simulated C-ITS capacitance transients on p–n diodes at different temperatures, while keeping $V_R = -30$ V, under different modeling assumptions: traps included in (a) body only, (b) drift only, and (c) both in body and drift regions. Dispersion in case (a) More closely agrees quantitively with experimental data fitting curves corresponding to the part of the transients attributed to carrier emission, reported in the inset for easier comparison.

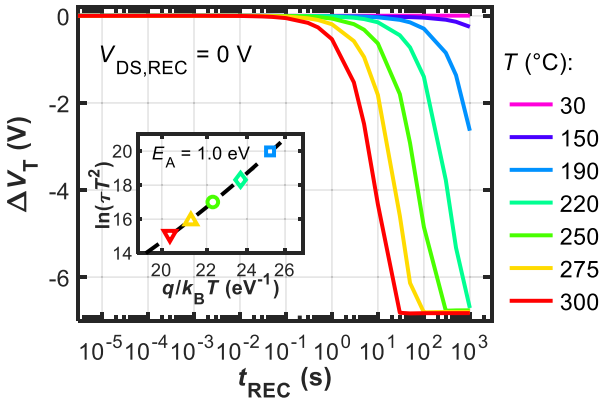

Fig. 10. Simulated V_T transients acquired while applying $V_{DS} = 0$ V starting from an initial condition with completely filled donors in the p-type region. (Inset) Arrhenius plot extracted from the simulation data.

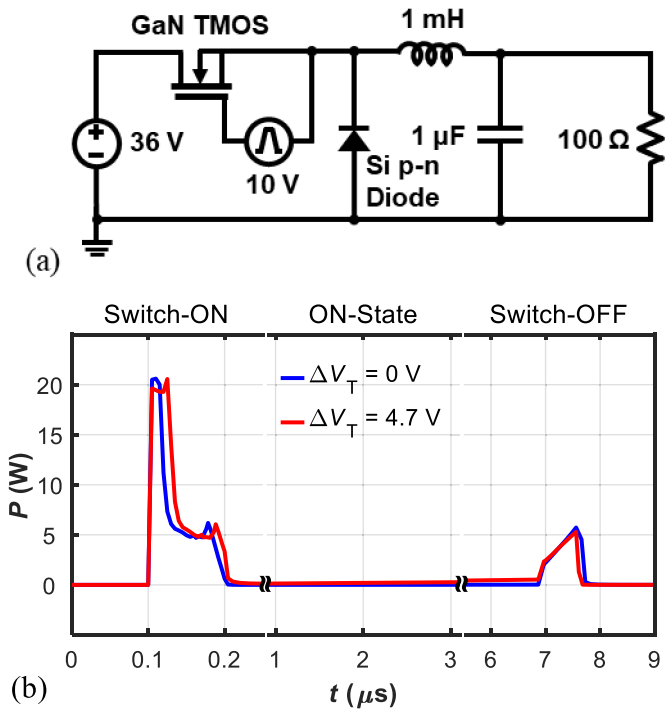

Fig. 11. (a) Circuit schematic of the simulated 36–12 V buck converter. (b) Simulated dissipated power by the TMOS during switch-ON, ON-state, and switch-OFF. Switching period is 20 μs. The origin on the x-axis corresponds to 3 ms, i.e., after 150 cycles from simulation start to ensure switching regime conditions are reached. The two curves correspond to the fresh TMOS (blue line) and the stressed TMOS with increased V_T (red curve) of 4.7 V, corresponding to the worst-case as obtained from experimental data in Fig. 4(a).

the simulation results, from which one can observe how ΔV_T is accelerated by temperature with $E_A = 1$ eV (see inset in Fig. 10) which corresponds to the trap ionization energy (given as input to the simulator). This confirms that it is the emission of electrons from donor traps that determines the V_T decrease. As a matter of fact, when emitting electrons, donor traps become positively charged thus reducing the effective p-body doping and decreasing V_T (i.e., $\Delta V_T < 0$ V).

Generally, having relatively low formation energy, nitrogen vacancies (V_N) act as compensating donor impurities in p-type GaN [33]. However, V_N transition energy is reported to be shallower than 1 eV [33]. Other defects with donor-type behavior and transition energies that can be associated with the 1-eV trap experimentally observed in this article are (defects are ordered from lowest to highest formation energy under p-type growing conditions): nitrogen interstitial (N_i); gallium interstitial (Ga_i); and gallium antisite (Ga_N) [33].

To quantify the ramifications of V_T instability in a practical scenario, we performed a mixed-mode, circuit/device simulation of a 36-12 V buck converter including the TMOS simulated at the device level.

Voltage and current at transistor terminals are obtained from the self-consistent solution of the circuit and drift-diffusion equations within the external network and within the TMOS itself, respectively. The passive elements of the LC low-pass filter are ideal, as well as the diode except for its forward-bias voltage drop.

Fig. 11(a) shows the circuit schematic and Fig. 11(b) shows the dissipated power by the TMOS during switch-ON, ON-state, and switch-OFF, in steady-state regime for two cases, namely: the unstressed TMOS (i.e., $\Delta V_T = 0$ V) and the stressed TMOS with $\Delta V_T = 4.7$ V corresponding to the worst-case as taken from experimental data in Fig. 4(a). As it can be seen from Fig. 11, V_T increase negatively impacts both switching and

conduction losses. The increased losses in the buck converter with the degraded TMOS lead to a reduction of the efficiency from about 84% to 78%.

VI. Conclusion

We evaluated the threshold voltage instabilities induced by the application of OFF-state bias in vertical GaN TMOS's. V_T was found to increase during application of the OFF-state stress bias and recover with a process that is accelerated by temperature with ≈1-eV activation energy (E_A). Vertical *p–n* diodes fabricated on the same wafer were also characterized and it was found that the depletion capacitance was also subjected to changes following the application of a reverse bias and accelerated by temperature with the same E_A as V_T recovery in TMOS devices. This indicates that the source of these instability is related to traps in the epitaxial layer. These observations were corroborated by numerical simulations showing that including donor traps in the *p*-type body layer at 1-eV from GaN conduction band edge allows both V_T and C_{DEP} instabilities to be reproduced. Specifically, V_T instability in TMOS is determined by the modulation of the effective *p*-type doping density, while C_{DEP} increase in the *p–n* diode is due to the decrease of the effective depletion layer width. The experimental conditions employed in this article are such that the results regarding V_T instability are relevant information for both device engineers as well as application engineers.

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Nicolò Zagni (Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Modena and Reggio Emilia, Modena, Italy, in 2021.

He is currently a Postdoc Researcher with the University of Modena and Reggio Emilia. In 2018 and 2019, he was a Visiting Scholar with Purdue University, West Lafayette, IN, USA. His research interests include the investigation of novel electron devices and circuits for applications, such as digital logic, power conversion, nonvolatile memory, and biosensors, and the modeling of stability and reliability of GaN lateral and vertical devices for power applications and reliability of ferroelectric FETs.

Manuel Fregolent received the M.Sc. degree in electronic engineering and the Ph.D. degree in information engineering from the University of Padova, Padua, Italy, in 2020 and 2024, respectively.

He is currently a Postdoc Researcher with the Department of Information Engineering, University of Padova. His research interests include the characterization, physical modeling, and reliability of wide bandgap semiconductor devices, including vertical GaN devices and Ga2O3, and the detection of deep levels in bulk material and on the analysis of charge trapping phenomena leading to threshold voltage instability.

Giovanni Verzellesi (Senior Member, IEEE) received the "Laurea" degree in electrical engineering from the University of Bologna, Bologna, Italy, in 1989, and the Ph.D. degree in electrical engineering from the University of Padova, Padova, Italy, in 1994.

From 1993 to 1994, he was a Visiting Graduate Student with the University of California, Santa Barbara, CA, USA. From 1994 to 1999, he was with the University of Trento, Trento, Italy, as an Assistant Professor of electronics. Since 1999, he has been with the University of Modena and Reggio Emilia, Italy, where he became Associate Professor in 2000 and Professor in 2006.

Francesco Bergamin, photograph and biography not available at the time of publication.

Davide Favero received the master's degree in electronic engineering in 2021 from the Department of Information Engineering, University of Padova, Padua, Italy, where he is currently working toward the Ph.D.

His research interests include the development of on-wafer characterization methodologies and in the assessment of dynamic behavior, reliability, and modeling of GaN-based power devices, with focus on both AlGaN/GaN HEMTs and vertical GaN MOSFETs.

Carlo De Santi (Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Padova, Padua, Italy, in 2013.

He has been an Assistant Professor with the University of Padova, Padua, Italy, since 2019. He is a coauthor of more than 250 journal and conference papers, including 43 invited ones. His research interests include the characterization, modeling of physical processes, and reliability of electronic and optoelectronic devices based on elemental and compound semiconductors, including various ternary and quaternary compounds, power electronics and radio frequency systems, LEDs and lasers in the UV, visible monochromatic and white spectral range, devices for silicon photonics, solar cells and photodetectors, and phosphors and systems for lighting applications.

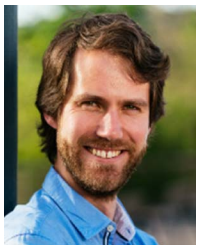
Gaudenzio Meneghesso (Fellow, IEEE) graduated in electronics engineering from the University of Padova, Padua, Italy, in 1992.

During his graduation he worked on the failure mechanism induced by hot electrons in MESFET sand HEMTs. Since 2011, he has been with the University of Padova as a Full Professor. He has authored or coauthored more than 800 technical papers (of which more than 100 invited papers). His research interests include the electrical characterization, modeling, and reliability of microelectronics devices.

Mr. Meneghesso was the recipient of 12 best paper awards. He has been nominated to IEEE Fellow class 2013, with the following citation: "for contributions to the reliability physics of compound semiconductors devices."

Enrico Zanoni (Life Fellow, IEEE) graduated in Physics summa cum laude at the University of Modena, Modena, Italy, in 1982.

He is currently a Professor of microelectronics with the Department of Information Engineering, University of Padova, Padua, Italy. At the University of Padova, he contributed to establish a research group involved in CMOS analog and RF-integrated circuit design, CMOS reliability and radiation hardness, compound semiconductor characterization, modeling, and reliability. He is the coauthor of more than 800 publications on the modeling and reliability physics of silicon and compound semiconductor devices and of four patents.



Christian Huber received the B.S., M.S., and Ph.D. degrees in physics from the Karlsruhe Institute of Technology, Karlsruhe, Germany in 2011, 2015, and 2019, respectively.

Between 2015 and 2018, he was a Ph.D. Candidate with the Corporate Research Division of the Robert Bosch GmbH. He continued his research career in the Advanced Technologies and Micro Systems Department, Robert Bosch GmbH, Renningen, Germany, in the field of wide band gap power electronics with special focus on vertical GaN power transistors. He is coordinator of the EU-funded project YESvGaN and develops front and backside process technology for vertical GaN-on-silicon membrane transistors.

Matteo Meneghini (Senior Member, IEEE) received the Ph.D. degree, with a focus on the optimization of gallium nitride (GaN)-based LED and laser structures, from the University of Padua, Padua, Italy, in 2008.

He is currently a Full Professor with the Department of Information Engineering, University of Padua. His main interests are the characterization, reliability, and modeling of compound semiconductor devices [LEDs, laser diodes, and high-electron-mobility transistors (HEMTs)], and optoelectronic components, including solar cells. Within these activities, he has published more than 400 journal articles and conference proceedings papers.

Paolo Pavan (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Padova, Padua, Italy, in 1994.

He is currently a Full Professor of electronics with the University of Modena and Reggio Emilia, Modena, Italy. He is currently Rectors Delegate for Scientific Research. His research interests include the characterization, modeling, and optimization of nonvolatile resistive memories (RRAMs), logic-in-memory and neuromorphic architecture, and the development of safety critical and energy-aware applications for low-power computing and automotive electronics.

Mr. Pavan was on the Technical Committee of IEEE IEDM, VLSI-TSA, IEEE IRPS, IEEE ESSDERC (TPC in 2014), and ESREF. He was the Guest Editor of IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY and Associate Editor for IEEE Journal of Electron Devices Society.

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