All-Port MIMO Admittance Passivity for Robust Stability of DC–DC Interlinking Converters

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***Abstract*—This article explores the passivity properties of a dc–dc converter's unterminated all-port MIMO admittance matrix, for analyzing and preventing the converter's destabilizing impact in grid-connecting (interlinking) scenarios with an arbitrary, even meshed, termination (grid impedance). In addition to the passivity properties of the converter's unterminated input and output self admittances, the coupling passivity property is examined, which accounts for the possible destabilizing impact of port-coupling. The dependence of these properties on the control loop parameters is exemplified using a current-controlled buck converter. Examples of two techniques for enhancing a converter's all-port MIMO admittance passivity, by active damping impedance emulation and multisampled pulse width modulation, are examined and shown to be effective. The proposed methodology is validated both in frequency and time domain, using control hardware-in-the-loop simulations, as well as experimentally, using a laboratory prototype.**

***Index Terms*—DC–DC converter, digital control, passivity, port-coupling, power electronics grid, stability, unterminated model.**

I. Introduction

STABILITY is of great concern in contemporary, power electronics dominated distribution systems/grids [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15]. For assessing the small-signal stability of a *grid-connected* converter, impedance-based method is typically applied at a point-of-connection (port) of interest [1], [2], [3], [4], [5], [6]. For this, the converter and the grid, being the subsystems seen at each side of that port, can be represented by the Norton and the Thevenin equivalent circuit [1], [3], [4]. Stability can then be determined by applying the (generalized) Nyquist stability criterion to the product of the corresponding grid's *terminated* impedance and the converter's *terminated* admittance [1], [3], [4], [5].

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Relying on this, admittance passivity criterion was derived and has become widely applied for analyzing and preventing destabilizing interactions between the converter and the grid [7], [8], [9], [10], [11], [12], [13], [14], [15]. Assuming a passive grid's *terminated* impedance, this standardly used criterion imposes the passivity of the converter's *terminated* admittance at the considered port as a sufficient condition for system stability [7], [8], [9], [10], [11], [13], [14], [15]. Nevertheless, to determine such admittance, information about termination at all other converter's ports is necessary [4], [5], [16], [17], which may be unknown or variable, e.g., for a *grid-connecting* (interlinking) converter [16]. If the impact of termination [17] is relevant, passivation of the converter's *terminated* admittance cannot guarantee stability due to the possible destabilizing impact of port-coupling [4], [16]. Another shortcoming of the standardly used admittance passivity criterion is that it is difficult to apply in grids with meshed (as opposed to radial) structures [18], e.g., multiterminal dc grids.

Though the unterminated modeling and measurement principles were established long-time ago [19], [20], [21], [22], [23], [24], they have only recently started being applied to all-port (unterminated) impedance-based stability analysis [18], [25], [26] and the corresponding admittance passivity-oriented design [27], [28]. Along this line, with an aim to overcome the above discussed limitations of the standardly used admittance passivity criterion, the all-port MIMO admittance passivity criterion for dc–dc converters was proposed in [27]. The criterion arises from the all-port MIMO impedance-based method [18], which assesses stability by applying the generalized Nyquist criterion to the product of the grid's *unterminated* MIMO impedance matrix and the converter's *unterminated* MIMO admittance matrix. Stemming from this and assuming a passive grid's *unterminated* MIMO impedance matrix, the all-port MIMO admittance passivity criterion imposes passivity of the converter's *unterminated* MIMO admittance matrix as a sufficient condition for system stability. This admittance matrix characterizes the converter's small-signal dynamics under ideal termination and can be used as a building block for analyzing interconnection dynamics [19], [20], [21], [22], [23], [24]. Thus, the all-port MIMO admittance passivity criterion allows to analyze the impact of the grid-connecting converter in a general case of an arbitrary (even meshed) termination.

The MIMO admittance passivity condition from [27] involves evaluating the positive semidefiniteness of the matrix obtained as one half of the sum of the converter's unterminated all-port

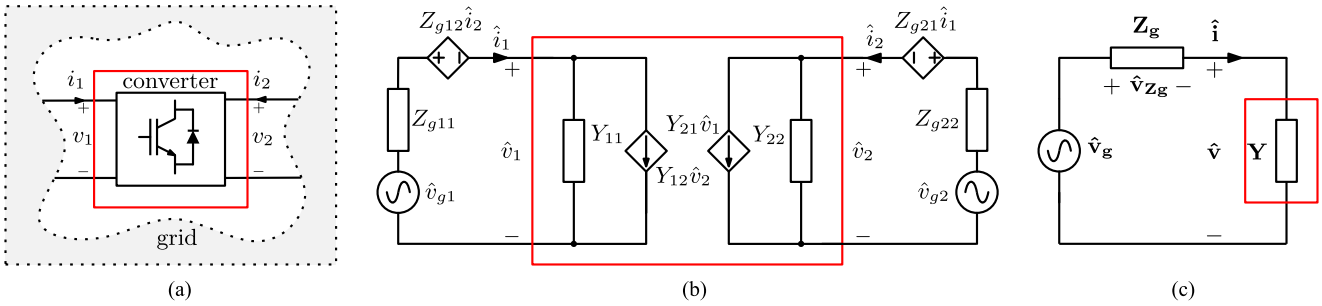

Fig. 1. (a) Two-subsystem representation for the impedance-based stability analysis of the two-port grid-connecting (interlinking) converter, (b) small-signal representation of the system from (a) and (c) the simplified equivalent representation of (b), featuring the all-port MIMO matrix notation. In (b) and (c), the converter's control system's reference perturbation $\hat{r}$ is justifiably assumed to be zero (see footnote 1).

MIMO admittance matrix and its complex conjugate transpose [29]. For this, the nonnegativity of the resulting matrix's principal minors [30], [31], termed MIMO admittance passivity properties, was evaluated in [27]. These properties were then used to predict the port-coupling induced instability of a current-controlled buck converter. However, this instability was not demonstrated experimentally and the methods for its prevention were not addressed in [27]. Furthermore, impact of different control loop parameters on the MIMO passivity properties was not examined.

With the methodology from [27] as a foundation, this article aims to fill in these gaps and present a generally applicable passivity-oriented controller design framework, exemplified through a simple digital current-controlled buck converter. The dependence of its all-port MIMO admittance passivity properties on several current control loop's parameters is examined at frequencies where contribution of outer loops can be neglected. Based on this, multisampled pulse width modulation (MS-PWM) [32], [33], [34], which has so far been known for enhancing only the converter's output (switched-node side) admittance passivity at high frequencies [13], [14], is shown to be advantageous for enhancing also the converter's all-port MIMO admittance passivity. Consequently, its capability to prevent the high-frequency port-coupling induced instability is experimentally demonstrated in this article. As an example of the control strategy that can successfully enhance the all-port MIMO admittance passivity at lower frequencies, input-voltage feedforward-based damping impedance emulation from [12] is explored, which has so far been known for enhancing only the converter's input (dc-link side) admittance passivity [12]. In addition, it is revealed in this article that, by combining MS-PWM and the input-voltage feedforward, the MIMO admittance passivity can be simultaneously enhanced at low- and high-frequencies. As an addendum, an alternative, input-feedforward passivity index-based approach for characterizing the MIMO admittance passivity is illustrated. It relies on the minimum eigenvalue-based positive semidefiniteness condition [30].

The rest of this article is organized as follows. Section II introduces the all-port MIMO admittance passivity criterion and the MIMO admittance passivity properties. Their impact on the stability in grid-connecting scenarios, as well as their dependence on the control loop's parameters is illustrated in Section III. In Section IV, the passivity enhancement methods are proposed and verified using control hardware-in-the-loop (C-HIL) simulations. Experimental validation, both in frequency- and time-domain, is addressed in Section V. Finally, Section VI concludes this article.

II. All-Port MIMO Stability Analysis

A. MIMO Impedance-Based Method

To determine small-signal stability properties of a grid-connecting (interlinking) converter, such as one from Fig. 1(a), the all-port MIMO impedance based-method can be used, which is thoroughly analyzed in [18]. Its fundamental principles, that are relevant for the methodology presented in this article, are outlined below. The detailed derivations can be found in [18]. As an example, a two-port dc–dc converter from Fig. 1(a) is considered hereafter, but the methodology is directly applicable to multiport dc–dc converters. Due to an added layer of complexity in small-signal modeling of systems with a time-varying operating point, ac–dc converters will be addressed in a separate work.

The MIMO impedance-based method relies on the equivalent small-signal s-domain representation shown in Fig. 1(b) [18]. It involves representing the converter via the unterminated MIMO admittance matrix $\mathbf{Y}(s)$

$$\mathbf{Y(s)} = \begin{bmatrix} Y_{11}(s) & Y_{12}(s) \\ Y_{21}(s) & Y_{22}(s) \end{bmatrix} \tag{1}$$

where s is the complex variable of the Laplace transform, and

$$Y_{11}(s) = \left.\frac{\hat{i}_1(s)}{\hat{v}_1(s)}\right|_{\hat{v}_2(s)=0}, \; Y_{22}(s) = \left.\frac{\hat{i}_2(s)}{\hat{v}_2(s)}\right|_{\hat{v}_1(s)=0},$$
$$Y_{12}(s) = \left.\frac{\hat{i}_1(s)}{\hat{v}_2(s)}\right|_{\hat{v}_1(s)=0}, \; Y_{21}(s) = \left.\frac{\hat{i}_2(s)}{\hat{v}_1(s)}\right|_{\hat{v}_2(s)=0} \tag{2}$$

where $\hat{i}_{1,2}(s)$, $\hat{v}_{1,2}(s)$ are Laplace transforms of small-signal perturbations of $i_{1,2}$, $v_{1,2}$ from Fig. 1(a). The expressions for $Y_{11}(s)$, $Y_{12}(s)$, $Y_{21}(s)$, and $Y_{22}(s)$ can be derived based on the small-signal model of the converter and its control system [35], which is addressed in Section III-B.

The grid is represented by the Thevenin voltage sources $\hat{v}_{g1}(s)$ and $\hat{v}_{g2}(s)$ and the unterminated MIMO impedance matrix $\mathbf{Z_g}(s)$

$$\mathbf{Z_g}(s) = \begin{bmatrix} Z_{g11}(s) & Z_{g12}(s) \\ Z_{g21}(s) & Z_{g22}(s) \end{bmatrix} \tag{3}$$

where Z_{g11}, Z_{g12}, Z_{g21}, and Z_{g22} are defined analogously to Y_{11}, Y_{12}, Y_{21}, and Y_{22} in (2). In case the system is not meshed, i.e., the ports of the converter under study are solely interconnected by the converter itself [18], the grid's impedance matrix becomes diagonal ($Z_{g12} = Z_{g21} = 0$).

According to Fig. 1(b), the following holds[1]:

$$\hat{\mathbf{v}}(s) = \left(\mathbf{I} + \mathbf{Y}(s)\mathbf{Z_g}(s)\right)^{-1} \hat{\mathbf{v}}_{\mathbf{g}}(s) \tag{4}$$

where $\mathbf{I}$ is the identity matrix, $\hat{\mathbf{v}}(s) = [\hat{v}_1(s), \hat{v}_2(s)]^T$, $\hat{\mathbf{v}}_{\mathbf{g}}(s) = [\hat{v}_{g1}(s), \hat{v}_{g2}(s)]^T$, and T is the transpose operator. Subsequently, the circuit from Fig. 1(b) can be represented in a compact form shown in Fig. 1(c). Then, assuming that the grid is standalone stable ($\hat{\mathbf{v}}_{\mathbf{g}}(s)$ is stable), stability of the grid-connecting converter can be determined by applying the generalized Nyquist stability criterion to the minor-loop gain $\mathbf{L}(s) = \mathbf{Y}(s)\mathbf{Z_g}(s)$ [18].

B. MIMO Admittance Passivity Criterion

For determining a sufficient condition for the stability of the system from Fig. 1, the all-port MIMO admittance passivity criterion can be used, which is derived by applying the frequency-domain passivity theory principles [29] to (4). Namely, provided that the grid's unterminated all-port MIMO impedance matrix $\mathbf{Z_g}(s)$ is passive, a sufficient condition for the stability of the interconnected system is passivity of the converter's unterminated all-port MIMO admittance matrix $\mathbf{Y}(s)$. The transfer function matrix such as $\mathbf{Y}(s)$ is called passive if $\mathbf{Y}(s)$ is stable and

$$\mathbf{P}(j\omega) = \frac{1}{2}\left(\mathbf{Y}(j\omega) + \mathbf{Y}^H(j\omega)\right) \geq 0, \forall \omega \in \mathcal{R} \tag{5}$$

where H is the Hermitian (conjugate transpose) operator [29]. Note that, due to the desired power conversion and regulation capabilities, as well as the system delays, a converter can never dissipate energy at all frequencies [7], [8]. Thus, in practice, the passivity condition (5) is usually relaxed to a frequency range Ω that is critical for stability [7], [8], [9], [10], [11], [12]. Though this may be ambiguous from the strict passivity theory principle point of view, it has proven sufficient in practical power electronics applications [7], [8], [9], [10], [11], [12]. Although there is still no unique regulation that defines the range Ω, some examples of the limits imposed by system integrators or standards can be found in [36], [37]. Also, the range Ω can be determined as a set of frequencies where grid's antiresonances (or high grid impedance magnitudes), are known to be present, or where control loops are known to introduce stability problems.

[1]In (4) and in Fig. 1(b) and 1(c), the converter's control-system reference perturbation $\hat{r}(s)$, and, consequently, the Norton current sources that account for its impact [18], are assumed to be zero. If the closed-loop reference tracking system is stable under the ideally stiff grid (which is reasonable to assume), this $\hat{r}(s) = 0$ allows for analyzing stability properties related solely to the converter's interaction with the nonideal grid [18].

Accordingly, instead of $\forall \omega \in \mathcal{R}$, $\forall \omega \in \Omega$ is considered in (5). For the presentation conciseness, this notation is omitted in the subsequent conditions (such as (6)–(8), (24)) that are derived from (5).

Inequality (5) can be evaluated via any of the approaches that are standardly used in linear algebra to determine positive-semidefiniteness of a matrix $\mathbf{P}$ [30]. Hereafter, the approach that evaluates nonnegativity of *all* its principal minors is used [31]. An alternative approach that evaluates nonnegativity of its minimum eigenvalue, which corresponds to the input feedforward passivity index of $\mathbf{Y}(s)$, is addressed in the Appendix.

According to the principal minors-based approach, for 2×2 $\mathbf{Y}(s)$ given by (1), (5) is equivalent to

$$P_1(j\omega) \geq 0 \tag{6}$$

$$P_2(j\omega) \geq 0 \tag{7}$$

$$P_{12}(j\omega) \geq 0 \tag{8}$$

where

$$P_1(j\omega) = Re\{Y_{11}(j\omega)\} \tag{9}$$

$$P_2(j\omega) = Re\{Y_{22}(j\omega)\} \tag{10}$$

$$\begin{aligned} P_{12}(j\omega) = {} & 2Re\{Y_{11}(j\omega)\}Re\{Y_{22}(j\omega)\} \\ & - \frac{1}{2}Re\{Y_{12}(j\omega) + Y_{21}(j\omega)\}^2 \\ & - \frac{1}{2}Im\{Y_{12}(j\omega) - Y_{21}(j\omega)\}^2. \end{aligned} \tag{11}$$

Note that if the edge case $\mathbf{P} = 0$ is excluded, it is sufficient to evaluate only the *leading* principal minors of $\mathbf{P}$ [31].

As for the physical meaning of the, so called, MIMO admittance passivity properties, P_1, P_2, and P_{12}, according to (9) and (10), P_1 and P_2 represent the effective conductance of the converter's input and output self admittances Y_{11} and Y_{22}, respectively. On the other hand, the coupling passivity property P_{12} is a mathematical term that, contrary to P_1 and P_2, reflects passivity considering also the coupling between the converter's ports, as, according to (11), it depends not only on Y_{11} and Y_{22}, but also on Y_{12} and Y_{21}. Thus, to take into account the risk for the port-coupling induced instability, evaluation of $P_{12}(j\omega)$ is vital in the frequency ranges where the coupling between the converter's ports is pronounced. Such frequency ranges can be inferred as those where $|Y_{12}(j\omega)Y_{21}(j\omega)|$ is relatively high. This is because when both Y_{12} and Y_{21} exhibit high magnitudes, impact of termination can become relevant (see e.g., (9) and (10) from [27]).

III. MIMO Admittance Passivity Properties

This section exemplifies the use of the above introduced MIMO admittance passivity properties for analyzing stability and developing robust-stability oriented control methods for an interlinking converter in several grid-connecting scenarios.

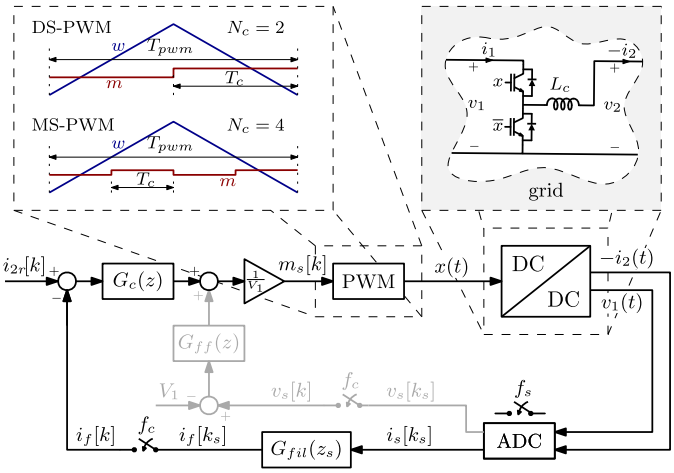

Fig. 2. Block diagram the considered digital output current-controlled pulsewidth-modulated two-level buck converter, used as an example of the grid-connecting converter from Fig. 1(a).

A. Control System Under Study

To illustrate core principles without introducing unnecessary complexity, hereafter, a single-stage digital output current-controlled pulsewidth-modulated two-level buck converter is considered. Nevertheless, the methodology from this article can be applied to other two-level and multilevel topologies, as well as other single- and multi-stage control system architectures. The block diagram of the considered control system is shown in Fig. 2 and described below.

The inductor current is sampled at the rate $f_s = \frac{1}{T_s} = N_s f_{\text{pwm}}$, where N_s is the multisampling factor and $f_{\text{pwm}} = \frac{1}{T_{\text{pwm}}}$ is the frequency of the triangular PWM carrier w. The (feedback) sampling instants are synchronized with w so that one of them always coincides with $w = 0$, while the others are equidistantly spaced across T_{pwm}. Without any nonidealities, this allows for the average current to be sampled when $N_s = 1$ or $N_s = 2$. To enhance noise immunity and/or modulator linearity [32], [34], [38], the sampled current may be processed by a digital filter $G_{\text{fil}}(z)$. Afterwards, in the case of multirate control strategies [32], [38], an example of which is discussed in Section V, a rate change from f_s to $f_c = \frac{1}{T_c} = N_c f_{\text{pwm}}$ may be imposed, where N_c and f_c are the control update factor and frequency, respectively. In the case of single-rate control strategies, considered in Sections III and IV as well as in one of the examples in Section V, $N_c = N_s$ and the entire digital domain is executed at a single rate, determined by the feedback sampling frequency f_s. In either case, the control update instants are synchronized with w so that one of them always coincides with $w = 0$ while the others are equidistantly spaced across T_{pwm}.

The (filtered and/or decimated) feedback signal i_f is subtracted from the current reference i_{2r} and the resulting error signal is processed by the current controller. As an example [39], the proportional integral (PI) controller is used, whose z-domain transfer function is

$$G_c(z) = k_p + k_i T_c \frac{z}{z-1} \tag{12}$$

where z is the complex variable of $\mathcal{Z}$ transform, $k_p = 2\pi f_{\text{cr}} L_c$ and $k_i = 2\pi 0.1 f_{\text{cr}} k_p$ are the proportional and integral gain, respectively, f_{cr} is the crossover frequency of the current control loop, and L_c is the inductance of the buck converter's output filter. The gain k_p is set to achieve the desired f_{cr}, while k_i is set so that the impact of the integral action is limited well-below f_{cr}. If, with the goal of enhancing the converter's admittance passivity, it is of interest to emulate the damping impedance at the dc-link (input) port, which is addressed in Section IV-B, a positive "feedforward" action ("FF") of the converter's input voltage[2] may be added to the output of the main, feedback, current controller [12]. The "feedforward" action is obtained by processing the difference between the sampled converter's input voltage v_s and the dc value V_1 of the input voltage v_1 through $G_{\text{ff}}(z)$, whose specific structure is addressed in Section IV-B.

The overall control action m_s, which is scaled to the range [0,1] and may be delayed due to a finite control algorithm computation time [39], is forwarded to the digital pulsewidth modulator. Within it, the impulse train $m_s[k]$ is held constant over one T_c to obtain the continuous-time modulating signal $m(t)$. Intersections between m and w define the switching signal $x(t)$, which is the square waveform whose steady-state duty cycle D determines the converter's conversion ratio. Note that, for $N_c > 2$, a proper logic is implemented to prevent multiple-switching and pulse-skipping, that, unless properly handled, can arise when intersections between m and w are vertical (as opposed to horizontal) [32].

As for the modulator, two different PWM types are considered, distinguished based on the value of N_c. For $N_c = 2$ the standardly used double-sampled PWM (DS-PWM) is obtained, where the control update is performed at peaks and valleys of the triangular carrier w [39]. For $N_c > 2$, the MS-PWM is obtained, where the control update is performed multiple times per modulation period [32], [33], [34]. Motivation for using MS-PWM arises from its inherent capability to reduce digital delays [32], [33], which can be seen from the modulator's pulse-to-continuous s-domain representation

$$G_{\text{pwm}}(s) = \frac{\hat{d}(s)}{\hat{m}(s)} \approx e^{-s\frac{T_{\text{pwm}}}{2N_c}} \tag{13}$$

where $\hat{m}(s)$ and $\hat{d}(s)$ are, respectively, Laplace transforms of the small-signal components of the continuous-time modulating signal $m(t)$ and duty cycle $d(t)$ of $x(t)$, used in averaged modeling [33], [39]. According to (13), the higher the control-update factor N_c, the lower the modulation delay. Consequently, by reducing modulation delay [33], [39], MS-PWM can enhance control loop's dynamic performance, as well as high-frequency admittance passivity, which is addressed in Sections IV-A, IV-C, and V.

[2]This can be considered as a feedforward action only in case the converter, without any input filter, is supplied from the grid with zero impedance [$Z_{g11} = Z_{g12} = 0$ in Fig. 1(b)], as only in this case $\hat{v}_1$ from Fig. 1 can be considered as an external disturbance. Otherwise, such an action should strictly be classified as a feedback. Still, it is in the literature most often referred to as feedforward [12]. Thus, to avoid misinterpretation, the term feedforward will be kept in this article, but denoted by "" to emphasize ambiguity.

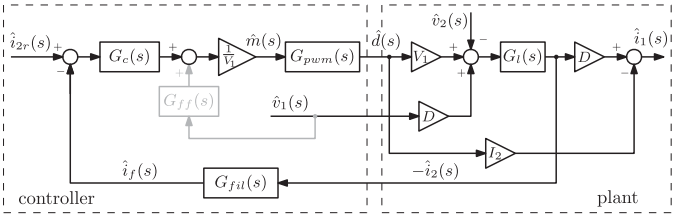

Fig. 3. Small-signal s-domain representation of the system from Fig. 2.

B. Small-Signal S-Domain Representation

The small-signal s-domain representation of the system from Fig. 2 is shown in Fig. 3. According to it, (2) yields

$$Y_{11}(s) = \frac{1}{1+T(s)}\left(-\frac{DI_{2r}T(s)}{V_1} + G_l(s)D^2 + G_{\text{ff}}(s)G_{\text{pwm}}(s)\left(G_l(s)D + \frac{I_{2r}}{V_1}\right)\right) \quad (14)$$

$$Y_{22}(s) = \frac{G_l(s)}{1+T(s)} \quad (15)$$

$$Y_{12}(s) = \frac{1}{1+T(s)}\left(-DG_l(s) + \frac{I_{2r}}{V_1}T(s)\right) \quad (16)$$

$$Y_{21}(s) = -\frac{G_l(s)}{1+T(s)}\left(D + G_{\text{ff}}(s)G_{\text{pwm}}(s)\right) \quad (17)$$

where $T(s) = G_c(s)G_{\text{pwm}}(s)G_l(s)G_{\text{fil}}(s)$ is the loop-gain of the reference tracking system. Further, $G_c(s)$, $G_{\text{fil}}(s)$, $G_{\text{ff}}(s)$ are the s-domain representations of the current controller $G_c(z)$, feedback filter $G_{\text{fil}}(z)$, and the "feedforward" action $G_{\text{ff}}(z)$. Finally, $G_l(s) = \frac{1}{sL_c+R_{L_c}}$, where R_{L_c} is the output filter inductor's parasitic resistance, $I_{2r} = -I_2$ is the output dc current reference, V_1 and I_2 are the steady-state values of v_1 and i_2, respectively. The delay due to finite computation time [39] can be included within $G_c(s)$ and $G_{\text{ff}}(s)$.

C. C-HIL Frequency Response Measurements

As a prerequisite for the subsequent passivity-based stability analysis, this section presents C-HIL frequency domain validation of the small-signal model discussed in Section III-B. For this, the simplest variant of the control system from Fig. 2, which involves a single-rate control with DS-PWM ($N_s = N_c = 2$) with neither the feedback filters ($G_{\text{fil}} = 1$) nor the "feedforward" action ($G_{\text{ff}} = 0$) is considered. The parameters of the buck converter under study and its control loop are given in Table I. The corresponding MIMO admittance passivity properties are shown in Fig. 4, within the frequency range from 10 Hz up to $f_{\text{pwm}} = 10\,\text{kHz}$. Note that, in case of control system architectures that feature outer, slower, loops (such as droop control), the passivity properties preserve qualitative resemblance to those discussed hereafter *only* if the contribution of the outer loops is negligible in the considered frequency range, which is typical at high frequencies [8]. Research along the line of wide-band MIMO admittance passivity in presence of outer loops is left for future work.

TABLE I
PARAMETERS OF THE BUCK CONVERTER USED FOR C-HIL VALIDATIONS

Parameter	Label	Value	Unit
Input dc voltage	V_{g1}	120	V
Output dc voltage	V_{g2}	85	V
Output dc current	I_{2r}	20	A
Steady-state duty cycle	D	0.75	V
Filter inductance	L_c	1.5	mH
Filter inductor's resistance	R_{L_c}	0.25	Ω
Switching frequency	f_{pwm}	10	kHz
Dead time	t_{dt}	0.8	μs
Multi-sampling factor	$N_s = N_c$	$\{2, 4\}$	–
Sampling frequency	$f_s = f_c$	$\{20, 40\}$	kHz
Crossover frequency	f_{cr}	1.4	kHz
Phase margin	PM	$\{48, 66\}$	°

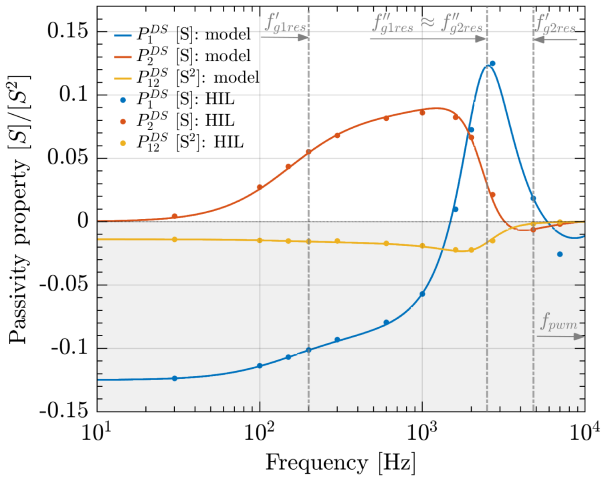

Fig. 4. Unterminated all-port MIMO admittance passivity properties (9), (10), (11) of the buck converter with parameters from Table I and single-rate control system from Fig. 2, with DS-PWM ($N_c = N_s = 2$), with neither feedback filters ($G_{\text{fil}} = 1$) nor "feedforward" action ($G_{\text{ff}} = 0$). The results obtained from C-HIL simulations (dots) and analytical model (full lines) are shown.

The waveforms shown in Fig. 4 with full lines are obtained from the analytical model. For this, the parameters from Table I and $s = j\omega$ are substituted in (14)–(17) and $P_1(j\omega)$, $P_2(j\omega)$, $P_{12}(j\omega)$ are calculated based on (9), (10), and (11). The waveforms shown in Fig. 4 with dot markers are obtained from the frequency response measurements of the C-HIL implementation of the system from Fig. 2. For this, the converter is emulated via Typhoon HIL 402, with the circuit solver time step of 0.5 μs. The inductor current is acquired from the HIL's analog output. The ADC, the current control, and the DPWM are realized within B-Board PRO control platform from Imperix. To obtain $Y_{11}(j\omega), Y_{12}(j\omega), Y_{21}(j\omega), Y_{22}(j\omega)$, and subsequently $P_1(j\omega)$, $P_2(j\omega)$, $P_{12}(j\omega)$, the series perturbation injection circuits were emulated in HIL, and the frequency responses of interest were obtained using HIL's dedicated SCADA widget. As seen in Fig. 4, the results obtained in this way from C-HIL simulations and those obtained from the analytical model are in agreement.

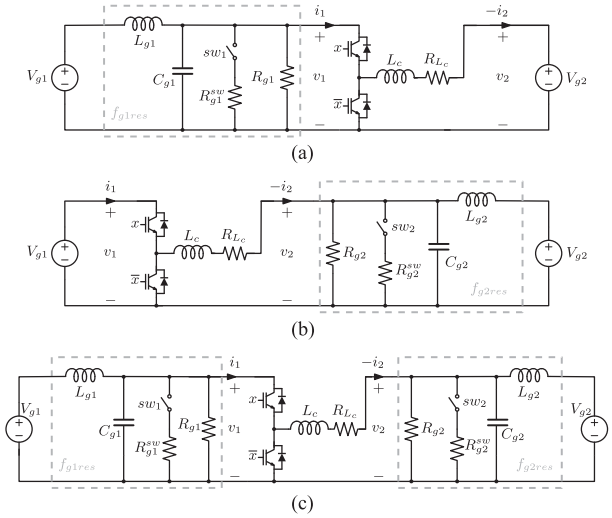

Fig. 5. Grid-connecting scenarios considered for analytical passivity-based instability risk predictions and C-HIL time domain stability tests. The grid features antiresonance at (a) port 1, (b) port 2, (c) both ports. By opening the switches $sw_{1,2}$, the grid's damping around antiresonant frequencies is reduced.

D. Grid-Connecting Scenarios Under Study

With the goal of illustrating the use of the MIMO admittance-passivity properties P_1, P_2, P_{12} for predicting the risk for the instability of the considered converter in various grid-connecting scenarios, that is addressed in Section III-E, this section briefly explains the three considered scenarios, which are shown in Fig. 5. A nonmeshed grid is assumed ($Z_{g12} = Z_{g21} = 0$), whose impedances Z_{g11} and/or Z_{g22} form parallel antiresonance circuits.

In Fig. 5(a) and 5(b), the antiresonance is present at a single port only and the grid is assumed to be ideally stiff at the other port. Such scenarios, which are standardly considered [7], [8], [13], [14], represent the applications where the impact of the port-coupling on the stability is negligible. One such application is the high-frequency passivity analysis of grid-connected voltage source converters, where, with a high-enough dc-link capacitor, the impact of the dc-link dynamics on the ac-side dynamics can be neglected [13], [14], [15], [40]. In such cases, the stability of the grid-connecting converter can be simply predicted by evaluating passivity of the converter's unterminated admittance where the grid's antiresonance is present. This involves evaluating (6) (or (7)) around f_{g1res} (or f_{g2res}).

Still, there are applications in which, to accurately predict the risk for the instability, the coupling between the ports must be accounted for [4] and [16]. Then, as derived from the MIMO admittance passivity condition (5) in Section II-B, it is not sufficient to evaluate only (6) or (7), but also (8) has to be evaluated to correctly account for the possibility of port-coupling induced instability. A scenario used in this article to represent such applications is shown in Fig. 5(c). There, the grid's impedance at both ports features the antiresonance.

E. Passivity-Based Instability Risk Prediction

Next, by evaluating whether, in the frequency range critical for stability, P_1, P_2, P_{12} from Fig. 4 satisfy (6), (7), and (8), it was of interest to predict the risk for the instability of the considered converter in grid-connecting scenarios shown in Fig. 5. Along this line, it should be emphasized, that, since (5) (which is equivalent to (6), (7), and (8)) is only a sufficient, but not necessary condition for stability [29], the instability will not necessarily arise in case (6), (7), or (8) are not satisfied. For example, stable operation will be achieved if the net sum of what is in this article referred to as the converter's *damping* and the grid's *damping* is positive at the critical frequency [29], [41], [42]. Thereby, in the unterminated all-port MIMO sense, the converter's *damping* at the frequency ω can be defined as the minimum eigenvalue of $\mathbf{P}(j\omega)$ [29], [42]. As such, according to the Appendix, it represents the joint effect of P_1, P_2, P_{12}, and corresponds to the input feedforward passivity index of $\mathbf{Y}(s)$ at the frequency ω. Analogously, the grid's *damping* at the frequency ω can be defined as the minimum eigenvalue of $\mathbf{P_g}(j\omega) = 0.5(\mathbf{Z_g}(j\omega) + \mathbf{Z_g}^H(j\omega))$, which corresponds to the output feedback passivity index of $\mathbf{Z_g}(s)$ at the frequency ω [29], [42].

The strict mathematical formulation and a quantitative application of the above informally stated *all-port MIMO positive-net damping criterion* is left for future studies. To preserve intuitiveness and simplicity, the subsequent analysis will indicate the instability risk by commenting on the extent of the converter's (negative) *damping*, which is determined by P_1, P_2, and P_{12}, and the grid's (positive) *damping* around the critical, i.e., the grid's antiresonant frequencies. To maintain the mathematical rigor, stability assessment is, for all of the hereafter discussed scenarios and test cases, performed also using the MIMO impedance based method from Section II-A, similar as in [18]. The results, which are all aligned with the corresponding time domain stability tests, are not shown due to space limitation.

The instability risk predictions in the grid connecting scenarios from Fig. 5 are discussed below for the two test cases, different in terms of the values of the grid's antiresonant frequencies (f_{g1res} and f_{g2res}). They are as follows.

1) Test case 1: $f'_{g1res} = 200$ Hz, $f'_{g2res} = 4800$ Hz.
2) Test case 2: $f''_{g1res} \approx f''_{g2res} = 2500$ Hz.

As seen from Fig. 4, where the grid's antiresonant frequencies are plotted as gray dash-dotted vertical lines, in the test case 1, (6) is not satisfied around f'_{g1res}. Thus, provided that the grid's damping around f'_{g1res} is low enough, instability is expected to arise in the scenario from Fig. 5(a). The same holds for the scenario from Fig. 5(b), since (7) does not hold around f'_{g2res}. Consequently, given that the converter is prone to being destabilized when the grid features the antiresonance at a single port only [the scenarios from Fig. 5(a) and 5(b)], it is also prone to being destabilized when the grid features the antiresonances at both ports [the scenario from Fig. 5(c)]. To verify these stability predictions, time domain stability tests of the circuits from Fig. 5 are performed using the above explained C-HIL implementation of the system from Fig. 2. By opening the switches $sw_{1,2}$, the grid's damping around antiresonant frequencies is reduced, and the transient is triggered. For the grid's antiresonances' parameters corresponding to the test case 1, the converter's input and output current and voltage waveforms in response to such a transient are shown in Fig. 6(a), (b), and (c) for the scenarios from Fig. 5(a), (b), and (c), respectively. As seen, the previously

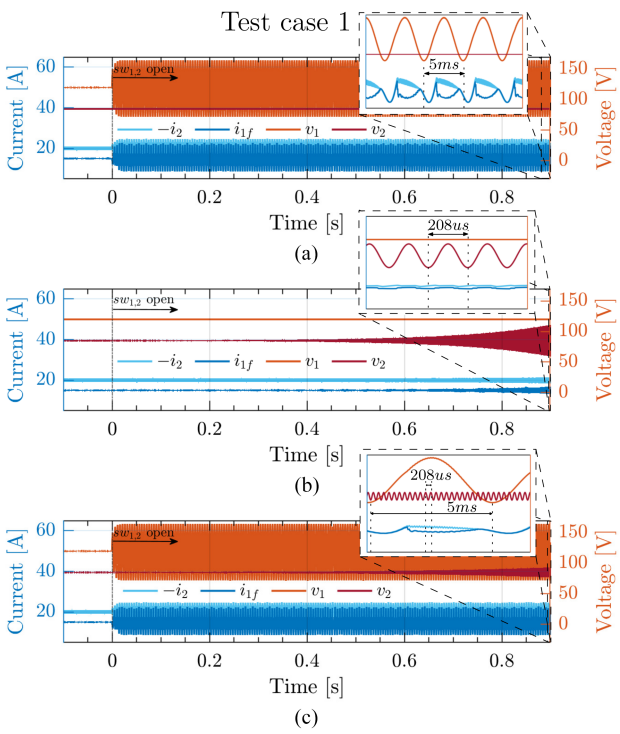

Fig. 6. Input and output current and voltage waveforms obtained from C-HIL simulations of the converter with the passivity properties from Fig. 4 (DS-PWM without the "feedforward"), operated in the grid-connecting scenarios from Fig. 5 with the grid's antiresonances' parameters corresponding to the test case 1. The transient is triggered by opening sw_{12} from Fig. 5 at $t = 0$ s. The results in (a), (b), and (c) correspond to the scenarios from Fig. 5(a), (b), and (c). For a better visualization, instead of i_1, i_{1f} is plotted, which is obtained by filtering out the switching ripple from i_1.

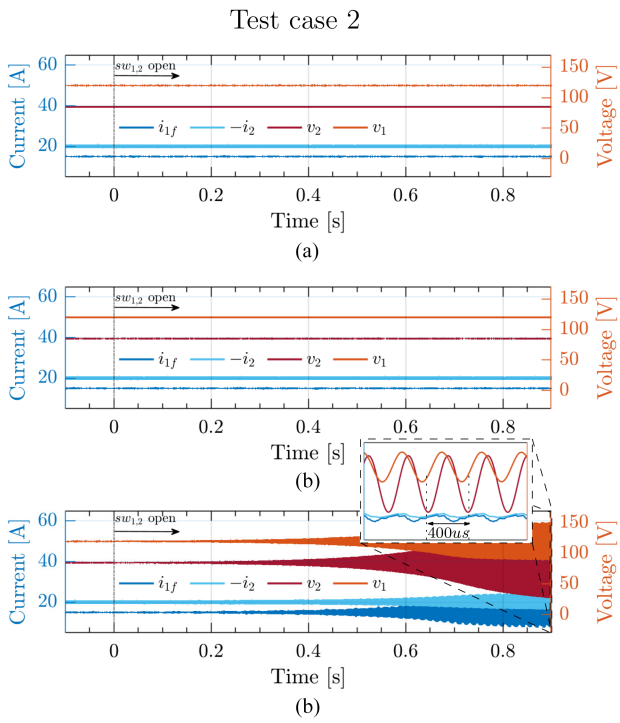

Fig. 7. Input and output current and voltage waveforms obtained from C-HIL simulations of the converter with the passivity properties from Fig. 4 (DS-PWM without the "feedforward"), operated in the grid-connecting scenarios from Fig. 5 with the grid's antiresonances' parameters corresponding to the test case 2. The transient is triggered by opening sw_{12} from Fig. 5 at $t = 0$ s. The results in (a), (b), and (c) correspond to the scenarios from Fig. 5(a), (b), and (c). For a better visualization, instead of i_1, i_{1f} is plotted, which is obtained by filtering out the switching ripple from i_1.

made passivity-based stability predictions are in agreement with the time domain stability tests. Furthermore, the frequencies of the resulting oscillations correspond to the grid's antiresonant frequencies.

As for the test case 2, the following passivity-based stability predictions can be made based on the results from Fig. 4. Namely, since both (6) and (7) are satisfied around $f''_{g1res} \approx f''_{g2res}$, regardless of how low the grid's damping around $f''_{g1res} \approx f''_{g2res}$ is, the system should remain stable in the scenarios from Fig. 5(a) and (b). However, despite (6) and (7) being satisfied, given that (8) is not satisfied around $f''_{g1res} \approx f''_{g2res}$, the instability is expected to arise in the scenario from Fig. 5(c), once the grid's damping around $f''_{g1res} \approx f''_{g2res}$ is reduced below a certain value. To verify this, C-HIL time domain stability tests are performed, similarly as above. For the grid's antiresonances' parameters corresponding to the test case 2, the converter's waveforms in response to the transients triggered by opening the switches $sw_{1,2}$ are shown in Fig. 7(a), (b), and (c) for the scenarios from Fig. 5(a), (b), and (c), respectively. As expected, the system remains stable in the scenarios when the grid features the antiresonance at a single port only. On the contrary, in the scenario when the grid features the antiresonances at both ports, the port-coupling induced instability arises. The risk for it was successfully predicted by the proposed, unterminated all-port MIMO admittance passivity-based method. Note that, though such a risk could have also been predicted by evaluating the passivity of the terminated admittance at the port of interest, this, as explained in [27], requires having the information about the termination at the other port(s), which may not be available and can also significantly vary during grid operation.

F. Impact of Control Loop's Parameters

To prevent the instabilities that may arise in the grid-connecting scenarios, such as those analyzed above, the MIMO admittance passivity properties should be enhanced in the frequency ranges critical for stability. Along this line, it is of interest to understand first what the MIMO admittance passivity properties depend on. In principle, these properties depend on all the parameters that figure out in Y_{11}–Y_{21} from (14)–(17). For the control system without the "feedforward" action, some of the parameters relevant for these dependencies are the current reference I_{2r}, the duty cycle D, the control loop's crossover frequency f_{cr} and the total delay τ_D present in the control loop, which can be due to modulation, computation, sensing and driving circuits, filters, etc. [39]. In this section, the dependence of the converter's all-port MIMO admittance passivity properties P_1, P_2, and P_{12} on the last two of these parameters (f_{cr} and τ_D) is investigated. For this, a simplified s-domain representation of the system from Fig. 2 without the "feedforward" action is used. It involves representing all the elements that introduce the

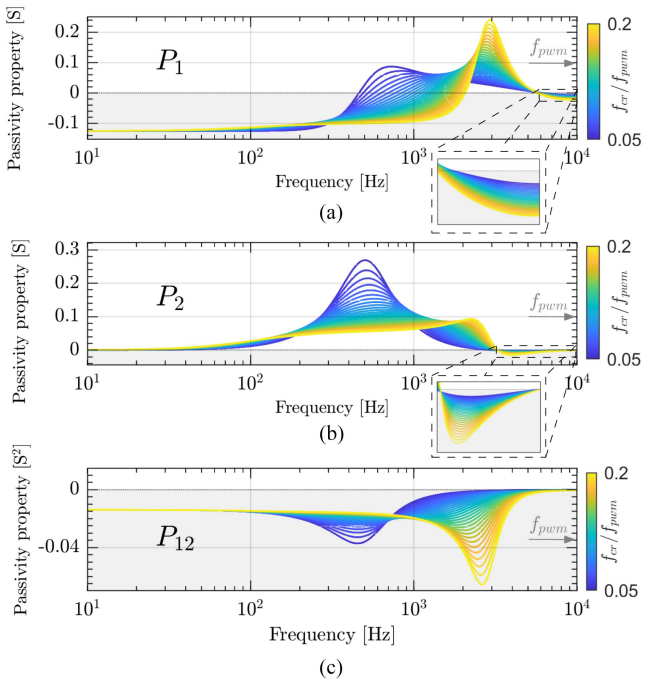

Fig. 8. Passivity properties (a) P_1, (b) P_2, and (c) P_{12} of the current-controlled buck converter from Fig. 2 ($G_{\text{ff}} = 0$) as a function of the control loop's crossover frequency (for a fixed $\tau_D = \frac{3}{4}T_{\text{pwm}}$). The results are obtained from the simplified s-domain analytical model, which involves representing all the delay elements as a lumped delay τ_D in the direct path.

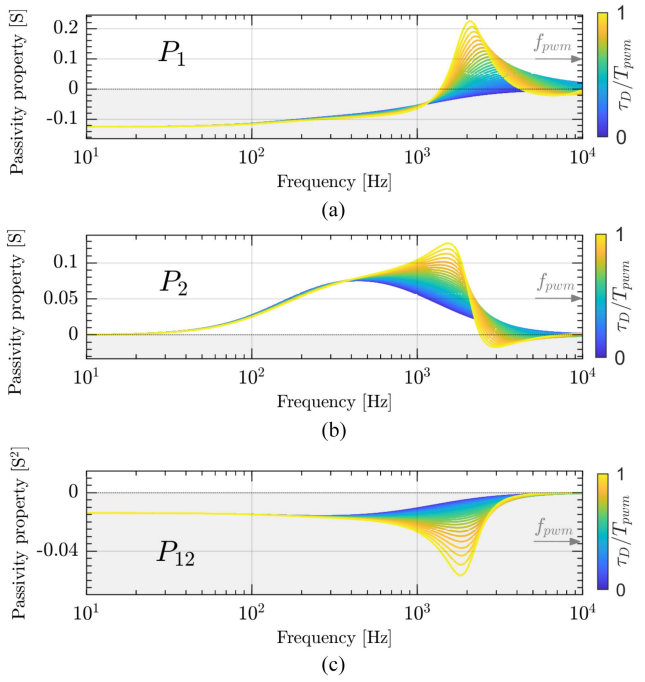

Fig. 9. Passivity properties (a) P_1, (b) P_2, and (c) P_{12} of the current-controlled buck converter from Fig. 2 ($G_{\text{ff}} = 0$) as a function of the control loop's delay (for a fixed $f_{\text{cr}} = 0.14f_{\text{pwm}}$). The results are obtained from the simplified s-domain analytical model, which involves representing all the delay elements as a lumped delay τ_D in the direct path.

delay in the control loop as a lumped delay τ_D in the direct path. Using the above described simplified analytical model, the passivity properties (9), (10), and (11) are calculated for different values of f_{cr} and τ_D.

First, the crossover frequency is swept from $0.05f_{\text{pwm}}$ to $0.2f_{\text{pwm}}$, while the delay is kept constant at $\tau_D = \frac{3}{2}\frac{T_{\text{pwm}}}{2}$. This value of τ_D is adopted as it corresponds to the standardly used single-rate control (without digital feedback filters) that involves DS-PWM and one-step computational delay. The other relevant parameters are the same as in Table I. The results for P_1, P_2, P_{12} are shown in Fig. 8(a), (b), and (c), respectively. As can be seen, the width of the first, low-frequency, active region of P_1 is lower for lower values of f_{cr}, which is a well-known property of the converter's negative input resistance behavior [6]. The negative dip of the second, high-frequency, active region of P_1 is also lower for lower values of f_{cr}. The same holds for the negative dip of the high-frequency active region of P_2, which is in agreement with the results from [13]. As for the impact of f_{cr} on P_{12}, reduction of f_{cr} reduces the width of the active region. The high-frequency negative dip is also reduced. Still, the low-frequency negative dip starts to arise for very low values of f_{cr}. Overall, according to the above outlined remarks, reduction of f_{cr}, i.e., control loop's bandwidth, can be considered beneficial for enhancing converter's all-port MIMO admittance passivity. However, by reducing f_{cr}, the control loop's primary function, i.e., regulation capability, is degraded, which can be acceptable only in some applications and only up to a certain extent. Thus, alternative methods for enhancing all-port MIMO admittance passivity should be investigated, which is addressed in Section IV.

To illustrate dependence of the converter's passivity properties on the delay, τ_D is swept from[3] 0 to T_{pwm}, while the crossover frequency is kept constant at $f_{\text{cr}} = 0.14f_{\text{pwm}}$, which yields a 48° phase margin for DS-PWM with one step computation delay. The other relevant parameters are the same as in Table I. The results for P_1, P_2, P_{12} are shown in Fig. 9(a), (b), and (c), respectively. As seen, τ_D has negligible impact at lower frequencies, while it significantly impacts the high frequency passivity. By reducing τ_D, the width of the first active region of P_1 is increased. Nevertheless, the second active region of P_1 can be completely eliminated by reducing τ_D. The same holds for the high-frequency active region of P_2, which is a well-known property of the converter's output admittance [13], [14]. Reduction of τ_D has positive impact on the coupling passivity property P_{12} as well, since its negative dip is reduced. Given all of the above mentioned, it can be concluded that the delay reduction enhances high-frequency all-port MIMO admittance-passivity. Furthermore, the delay reduction is also beneficial from the control loop's dynamic performance point-of-view, since, for the same crossover frequency, the lower delay yields the higher phase margin [32], [33]. This delay reduction is effectively obtained using MS-PWM, as addressed in the following section.

[3]Very low values of τ_D, which are close to 0, may be present in digital applications with MS-PWM, delay compensators (predictors), etc., as well as with analog control.

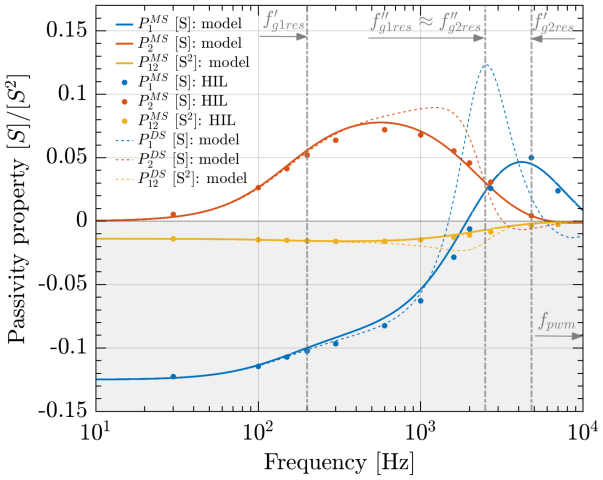

Fig. 10. Unterminated all-port MIMO admittance passivity properties (9), (10), and (11) of the buck converter with parameters from Table I and single-rate control from Fig. 2 with MS-PWM ($N_c = N_s = 4$), with neither feedback filters ($G_{fil} = 1$) nor "feedforward" action ($G_{ff} = 0$). The results obtained from C-HIL simulation (dots) and analytical model (full lines) are shown. Dashed lines correspond to the analytical results from Fig. 4.

TABLE II
OVERVIEW OF THE CONTROL-HARDWARE-IN-THE-LOOP TIME DOMAIN STABILITY TEST RESULTS

	Test scenario	DS-PWM	MS-PWM	DS-PWM with "FF"	MS-PWM with "FF"
test-case 1	f'_{g1res}	unstable	unstable	stable	stable
	f'_{g2res}	unstable	stable	unstable	stable
	f'_{g1res} & f'_{g2res}	unstable	unstable	unstable	stable
test-case 2	f''_{g1res}	stable	stable	stable	stable
	f''_{g2res}	stable	stable	stable	stable
	f''_{g1res} & f''_{g2res}	unstable	stable	unstable	stable

IV. Methods for Enhancing All-Port MIMO Admittance Passivity

A. Multisampled Pulse Width Modulation (MS-PWM)

The positive impact of MS-PWM on the high-frequency passivity of the converter's output admittance Y_{22}, which is described by P_2, is well-documented in the literature [13], [14]. Nevertheless, its positive impact on the converter's unterminated all-port MIMO admittance passivity has not been reported before. To illustrate this, the system from Fig. 2 that involves a single-rate control with MS-PWM ($N_c = N_s = 4$) with neither the feedback filters nor the "feedforward" action is considered. The parameters from Table I are used. The passivity properties P_1, P_2, and P_{12} of such a system are plotted in Fig. 10. As before, the frequency responses obtained from the analytical model (full lines) and C-HIL simulations (dot markers) are shown, and, as seen, an excellent match between them is achieved. In addition, the analytically obtained passivity properties corresponding to the previously analyzed system with DS-PWM (shown with full lines in Fig. 4) are also shown in Fig. 10 (with dashed lines). As seen, by reducing digital delays, at high frequencies MS-PWM significantly reduces negativity of not only P_2, but also P_1 and P_{12}. As such, MS-PWM can be considered beneficial for enhancing the converter's unterminated all-port MIMO admittance passivity at high frequencies.

To further elaborate on this, the stability in the grid-connecting scenarios from Fig. 5 is discussed next, considering the same test-cases and the grid's antiresonances' parameters as in Section III-E. Since, contrary to DS-PWM, with MS-PWM (7) is satisfied around f'_{g2res}, for the test case 1, the stability should be guaranteed in the scenario from Fig. 5(b). Furthermore, since, compared to DS-PWM, the coupling passivity property P_{12} is considerably enhanced with MS-PWM (its negative dip is lower) around $f''_{g1res} \approx f''_{g2res}$, for the test case 2, the system is less prone to getting destabilized in the scenario from Fig. 5(c). Then, provided that the grid's positive damping is higher than the converter's remaining negative damping around $f''_{g1res} \approx f''_{g2res}$, the port-coupling instability can be prevented. As for the rest of the scenarios and test cases from Section III-E, stability with MS-PWM should remain the same as with DS-PWM.

To validate this, the time domain stability tests are performed using C-HIL, where the transient is triggered by reducing the grid's damping, as in Section III-E. The plots of the converter waveforms in response to such transients are not included due to space limitations, but the overview of the results is provided in Table II. As seen, MS-PWM successfully prevents the high frequency instabilities that arise with DS-PWM, which is in agreement with the above discussed passivity-based stability predictions, derived from the proposed method. Not only is the instability caused by solely the interactions at the second port [test case 1, scenario from Fig. 5(b)] prevented by MS-PWM, but so is the port-coupling induced instability [test case 2, scenario from Fig. 5(c)].

Therefore, due to its capability to enhance the converter's unterminated all-port MIMO admittance passivity at high frequencies, MS-PWM can be considered very effective for preventing the converter's high-frequency destabilizing interactions with the grid. Note that similar properties are expected with other low phase-delay modulators, such as double-sampled asymmetric dual-edge modulator [43]. Nevertheless, since the converter's active behavior at lower frequencies is not caused by the delays, digital delay reduction methods, on their own, do not have the capability to enhance the low-frequency passivity. For this, alternative methods are needed, one example of which is addressed below.

B. "Feedforward"-Based Damping Impedance Emulation

The positive "feedforward"-based damping impedance emulation has been proposed in [12] as an effective method for enhancing the converter's input admittance in a bandlimited low-frequency range. The idea behind using the "feedforward" action, marked in gray color in Figs. 2 and 3, for emulating the damping impedance at the converter's input can be explained as

follows. According to (14), $Y_{11}(s)$ can be written as

$$Y_{11}(s) = Y_{11}^{\text{noff}}(s) + Y_{11}^{\text{vi}}(s) = Y_{11}^{\text{noff}}(s) + \frac{1}{Z_{\text{vi}}(s)} \tag{18}$$

where

$$Y_{11}^{\text{noff}}(s) = \frac{1}{1+T(s)}\left(-\frac{DI_{2r}T(s)}{V_1} + G_l(s)D^2\right) \tag{19}$$

is the converter's unterminated input admittance without the "feedforward" action, while

$$Y_{11}^{\text{vi}}(s) = \frac{G_{\text{ff}}(s)G_{\text{pwm}}(s)}{1+T(s)}\left(G_l(s)D + \frac{I_{2r}}{V_1}\right) \tag{20}$$

is the unterminated admittance's part added by the "feedforward" action. Accordingly, the contribution of the input-voltage "feedforward" action can be seen as an additional parallel damping impedance Z_{vi} at the converter's input port.

In the presence of nonzero grid's impedance at the converter's input port (such as Z_{g11}), the "feedforward" action may have the negative impact on the performance of the main feedback control loop [12]. To minimize this, it is of interest to choose $Z_{\text{vi}}(s)$ so that its impact is limited only within the narrow frequency range that is critical for stability [12]. As elaborated in [12], this can be achieved if the virtual damping impedance $Z_{\text{vi}}(s)$ exhibits the structure of the series RLC circuit

$$Z_{\text{vi}}(s) = R_{\text{vi}} + sL_{\text{vi}} + \frac{1}{sC_{\text{vi}}} \tag{21}$$

where R_{vi}, L_{vi}, and C_{vi} can be chosen to achieve the desired damping in the desired frequency range. This involves setting the appropriate values of the resonant frequency, quality factor, and characteristic impedance [35] that the resonance formed by R_{vi}, L_{vi}, and C_{vi} shall satisfy. The "feedforward" action, through which the desired damping impedance $Z_{\text{vi}}(s)$ can be emulated, can be calculated from (20)

$$G_{\text{ff}}(s) = \frac{1 + G_c(s)G_l(s)}{\left(G_l(s)D + \frac{I_{2r}}{V_1}\right)Z_{\text{vi}}(s)}. \tag{22}$$

Along this line, a few aspects should be noted. First, to ensure the desired damping performance despite possible variation of D, L_c, R_c, and other parameters, adaptive control may have to be employed. Second, all the delay-like elements (such as modulation, computation, or feedback filtering) are neglected in (22), to make the practical realization of $G_{\text{ff}}(s)$ feasible. With such a virtual damping design approach, which is used in this article as an example, depending on the desired frequency range for the virtual damping impedance emulation (the resonant frequency of Z_{vi} from (21)), the emulated virtual damping impedance's frequency response will differ from the desired one (described by (21)), to an extent determined by the amount of the delays present within the control loop. Thus, unless combined with some delay reduction methods, the resonant frequency of Z_{vi} from (21) should be kept below frequencies where delays significantly change phase of the system. Next, unless combined with some online resonance detection algorithm and adaptive control [44], the "feedforward" method will be effective only if the frequency range where the damping is needed does not change significantly. Finally, for the implementation within a digital control system, $G_{\text{ff}}(s)$ should be discretized to obtain $G_{\text{ff}}(z)$, for which the pole–zero matching discretization method is used in this article.

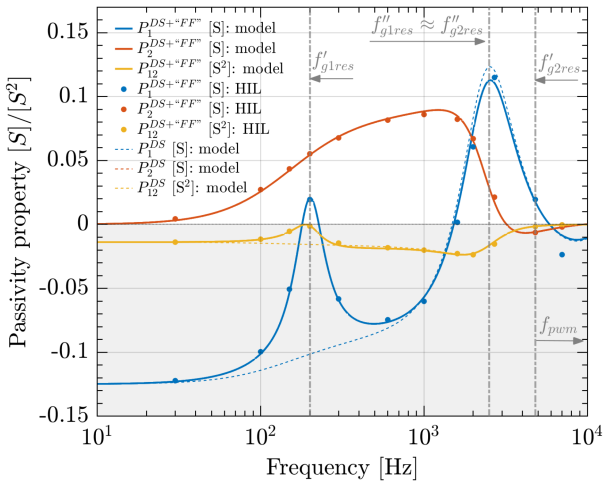

Fig. 11. Unterminated all-port MIMO admittance passivity properties (9), (10), and (11) of the buck converter with parameters from Table I and single-rate control from Fig. 2, without feedback filters ($G_{\text{fil}} = 1$), with DS-PWM ($N_c = N_s = 2$) and the "feedforward" action (from (22)). The results obtained from C-HIL simulations (dots) and analytical model (full lines) are shown. Dashed lines correspond to the analytical results from Fig. 4.

Though reported as effective for enhancing passivity of the converter's input admittance [12], the capabilities of the above described control method to enhance the converter's unterminated all-port MIMO admittance passivity have not been explored in the literature so far. Along this line it should be mentioned first that, since the "feedforward" action affects not only Y_{11}, but also Y_{21}, it impacts both P_1 and P_{12}. Still, according to (14) and (17), this impact is "of opposite sign." Accordingly, though the lower R_{vi} always enhances P_1, this does not necessarily hold for P_{12}. Thus, care has to be taken when designing the feedforward action to ensure enhancement of both P_1 and P_{12}. Research along this line is left for future.

As an example that illustrates the impact of the "feedforward" action on the all-port MIMO admittance passivity, the system from Fig. 2 that involves a single-rate control with DS-PWM ($N_c = N_s = 2$) without feedback filters and with the "feedforward" action is considered. Same as before, the parameters of the converter and the main feedback current control loop from Table I are used. The "feedforward" action is designed so that the virtual damping impedance (21) ensures passivity of Y_{11} around f'_{g1res}, which corresponds to the standard input admittance passivity-oriented design [12].

The passivity properties P_1, P_2, and P_{12} of such a system are plotted in Fig. 11. As before, the frequency responses obtained from the analytical model and C-HIL simulations are shown. In addition, the analytically obtained passivity properties corresponding to the system with DS-PWM and without the "feedforward" action (analyzed in Section III-C) are also shown in Fig. 11, for comparison. As seen, the addition of the

"feedforward" action enhances passivity around f'_{g1res} of not only P_1, but also P_{12}.

To further elaborate on the impact of the "feedforward" action on the converter's admittance passivity, the stability in the grid-connecting scenarios from Fig. 5 is discussed next, considering the same test-cases and the grid's antiresonances' parameters as in Section III-E. Contrary to DS-PWM without the "feedforward" action, for DS-PWM with the "feedforward" action, (6) is satisfied around f'_{g1res}. Thus, for the test case 1, stability should be guaranteed in the scenario from Fig. 5(a). However, by adding the "feedforward" action P_2 and P_{12} remain unaltered around f'_{g2res} and $f''_{g1res} \approx f''_{g2res}$, respectively. Therefore, same as the system with DS-PWM and without the "feedforward" (Section III-C), the system with DS-PWM and the "feedforward" action is expected to be destabilized in the scenarios from Fig. 5(b) and (c), for test case 1, and in the scenario from Fig. 5(c), for test case 2.

To validate this, the time domain stability tests are performed using C-HIL, where the transient is triggered by reducing the grid's damping, as in Section III-E. The plots of the converter waveforms in response to such transients are not included due to space limitations, but the overview of the results is provided in Table II. As predicted, the addition of the input voltage "feedforward" action successfully prevents the instability from Fig. 6(a), which is caused by the low-frequency active region of Y_{11}. Nevertheless, as discussed above, the high-frequency destabilization issues from Fig. 6(b) and (c), as well as Fig. 7(c) are not solved by adding the input-voltage "feedforward" action (see Table II). This is because the "feedforward"-based damping impedance emulation is in the considered example intentionally designed as a low-frequency bandpass action (in this case around f'_{g1res}), to limit its negative impact on the main control loop and achieve the desired damping action in presence of nonnegligible digital delays. Furthermore, this method does not alter Y_{22} at all, as seen from (15). Therefore, with the goal of enhancing the converter's unterminated all-port MIMO admittance passivity simultaneously at low- and high-frequencies, it may be of interest to combine the input voltage "feedforward"-based damping impedance emulation with other methods, like MS-PWM, which is addressed below.

C. Combination of MS-PWM and the "feedforward"

In this subsection, the system from Fig. 2 that involves a single-rate control with MS-PWM ($N_c = N_s = 4$) without feedback filters and with the "feedforward" action is considered. Same as before, the parameters of the converter and the main feedback current control loop from Table I are used, while the parameters of the "feedforward" action are the same as in Section IV-B. The passivity properties P_1, P_2, and P_{12} of such a system, obtained from the analytical model and C-HIL simulations, are plotted in Fig. 12, again benchmarked against the case of DS-PWM without the feedforward action. As seen, the "feedforward" action and the MS-PWM act independently, enhancing thereby the converter's unterminated all-port MIMO admittance passivity in the two distinct frequency ranges. The

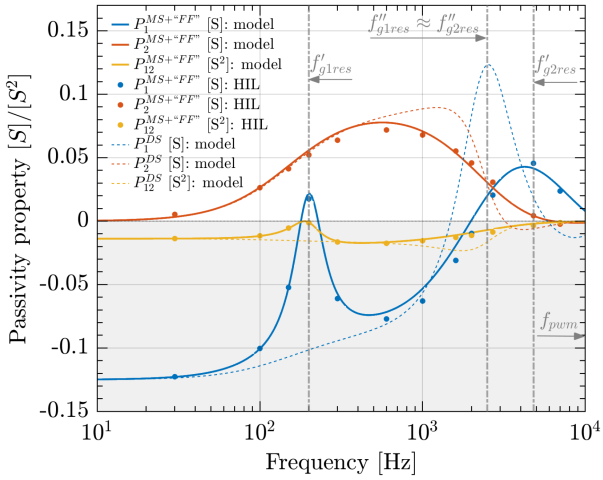

Fig. 12. Unterminated all-port MIMO admittance passivity properties (9), (10), and (11) of the buck converter with parameters from Table I and single-rate control from Fig. 2, without feedback filters ($G_{\text{fil}} = 1$), and with both MS-PWM ($N_c = N_s = 4$) and the "feedforward" action (from (22)). The results obtained from C-HIL simulations (dots) and analytical model (full lines) are shown. Dashed lines correspond to the analytical results from Fig. 4.

former contributes to P_1 and P_{12} becoming positive at low frequencies, specifically around f'_{g1res} for the considered design of the "feedforward" action. The latter contributes to improving P_1, P_2, and P_{12} at high-frequencies (which includes f'_{g2res} and $f''_{g1res} \approx f''_{g2res}$). Thus, all the instabilities (from Figs. 6 and 7) that the system with DS-PWM and without the "feedforward" action was causing in the grid-connecting scenarios from Fig. 5 are expected to be successfully overcome by using MS-PWM and the "feedforward" action. To demonstrate this, time-domain stability tests using C-HIL are performed. The transient is triggered by reducing the grid's damping, same as before.

The converter's input and output current and voltage waveforms in response to such transients are shown in Figs. 13 and 14 for the test case 1 and 2, respectively. Compared to the results from Figs. 6 and 7, obtained for DS-PWM without the "feedforward" action, by using MS-PWM with the "feedforward" action, not only are the instabilities caused by, respectively, low- and high-frequency nonpassive regions of Y_{11} and Y_{22} successfully prevented, but so is the port-coupling induced instability. As seen from Table II, where an overview of all the previously discussed time-domain stability test results is provided, only by using both MS-PWM and the "feedforward" action is the stability ensured in all considered grid-connecting scenarios and test-cases. It is worth mentioning that, as opposed to the above discussed independent action of the MS-PWM and the "feedforward" in the two distinct frequency ranges, these methods can also be combined in a way to act jointly in the same frequency range (e.g., near or slightly above f_{cr}). Research along this line is left for future studies. Finally, depending on the properties of the grid under study, i.e., the frequency ranges where it exhibits (anti)resonances, use of only one of the above discussed methods may be sufficient. One such application example is considered for the experimental validation in Section V.

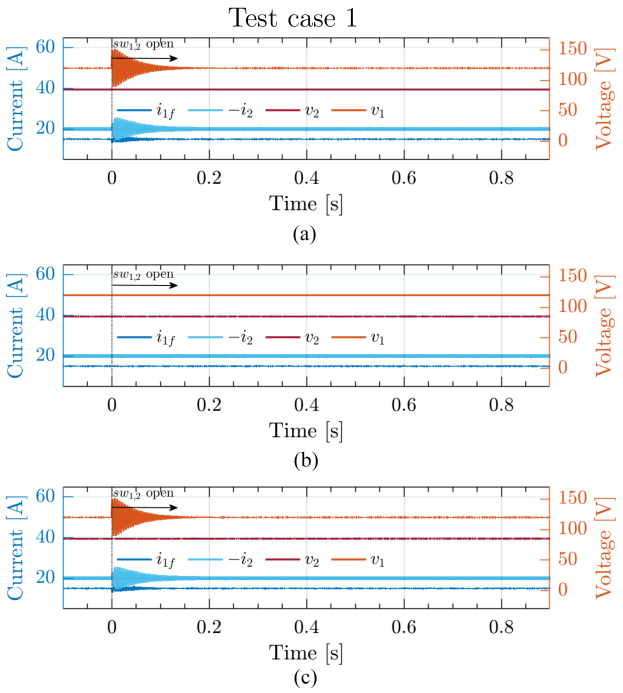

Fig. 13. Input and output current and voltage waveforms obtained from C-HIL simulations of the converter with the passivity properties from Fig. 12 (MS-PWM with the "feedforward"), operated in the grid-connecting scenarios from Fig. 5 with the grid's antiresonances' parameters corresponding to the test case 1. The transient is triggered by opening sw_{12} from Fig. 5 at $t = 0$ s. The results in (a), (b), and (c) correspond to the scenarios from Fig. 5(a), (b), and (c). For a better visualization, instead of i_1, i_{1f} is plotted, which is obtained by filtering out the switching ripple from i_1.

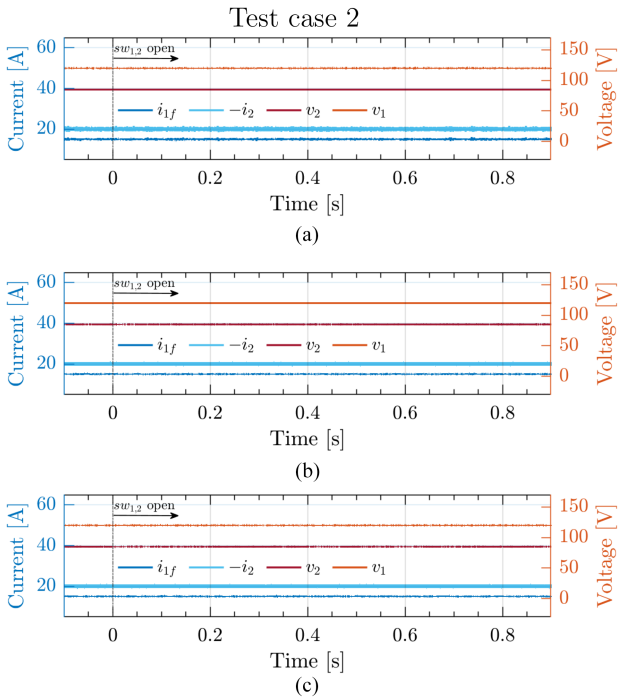

Fig. 14. Input and output current and voltage waveforms obtained from C-HIL simulations of the converter with the passivity properties from Fig. 12 (MS-PWM with the "feedforward"), operated in the grid-connecting scenarios from Fig. 5 with the grid's antiresonances' parameters corresponding to the test case 2. The transient is triggered by opening sw_{12} from Fig. 5 at $t = 0$ s. The results in (a), (b), and (c) correspond to the scenarios from Fig. 5(a), (b), and (c). For a better visualization, instead of i_1, i_{1f} is plotted, which is obtained by filtering out the switching ripple from i_1.

TABLE III
PARAMETERS OF THE BUCK CONVERTER USED IN EXPERIMENTS

Parameter	Label	Value	Unit
Input dc voltage	V_{g1}	48	V
Output dc voltage	V_{g2}	36	V
Output dc current	I_{2r}	20	A
Steady-state duty cycle	D	0.85	V
Filter inductance	L_c	1.5	mH
Filter inductor's resistance	R_{L_c}	0.25	Ω
Switching frequency	f_{pwm}	5	kHz
Dead time	t_{dt}	0.8	μs
Multi-sampling factor	N_s	10	–
Feedback sampling frequency	f_s	50	kHz
Control-update factor	N_c	$\{2, 10\}$	–
Control update frequency	f_c	$\{10, 50\}$	kHz
Crossover frequency	f_{cr}	1	kHz
Phase margin[4]	PM	$\{15, 27\}$	°

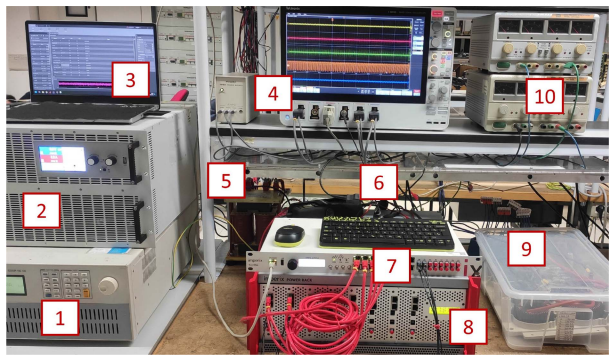

Fig. 15. Picture of the test-setup for experimental validation: 1) input DC power supply Chroma 62050P-100-100; 2) electronic load EA-EL 9750-120; 3) laptop; 4) Tektronix MS056 oscilloscope; 5) filter inductor; 6) capacitors for the grid's antiresonances; 7) B-Box control platform; 8) PEB8024 half-bridge modules; 9) inductors for the grid's antiresonances and perturbation injection; 10) power supplies GW GPC-3030 for perturbation injection.

V. EXPERIMENTAL VALIDATION

A. System Under Test

In this section, experimental validation of the previously analyzed phenomena is presented. For this, the test-setup from Fig. 15 is used, which features a digital current-controlled buck converter with the parameters from Table III. The converter is realized using the half bridge modules PEB8024 from Imperix

[4]The phase margin values are lower than typically targeted due to the control loop's total delay τ_D and crossover frequency f_{cr} both being high. High τ_D is due to the feedback filters, which are added to suppress the detrimental impact of the switching noise [38]. High f_{cr} was necessary to trigger the port-coupling induced instability due to very large parasitic resistances of the LC elements used to form the grid's antiresonances (see Section V-C).

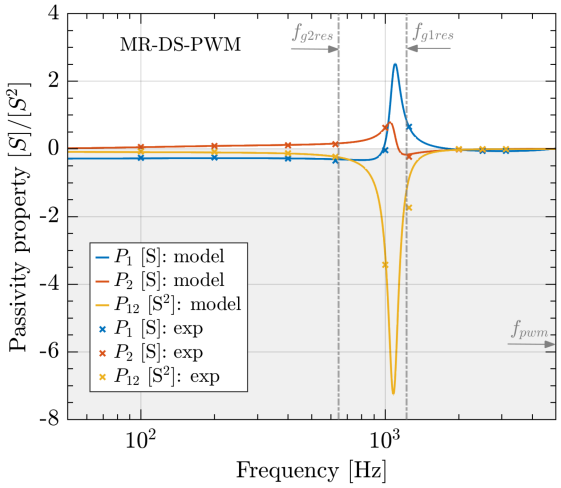

Fig. 16. Unterminated all-port MIMO admittance passivity properties (9), (10), and (11) of the buck converter with parameters from Table III and multirate control system from Fig. 2 ($G_{\text{ff}} = 0$) that involves MR-DS-PWM with $N_c = 2$, $N_s = 10$, and the feedback filtering from [38]. Results obtained experimentally (crosses), using the setup from Fig. 15, and analytically (full lines) using the model from Section III-B, are shown.

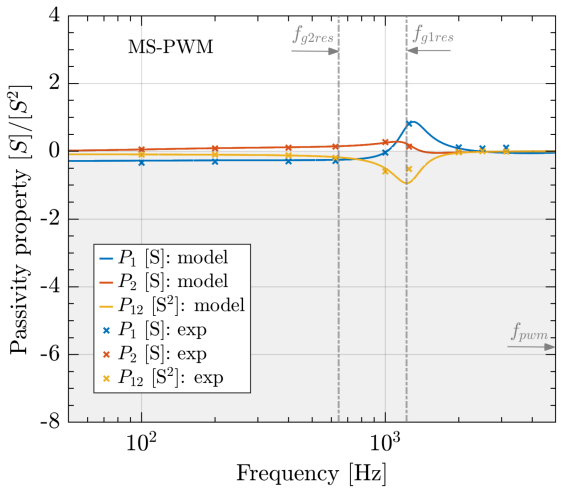

Fig. 17. Unterminated all-port MIMO admittance passivity properties (9), (10), and (11) of the buck converter with parameters from Table III and single-rate control system from Fig. 2 ($G_{\text{ff}} = 0$) that involves MS-PWM with $N_c = N_s = 10$, and the feedback filtering from [38]. Results obtained experimentally (crosses), using the setup from Fig. 15, and analytically (full lines) using the model from Section III-B, are shown.

and an external inductor. The dc voltages at the converter's input and output ports are provided by the dc power supply Chroma 62050P-100-100 and the electronic load EA-EL 9750-120 B. The inductor current is sensed by the current sensor LEM CKSR 50-P and the digital control is realized on B-Box rapid prototyping control platform from Imperix.

Two different control system architectures are tested, both corresponding to Fig. 2 without the "feedforward" action and with the digital feedback filtering from [38]. The latter, which was necessary in order to prevent the deteriorating impact of the switching noise, involves the cascade of a repetitive ripple removal and median filter [38]. The first tested architecture involves a multirate control with DS-PWM ($N_s = 10$ and $N_c = 2$), hereafter referred to as MR-DS-PWM [32], [38]. As explained in Section II-A and illustrated in Fig. 2, in such an architecture, the feedback signal is first oversampled at the rate $f_s = 10 f_{\text{pwm}}$, then filtered, and finally decimated to $f_c = 2 f_{\text{pwm}}$ [32], [38]. The second control system architecture involves a single-rate control with MS-PWM ($N_s = N_c = 10$), hereafter referred to as MS-PWM. Same as for C-HIL validations, the PI controller was used for both experimentally tested control system architectures.

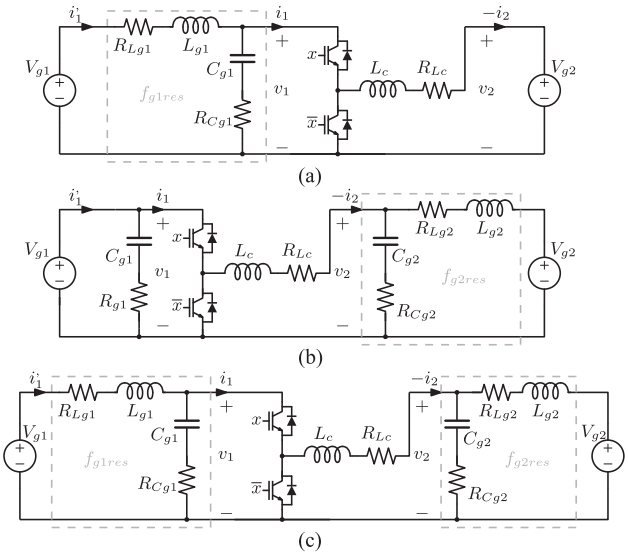

Fig. 18. Grid-connecting scenarios used to experimentally validate the passivity-based instability risk predictions derived from the converters' unterminated all-port MIMO admittance passivity properties of Figs. 16 and 17. The grid features antiresonance at (a) port 1, (b) port (2), (c) both ports.

B. Frequency Response Measurements

First, it was of interest to characterize the system in the frequency domain, by obtaining $P_1(j\omega)$, $P_2(j\omega)$, and $P_{12}(j\omega)$ from the experimentally measured frequency responses $Y_{11}(j\omega)$, $Y_{12}(j\omega)$, $Y_{21}(j\omega)$, and $Y_{22}(j\omega)$. For this, the measurement procedure from [27] is used. It involves injecting a sinusoidal perturbation current, independently at the converter's input and output, and collecting the corresponding current and voltage waveforms of interest using Tektronix MS056 oscilloscope. The acquired data is imported in MATLAB where the Fast Fourier transform is performed to obtain $Y_{11}(j\omega)$, $Y_{12}(j\omega)$, $Y_{21}(j\omega)$, and $Y_{22}(j\omega)$. Finally, $P_1(j\omega)$, $P_2(j\omega)$, and $P_{12}(j\omega)$ are calculated using (9), (10), and (11). The resulting MIMO admittance passivity properties for MR-DS-PWM and MS-PWM (both obtained with $I_{2r} = 20$ A) are shown in Figs. 16 and 17, respectively, with the same y axis scale to emphasize the passivity improvement brought by MS-PWM. In addition to the results obtained from the experimental frequency response measurements (shown with cross markers), the results obtained from the analytical model, discussed in Section III-B, are also plotted (with full lines). As seen, both for MR-DS-PWM and

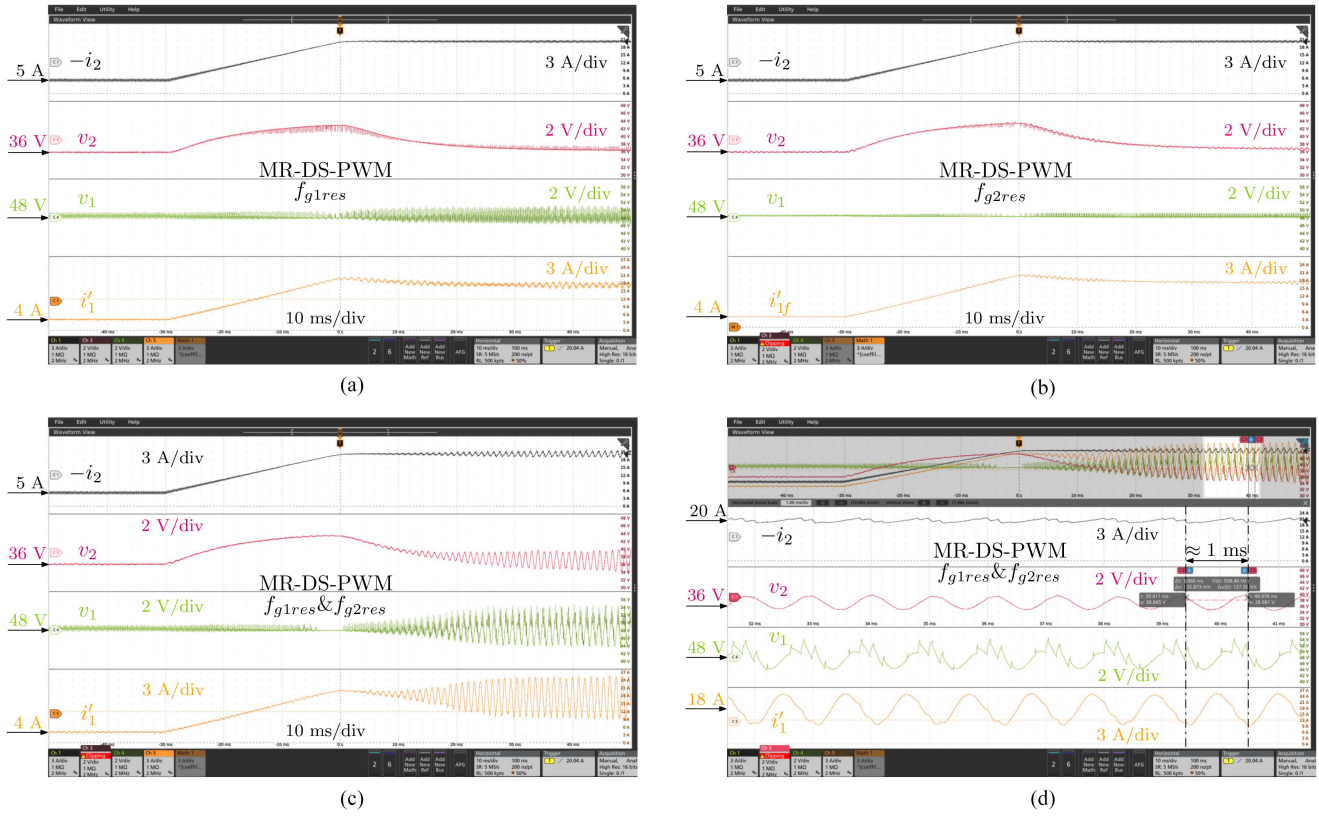

Fig. 19. Experimental stability test results in the grid-connecting scenarios from Fig. 18, for the converter with MR-DS-PWM and parameters from Table III. The waveforms are measured in response to the current reference ramp change from $I_{2r} = 5$ A to $I_{2r} = 20$ A. For $I_{2r} = 20$ A the converter is operated in the regime described by the passivity properties from Fig. 16. The results in (a), (b), and (c) correspond to the scenarios from Fig. 18(a), (b), and (c). In (b), for a better visualization, i'_{1f} is shown, which corresponds to i'_1 with the switching ripple removed by the oscilloscope math function. (d) Zoomed-in waveforms of the results from (c). The frequency at which the port-coupling induced instability seen in (c) and (d) arises corresponds to the frequency at which P_{12} from Fig. 16 exhibits the negative dip.

MS-PWM, the trends of the experimentally and analytically obtained results are in agreement.

C. Time-Domain Stability Tests

Next, based on the converter's all-port MIMO admittance passivity properties P_1, P_2, P_{12} from Figs. 16 and 17, it was of interest to examine the instability risk and experimentally test stability of the considered converter in the grid-connecting scenarios from Fig. 18, similarly as in Sections III-E and IV. For this, a nonmeshed grid is considered. Its dc bus voltages are formed by the same source and load as in Section V-A. The grid's impedances are formed by passive *LC* elements, such that they form parallel antiresonant circuits (see Fig. 18). The parameters of *LC* elements are the same as in [18], which yield the antiresonant frequencies at port 1 and at port 2 equal to, respectively, $f_{g1res} = 1200$ Hz and $f_{g2res} = 640$ Hz.

In Fig. 18(a) and (b), the antiresonance is present at a single port only. As explained in Sections III-D and III-E, in such scenarios, stability can be simply predicted by evaluating P_1 around f_{g1res} (for Fig. 18(a)) or P_2 around f_{g2res} [for Fig. 18(b)]. Since for P_1 and P_2 from Fig. 16, (6) and (7) hold, respectively, around f_{g1res} and f_{g2res}, the system with MR-DS-PWM, which is first analyzed, should remain stable in the scenarios from Fig. 18(a) and (b). Differently from the scenarios in Fig. 18(a) and (b), in the scenario from Fig. 18(c), the antiresonances are present at both ports. Thus, to accurately predict the risk for the instability, in this scenario, the coupling passivity property P_{12} must be evaluated as well. Given that P_{12} from Fig. 16 is negative around f_{g1res} and f_{g2res}, a risk for the port-coupling induced instability exists. Specifically, since the negative dip of P_{12} is pronounced around 1 kHz, in the scenario from Fig. 18(c) the system is prone to being destabilized at this frequency.

To verify these stability predictions, experimental time domain stability tests are performed in the following way. The converter is at first operated with $I_{2r} = 5$ A, which significantly reduces the negative dip of P_{12}, so that the grid's damping is sufficient to ensure stable operation also in the scenario from Fig. 18(c)[5]. The ramp change of the current reference is then imposed from $I_{2r} = 5$ A to $I_{2r} = 20$ A (the latter corresponding to the passivity properties from Fig. 16). The converter's input and output current and voltage waveforms in response to such a ramp reference change are shown in Fig. 19(a), (b), and (c) for the scenarios from Fig. 18(a), (b), and (c), respectively. As

[5]A more detailed stability analysis, which includes application of the generalized Nyquist criterion to the minor loop gain $\mathbf{L}$ (defined in Section II-A), can be found in [18].

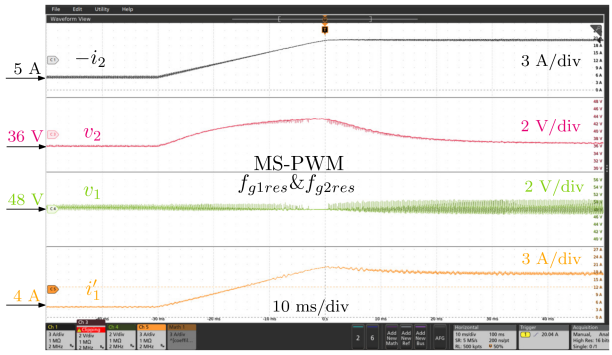

Fig. 20. Experimental stability test results in the grid-connecting scenario from Fig. 18(c) for the converter with MS-PWM and parameters from Table III. The waveforms are measured in response to the current reference ramp change from $I_{2r} = 5$ A to $I_{2r} = 20$ A. For $I_{2r} = 20$ A, the converter is operated in the regime described by the passivity properties from Fig. 17.

seen, the previously made passivity-based stability predictions are in agreement with the time domain stability tests. The port-coupling induced instability is clearly visible in Fig. 19(c). Furthermore, as seen from the corresponding zoomed in waveforms in Fig. 19(d), the frequency of the resulting oscillations is close to 1 kHz, which, as predicted, corresponds to the frequency where the coupling passivity property exhibits the negative dip. This is an important result which, for the first time, experimentally demonstrates that in order to guarantee stability in a passive grid, the converter's control system design should, at least in the frequency range that is critical for stability, strive for the all-port MIMO passivity (or, at least, its enhancement).

As discussed in Section IV, due to its inherent digital delay reduction property, MS-PWM can be very effective for enhancing the converter's all-port MIMO admittance passivity at high frequencies, and, consequently, for preventing the high-frequency port-coupling induced instability, such as one from Fig. 19(c) and 19(d). As seen from Fig. 17, the passivity properties obtained with MS-PWM are significantly improved at high frequencies compared to the ones (from Fig. 16) obtained with MR-DS-PWM. Specifically, the negative dip of the coupling passivity property P_{12} is considerably reduced with MS-PWM. Thus, in the scenario from Fig. 18(c), the system with MS-PWM is less prone to being destabilized than the system with MR-DS-PWM. Then, provided that the grid's positive damping is higher than the converter's remaining negative damping, the port-coupling instability can be prevented. As for the scenarios from Fig. 18(a) and (b) stability shall be retained also with MS-PWM, since, as in the case with MR-DS-PWM, P_1 and P_2 from Fig. 17, satisfy (6) and (7) around, respectively, f_{g1res} and f_{g2res}.

To verify this, time domain stability tests are performed for MS-PWM, in the same way as above for MR-DS-PWM. Stable response to the ramp reference change from $I_{2r} = 5$ A to $I_{2r} = 20$ A is achieved in all three scenarios from Fig. 18. Due to space limitations the results are shown in Fig. 20 only for the scenario from Fig. 18(c). As seen from Fig. 20, the instability from Fig. 19(c) and (d), that was observed with MR-DS-PWM, is successfully prevented by MS-PWM. This is an important results, which, for the first time, experimentally demonstrates the effectiveness of MS-PWM in preventing the port-coupling induced instability at high frequencies, thereby further enhancing the grid-connecting converter's stability. Note that this property of MS-PWM, achieved by its capability to improve the converter's all-port MIMO admittance passivity, is different from the one analyzed in [13] and [14], where the capability of MS-PWM to enhance only the converter's unterminated output admittance passivity was demonstrated.

VI. Conclusion

To analyze and prevent a dc–dc interlinking converter's destabilizing impact in grid-connecting scenarios with an arbitrary, even meshed, termination (grid impedance), this article presents the unterminated all-port MIMO admittance passivity-oriented controller design framework, exemplified through a buck converter with a digital current-control system. Impact of the control loop's crossover frequency and overall delay on its MIMO admittance passivity properties is illustrated, and a higher value of each parameter is indicated to worsen these properties. Along this line, examples of two techniques for enhancing a converter's all-port MIMO admittance passivity, by active damping impedance emulation and multisampled pulse width modulation, are investigated and shown to be effective. Both frequency and time domain validations of the presented methodology are performed, using C-HIL simulations, as well as experimentally, using a laboratory prototype. Future studies will focus on extending the presented methodology to ac–dc interlinking converters. In addition, future research could explore how to combine the methodology from this article with the methods for reducing the conservatism that may arise from the passivity-oriented controller design [45].

Appendix

Alternatively to evaluating the principal minors of $\mathbf{P}(j\omega)$, which is considered throughout the article, the eigenvalues of $\mathbf{P}(j\omega)$ can be evaluated to examine passivity of $\mathbf{Y}(s)$ [10], [30]. Namely, condition (5) is equivalent to all the eigenvalues of $\mathbf{P}(j\omega)$ (which are by definition real) being nonnegative [30]. This is further equivalent to the smallest of the eigenvalues being nonnegative. Accordingly, for $\mathbf{Y}(s)$ given by (1), the condition (5) is equivalent to

$$\lambda_{\min}(j\omega) \geq 0 \tag{23}$$

where

$$\lambda_{\min}(j\omega) = \frac{P_1(j\omega) + P_2(j\omega)}{2} - \frac{\sqrt{(P_1(j\omega) + P_2(j\omega))^2 - 2P_{12}(j\omega)}}{2}. \tag{24}$$

It is interesting to note that $\lambda_{\min}$ is in fact the input feedforward passivity index of $\mathbf{Y}(s)$ at the frequency ω [29], [42].

To illustrate the use of $\lambda_{\min}$ for characterizing the converter's all-port MIMO admittance passivity, a few examples, previously addressed via the principal minors-based approach, are addressed below via the minimum eigenvalue-based approach. First, $\lambda_{\min}$ of the current controlled buck converter analyzed in

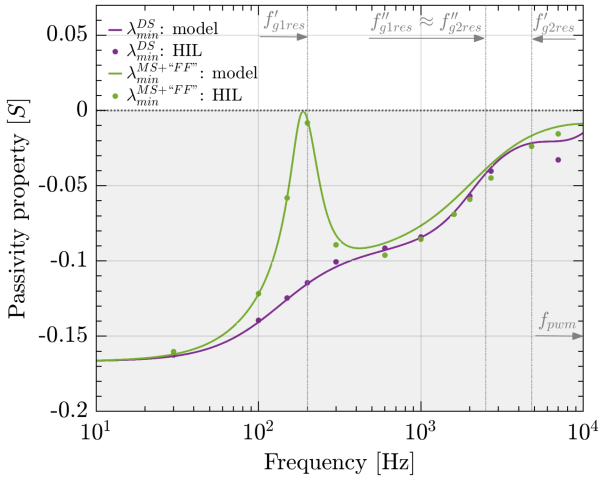

Fig. 21. Passivity property (24) of the buck converter with parameters from Table I and single-rate control system from Fig. 2 without feedback filters ($G_{\text{fil}} = 1$). The results shown in purple and green color correspond to those from Figs. 4 and 12, which are obtained for DS-PWM ($N_c = N_s = 2$) without the "feedforward" action and MS-PWM ($N_c = N_s = 4$) with the "feedforward" action, respectively. The results obtained from C-HIL simulations (dots) and analytical model (full lines) are shown.

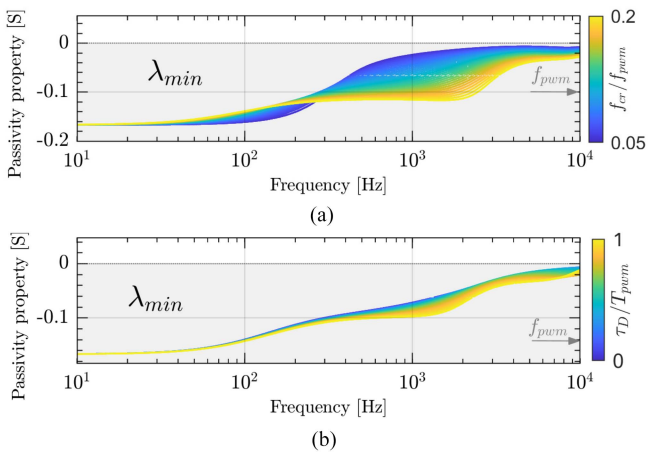

Fig. 22. Passivity property (24) of the current-controlled buck converter from Fig. 2 ($G_{\text{ff}} = 0$) as a function of (a) f_{cr} for $\tau_D = \frac{3}{4}T_{\text{pwm}}$ (which corresponds to the results from Fig. 8) and (b) of τ_D for $f_{\text{cr}} = 0.14 f_{\text{pwm}}$ (which corresponds to the results from Fig. 9). The results are obtained from the simplified s-domain analytical model, which involves representing all the delay elements as a lumped delay τ_D in the direct path.

Section III-C (featuring DS-PWM without the "feedforward" action) and Section IV-C (featuring MS-PWM with the "feedforward" action) are plotted in Fig. 21. Same as before, the results obtained from the analytical model are plotted with full lines and those obtained from C-HIL simulations are shown with dot markers. The results for λ_{min} shown in Fig. 21 in purple and green color correspond to those for P_1, P_2, and P_{12} shown in Figs. 4 and 12, respectively. As can be seen, the reasoning about the converter's MIMO admittance passivity that was made by evaluating P_1, P_2, and P_{12} is in agreement the trends of λ_{min}.

Next, similar as in Section III-F, dependence of λ_{min} on f_{cr} and τ_d is shown in Fig. 22(a) and (b), which corresponds to the results from Figs. 8 and 9, respectively. As seen, the reasoning about the impact of f_{cr} and τ_d on the all-port MIMO passivity that was made in Section III-F from the plots of P_1, P_2, and P_{12} is in agreement with the trends of λ_{min}. Still, compared to P_1, P_2, and P_{12}, λ_{min} seems to be less sensitive to variations of τ_d. Moreover, contrary to P_1, P_2, and P_{12}, λ_{min} provides limited physical insight on the converter's active behavior, e.g., whether it is related to the input port, the output port, or the coupling between them, etc. Nevertheless, the minimum eigenvalue-based approach may also be advantageous to use, as it characterizes the all-port MIMO admittance passivity by a single parameter only (also when the dimension of $\mathbf{Y}(s)$ is higher than 2, e.g., for multiport or ac–dc converters). A more detailed discussion about the strengths and weaknesses of the minimum eigenvalue-based, i.e., the input feedforward passivity index-based, and the principal minors-based approach for describing the converter's all-port MIMO admittance passivity is out of the scope of this article and is, therefore, left for future work. Finally, in order to provide more physical insight into the design process, the use of relative passivity index [46] should be explored in future studies.

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