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Simulation Study on Single-event Burnout Reliability of 900V 4H-SiC Quasi Vertical Double Diffused MOSFET

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ABSTRACT In this work, the single-event burnout (SEB) performance and reasons of the proposed 900V SiC quasi-vertical double diffusion MOSFET with deepened drain (T-QVDMOSFET) are analyzed from the spatial distribution of physical quantities such as power density, lattice temperature and total current density by 2-D numerical simulation, and a SEB-hardened structure (TB-QVDMOSFET) with buried oxygen layer (BOX) and heavily doped N-type current expansion layer (CSL) inside the device is proposed. Simulation results indicate that when heavy-ion with linear energy transfer (LET) of 0.5 pC/μm strikes the device, the primary cause of SEB in the SiC T-QVDMOSFET is the high transient current density and electric field at the trench gate corner. This phenomenon leads to increased power dissipation, resulting in excessive temperatures that ultimately cause thermal failure. The BOX and a heavily doped N-type CSL added in the SEB-hardened structure change the current flow path, and the transient current concentrated in the region is dispersed. This modification reduces the high current density and power dissipation at the trench corner, thereby significantly enhancing the device's resistance to SEB. Compared to the original device, the SEB threshold voltage is increased from 270V to 478V, marking a 77% improvement.

INDEX TERMS SiC, QVDMOSFET, single-event effect, SEB hardening.

I. INTRODUCTION

Silicon carbide (SiC) exhibits exceptional properties, including high thermal conductivity and superior breakdown electric field strength, making it an optimal material for high-power, high-frequency, and high-radiation applications [1-4]. Advancement of SiC integrated circuits (ICs) has facilitated the integration of control and power stages, enabling genuine high-temperature and high-voltage operation within compact packaging. Previous studies have proposed CMOS integrated circuits of 6H-SiC and 4H-SiC integrated circuits [5-7].

SiC MOSFET, known for their superior voltage blocking capability and faster switching speed, are anticipated to replace silicon insulated-gate bipolar transistors (IGBTs) in medium to low voltage and high-power applications [8]. High-voltage QVDMOSFET are commonly employed in gate driver ICs for high-voltage level shifting functions, rendering them the preferred choice for level shifting and driving modules in power integrated circuits [9].

In 2014, R.R. Lamichane and others proposed a SiC gate driver suitable for high temperature and high voltage applications [10]. In the same year, M. N. Ericson and others demonstrated a 4H-SiC integrated gate driver for power conversion applications [11]. In 2019, M. Barlow and others proposed an integrated SiC complementary metal oxide semiconductor (CMOS) gate driver for power module integration. The performance of the gate driver at the temperature as high as 470°C is verified by the high-temperature test device, which provides a reliable solution for high-temperature applications [12]. In 2014, Qing Hua et al. proposed an SOI-based high-voltage half-bridge IGBT gate driver IC for motor drive applications. The gate drive integrated circuit uses two high-voltage quasi-vertical double-diffused metal oxide semiconductor

(QVDMOS) transistors to realize the high-level shift function. The experimental results show that it has excellent characterization at 650V, requires very low quiescent current and provides high gate driver capability [9]. SiC QVDMOSFET has great potential in high performance gate drive IC. SiC QVDMOSFET discrete devices offer distinct advantages in high-voltage, high-frequency, and high-temperature environments.

GE [13-15] has concentrated on the development and systematic validation of 1.2kV to 3.3kV SiC MOSFETs for aerospace and industrial applications, achieving notable progress toward demonstrating reliability on par with mature silicon IGBTs [16]. The 1.2kV MOSFET has already seen early adoption in aerospace applications [15]. However, integrated circuits (ICs) used in aerospace applications face significant challenges in extreme environments, such as space radiation, where protons, ions, neutrons [17], and other particles can induce various radiation effects on power devices. Among these, SEB is a major catastrophic radiation effect, leading to permanent damage to power devices [18], [19]. SiC MOSFETs are particularly vulnerable to SEB, often failing at blocking voltages less than 50% of their rated voltage, thereby limiting their ability to meet the stringent performance requirements of aerospace applications [20], [21].

The SiC T-QVDMOSFET device examined in this paper utilizes a trench gate and deep drain structure, enabling the integration of multiple power devices on a single chip while maintaining favorable conduction characteristics. Research on the single-event effects of SiC QVDMOSFET remains limited, with no studies to date focusing specifically on SEB effects or the development of SEB-hardened structures to improve SEB resistance. Consequently, investigating SEB in SiC QVDMOSFET holds substantial significance.

Most studies have shown that when the ohmic contact temperature between silicon carbide (SiC) and metal and in the gate oxide region exceeds 1500K, significant degradation or even damage will occur [22]. Wang Ying et al. [23] asserted that analyzing SEB simulation results based on temperature instead of leakage current would produce more accurate prediction in the study of single event effect (SEE) of SiC trench gate MOSFET. Therefore, in this work, SEB occurs in devices when the maximum lattice temperature exceeds 1500K.

Firstly, this work uses TCAD simulation to analyze the (SEB) effects of SiC T-QVDMOSFET devices. Based on the simulation results, the causes of SEB are analyzed, and a SiC TB-QVDMOSFET device with an added BOX and a heavily doped N-type CSL is proposed. After heavy-ion irradiation, the combined effect of the BOX and the CSL enables the dispersion of current within the device, reducing the transient maximum current density in the region. As a result, the power dissipation in the burnout area decreases, the maximum device temperature is reduced to below 1500K, and catastrophic damage is avoided, leading to a 77% increase in the SEB threshold voltage of the device.

II. DEVICE STRUCTURE ANDSIMULATION SETUP

Fig. 1(a) presents the cross-sectional view of the T-QVDMOSFET, featuring a trench gate and deep drain, with a single cell width of 28 μm. During forward conduction, the current flows through the drain, N-sinker, N-buried layer, drift region, and source.The stepped gate structure modulates the electric field near the gate trench under reverse voltage conditions [24], [25], [26]. Additionally, the deep drain is designed to shorten the current conduction path, thereby enhancing the device's conduction characteristics [27], [28]. Fig. 1(b) illustrates the improved TB-QVDMOSFET structure. In this enhanced design, a silicon dioxide buried oxide layer is introduced beneath the trench gate within the N-buried layer. The insulating properties of silicon dioxide modify part of the current path [29]. Moreover, a heavily doped N-type CSL is incorporated into the N-sinker [30].

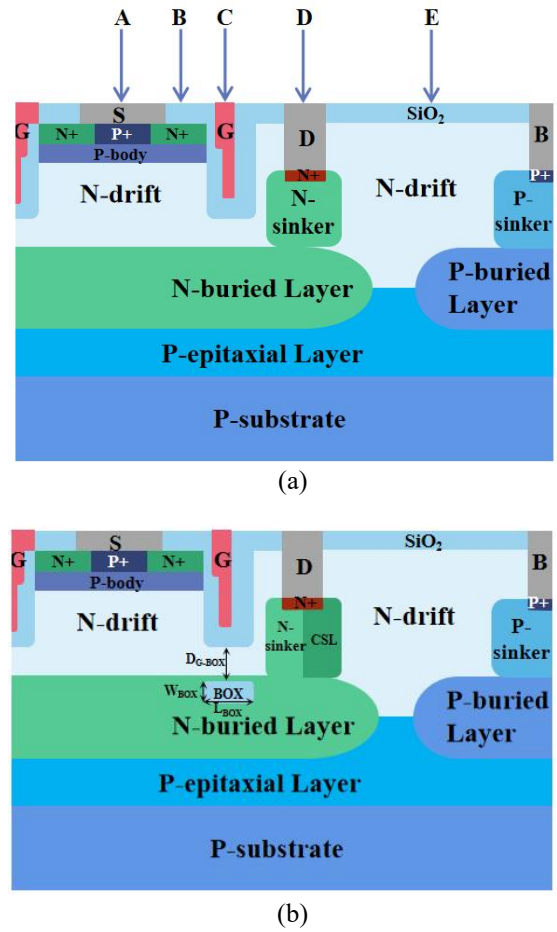

FIGURE 1. Schematic cross-sectional view of the (a) T-QVDMOSFET (b) TB-QVDMOSFET.

Aside from the addition of the BOX and CSL, all other parameters remain identical between the two structures. During forward conduction, the N-sinker and N-buried layers offer a high-conductivity path. The bulk electrode,

low-doped P-sinker layer, and P-buried layer function as isolation and grounding in multicellular configurations. The width of BOX in the TB-QVDMOSFET is 0.5μm, with a length of 2.1μm.The specific parameters of the device are shown in Table 1.

The width of the BOX aligns with the gate trench width, as shown in Fig. 1(b). Later, the influence of BOX parameters on the SEB-hardened effect will be discussed. Before this, the concept of adding a BOX for optimizing SiC devices has been studied, with a focus on reinforced structures [31]，[32]. The process for forming the BOX is as follows: First, a gate oxide trench is etched. Then, through multiple oxygen ion implantations [33] and subsequent annealing, the BOX is formed in the NBL beneath the trench. To simplify the process, the length of the BOX is kept consistent with the width of the gate trench, and multiple ion implantations are carried out at the bottom of the etched gate trench to form the BOX.

TABLE 1. Device parameters in simulation

PARAMETER	T-QVDMOSFET	TB-QVDMOSFET
Thickness of the drift region	6.1μm	6.1μm
Thickness of NBL	4.3μm	4.3μm
N-sinker layer Junction Depth	4.7μm	4.7μm
Thickness of P-substrate	15μm	15μm
Width of CSL	-	0.6μm
Width of BOX	-	0.5μm
Length of BOX	-	2.1μm
Thickness of Gate oxide	0.05μm	0.05μm
N-drift doping concentration	2.5×10^{15} cm^{-3}	2.5×10^{15} cm^{-3}
P-body doping concentration	1.2×10^{17} cm^{-3}	1.2×10^{17} cm^{-3}
P+ source doping concentration	1.0×10^{19} cm^{-3}	1.0×10^{19} cm^{-3}
N+ source doping concentration	1.0×10^{19} cm^{-3}	1.0×10^{19} cm^{-3}
P-Substrate doping concentration	1.0×10^{14} cm^{-3}	1.0×10^{14} cm^{-3}
CSL doping concentration	-	1.0×10^{17} cm^{-3}
N-sinker layer doping concentration	8.0×10^{16} cm^{-3}	8.0×10^{16} cm^{-3}
NBL doping concentration	1.2×10^{16} cm^{-3}	1.2×10^{16} cm^{-3}
P-epitaxial layer concentration	1.2×10^{14} cm^{-3}	1.2×10^{14} cm^{-3}

The fundamental electrical characteristics and SEB behavior of the two devices were simulated using the 2-D simulator Silvaco ATLAS. The simulation is based on some physical models which include the Analytic model, the mobility dependent parallel electric field (FLDMOB) model. The bandgap narrowing (BGN) model played a crucial role in the simulation, particularly due to the presence of heavily doped regions. The composite model incorporated both the doping and temperature-dependent Shockley-Read-Hall (SRH) model and the AUGER model. The incomplete ionization model and the Selberherr model were used to calculate the impact ionization rate and the breakdown voltages. To evaluate lattice temperature, the lattice self-heating model (LAT.TEMP) was utilized [34-37]. When heavy-ion in space strike the device, the deposited charge, measured in pC/μm, induces a high density of non-equilibrium electron-hole pairs along the heavy-ion track. The linear energy transfer (LET) parameter is commonly used to quantify the energy characteristics of these heavy- ions [38]. To simplify the SEB simulation, the track charge generation rate for a vertical track is function of the spatial and temporal Gaussian which is described by the (1) [39], [40]. In 2-D simulation, the carrier distribution is non-cylindrical, rendering the simulation results qualitative rather than quantitative. The parameters employed in the SEB simulation are presented in Table 2.

$$\mathrm{rate}(x,y)=\frac{\mathrm{LET}}{\mathrm{q}\pi\omega_0\mathrm{T_C}}\exp\left(-\frac{(x-x_0)^2}{\omega_0^2}\right)\cdot\exp\left(-\frac{(\mathrm{t}-\mathrm{T}_0)^2}{\mathrm{T}_c^2}\right)(1)$$

The lateral position of the ion track is defined by x_0. while the starting and ending points of the heavy-ion's vertical trajectory are denoted as y_0 and y_1, respectively. The LET value used during the simulation is 0.5 pC/μm.

TABLE 2. Parameters used in simulation

PARAMETER	VALUE
Track Radius ω_0 (μm)	0.05
Temporal Gaussian Function Width Tc (ps)	2
Initial Charge Generation Time T_0 (ps)	4
Linear Energy Transfer (LET) (pC/μm)	0.5

III. NUMERICAL SIMULATION RESULTS AND DISCUSSION

A. BASIC ELECTRICAL CHARACTERISTIC

Fig. 2 illustrates the breakdown voltage characteristics of the two MOSFETs when V_{GS} = 0V. The reverse breakdown voltages of the T-QVDMOSFET and TB-QVDMOSFET are 903V and 893V, respectively. Additionally, Fig. 2 presents the internal electric field distribution at the breakdown voltage for the improved structure. Because the P-type base region is completely depleted, a high electric field appears at the junction of the bottom of the gate trench and the drift region, which leads to device breakdown. The peak electric field and electric field distribution of the two devices during breakdown are basically the same, It shows that the SEB-hardened structure has no obvious influence on the electric field value and electric field distribution during breakdown.

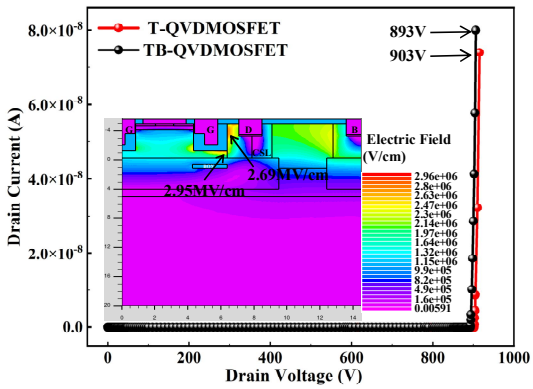

FIGURE 2. OFF-state characteristic curves of the T-QVDMOSFET and the TB-QVDMOSFET.

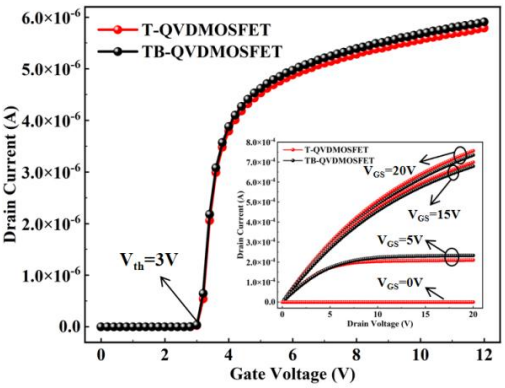

FIGURE 3. The transfer characteristic curves of devices and the ON-state characteristic curves of devices.

Fig. 3 shows the transfer characteristic curves and on-state characteristic curves of the two devices. Because of their same P-base region doping concentration, the two devices show the same threshold voltage. When V_{GS} is biased at 5V, 15V and 20V, the on-state curves almost overlap in the linear region. Under the condition of V_{GS} = 20V [41], the specific on-resistance of both the T-QVDMOSFET and TB-QVDMOSFET is 2.2 mΩ·cm². Thus, the SEB-hardened device does not exhibit a significant change in basic electrical characteristics compared to the original device.

B. SINGLE-EVENT BURNOUT CHARACTERISTIC

To determine the most sensitive incident position on the device, five vertical locations—A, B, C, D, and E—were selected above the device, as illustrated in Fig. 1(a). These positions correspond to the source, heavily doped N+ region, gate, drain, and drift region, respectively. The SEB threshold voltage is defined as the V_{DS} at which the device's maximum temperature exceeds 1500K. The SEB thresholds for the T-QVDMOSFET and TB-QVDMOSFET at each incident position are presented in Fig. 4. The results indicate that the most sensitive incident position for the T-QVDMOSFET is above the drain, and the later research of this work is based on this position.

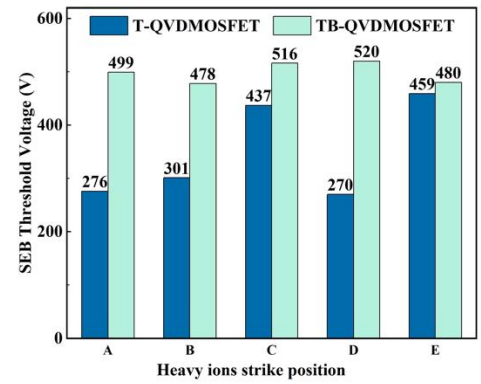

FIGURE 4. SEB thresholds of devices at different incident positions.

Previous analyses of SEB mechanisms in SiC MOSFETs indicate that when heavy-ion strike the device, ionization of electron-hole pairs along the ion track creates a plasma column. Under the influence of the drain-source voltage, the generated holes flow upward through the P-base region towards the source, causing a voltage drop between the base and emitter of the parasitic transistor. This voltage drop triggers the forward conduction of the parasitic transistor, leading to the generation of a high concentration of non-equilibrium electron-hole pairs [28], [42]. The resulting high impact ionization produces additional secondary carriers, causing a substantial steady-state transient current and localized overheating, ultimately leading to SEB through thermal breakdown [43-45]. In addition, the research shows that the region with the highest lattice temperature in the device corresponds to the region with the highest power density [46]. Power density, defined as the product of current density and electric field strength, reflects the local power dissipation in the SiC MOSFET. The localized avalanche effect within the device can produce high current density and strong electric field, resulting in significant power dissipation, which will increase the temperature of the device and lead to thermal damage [47].

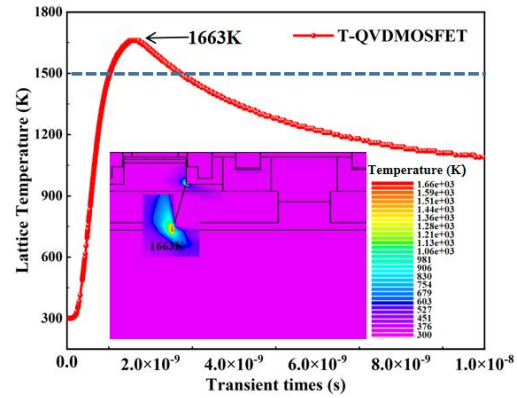

FIGURE 5. When V_{DS} = 300 V and LET = 0.5 pC/μm, temperature change of the device after heavy-ion strike in T-QVDMOSFET.

As shown in Fig. 5, the 2-D numerical simulation reveals the device's temperature variation over time and the distribution of the maximum lattice temperature. the highest temperature in the device was observed at the corner of the trench gate oxide 1.6 ns after heavy-ion strike the region above the drain of the T-QVDMOSFET, reaching 1663K. At this temperature, the device has reached the surface contact melting point, posing a significant risk of damage.

As the heavy-ion incidence time progresses from 0.1 ns to 4 ns, the spatial distribution and variation of power density within the device are illustrated in Fig. 6. The results reveal that the power density reaches its peak at 0.6 ns after the heavy-ion incidence. This peak occurs at the bottom corner of the gate trench, reaching 7.37×10^{12} W/cm^3, corresponding to the highest temperature region of the device. This indicates that the high power dissipation in the T-QVDMOSFET leads to excessive device temperature, resulting in thermal damage. Therefore, the SEB threshold voltage can be improved by reducing the high power density generated in the device.

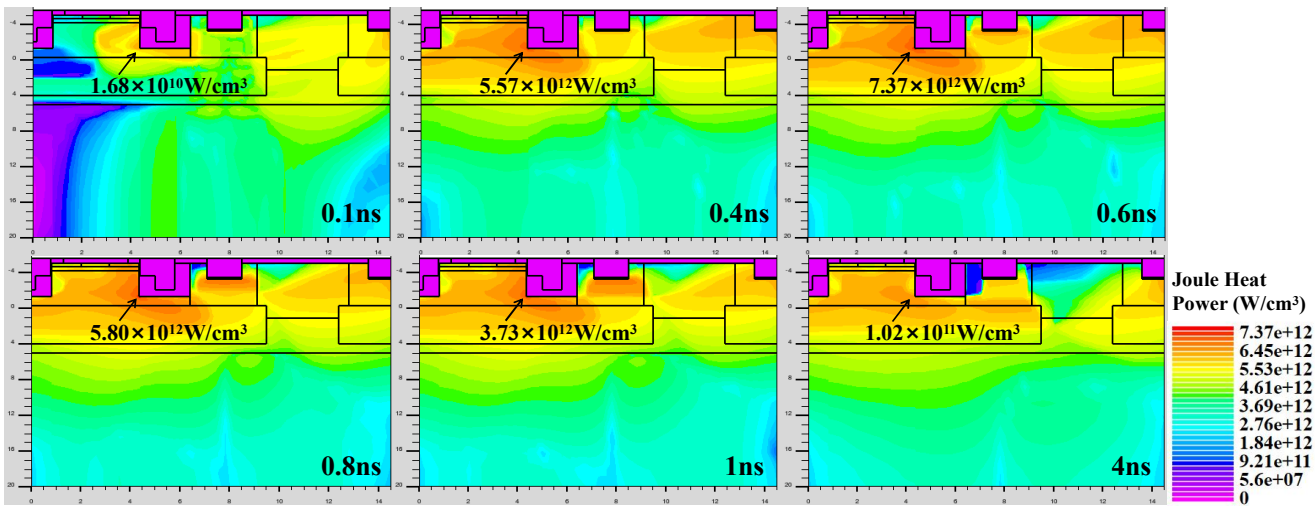

FIGURE 6. When V_{DS} = 300 V and LET = 0.5 pC/μm, power density distribution of devices at different time after heavy-ion incidence in T-QVDMOSFET.

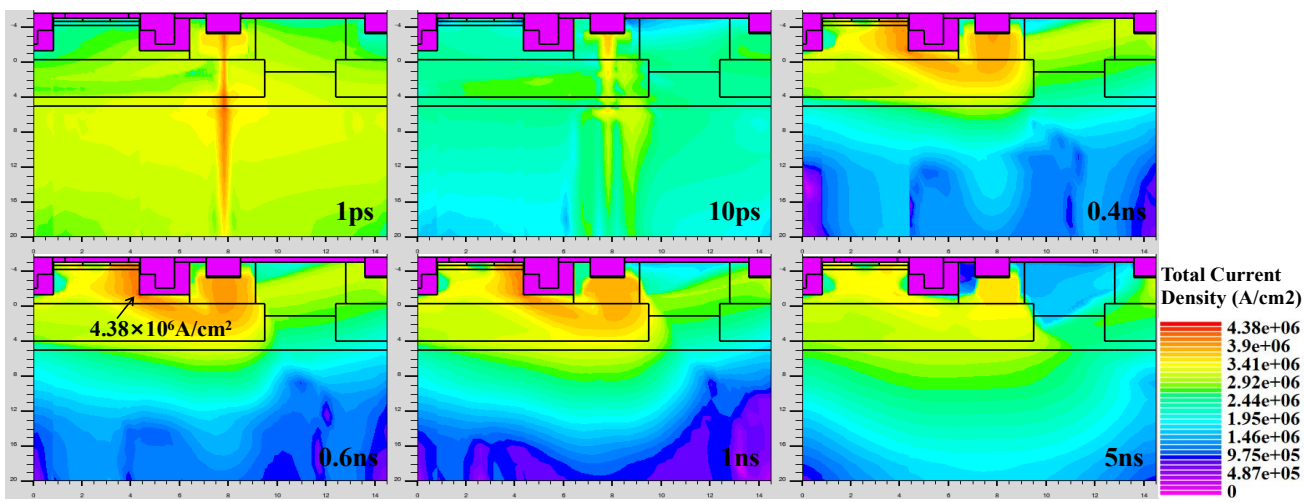

FIGURE 7. Total current density distribution of T-QVDMOSFET at different time after heavy-ion incidence when V_{DS} = 300 V and LET = 0.5 pC/μm.

Fig. 7 shows the spatial distribution of the total current density in the device with the incident time of heavy-ion from 1 ps to 5 ns after heavy-ion strike above the drain. The strike of the heavy-ion generates a high electric field, causing the energy deposited in the device to excite electron-hole pairs, which leads to a high concentration of non-equilibrium carriers due to intense impact ionization. The holes move toward the source, while the electrons move toward the drain. The resulting transient current flows through the corner beneath the gate trench, where current congestion occurs at 0.6 ns, resulting in a peak current density of 4.38×10^6 A/cm^2. With the passage of time, up to 5 ns, with a large number of carriers leaking out through the electrodes, resulting in a decrease in total current density. At 0.6 ns, the peak point of total current density corresponds to the peak point of power density. This analysis indicates that the high local current density is a contributing factor to the elevated temperature

observed at the corner beneath the gate trench in the T-QVDMOSFET.

C. SEB PERFORMANCE COMPARISON OF TWO DEVICE

The effect of BOX parameters on radiation hardening will be discussed below to determine the optimal BOX parameters for TB-QVDMOSFET. Since the BOX length is fixed at 2.1μm, only the width of BOX and the distance between the gate trench and BOX will be considered. The BOX thickness is 0.5μm, and the distance between the gate trench and BOX ($D_{G\text{-}BOX}$) varies from 1.3μm to 2.3μm. The influence of $D_{G\text{-}BOX}$ variation on the device's breakdown and conduction characteristics, as well as the device's maximum temperature change curve with respect to the incident time, is shown in Fig. 8. According to Fig. 8, changing $D_{G\text{-}BOX}$ has little effect on the breakdown characteristics and conduction characteristics of the device. When $D_{G\text{-}BOX}$ is 1.9μm, the temperature peak value is the lowest, which shows that the SEB-hardened effect on the device is the best when $D_{G\text{-}BOX}$=1.9μm, so the distance between gate trench and BOX is determined to be 0.5μm in subsequent research.

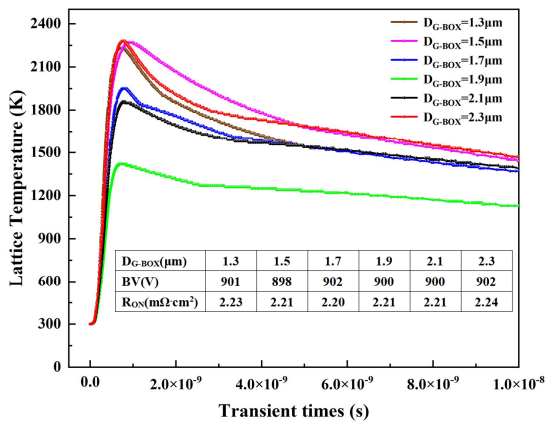

FIGURE 8. **V_{DS}=500V, LET=0.5 pC/μm, the variation curve of the highest temperature of the device with the increase of heavy-ion incident time for different $D_{G\text{-}BOX}$.**

As shown in Fig. 9, when $D_{G\text{-}BOX}$ = 1.9μm, the width of the BOX(W_{BOX}) is varied from 0.3μm to 0.7μm under the bias conditions of V_{DS} = 500V and LET = 0.5 pC/μm. The change in the device's maximum temperature as a function of the heavy-ion incident time is plotted. In addition, Fig. 9 also shows that the breakdown and conduction characteristics of the TB-QVDMOSFET remain largely unchanged with variations in W_{BOX}. As shown in Fig. 9, when W_{BOX} = 0.5μm, the device's peak temperature is the lowest. When the width of BOX is too small, the shunt effect is not obvious, and the temperature is not effectively reduced. When the width of BOX is too large, it may hinder the current flow, the carriers cannot efficiently leak out of the electrode, resulting in a weakened reinforcement effect. Therefore, for subsequent studies, the width of BOX is set to 0.5μm.

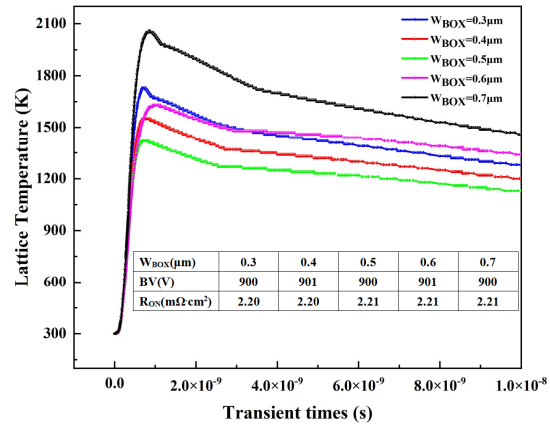

FIGURE 9. **V_{DS}=500V, LET=0.5 pC/μm, the variation curve of the highest temperature of the device with the increase of heavy-ion incident time for different W_{BOX}.**

As shown in Fig. 10, under the conditions of V_{DS} = 500V and LET = 0.5 pC/μm, the maximum lattice temperature of the T-QVDMOSFET reaches 2757K, significantly exceeding the surface contact melting point of 1500K, which could lead to device failure. In contrast, the maximum lattice temperature of the TB-QVDMOSFET is 1421K, which avoids thermal damage to the device. Fig. 10 also indicates that the location of the maximum lattice temperature in the SEB-hardened TB-QVDMOSFET structure remains unchanged compared to the T-QVDMOSFET. However, under the same conditions, the maximum lattice temperature in the TB-QVDMOSFET is reduced by 1336K.

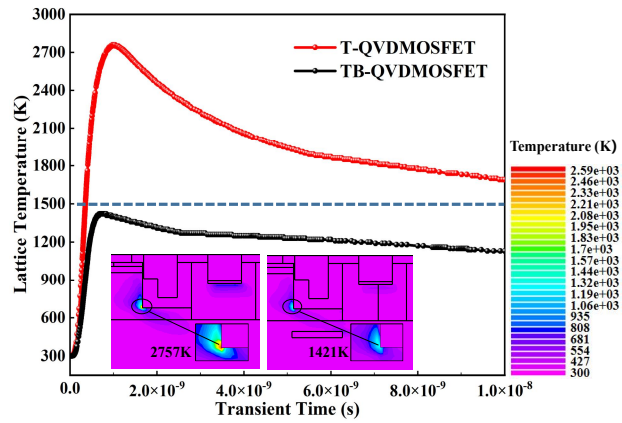

FIGURE 10. **V_{DS} = 500V, LET = 0.5 pC/μm, the lattice temperature change curves of the two devices after heavy-ion incidence.**

In order to reduce the current congestion and lower the total current density flowing through this area, a SEB-hardened structure TB-QVDMOSFET is proposed. As shown in Fig. 11(a), at V_{DS} = 500V, the transient high

current of the original device generates current congestion at the gate corner at 0.4ns, and the total current density reaches its peak at this time, which is 7.91×10^6 A/cm^2. As shown in Fig. 11(b), a part of the current flows through the area above the BOX, while the other part flows through the area below the BOX, thus expanding the current leakage area, and the BOX can also extend the path length of the current flowing into the electrode. In addition, the heavily doped N-type CSL makes the current flow more in the high doping concentration region. Both of these actions reduce the high transient total current density at the gate trench corner in the same drain bias condition, and the total current density at the gate trench corner of the TB-QVDMOSFET is smaller than that of the T-QVDMOSFET at the same time.

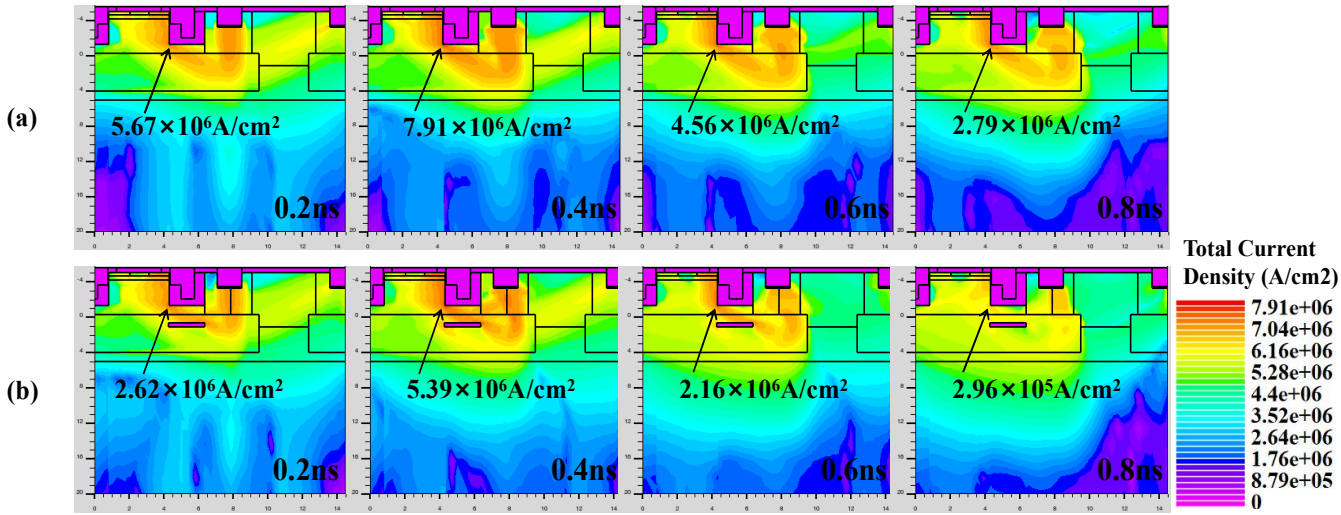

FIGURE 11. When V_{DS} = 500 V and LET = 0.5 pC/μm, the total current density of the device changes with time after ion incidence (a) T-QVDMOSFET (b) TB-QVDMOSFET.

IV. CONCLUSION

This work initially analyzed the single-event burnout (SEB) effect of a 900V SiC T-QVDMOSFET using 2-D numerical simulation, followed by a comparative analysis of SEB performance between the T-QVDMOSFET and the optimized TB-QVDMOSFET, which incorporates a BOX within the N-buried layer and an N-type CSL within the N-sinker. The simulation identified the most sensitive ion incident position for the T-QVDMOSFET as being above the drain. The parameters of the added BOX were discussed, and the optimized parameters were finally determined. The simulation results show that the optimized structure has little effect on the basic electrical characteristics of QVDMOSFET. However, the inclusion of the BOX and N-type CSL can change the current distribution path after heavy-ion radiation, reduce the regional high transient total current density and reduce the power dissipation of the device, thus reducing the highest lattice temperature of the device This improvement substantially increases the SEB threshold voltage, with the proposed TB-QVDMOSFET achieving an SEB threshold of 478V (53.5% of the breakdown voltage), representing a 77% increase compared to T-QVDMOSFET. This SEB-hardened design and mechanism offer valuable insights for the development of robust SEB-hardened structures in SiC QVDMOSFETs.

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