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Numerical Simulations of Gate-Granularity-Induced Subthreshold Characteristics Deterioration of MOSFETs Magnified at Cryogenic Temperatures

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ABSTRACT While gate workfunction fluctuation causes the threshold voltage shift of transistors, it leads to off- and on-state current variations with a given supply voltage and circuit performance degradation at room temperatures. However, the impacts of gate workfunction fluctuation on device electrical characteristics at cryogenic temperatures are still unclear yet. Based on self-consistent numerical simulations, we report in this work that cryogenic operation of n-channel transistors magnifies the influence of gate granularity on the device performance variation in terms of threshold voltage, subthreshold swing and drain currents. Gate granularity roughens the channel potential landscape and forms the local minima on the conduction band for electron transport, and which effectively reduces the device channel width. Our results highlight current deterioration in the subthreshold and weak inversion regions at cryogenic temperatures due to gate granularity. It may result in subthreshold swing saturation at cryogenic temperatures and pose a challenge to supply voltage scaling for power management. Device physics is explained and potential solution is discussed in this paper.

INDEX TERMS cryogenic MOSFET, gate granularity, gate workfunction fluctuation, subthreshold swing, supply voltage, TCAD simulation.

I. INTRODUCTION

As we continue to scale down the device dimensions by following Moore's law for advanced technology nodes, device variability has become a crucial challenge in mass production of integrated circuits. There are multiple factors that may significantly impact device performance and cause device variability: line edge roughness [1], random dopant fluctuation [2], gate granularity (GG) [3] and other process-induced non-uniformity. Among these unwanted and inevitable factors originating from process variation, GG may have become the dominating one at the 22 nm technology node and beyond [4].

Because of the process conditions and the nature of underlying materials, the microstructure of a deposited metal is usually poly-crystalline with different nanocrystal orientations within the film. Different orientations of nanocrystal grains result in different surface atomic densities, dipole densities and hence workfunction [5-6]. Therefore, the workfunction of a specific metal film is not simply constant, but the value can fluctuate in random positions across the metal surfaces. On the other hand, it is well known that the metal gate workfunction is a crucial parameter determining the threshold voltage V_{th} of a MOSFET and hence the circuit performance [7]. As a consequence, GG may lead to variations in V_{th} of individual MOSFETs, resulting in complementary-device mismatch and degraded circuit performance. Nevertheless, grain size reduction (or decrease in the ratio of grain size to gate area) may mitigate the impact of GG on device performance variability [8-9].

MOSFETs and CMOS working at cryogenic temperatures have gained much attention because of the novel applications based on high performance computing and quantum computing [10-20]. The carrier mobility μ can be increased by lowering the temperature due to the suppression of phonon scattering, improving the on-state currents of devices. The V_{th} roll-up is mainly a consequence of Fermi-Dirac distribution sharpening in energy when temperature decreases. Note that the variations of μ and V_{th} may tend to saturate at lower temperatures [11-16]. On the other hand, as heat is a crucial issue in the novel applications, cryogenic operation reduces the subthreshold leakage currents and subthreshold swing (*SS*), benefiting power management. Theoretically, *SS* decreases linearly with temperature [7], but many experimental results have shown *SS* saturation at a few tens of Kelvins [10-13]. This may place an obstacle to further scaling down the supply voltage and power dissipation of integrated circuits. Moreover, *SS* saturation has been attributed to the non-ideal band tail states at channel-oxide interface [15] and quantum tunneling through the channel region [16]. Design and optimization of device fabrication, dimensions and operation temperature for cryogenic CMOS are required to minimize the impacts of the two unfavourable factors.

According to our best knowledge, all prior studies discuss impacts of GG on MOSFETs and electrical circuits at around room temperatures [3-4,8-9,21-22]. There seems no prior literatures investigating the impacts of GG on device variation at different supply biases. In this work, using a self-consistent numerical device simulator [23], we show that the negligible nuance of room-temperature transfer characteristics of devices suffering from GG can be magnified at cryogenic temperatures. We also unveil that GG is the third reason of *SS* saturation at cryogenic temperatures. The impacts of GG on device performance variation at different supply biases are discussed as well for the first time. Device Simulation is detailed in Sec. II, followed by Result & Discussion and Conclusion in Sec. III and IV, respectively.

II. DEVICE SIMULATION

To correctly estimate the impacts of metal GG on the device performance, three-dimensional simulations considering random positions of local workfunction values are compulsory [8-9]. A device structure with fixed $16 \times 16 \times 16$ nm^3 gate volume and $4 \times 4 \times 4$ (or $2 \times 2 \times 2$) nm^3 grain size is adopted as shown in Fig. 1. While all device parameters remain permanent (doping profile and gate oxide), the only exception is the metal gate with randomly-generated grains and local workfunction values. The workfunction values used in the simulations are 4.4 and 4.6 eV with 40% and 60% present probability, respectively, and which correspond to <200> and <111> crystal orientations of TiN [22]. Then, a group of one hundred MOSFETs with one hundred distinct GG patterns are generated. With the same group of MOSFETs, device electrical characteristics is calculated by solving Poisson and current equations self-consistently with Fermi statistics at different temperatures [23]. Therefore, the simulated transfer characteristics variation at a given temperature between the one hundred devices originates purely from GG variation. Note that to highlight the impacts of GG on *SS* saturation, band tail and quantum tunneling models are intentionally turned off in our study although they both are available in the simulation package [23].

Given that short channel devices with constant gate length of 16 nm are simulated in this work, the validity of drift-diffusion transport with default mobility models in device simulators may be questionable. Invalidity would be worse when lowering the device operation temperature because of the increase of carrier ballisticity. However, the standard drift-diffusion model has been extended and used widely to simulate short channel devices with empirical ballistic mobility and Matthiessen's rule [24-25]. In addition, mobility models of the simulator may have not been well calibrated for MOSFETs working at cryogenic temperatures. Therefore, the effective mobility values are calibrated against our experimental data obtained by measuring the 16-nm device at different temperatures (Fig. 2). The mobility at 4 K is about 2.5 times higher than that obtained at 300 K, and this trend is in good agreement with prior literatures based on short channel devices [12,17-18].

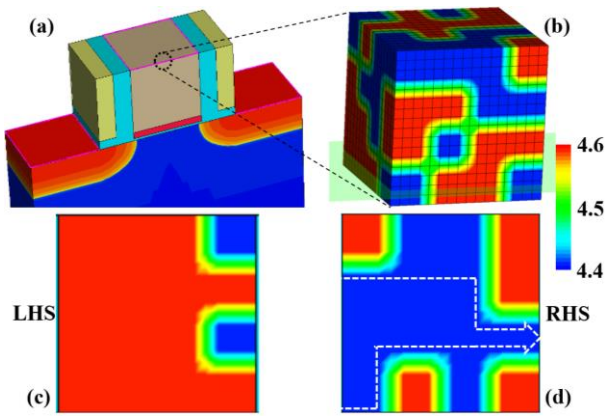

FIGURE. 1. (a) An n-channel MOSFET with metal gate granularity used in numerical simulations. A constant doping density of 4×10^{18} cm^{-3} is defined in the p-type substrate and the maximal doping density of 3×10^{20} cm^{-3} is defined in the n-type source/drain region. The whole metal region in (b) is assumed to be a $16\times16\times16$ nm^3 cube with $4\times4\times4$ (or $2\times2\times2$) nm^3 cubic granularity. Two representative metal gate workfunction pattern examples at the metal/oxide interface are shown in (c) and (d) for $4\times4\times4$ nm^3 cubic granularity. Hereafter, the metal workfunction patterns in (c) and (d) are referred to as LHS and RHS patterns, respectively. The color bar indicates the workfunction value in eV for (b), (c) and (d). The white dashed arrow in (d) mirrors and indicates the current flow path from source (left) to drain (right) in the channel region.

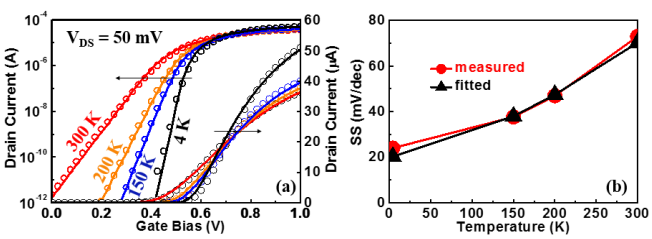

FIGURE. 2. (a) The measured (symbol) and fitted (line) transfer characteristic curves of the 16-nm device at different temperatures, and fitting is performed with the BSIM-CMG compact model [26]. (b) Extracted average *SS* from (a) in the current range of 10^{-11} and 10^{-7} A at different temperatures.

Another issue might be the direct tunneling from source to drain through the short channel length L_{ch}, and which is not considered in the calculations as mentioned. It has been shown that with small drain bias V_{DS} and a narrow tunneling energy window the drift-diffusion current can be dominant over the tunneling current in short channel ($15 < L_{ch} < 30$ nm) MOSFETs [12,16,20]. Hence, this is the reason that $V_{DS} = 50$ mV is used in all simulations. Also, the measured transfer characteristics of 16-nm devices at $V_{DS} = 50$ mV in Fig. 2 does not show superlinear subthreshold slope, which is the feature of tunneling leakage currents [12,16,20]. That implies the simulated device was not affected by direct tunneling currents at $V_{DS} = 50$ mV.

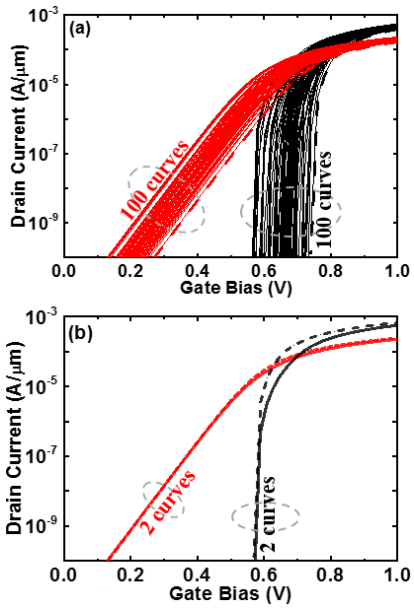

FIGURE. 3. (a) Simulated transfer characteristics of the one hundred nMOSFETs and the dashed curves denoting the results with the highest V_{th} at 300 (red) and 5 (black) K, respectively. (b) Starting from (a), only retaining the results with the highest and lowest V_{th} at each temperature, after shifting the dashed curves to the counterparts (with the lowest V_{th}) at the same gate bias corresponding to the drain current of 10 nA/μm, the difference between the two curves are compared. Note that, in (b), the solid (dashed) lines are the results of the MOSFET with the RHS (LHS) GG pattern, exhibiting the lowest (highest) V_{th} in (a).

III. RESULT AND DISCUSSION

With the same group of the one hundred MOSFETs, one hundred transfer characteristics curves are simulated at different temperature T (= 300 ~ 5 K). The results with T = 300 and 5 K are exhibited in Fig. 3(a). Generally, the trend with decreasing T is consistent with prior literatures, namely the V_{th} roll-up and steeper SS, as displaced in Fig. 4 as well, and GG is responsible for the V_{th} variation even at 5 K. SS may be defined at a specific current level (point SS) or within a range of currents (average SS). The latter is adopted in this work owing to two reasons: (1) Compared to point SS, average SS with a proper range of drain currents can provide more relevant and complete characteristics to gauge the device performance. (2) Because the gate bias ramping step may affect the outcome of SS extraction, especially at cryogenic temperatures, average SS is a better choice with sufficient data points within the current range. Assuming the minimal SS of 10 mV/dec at 5 K (see Fig. 4), the narrowest gate ramping step of 5 mV used in our simulations provides at least three data points within the current range of $10^1 \sim 10^4$ nA/μm. SS and ΔSS (defined as the difference of the maximal and minimal SS among the one hundred devices) are plotted against temperature in Fig. 4(b). Obviously, the impact of GG is magnified at lower temperatures, leading to enlarged SS variation and greater ΔSS. Moreover, all gray curves with GG variation deviate from the dashed trend (GG-free) in Fig. 4(b), showing that GG tends to degrade SS at each temperature and to cause SS saturation at cryogenic temperatures. Because band tail and quantum tunneling models are not activated intentionally in our simulations, GG can be deemed to be a third reason leading to SS saturation at cryogenic temperatures.

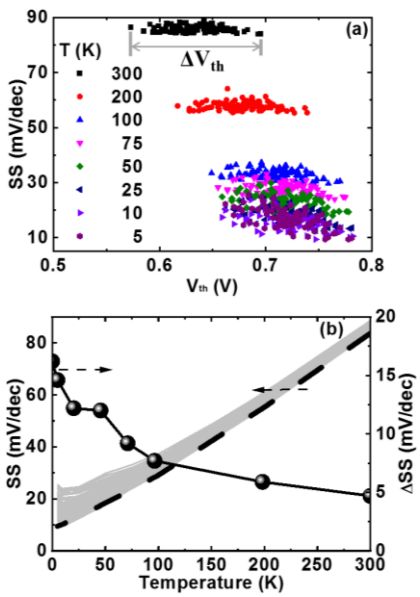

FIGURE. 4. Device parameters extracted from the simulated transfer characteristics of the same group of the one hundred MOSFETs at each temperatures. (a) Average SS versus V_{th}, and the latter is determined by the linear extrapolation method [17,27]. ΔV_{th} (ΔSS) is the difference of the maximal and minimal V_{th} (SS) among the one hundred devices at a given temperature. (b) Average SS and ΔSS versus temperature. The black dashed denotes the average SS obtained from simulations based on a MOSFET with an ideal uniform workfunction value (GG-free).

It is not surprising that in our simulations the LHS (RHS) GG pattern of Fig. 1 always results in the highest (lowest) V_{th} among the one hundred devices at each temperature. By analyzing the electrical characteristics of the two MOSFETs with LHS and RHS GG patterns, we may explore the maximum difference between the simulated one hundred devices. On the other hand, the device physics behind Fig. 4(b) can be unveiled by investigating Fig. 3(b), where shows that the negligible nuance of the two red curves of MOSFETs with the RHS and LHS GG patterns at 300 K is magnified at 5 K (black curves). The most obvious difference occurs in the subthreshold and weak-inversion current ranges. It is because that GG of the RHS pattern narrows the effective channel width (see the potential saddle in Fig. 5(a)), but this

effect is reduced at a high gate bias (Fig. 5(b)). Before entering strong inversion, the channel location under the blue region (WF = 4.4 eV in Fig. 1) has a higher electron density than that under the red region (WF = 4.6 eV in Fig. 1) due to the electrostatic potential difference caused by GG. This potential difference is then decreased gradually when entering strong inversion (Fig. 5), leading to similar drain currents at a high gate bias, as shown by the two black curves at gate bias of 1 V in Fig. 3(b). This phenomenon is relatively obscure at 300 K because electrons are able to occupy in higher energy (see Fig. 6), reducing the impact of saddle potential on the carrier transport. As a consequence, the GG patterns may degrade the currents in subthreshold and weak inversion regions, explaining the increased ΔSS and SS saturation at cryogenic temperatures in Fig. 4(b).

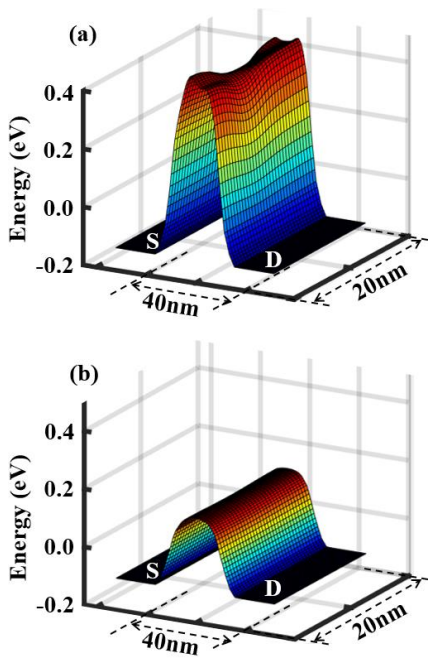

FIGURE. 5. Simulated landscapes of conduction bands of the MOSFET with the RHS GG pattern of Fig. 1 at (a) low and (b) high gate bias. S: source; D: drain; Drain bias V_{DS} = 0 V.

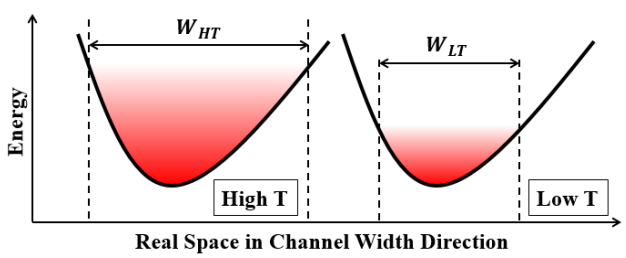

FIGURE. 6. Schematic conduction band diagrams (black curves) of a local minimum induced by GG along the channel width W direction at high and low temperatures. Following Fermi Dirac statistics, at a higher temperature, electron occupation increases at higher energy, leading to a wider effective channel width ($W_{HT} > W_{LT}$) for electron transport from source to drain.

Comparing the transfer characteristics of the two MOSFETs with the LHS and RHS GG patterns allows us to evaluate the on-state current (I_{on}) variation (Fig. 7), and which may be defined as

$$\frac{I_{on,LHS} - I_{on,RHS}}{I_{on,LHS}}. \quad (1)$$

$I_{on,LHS}$ and $I_{on,RHS}$ are the I_{on} of MOSFETs with the LHS and RHS GG patterns, respectively, and they are extracted with a constant gate voltage overdrive (V_{ov}) beyond the gate bias corresponding to a current level of 10 nA/μm. As displayed in Fig. 7, there is crossover at $T \approx 200$ K between the two V_{ov} lines, manifesting the influence of subthreshold swing deterioration on I_{on} variation. This can be discovered as well in Fig. 3(b) when considering different V_{ov}. Furthermore, a smaller V_{ov} leads to greater I_{on} variation when $T \leq 100$ K in Fig. 7. As a consequence, GG may be a potential challenge to supply voltage scaling of cryogenic CMOS.

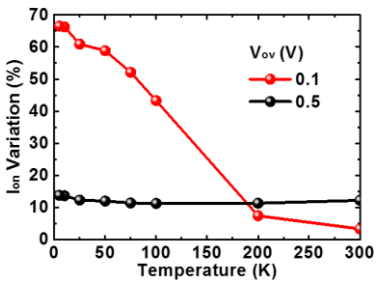

FIGURE. 7. I_{on} variation versus temperature with constant gate overdrive of 0.1 and 0.5 V.

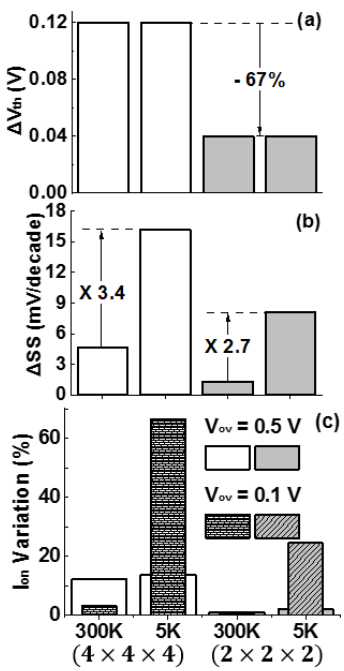

FIGURE. 8. (a) ΔV_{th} and (b) ΔSS for grain sizes of (4 × 4 × 4) and (2 × 2 × 2) nm^3 at 300 and 5 K. (c) benchmarks I_{on} variation with different V_{ov}.

So far, the simulation and discussion are based on GG with single grain size of 4 × 4 × 4 nm^3. Fig. 8 benchmarks the variations caused by GG with two different grain sizes. ΔV_{th} decreases with grain size, and which is consistent with prior literatures [8-9], however, it seems unchanged at different temperatures (also see Fig. 4(a)). It is noticed that the ΔSS

with 4 (2) nm grain size increases by a factor of 3.7 (2.7) when decreasing the temperature from 300 down to 5 K. According to Fig. 4, the minimal SS_{min} is about 85 mV/dec at 300 K, and ΔSS is roughly 5 mV/dec in Fig. 8(b), resulting in ignorable $\Delta SS/SS_{min} \approx 5\%$ for 4 nm grain size. This value (with 4 nm grain size) raises up to ~160% at 5 K because approximately the numerator ΔSS increases to ~16 mV/dec in Fig. 8(b) and the denominator SS_{min} decreases to ~10 mV/dec in Fig. 4. With 2 nm grain size, $\Delta SS/SS_{min}$ reduces to 64%. The larger ΔSS is responsible to the greater I_{on} variation at 5 K in Fig. 8(c), and which is further magnified by a lower V_{ov}. *SS* and I_{on} variations may significantly cause reliability issues of integrated circuits working at 5 K.

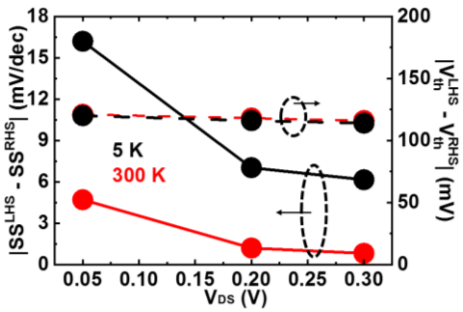

FIGURE. 9. The *SS* and V_{th} difference between the devices with LHS and RHS gate patterns for 300 (in red) and 5 (in black) K at different V_{DS}.

So far, the simulations and discussions are done with V_{DS} = 50 mV. To investigate the impact of gate granularity on device variation at higher V_{DS} biases, Fig. 9 shows the variation between devices with LHS and RHS gate patterns in terms of $|V_{th}^{LHS} - V_{th}^{RHS}|$ and $|SS^{LHS} - SS^{RHS}|$ at different temperatures and V_{DS}. As $|V_{th}^{LHS} - V_{th}^{RHS}|$ seems insusceptible to temperature and V_{DS}, $|SS^{LHS} - SS^{RHS}|$ increases with decreasing the temperature and V_{DS}, being consistent with Fig. 8(b). Moreover, $|SS^{LHS} - SS^{RHS}|$ decreases with increasing V_{DS}, which reduces the difference between the conduction band landscapes of the devices with LHS and RHS gate patterns.

Although we have tried to include band tail and quantum tunneling models in our simulations, convergence issues come along with lowering the temperatures. This is probably because that the small value of carrier density, e.g., ~ 10^{-600} cm^{-3} at 4 K, impacts the numerical procedure, becoming practically singular to finite precision arithmetics [28]. Hence, future work might lie in quantifying the contribution of each of the three reasons (band tail, tunneling and GG) on *SS* saturation at cryogenic temperatures.

IV. CONCLUSION

A Gate granularity (GG) is a critical and practical issue in advanced semiconductor manufacturing, particularly in the regard of designing high performance and reliable integrated circuits. GG-induced drain current degradation in the subthreshold and weak inversion regions may be magnified at a lower temperature due to a narrower effective channel width and lower carrier occupation in energy. Apart from band tail and quantum tunneling, we have in this work shown that GG may be a third cause of subthreshold swing saturation at cryogenic temperatures. For the applications of cryogenic CMOS, the influence of GG has been shown to be magnified at a lower temperature and smaller gate overdrive. A smaller grain size can effectively alleviate the impact of GG on the electrical performance variation of cryogenic MOSFETs.

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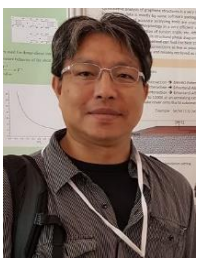

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