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Four-Level Single-Stage Single-Source Boost-Inverter

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ABSTRACT This paper presents a novel concept of a DC-AC converter that ensures AC voltage modulation on four levels using a single branch and achieves voltage boosting. The proposed boost inverter is based on a single-stage topology and does not use a DC-DC boosting part. Compared with a cascaded boost inverter topology, the proposed converter is bidirectional and allows operation at a lower DC-link voltage, which reduces voltage stress across devices. The inverter topology contains an additional DC capacitor. An adequate voltage level for this capacitor is maintained by a switched-capacitor-based (SC)-based balancing circuit. The balancing process is of low complexity because it only requires the synchronization of the SC branch control signals with the PWM of the inverter. The balancing circuit operates in resonant mode to avoid inrush currents. The main power circuit of the converter does not use diodes, and can be adequate for MOSFET or GaN-based implementations. It can be configured as a single-phase or multiphase system. The results presented in this paper demonstrate the correctness of the converter concept and its modulation, voltage stresses of switches, and balancing process of the auxiliary capacitor. The experimental results confirm the feasibility of this concept and demonstrate the operation and efficiency of the inverter.

INDEX TERMS Boost inverters, Buck rectifiers, DC-AC power converters, Multilevel inverters, Switched capacitor circuits, Voltage source inverters.

I. INTRODUCTION

Multilevel inverters (MLIs) are beneficial for applications at low, medium, and high voltages because of the reduced voltage stress across the semiconductor switches, du/dt, AC output filter volume, and improved output voltage. Traditional MLI systems include those that use the topologies of the cascaded H-bridge (CHB), flying capacitor (FC), and neutral point clamped (NPC); however, MLI concepts are still being developed. An important factor in MLI conversion systems is device count reduction [1], [2]. This can be achieved using novel topology concepts, such as switched-capacitor (SC)-based circuits, which allow the creation of high-voltage-gain converters with boosting ability [3]. In many classic systems with a photovoltaic source [4], cascaded systems composed of a DC-DC boost converter and an inverter are used because the voltage of the PV strings may not be high enough for the correct operation of the grid-connected inverter. DC-AC systems with a step-up DC-DC converter may also be required for the implementation of a battery-powered drive or can be beneficial in some uninterruptible power supply concepts. The classic topologies of inverters have the property of a step-down system; however, in the aforementioned applications, an inverter with integrated gain is an advantageous solution because the use of a DC-DC converter at the input or a

transformer at the output of the inverter can cause additional losses and costs.

The principle of operation of SC circuits involves parallel connection of capacitors to a DC source to charge them and configure them in a series circuit during discharge. In this way, SCs may add several levels to the output voltage waveform of an inverter and simultaneously provide voltage gain. The topologies presented in [1]–[6] are based on the SC concept and have features of modular construction. Several concepts for double-port inverters have been proposed in the field of single-phase inverters. In such topologies, the voltage source is connected in series to a network of switched capacitors to produce an appropriate level of output voltage. Some of these SC-based converters can be used to create multiphase inverters [5], [6]. In the concept of a multi-source system, the gain is obtained by summing the voltages from different sources in the DC-bus voltage, as in [9].

One of the implementation concepts of the boost-type inverter is a system with a regulated voltage on the input side [7], [8]. However, these approaches have limitations because the semiconductor switches in the inverter are exposed to high voltage stress.

A three-phase multilevel boost inverter with an SC circuit is presented in [10]. This inverter has an effective phase-branch structure because it uses four transistors, two diodes, and two floating capacitors in a branch. However, the parallel connection of the switched capacitors to the source can be considered a potential problem resulting from the inrush current flow. Moreover, with the current flowing in a circuit composed of MOSFETs and diodes, conduction power losses can be uneven in these components. In [11], seven-level inverter branches with a cascaded connection of an H-bridge converter and a flying capacitor are used. The converter requires additional control for the DC link and flying-capacitor voltage balance. Furthermore, the three-level structure connected to the DC link is characterized by high voltage stress across the transistors. In [12], a six-level inverter topology that achieved a two-and-a-half-fold voltage gain is demonstrated. The inverter uses three floating capacitors in a phase leg, and a network composed of six transistors and four diodes. The operating states of the inverter create circuits with transistors and diodes that are connected in series. When low $R_{DS(on)}$ MOSFET transistors are used, the conduction losses of the diode may significantly deteriorate the converter efficiency. However, the balance of power loss given in [12] indicates a loss of 27.5% in diodes and 44.2% in transistors for the components used at an input voltage of 100 V and a frequency of 100 kHz.

In [13], a switched-capacitor-based three-phase inverter that generates a seven-level line-to-line voltage is presented. The inverter achieves an inherent threefold voltage gain using a low number of devices. Threefold voltage boosting in a seven-level inverter with three floating capacitors is presented in [14]. Despite the interesting parameters of the inverters presented in [13] and [14], recharging the capacitor in parallel connections may trigger inrush currents and limit their power.

Topologies based on the active-neutral-point-clamped (ANPC) structure of the inverter [15] are of great importance for the development of multiphase multilevel voltage inverters with a single voltage source and built-in voltage gain [16]–[25]. References [16]–[19] demonstrate the obtaining of 7 levels of output voltage, paper [20] – 11 levels, and publications [21]–[25] present five-level modulation. When ccomparing the number of levels obtained with a given number of switches, the proposed inverter does not gain in relation to most such systems, for example, those in [16]–[20]. However, it has the advantage of limiting inrush currents in systems with switched capacitors. In addition to the DC link, the inverters utilize one floating capacitor, and a mechanism for self-balancing its voltage is proposed. The voltage of the floating capacitor can be balanced using redundant voltage modulation states [19]. However, in [16]–[23] and [25]–[26] the balancing process works by connecting the capacitor in parallel with the DC-link capacitors, thereby exposing the converter to an inrush current flow.

An important advantage of the inverter proposed in this paper is the concept of recharging the floating capacitor, which allows avoiding an inrush current because a resonant switched-capacitor circuit is used for this purpose, as presented in [27]. In this system, in addition to the load current, the currents of the oscillating nature flow. Therefore, there is no risk associated with inrush currents, which can negatively affect the level of electromagnetic interference and energy loss. The application of this idea of inrush current mitigation, along with the other elements of the system and its control, allows us to conclude that the article presents an innovative four-level single-stage inverter with the ability to increase the voltage (Fig. 1), which is the major contribution of this paper.

A boost inverter system can be implemented using concepts other than the use of switched-capacitor circuits, as proposed in this paper. Publications [28]–[39] present different cases of such solutions. For example, the advantage of the circuit presented in [28] is the small number of semiconductor switches, that is, only six transistors and six diodes, in a three-phase inverter. Three input chokes are used in the system. When comparing the inverter proposed in this study with the systems of different topologies presented in [28]–[39], it should be noted that it is a switched-capacitor system that does not use large chokes in the topology and has a limited voltage stress across the transistors of the main inverter circuit.

This paper also presents numerous simulation results that allow the identification of the impact of the inverter and balancing circuit parameters on its efficiency. The concept of the operation and efficiency of the inverter were verified by the demonstration of the experimental MOSFET-based inverter and the results of the measurements. The inverter can operate as a single-phase or multiphase inverter, and is therefore a competitive solution compared to typical single-

phase double-port inverters. Compared to the cascade boost-inverter topology, the proposed converter operates at a lower voltage across the DC link. In a two-stage system, both the DC-DC boost converter and inverter must be designed considering the voltage stress across devices resulting from the DC-link voltage. Eliminating the DC-DC boost part from the system allows the power choke to be removed on the DC side and decreases the voltage stress of the semiconductor components in the inverter.

This paper develops a concept previously presented at a scientific conference [27]. However, all the results presented and the experimental platform are novel and were not included in [27], as well as the results related to the efficiency, component power dissipation distribution, and four-quadrant operation.

This paper is organized as follows. Section II presents the concept of inverter operation, switching pattern, and simulation verification of converter operation in inverter and rectifier modes. Section III presents the results of the simulation tests that demonstrate the effect of converter parameters on efficiency, allowing us to justify the choice of system parameters. The operation of the converter was experimentally verified in a high-frequency system, and the results of the experiments are presented in Section IV. Section V compares the proposed inverter parameters with known ANPC-based inverter systems. References to the literature are also included [28]–[39], allowing for a comprehensive estimation of the parameters of the amplified inverters obtained in other topologies.

II. CONCEPT OF THE INVERTER

A. THE TOPOLOGY

The proposed inverter (Fig. 1) is composed of a DC link (C_1, C_2) and DC-AC branches that contain an auxiliary floating capacitor (C_3), network of semiconductor switches (S_1–S_6), and active balancing circuit (S_7, S_8, C_S, L_r, D_1, D_2). Four-level modulation of the output voltage of the single-phase inverter was achieved using a floating capacitor (C_3). The voltage across this capacitor can be added to or subtracted from the DC-link voltage. To ensure the proper operation of the inverter, the voltage of the floating capacitor should satisfy the following condition:

$$U_{C3} = U_{in} \tag{1}$$

The floating capacitor (C_3) is not connected directly to the energy source but is charged or discharged by the balancing circuit. The balancing circuit contains a switched capacitor (C_S) that transfers energy between the DC-link capacitors (C_1 and C_2) and a third DC capacitor (C_3). Its operation is synchronized with the inverter PWM pattern, and is required when the inverter generates low-level voltages on the output. The current of the L_rC_S branch was oscillatory. Because the duty cycle of the switching signals varies, the current oscillation in the L_rC_S circuit may be terminated; however, the inductor current continues to flow through diodes D_1 and D_2.

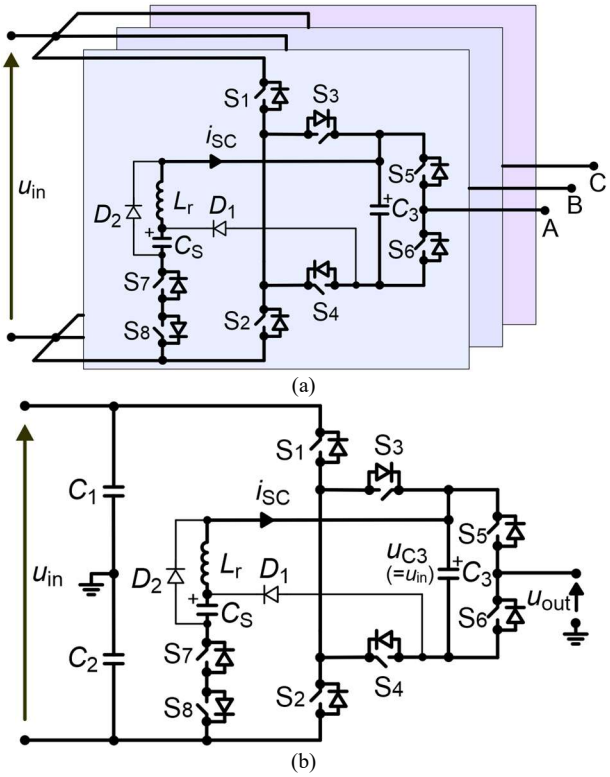


FIGURE 1. The proposed four-level boost inverter. (a) Three-phase topology. (b) Its single-phase implementation.

B. STATES OF OPERATION

Figs. 2 and 3 present the concept of inverter operation with marked current paths. The highest value of the output voltage ($1.5U_{in}$) is achieved in the SP2 configuration as the sum of the voltages on the DC link and capacitor C_3. A lower positive voltage can be obtained in two redundant states: SP1a and SP1b. These states produce the same output voltage value ($0.5U_{in}$). The balancing circuit is activated in the SP1a and SP2a states, exchanging energy with the DC-link capacitors in the SP1a and capacitor C_3 in the SP1b state. This allows the voltage values of the DC link and capacitor C_3 to approach the input voltage u_{in}. The generation of negative voltages at high and low levels is possible using the states presented in Fig. 3. Similar to the case in which a positive voltage is generated (Fig. 2), the highest negative voltage ($–1.5U_{in}$) occurs when the output voltage is the sum of the DC-link voltage and the floating capacitor voltage (C_3). In the other states presented in Fig. 3, a low negative voltage ($–0.5U$ in) is generated in two redundant states. In both states, the balancing circuit is activated, and the use of these states alternately allows energy exchange between the DC link and the floating capacitor (C_3).

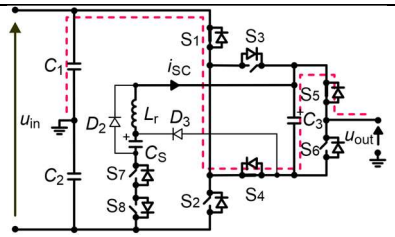
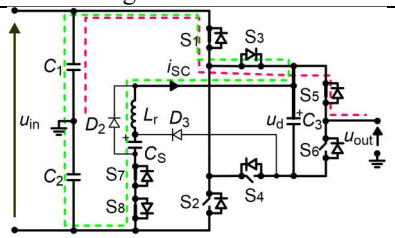
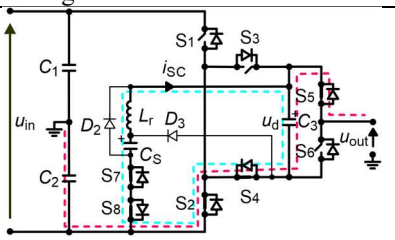
STATE	CONFIGURATION
Positive State 2 (SP2) The output voltage is at the high positive level.	 $U_{out} = 0.5U_{in}+U_{C3} = 0.5U_{in}+U_{in} = 1.5U_{in}$ The balancing circuit is not active.
Positive State 1a (SP1a) The output voltage is at the low positive level. Capacitor C_3 is not used to supply the load.	 $U_{out} = U_{C1} = 0.5U_{in}$ The balancing circuit is connected to the DC link. C_S is being charged or discharged from the DC link.
Positive State 1b (SP1b) The output voltage is at the low positive level.	 $U_{out} = -U_{C2}+U_{C3} = 0.5U_{in}$ The balancing circuit is connected to the DC capacitor C_3. C_S is being charged or discharged from the C_3 capacitor.

FIGURE 2. States with a high positive voltage (U_{out} = 1.5U_{in}) and two redundant states with a low positive voltage (U_{out} = 0.5U_{in}) on the output of the inverter branch.

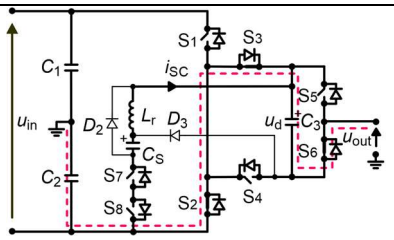
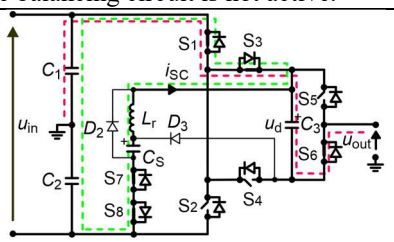
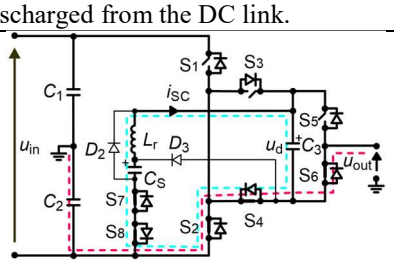
STATE	CONFIGURATION
Negative State 2 (SN2) The output voltage is at the high negative level.	 $U_{out} = -0.5U_{in}-U_{C3} = -0.5U_{in}-U_{in} = -1.5U_{in}$ The balancing circuit is not active.
Negative State 1a (SN1a) The output voltage is at the low negative level.	 $U_{out} = 0.5U_{in} - U_{C3} = -0.5U_{in}$ The balancing circuit is connected to the DC link. C_S is being charged or discharged from the DC link.
Negative State 1b (SN1b) The output voltage is at the low negative level. Capacitor C_3 is not used to supply the load.	 $U_{out} = -U_{C2} = -0.5U_{in}$ The balancing circuit is connected to the DC capacitor C_3. C_S is being charged or discharged from the C_3 capacitor.

FIGURE 3. States with a high negative voltage (U_{out} = –1.5U_{in}) and two redundant states with a low negative voltage (U_{out} = –0.5U_{in}) on the output of the inverter branch.

The output voltage as a function of modulation can therefore take the following values:

$$U_{out} = \begin{cases} 1.5U_{in} & \text{in state SP2} \\ 0.5U_{in} & \text{in states SP1a, SP1b} \\ -0.5U_{in} & \text{in states SP1a, SP1b} \\ -1.5U_{in} & \text{in state SP2} \end{cases} \quad (2)$$

To ensure the correct voltage across the capacitor C_3 (1), the balancing circuit, based on the switched capacitor, performs the energy exchange between C_3 and the front DC-link capacitors (C_1 and C_2). This is accomplished in the SP1a, SP1b, SN1a and SN1b states in a resonant circuit consisting of $C_S L_r$ and $S_{7\text{-}8}$ (diodes D_2 and D_3 have a protective function). The resonant circuit performs charge transfers from capacitors with higher voltage to capacitors with lower voltage. The voltage difference is produced by the load current, which, for example, discharges capacitor C_3 but this process can work bidirectionally.

Fig. 4 shows equivalent diagrams of the balancing circuits created by modulation. The approximate waveform of the balancing current is a sine wave described by

$$i_{SC(SP1a)} = \frac{U_{in}-U_{CS_{init}}}{\sqrt{\frac{L_r}{C_S}}} \sin\left(\frac{1}{\sqrt{L_r C_S}} t\right)$$
$$i_{SC(SP1b)} = \frac{U_{C3}-U_{CS_{init}}}{\sqrt{\frac{L_r}{C_S}}} \sin\left(\frac{1}{\sqrt{L_r C_S}} t\right) \quad (3)$$

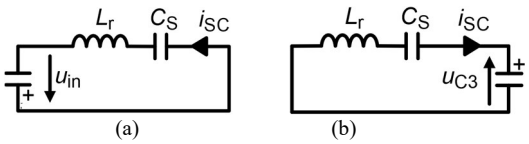


FIGURE 4. Circuit models for balancing current: (a) when charging C_S from the input source, (b) when charging capacitor C_3 from the switched capacitor C_S.

C. THE SWITCHING PATTERN

The proposed inverter modulation uses four single-phase output voltage levels. The highest voltages are produced using the SP2 and SN2 states, whereas low voltages are generated in the SP1a, SP1b, SN1a, and SN1b states.

The following guidelines for the implementation of modulation are provided based on the diagrams of the current flow in particular operating states:

- Redundant states should be used alternately to obtain the possibility of energy exchange between the DC-link capacitors and capacitor C_3 in both directions. Therefore, the switching pattern for modulation between high and low levels (for example, $1.5U_{in}$ to $0.5U_{in}$ and $-1.5U_{in}$ to $-0.5U_{in}$) is as follows:

$$\text{SPp} = \{\text{SP1a, SP2, SP1b, SP2, SP1a, } \ldots\}. \quad (4)$$

$$\text{SPn} = \{\text{SN1a, SN2, SN1b, SN2, SN1a, } \ldots\} \quad (5)$$

- Modulation between low levels ($-0.5U_{in}$ to $0.5U_{in}$) should take place without the use of the floating capacitor (C_3) and without involving the balancing circuit. In this case, the switching pattern is as follows:

$$\text{SPpn(1)} = \{\text{SP1a, SN1b, } \ldots\} \quad (6)$$

A model control using the proposed switching pattern is shown in Fig. 5. Modulation at the highest levels is optimal in view of the switching losses, as only two transistors change their states in a switching cycle. Modulation between the low levels avoids the loading of capacitor C_3 and the balancing circuit, which is, however, achieved by a larger number of transition states in the inverter transistors.

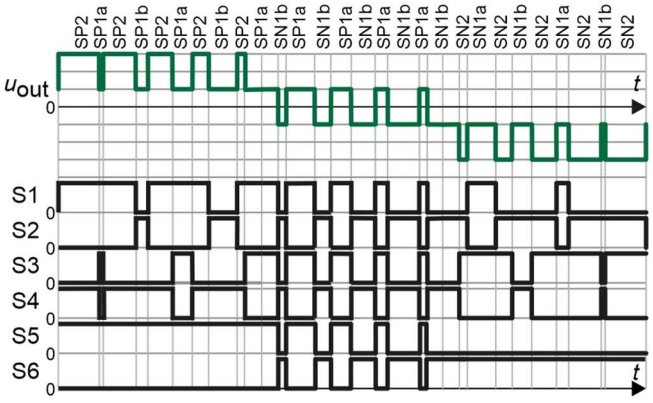


FIGURE 5. The output voltage and logic switching signals of the inverter transistors.

Switching the transistors in the inverter can interrupt the circuit through which the resonant choke current flows. Because the inverter operates with a variable duty-cycle factor of transistor control, this phenomenon is normal and occurs with a frequency that depends on the depth and type of modulation. Diodes D_1 and D_2 provide protection against choke current interruption regardless of the state of the transistors, as shown in Fig. 6.

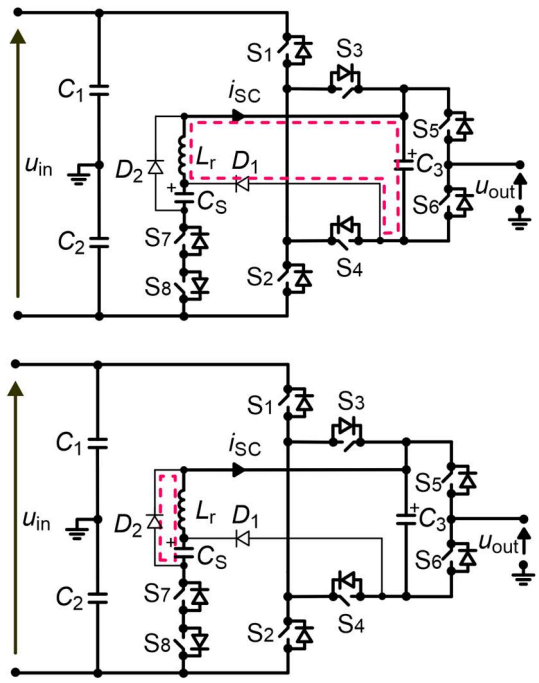


FIGURE 6. Choke current flow with transistors turned off.

D. VERIFICATION OF THE CONVERTER OPERATION IN THE SIMULATION MODEL

The simulation model allows us to assess the correctness of the proposed inverter concept and its modulation strategy.

Fig. 7 presents the steady-state waveforms in the boost-inverter mode, and Fig. 8 depicts those in the buck/rectifier mode. In both cases, the modulation method was the same, which allowed us to conclude that the balancing system provided the possibility of a bidirectional energy transfer.

The analyzed inverter works with a DC voltage source and, on the AC side, with an *LC* filter and resistive load. From the results of the inverter operation (Fig. 7), it can be observed that the voltage of capacitor C_3 is equal to the input voltage, which allows the correct modulation of the output voltage. In addition, the capacitor overcharges in the resonant balancing circuit were correct.

In the rectifier mode (Fig. 8), in the analyzed case of converter operation, the DC voltage is marked as in Fig. 1 (u_{in}), but a resistive receiver is attached to this voltage. On the AC side, there is an *L*-type filter (L_f) and an AC voltage source u_{AC}. The waveforms depicted in Fig. 8 show that the DC voltage on the DC link is maintained at the voltage value of capacitor C_3 and that the converter maintains the correct modulation.

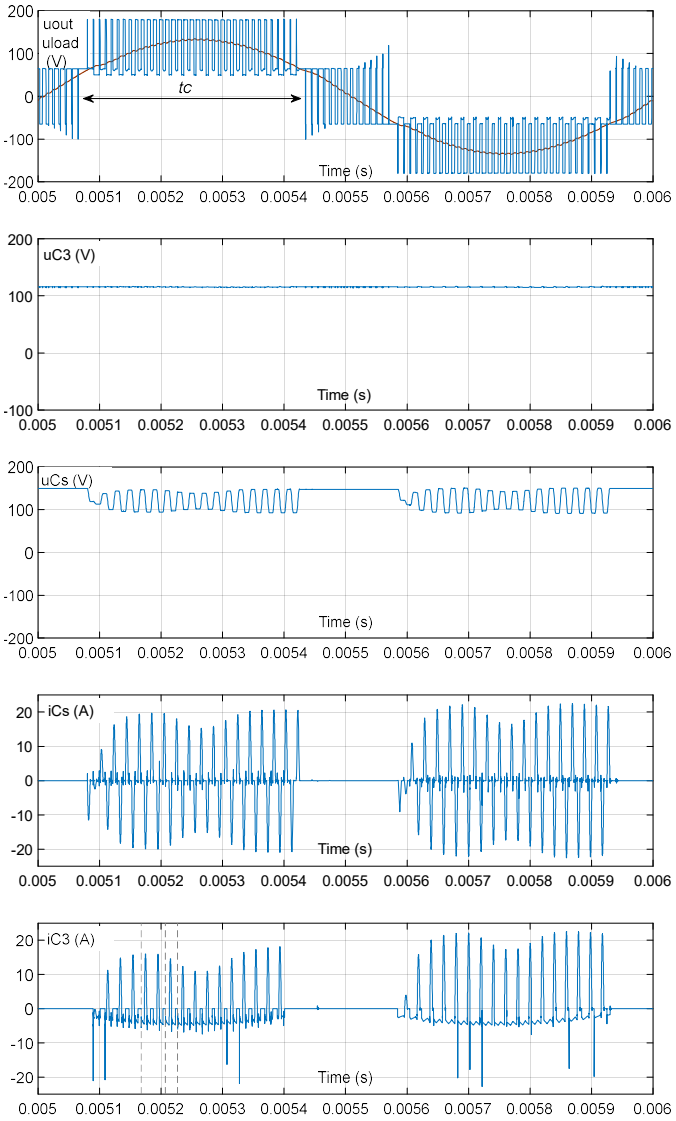


FIGURE 7. **Steady-state operation in boost-inverter mode. Waveforms of the output voltage and current, voltage across the DC capacitor C_3, as well as currents of the resonant inductor and the switched capacitor. P_{AC} = 250 W, m_a = 0.75, L_r = 1900 nH, C_S = 1100 nF, f_S = 100 kHz, DC voltage source U_{in} = 130 V, AC filter (Table II): L_F = 147 µH, C_F = 4400 nF. Matlab/Simulink results.**

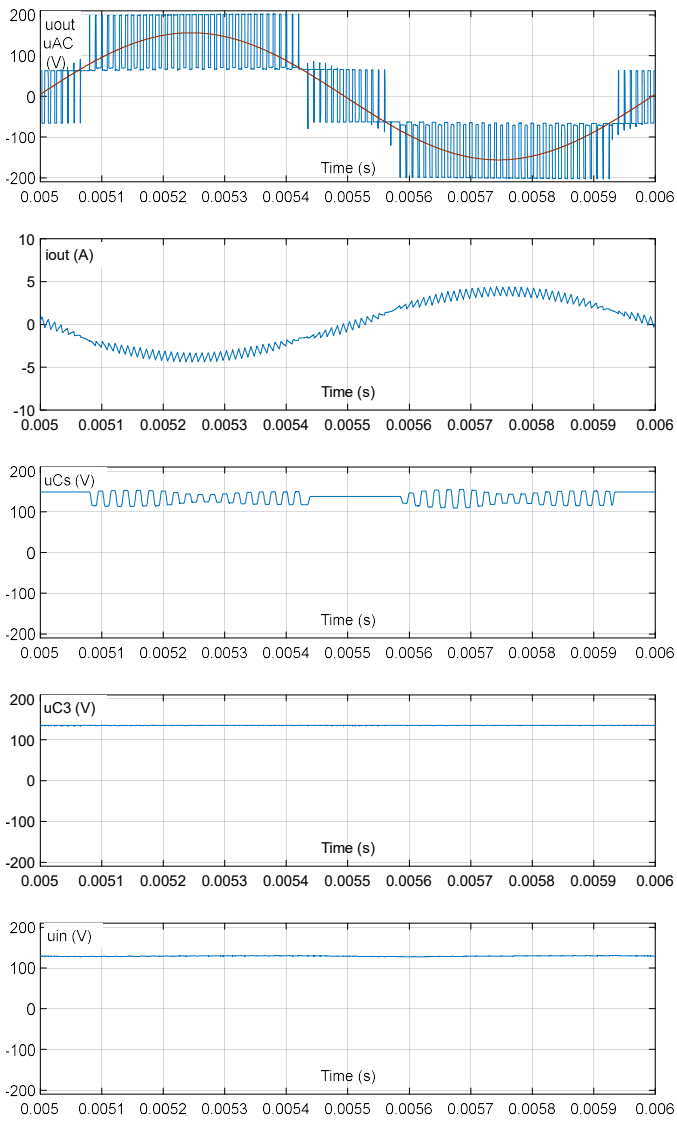


FIGURE 8. **Steady-state operation in buck/rectifier mode. Waveforms of the output voltage and current, voltage across the DC capacitor C_3, as well as currents of the resonant inductor and the switched capacitor. P_{DC} = 250 W, m_a = 0.76, L_r = 1900 nH, C_S = 1100 nF, f_S = 100 kHz, AC voltage source U_{AC} = 110 V, AC filter: L_F = 147 µH. Matlab/Simulink results.**

III. *SELECTION OF COMPONENTS*

A. BASIC PARAMETER SELECTION

The components were selected based on analysis and simulations. Simulation tests of the proposed circuit were performed in the MATLAB/Simulink environment. The basic parameters of the converter used in the simulation and experimental research are listed in Table I. The results demonstrate the quality of the converter, the relationship between the parameters, and the procedure for adjusting the parameters to the operating conditions. An inverter with an assumed input voltage and power can be rescaled for the desired applications.

The application of the MOSFET transistors and diodes listed in Table I ensures safe operation at the assumed input voltage and output power. The appropriate switching

TABLE I
PARAMETERS OF THE SIMULATION SETUP

Parameter	Type and range
Topology	Single-phase, with the input voltage divider
Output power	P_{out} = 50–500 W
Transistors	V_{DS} = 200 V, $R_{ds(on)}$ = 20mΩ
Diodes	V_F = 1.2 V, Q_{rr} = 640 nC
Dead time	100 ns
Input DC voltage	100–150 V
Modulation index	0.75–0.95
Output fundamental frequency	f_{out} = 500–1000 Hz
Switching frequency	f_S =60–100 kHz
Switched capacitor	C_S = 660–1100 nF
Resonant inductor	L_r = 1900–5700 nH

frequency f_S, resonant inductance L_r, and capacitance of the switched capacitor C_S were selected based on the optimization of converter efficiency.

B. SWITCHED CAPACITOR AND INDUCTOR FOR INRUSH CURRENTS MITIGATING

When the switching pattern determined by (4) and (5) is used (Fig. 2), the balancing circuit is used in the time interval when modulation at the highest levels is performed (e.g., during the time indicated in Fig. 7 as t_c).

The voltage across capacitor C_3 is maintained at the value of the input voltage (U_{C3}-U_{in}). The output current does not flow through the switched capacitor C_S and DC capacitor C_3 during the time intervals in which the instantaneous absolute value of the basic harmonic of the output voltage is in the interval of $\pm U_{in}/2$ (Fig. 9).

$$\left| m_a \frac{2}{3} U_{in} \sin(x) \right| \geq \frac{1}{2} U_{in} \tag{7}$$

The modulation interval in which C_3 capacitor and the switched capacitor are used starts when

$$m_a |\sin(x)| = \frac{1}{3} \tag{8}$$

For the maximum value of the modulation index $m_a = 1$, modulation at the highest positive level begins and ends at the following angle values:

$$x_{min} = x_1 = \arcsin\left(\frac{1}{3}\right) = 19{,}5 \text{ deg},$$
$$x_{max} = 160.5 \text{ deg} \tag{9}$$

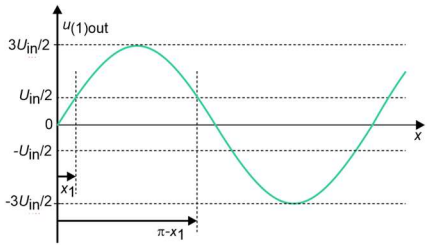


FIGURE 9. The fundamental harmonic of the output voltage.

Capacitor C_3 participates in modulation over a time interval:

$$t_c = \frac{2(x_{\max} - x_{\min})}{360} T_{ac} = 0.78 T_{\text{out}} \tag{10}$$

where $T_{out}=1/f_{out}$ is the fundamental period of output voltage.

The switched capacitor C_S is connected in series with inductor L_r to form a second-order circuit, in which the amplitude of the current depends on its characteristic impedance. Therefore, the choke in the circuit of the switched capacitor allows us to mitigate the peak values of the inrush currents that occur during the parallel connection of the switched capacitor to the voltage source. The inductance in this circuit ($C_S L_r R_{stray}$) determines its resonant frequency, which is close to the frequency of natural current oscillation. The resonant frequency is an important parameter in the design of the system, which is why the L_r choke is referred to as resonant choke (L_r).

The resonant frequency of this circuit (f_{sc}) was assumed to be higher than the switching frequency of the converter.

$$f_{sc} = \frac{1}{2\pi\sqrt{L_r C_s}} \geq f_s \tag{11}$$

During the period T_{out}, the number of recharges of the switched capacitor C_S is smaller than f_{sc}/f_{out}. This is because this circuit operates in time interval t_c, as defined by (10). Therefore, it is possible to introduce the average frequency of recharging C_S over a period of fundamental output frequency (T_{out}):

$$f_{sc\_av} = f_s \frac{t_c}{T_{\text{out}}} = 0.78 f_s. \tag{12}$$

When capacitor C_S is completely discharged and then charged to $2U_{in}$ from the DC-link capacitors in each switching cycle, the balancing circuit operates with its maximum power:

$$P_{SCmax} = 0.5 C_s (2U_{in})^2 f_{sc\_av} = 1.56 C_s U_n^2 f_s \tag{13}$$

In an inverter, the switched-capacitor resonant circuit cannot operate continuously at its maximum power (13) owing to the variation in the switching pulse width (Fig. 10). In some switching periods, the lead time of SP1a(b) or SN1a(b) is shorter than the half-period of the current oscillation in the L_rC_S circuit. This causes incomplete charging or discharging of the C_S capacitor and decreases the power of the switched-capacitor circuit. Therefore, the maximum power of a circuit with a switched capacitor in the inverter can be defined as

$$P_{SC\max\_inv} = 1.56 C_s U_{in}^2 f_s \alpha \tag{14}$$

where d is the coefficient and $d < 1$. Assuming $m_a = 1$, the duty factor at the highest modulation level changed from $D = 0$ to $D = 1$. Therefore, coefficient a approximates the value of $\alpha = 0.5$.

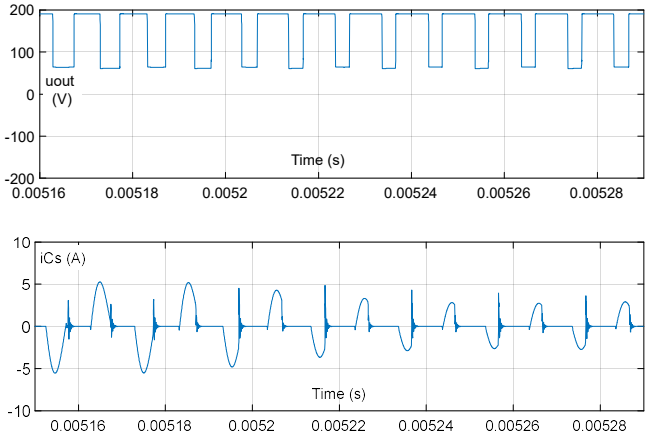


FIGURE 10. Variation of the modulation duty cycle during the time interval t_C and shortening the time of overcharging of the switched capacitor in the states SP1a(b) and SN1a(b). m_a = 0.8, L_r = 5700 nH, C_S = 1100 nF, f_S = 100 kHz. Matlab/Simulink results.

Assuming that the parameters of the tested inverter are fs = 60 kHz, U_{in} = 130V, C_S = 1100 nF, the maximum power of the resonant circuit is P_{SCmax} = 870 W. This value exceeds the assumed power of the inverter tested (P_{out} = 500 W). In the experimental tests, the capacitance value of capacitor C_S is assumed to be equal to C_S = 1100 nF because under real conditions, the maximum power of the resonant circuit to balance the voltage of capacitor C_3 will be lower than the theoretical value described in (14) due to the parasitic resistances of the circuits. This also ensures the possibility of operation in the event of inverter overload. Using the assumed value of the capacitance of the switched capacitor C_S, the value of the resonant inductance L_r is calculated based on (11).

An important design parameter is the current and voltage stress of the system components. Fig. 11 shows the current stress of the individual transistors in the inverter versus the load current. These results demonstrate that the output transistors (S_5 and S_6) are the least stressed transistors because they do not participate in voltage boosting. The highest current occurs in the switched-capacitor branch (S_7 and S_8), while transistors S_1-S_4 are loaded to a similar degree. Diodes D_1 and D_2 protect the balancing circuit against interruption of the choke current, and their current conduction times are very short. However, their switching losses can be important for inverter efficiency. The voltage and current stresses of the transistors in terms of maximum values are presented and compared with those of the reference inverters in Table IV.

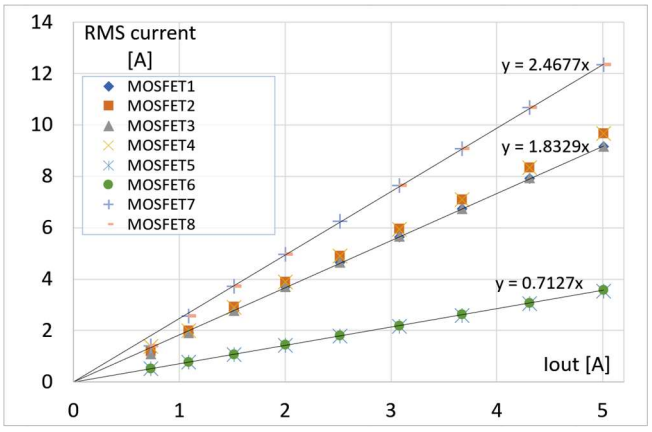


FIGURE 11. Current stress of the inverter transistors at m_a = 0.75, L_r = 5700 nH, C_S = 880 nF, f_S = 60 kHz. Matlab/Simulink results.

C. DESIGN GUIDELINES

The design process of the proposed boost-inverter is less typical than that of classic topologies because of the operation of an active balancing system. The input parameters are the input voltage range, modulation factor, and output power. In the first iteration, the switching frequency (f_s) is assumed.

The capacitance of the switched capacitor in the balancing circuit ensures adequate charging power for the floating capacitor (14), and the inductance of the resonant choke determines the resonant frequency of the circuit (11)

In the next step, it is possible to determine the voltage stress across switches that results from the topology and then the E_{oss} of the transistors (taking into account the switching loss limit). The approximate current stress of transistors (e.g., as in Fig. 11) allows us to estimate the conduction losses and finally select $R_{ds(on)}$ of transistors.

The iterative correction of the switching frequency affects the value of the switching circuit, as well as the parameters of the balancing circuit (L_r, C_S).

The selection of the DC-link capacitor capacitances, output filters, and gate drivers is analogous to that of typical inverter designs.

If the inverter does not satisfy the efficiency requirements, the design and parameters of the components that determine the energy loss, as well as the PCB, should be improved, which may increase the converter cost.

D. EFFICIENCY AND POWER LOSSES ANALYSIS IN THE SIMULATION MODEL

The simulation research was performed on a physical model created using the components of the Simscape library of the MATLAB/Simulink software. The model allows one to calculate the losses of semiconductor devices and the efficiency of the converter by considering the conduction and switching losses. The parasitic resistances of the passive components and connections as well as the losses of the output filter were also considered in the model.

The first assessment of the inverter efficiency focused on the selection of the switched capacitance in the balancing circuit. The results presented in Fig. 12 show a small positive effect of increasing the capacitance of the switched capacitor on the inverter efficiency. Additionally, an increase in the resonance inductance in the analyzed range increased the inverter efficiency (Fig. 13).

From the graphs showing the power losses in the inverter transistors (Fig. 14), it was possible to estimate their C_{oss} losses (at P_{out}= 0 W). For transistors S_1-S_4, P_{oss} = 0.47 W; for S_5-S_6, P_{oss} = 0.23 W, and for S_7-S_8, P_{oss} = 0.4 W. The total C_{oss} loss is P_{oss} = 3.14 W. Switching losses are also increased by diode losses and those of magnetic components.

The maximum efficiency estimation of the inverter can be performed under the assumption that the following main loss sources occur in the converter:

- conduction resistive losses $P_c = f(I_{out}^2)$,
- switching losses in semiconductor devices: $P_S = f(I_{out})$,
- C_{oss} losses that are independent of the load.

Diodes D_1 and D_2 are also lightly loaded because they are involved in conduction only during periods when the duration of the recharge of the switched capacitor is shorter than the resonant frequency of the LC elements of the balancing circuit. Their conduction losses can be neglected in this model.

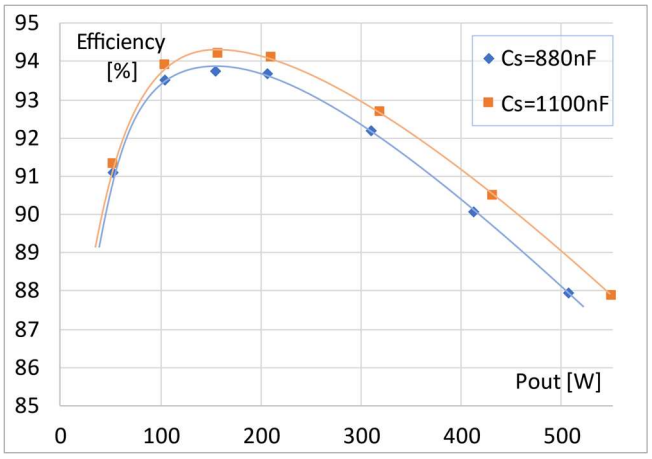


FIGURE 12. Efficiency characteristic for various capacitances of the switched capacitor in the inverter at m_a = 0.75, L_r = 5700 nH, f_s = 60 kHz, f_{out} = 1000 Hz. Matlab/Simulink results.

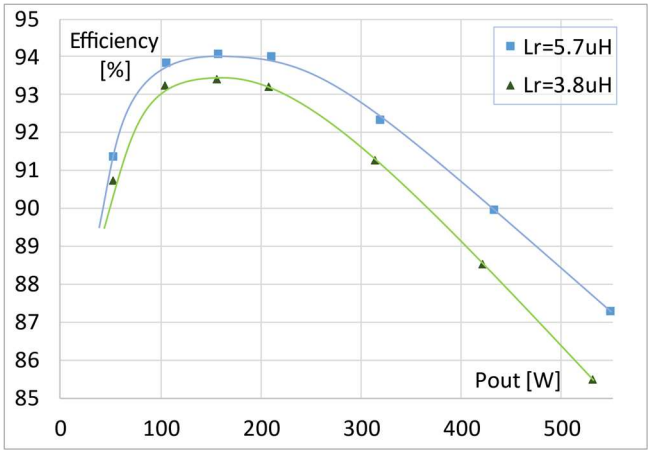


FIGURE 13. Efficiency characteristic for various resonant inductances in the inverter at m_a = 0.75, C_S = 880 nF, f_s = 60 kHz. Matlab/Simulink results.

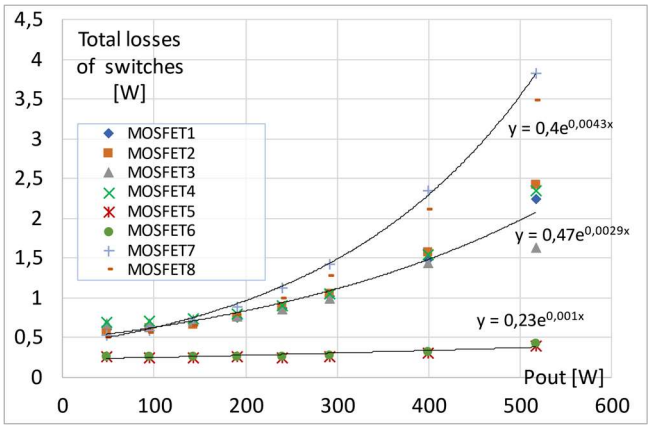


FIGURE 14. Power losses of the inverter transistors at m_a = 0.75, C_S = 880 nF, f_s = 60 kHz. Matlab/Simulink results.

Fig. 15 presents the total inverter loss characteristics and their approximations using a second-order polynomial. The approximation provides a function that depends on the load current; therefore, it can be used as an inverter loss model:

$$P_{\text{loss total}} = RI_{\text{out}}^2 + U_{\text{eq}}I_{\text{out}} + P_{\text{oss}} \quad (15)$$

where R is the equivalent of the total resistance of the inverter and U_{eq} represents the equivalent voltage component responsive to switching losses.

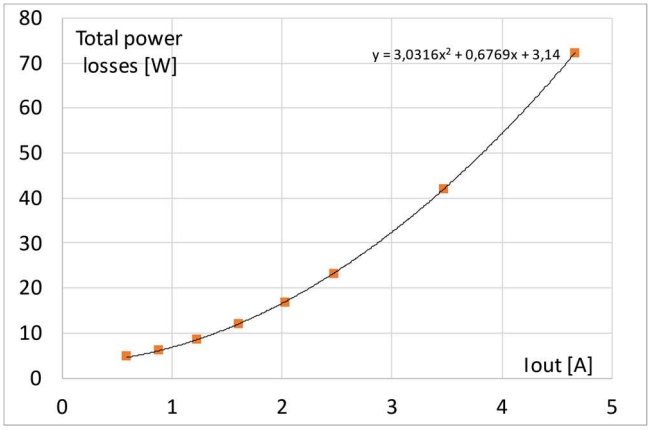


FIGURE 15. Total power losses of the inverter at m_a = 0.75, C_S = 880 nF, f_s = 60 kHz. Matlab/Simulink results.

Based on model (15), the inverter efficiency is expressed as follows:

$$\eta = \frac{P_{out}}{P_{out}+P_{loss}} = \frac{U_{out}I_{out}}{U_{out}I_{out}+RI_{out}^2+U_{eq}I_{out}+P_{oss}} \quad (16)$$

The derivative of the efficiency versus I_{out} gives:

$$\frac{d\eta}{dI_{out}} = \frac{U_{out}(P_{oss}-RI_{out}^2)}{(U_{out}I_{out}+RI_{out}^2+U_{eq}I_{out}+P_{oss})^2} \quad (17)$$

The following relationship provides the value of the current at which the efficiency reaches its maximum:

$$\frac{d\eta}{dI_{out}} = 0 \Longrightarrow (P_{oss} - RI_{out}^2) = 0 \quad (18)$$

The maximum efficiency occurs at a point dependent on the parameters P_{oss} and the equivalent loss resistance of the entire system R as follows:

$$\eta = \eta_{max} \Leftrightarrow I_{out} = \sqrt{\frac{P_{oss}}{R}}, \text{ for } R > 0 \quad (19)$$

From (19), it follows that a substantial resistance of the converter reduces the power at which the maximum efficiency occurs. In the experimental setup investigated, the maximum efficiency is located at the $P_{\text{out}} \approx 150$ W ($I_{\text{out}} \approx 1.5$ A). The parasitic resistances represent the PCB conduction losses at a high frequency of 60 kHz, transistor resistance, equivalent resistance of the resonant choke (L_r), switched capacitor (C_S), filter (L_F), and DC-link capacitors. It would be beneficial to reduce the resistive losses for high-frequency currents by using PCBs with a larger number of layers, capacitor banks with lower resistance, and reducing the resistance of transistors S_7 and S_8 by parallelizing them. The presented solution is cost-effective and is used to demonstrate the operation of the system (4-layer PCB typical stack with 35/18 µm copper thickness).

Fig. 16 shows the power loss balance in the converter transistors and diodes. The total losses in the elements were compared with the conduction losses calculated based on the values of the currents presented in Fig. 11 and the C_{oss} losses. Output transistors S_5 and S_6 are the least loaded transistors because they do not participate in the process of boosting the voltage by charging capacitor C_3.

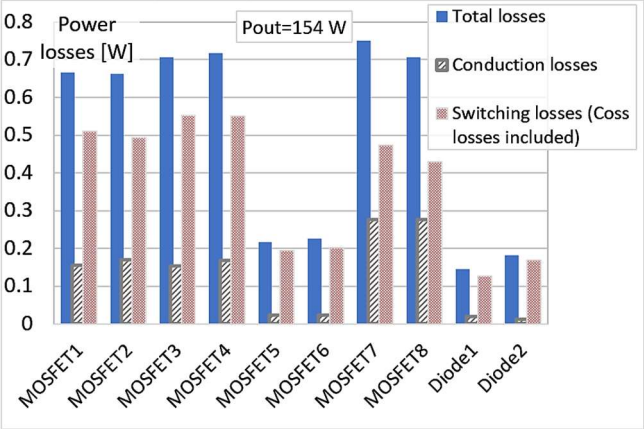


FIGURE 16. Power losses of semiconductor devices in the inverter for modulation index m_a = 0.75, L_r = 5700 nH, C_S = 880 nF, f_s = 60 kHz. Matlab/Simulink results.

The results showing the power loss balance in the semiconductor switches (Fig. 16) were obtained with the following physical parameters of the model: $R_{ds(on)}$ = 20 mΩ, C_{oss} ≈ 1500 pF, $V_{F,D1,D2}$ = 1.2 V, $Q_{rr,D1,D2}$ = 640 nC, resistance of the diodes R_D = 7 mΩ. The remaining capacitances of the modeled transistors have values of C_{iss} = 7100 pF and C_{rss} = 5 pF. The transistors are controlled by gate drivers with voltage V_{Gate_driver} = 15 V.

All simulation results were obtained using physical models of the elements, also containing the ESRs and distributed parasitic resistances in the branches of the system.

The results presented in Fig. 16 also show that, at the point of maximum efficiency, the semiconductor switches exhibit 5 W losses (3.2% of the output power). The conduction losses of transistors with resistance $R_{ds(on)}$ = 20 mΩ and output capacitance C_{oss} ≈ 1500 pF are less than the switching losses at this point. In the case of diodes D_1 and D_2, switching losses occur mainly. A reduction in switching losses in transistors and diodes, e.g., by using GaN transistors with a lower E_{oss}, would also be beneficial. From the operating principle of the circuit shown in Figs. 2 and 3, it follows that the transistors can be switched on at a charged output capacitance. For example, with a positive output current, during the dead time, the current flows through transistors S_2 and S_3, and transistor S_1 blocks the voltage to U_{in}. The output charge of transistor S_1 is then dissipated during the turn-on process (Fig. 2).

An analytical estimation of power losses can be performed using the inverter diagram presented in Fig. 17. It is seen from it that:

- there are three half-bridges in the main power circuit and the DC voltage of all of them is U_{in},
- the half-bridge composed of transistors S_5/S_6 conducts only the load current,
- the half-bridges composed of S_1/S_2 and S_3/S_4 conduct both the load current and the balancing current.

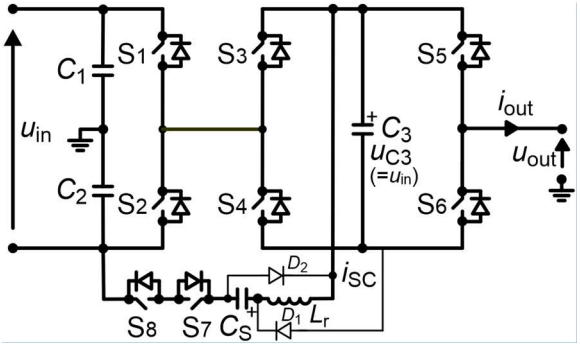


FIGURE 17. Inverter diagram for power loss analysis.

The output half-bridge transistors (S_5 and S_6) switch synchronously and the conduction power losses in this branch are:

$$P_{cS5/S6} = I_{out}^2 R_{ds(on)} \tag{20}$$

where I_{out} is the rms value of the sinusoidal output current.

Assuming that both transistors are equally loaded, their losses are as follows:

$$I_{S5}^2 R_{ds(on)} = I_{S6}^2 R_{ds(on)} = 0.5(I_{out}^2 R_{ds(on)}) \tag{21}$$

$$I_{S5} = I_{S6} = I_{S5\text{-}S6} = I_{out}(\sqrt{2})/2 = 0.707 I_{out} \tag{22}$$

Equation (22) shows the theoretical dependence between the rms value of a sinusoidal current of I_{out} and the pulsed wave of I_{S5} or I_{S6} that needs to be scaled by $1/(\sqrt{2})$. The current stress of the transistors presented in Fig. 11, obtained from the simulation model, shows an accurate approximation of the relationship (22) for transistors S_5 and S_6. For the remaining transistors of the main circuit, the relationship between the rms value of the current flowing through them and the output current is as follows (Fig. 11):

$$I_{S1\text{-}S4} = 1.83 I_{out} \tag{23}$$

Transistors S_1-S_4 conduct not only the load current but also the balancing current in some fragments of time, while through transistors S_7 and S_8 flows the full balancing current. The shape of the balancing current is created from pulses of variable amplitude, and its effective value is related to the load current as follows (Fig. 11):

$$I_{S7\text{-}S8} = 2.47 I_{out} \tag{24}$$

The relationships (22)–(24) also determine the current values in the individual branches of the system that cause losses in parasitic resistances (R_p). The estimation of this parameter should consider not only the DC resistance of PCB traces and connections but also the increase in resistance as a function of frequency and temperature. In the modeling result presented in

Fig. 18, this parameter was unified for all branches. The approximate resistive losses in the system are the following:

$$P_c = 4(I_{S1\text{-}S4})^2(R_{ds(on)S1\text{-}S4} + R_p) + 2(I_{S5\text{-}S6})^2(R_{ds(on)S5\text{-}S6} + R_p) + 2(I_{S7\text{-}S8})^2(R_{ds(on)S7\text{-}S8} + R_{ESRLrCs} + R_p) + I_{out}^2 R_{ESRLout} \quad (25)$$

where $R_{ESRLout}$ is the output choke resistance.

Figs. 2, 3, 5 and 9 show that the modulation varies depending on whether the voltage reference signal is greater or less than $U_{in}/2$. In order to determine the switching losses, the relation of these intervals to the half-period of the output voltage is important. The change in the modulation method occurs four times during the output voltage period, and the phase angle of the first change can be determined from the reference voltage equation described in relative values (related to U_{in}) for $0 \leq \omega t < \pi/2$ rad:

$$m_a(3/2)\sin(\omega t) = 1/2 \quad (26)$$

The angle at which the modulation method changes is as follows:

$$\omega t = \arcsin(1/3m_a) = x_1 \text{ (in Fig. 9), for } 1/3 \leq m_a < 1. \quad (27)$$

The subsequent changes take place at the angles $\pi - x_1$, $\pi + x_1$, and $2\pi - x_1$.

If $m_a < 1/3$, the converter does not implement higher levels of modulation. This is a simpler case, but it will not be analyzed.

In the half-period of the output voltage and when $x_1 \leq \omega t < \pi - x_1$, transistors S_1-S_6 operate at frequency f_s. In the half-period of output voltage when $0 \leq \omega t < x_1$ and $\pi - x_1 \leq \omega t < \pi$, transistors S_5-S_6 do not operate, the switching frequency of transistors S_1-S_4 is $f_s/2$ each and that of transistors S_7-S_8 is equal to f_S. The average operating frequencies of transistors are therefore as follows:

$$f_{S5\text{-}S6} = f_S(1\text{-}2x_1/\pi) \quad (28)$$

$$f_{S1\text{-}S4} = f_S(1\text{-}2x_1/\pi) + (f_s/2)(2x_1/\pi) = f_s[(1\text{-}x_1/\pi)] \quad (29)$$

$$f_{S7\text{-}S8} = f_S(2x_1/\pi) \quad (30)$$

The C_{oss} losses can therefore be expressed as follows:

$$P_{Coss} = 0.5C_{oss}U_{in}^2[0.5(4f_{S1\text{-}S4}+2f_{S5\text{-}S6})] + 0.5C_{oss}(0.75U_{in})^2 2f_{S7\text{-}S8} \quad (31)$$

Equation (31) uses the assumption that the voltage across transistors S_7 and S_8 is divided equally, and in each branch of the main inverter circuit, only one transistor has a hard turn on.

To calculate the switching losses, the current value of the transistors is required. Through transistors S_1-S_4 the current flows throughout the half-period of the output waveforms, while in S_5 and S_6 in the interval $x_1 \leq \omega t < \pi - x_1$. It is assumed that transistors S_7 and S_8 do not have switching losses and operate in the ZCS mode. Zero balancing current at switching times does not increase the switching losses in transistors S_1-S_4, either. Approximately the switching energy of the transistor during the switching period determined by the time point tx will be as follows:

$$e_{s,Sn}(t_x) = 0.5i_{Sn}(t_x)(t_r+t_f)U_{in} \quad (32)$$

where t_r and t_f are the rise and fall times of the transistor voltage.

The output current of the inverter is assumed to be described by the following function:

$$i_{out} = (\sqrt{2})I_{out}\sin(\omega t) \quad (33)$$

To calculate the switching losses, the average values of the switching energy of the S_n transistor from the intervals of a given switching frequency will be used

$$E_{s,Sn} = 0.5I_{sw,av,Sn}(t_r + t_f)U_{in} \quad (34)$$

where: $I_{sw,av}$ is the average current in the time interval of the transition. For $x_1 \leq \omega t < \pi - x_1$, its average value during switching for transistors S_1-S_4 (S_5 i S_6 they do not operate in this range) is equal to:

$$I_{sw,av,S1\text{-}S4} = 0.5(\sqrt{2}/\pi)I_{out}2\cos(x_1) = ((\sqrt{2})/\pi)I_{out}\cos(x_1) \quad (35)$$

In turn, when $0 \leq \omega t < x_1$, it yields for all transistors:

$$I_{sw,av,S1\text{-}S6} = ((\sqrt{2})/\pi)I_{out}(1 - \cos(x_1)) \quad (36)$$

Switching losses in the main circuit transistors are then the following:

$$P_s = 0.5U_{in}(t_r + t_f)\left[4\frac{f_s}{2}\frac{\pi-2x_1}{\pi}I_{sw,av,S1-S4} + 6f_s\frac{2x_1}{\pi}I_{sw,av,S1-S6}\right] \quad (37)$$

This relationship, taking into account (35) and (36), can be written differently:

$$P_s = U_{in}I_{out}(t_r + t_f)\frac{\sqrt{2}}{\pi}f_s\left[6\frac{x_1}{\pi} - \cos(x_1)\left(8\frac{x_1}{\pi} - 1\right)\right] \quad (38)$$

Reverse recovery losses in the reverse diodes are as follows:

$$P_{rr} = 0.5U_{in}\frac{1}{3}Q_{rr}[2f_{S5-S6} + 4f_{S1-S4}] \quad (39)$$

Since during dead-time the current flows through the reverse diodes, and these losses are much higher than in the transistor, the dead-time losses in reverse diodes will be added to the conduction losses:

$$P_{dt} = 0.5\frac{\sqrt{2}}{\pi^2}V_F I_{out}t_{dt}f_s[(\pi - 2x_1)\cos(x_1) + 6x_1(1 - \cos(x_1))] \quad (40)$$

Taking into account equations (25), (31), (38), (39) and (40), the inverter efficiency model is obtained:

$$P_{tot} = P_c + P_{Coss} + P_s + P_{rr} + P_{dt} \quad (41)$$

Equation (41) gives an unusual efficiency model due to the topology and modulation of the inverter analyzed. The analytical model described by (41) is presented graphically in Fig. 18 The loss model neglects the losses in the protection diodes D_1 and D_2. Furthermore, the measured efficiency will be lower due to magnetization losses of the output filter choke core and ESR in capacitors, which is typical for all inverters, but for calculation it requires knowledge of passive component materials.

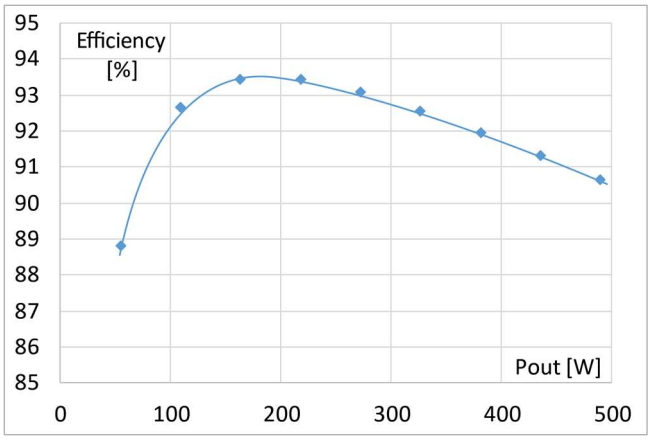


FIGURE 18. **Analytical characteristic of inverter efficiency m_a = 0.75, V_F = 1.2 V, V_{in}=130V, $R_{ESCLout}$ = 100 mΩ, R_p = 150 mΩ., f_s = 60 kHz, t_r = t_f = 50 ns, t_{dt} = 100 ns, C_{OSS} = 1.53 nF, Q_{rr} = 640 nC.**

IV. EXPERIMENTAL RESULTS

The parameters selected for the experimental setup are listed in Table II and a photograph of the inverter is shown in Fig. 19. The modulation concept is implemented in FPGA hardware in a system that integrates carrier-based pulse generators and state-machine decoders (Fig. 20).

FIGURE 19. **The laboratory model of the inverter.**

Based on the simulation results of the efficiency achieved, further experimental research was performed for the capacitance of the switched capacitor of 8800 nF and the resonant inductor inductance of 5700 nH in the balancing circuit. The experiments were performed using the modulation principle described in Section I and were generated using FPGA-based hardware.

The AC filter (Table II) is connected externally to the main inverter module (Fig. 26).

The experimental results are shown in Figs. 21–25. The measured logic switching signals are presented in Fig. 21 together with the output voltage of the inverter. This result shows the modulation of all transistors and its effect on the output voltage. The input voltage for this demonstration was reduced to produce clear and readable waveforms.

TABLE II
PARAMETERS OF THE EXPERIMENTAL SETUP

Quantity	Type and range
Output power, P_{out}	50 – 400 W
Input DC voltage, U_{in}	130 V
Switching frequency, f_S	60 -100 kHz
Output fundamental frequency, f_i	500 Hz
Transistors	IPB107N20N3
Diodes	DPG60IM300PC
Gate drivers	1EDI60H12AH
Controller	FPGA Intel Cyclone V
Switched capacitor, C_S	8800 nF
Resonant inductor, L_r	5700 nH
Output filter, C_F, L_F	4400 nF, 147 µH
Dead time	100 ns
Laboratory equipment	Oscilloscope: MSO6 Tektronix, Power meter: Yokogawa WT 1800, Power analyzer: Hioki PW 8001.
Size and weight of the inverter module presented in Fig. 19	Size: 125 x 125 x 65 mm Weight: 520 g

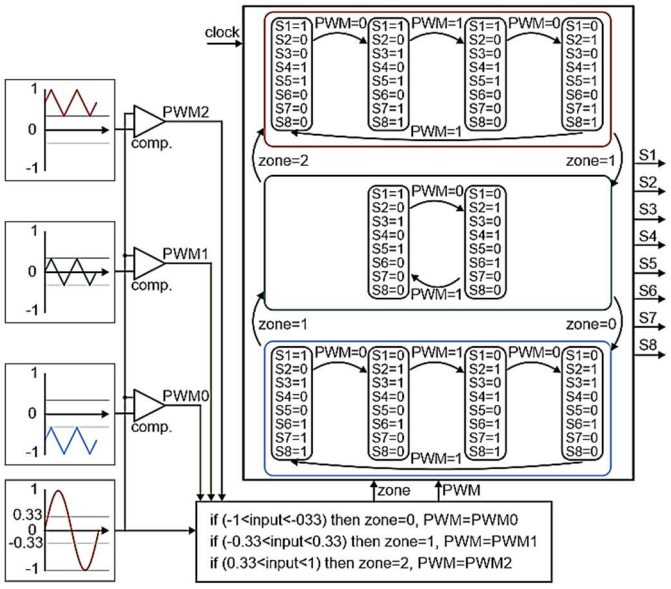


FIGURE 20. **PWM concept for the inverter (S*n* represents logic control signals of transistors).**

The waveforms of the voltages and currents of the loaded inverter are shown in Figs. 22 and 23, respectively. From these waveforms, it is observed that the modulation of the output voltage is implemented correctly and that the voltage on the floating capacitor is maintained at the level of the input voltage. The waveforms shown in Fig. 22 demonstrate that the balancing circuit works with oscillating current waveforms. This is very important and shows that the floating capacitor is charged without the risk of inrush currents, as occurs in some switched-capacitor systems where capacitors are connected in parallel with a voltage source.

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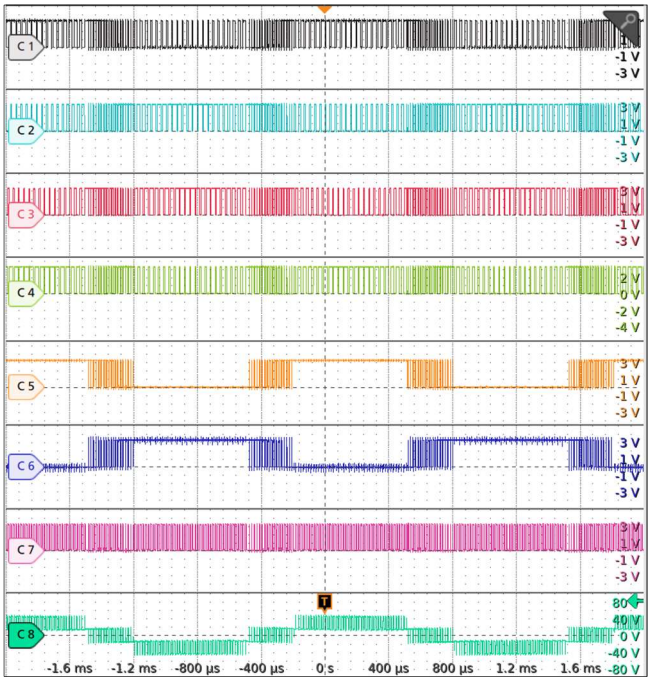
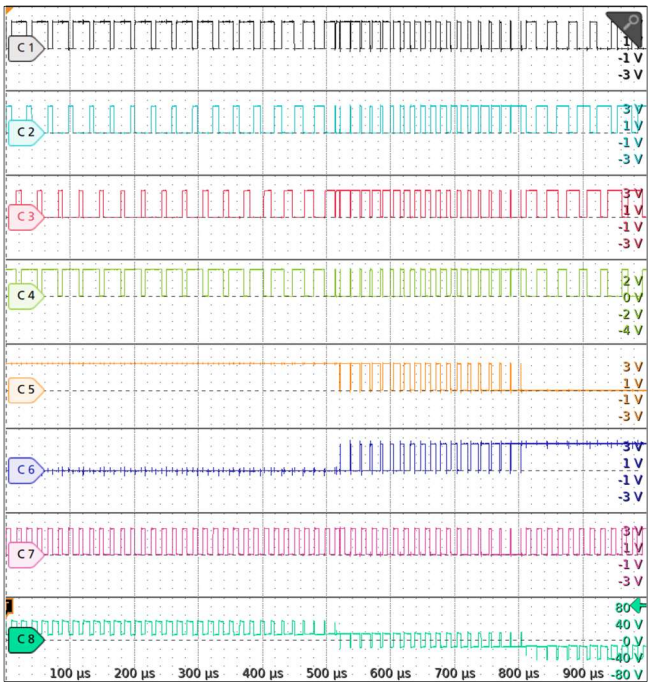
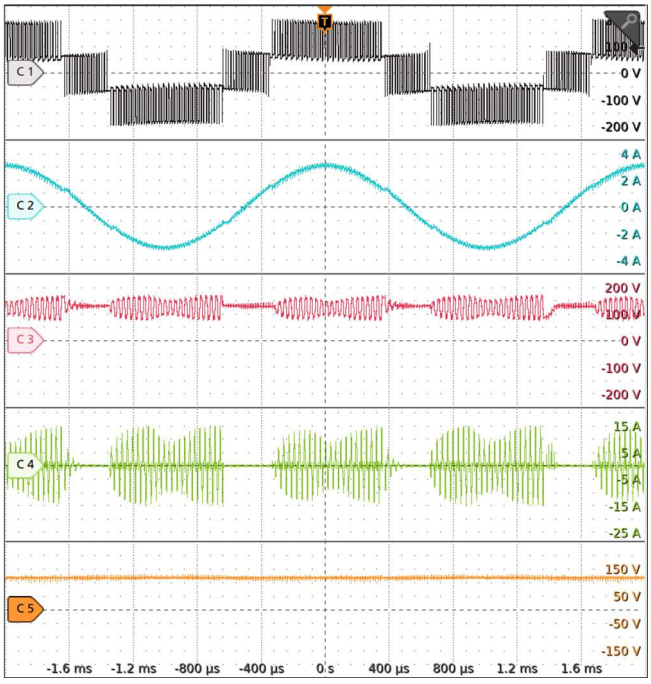


(a)

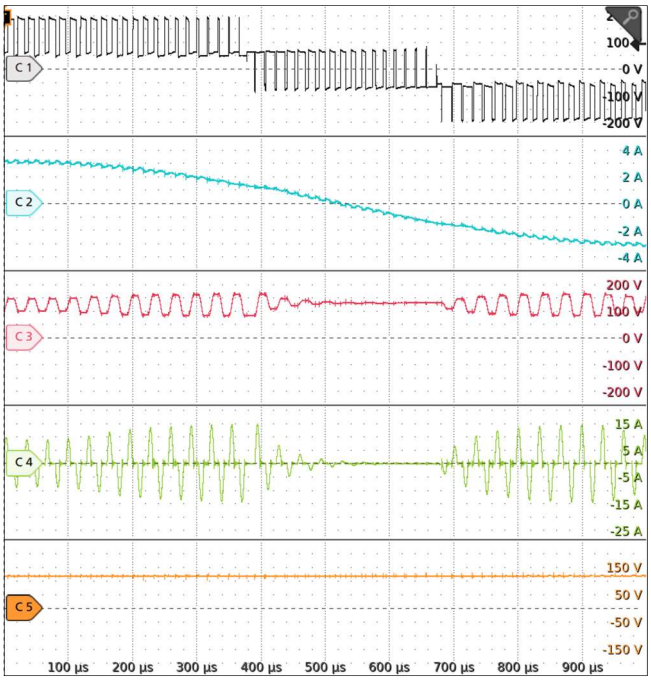


(b)

FIGURE 21. **Modulation pattern. Gate signals of transistors (C1-C7) and inverter output voltage (C8). (a) Steady-state waveforms in the time interval of two fundamental frequency periods. (Gate signals for transistors S1-S6 are displayed in channels C1-C6, and control signal of S7 and S8 - in channel C7). (b) Zoomed waveforms.**



(a)



(b)

FIGURE 22. **Waveforms of voltages and currents of the inverter. C1 - inverter output voltage, C2 - load current, C3 - voltage across the switched capacitor, C4 - current of the resonant inductor, C5 - voltage across the auxiliary DC capacitor (C_3). P_{out} = 200 W. (a) Steady-state waveforms in the time interval of two fundamental frequency periods. (b) Zoomed waveforms.**

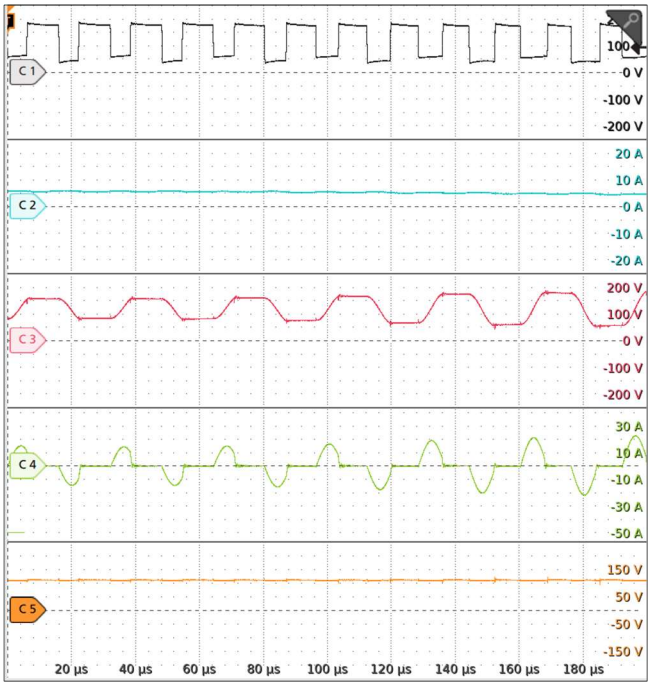


FIGURE 23. Waveforms of voltages and currents of the inverter. C1 - inverter output voltage, C2 - load current, C3 - voltage across the switched capacitor, C4 - current of the resonant inductor, C5 - voltage across the auxiliary DC capacitor (C_3). P_{out} = 350 W.

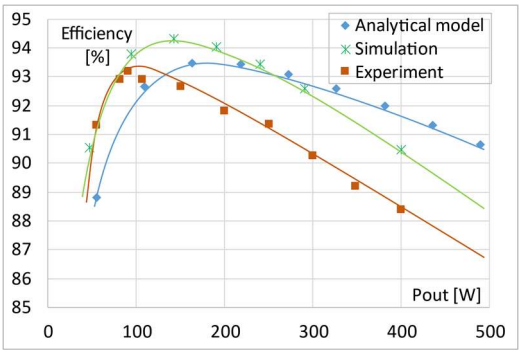
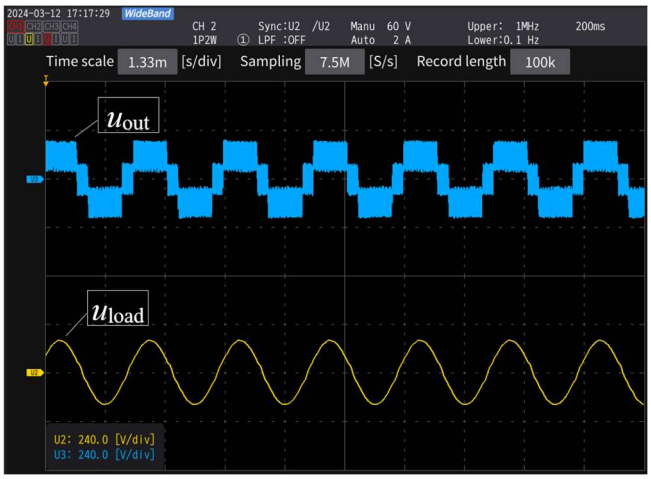


FIGURE 24. Results of efficiency measurement. Inverter parameters as shown in Table II. Comparison to results of analytical modeling (Fig. 18) and simulations (Fig. 12).

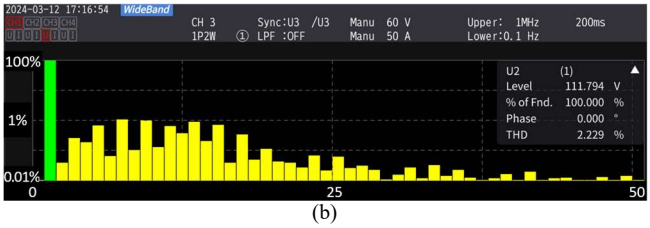
Fig. 24 shows the measured values of the inverter efficiency. The measurements were made using a Yokogawa WT 1800 power meter. Compared to the results of the analytical modeling (Fig. 18), a convergence in the maximum efficiency is seen, and some deviations in the rate of efficiency decrease with an increase in power (3.3% for P_{out} = 400 W and about 4% difference is seen approximating the experimental characteristics to P_{out} = 500 W). As stated in Section IIID, the analytical model did not contain some losses, such as losses in the protection diodes D_1 and D_2, magnetization losses of the inductors, and those in the ESRs of the capacitors. Greater convergence can be achieved by modifying the C_{oss} value of the capacitors with respect to the catalog data and changing the resistive parameters. As a result of simulation studies, a better convergence was obtained for small and large power values to the experimental results (the difference for P_{out} = 400 W is about 2% and for approximated characteristics to P_{out} = 500 W about 1.5%) and about 1% difference in the maximum efficiency values. To improve the efficiency of the inverter, the parasitic resistances of the devices and the PCB should be decreased.

Fig. 25a shows the results of the voltage quality measurements of the load supplied by the inverter with *LC* filter (filter parameters in Table II). The waveforms presented in Fig. 25a show the inverter voltage and the voltage at the output of the AC filter. The RMS value of the load voltage was 110V in this test.

Fig. 25b shows the voltage and current spectra of the load powered by the inverter. The THD value of the load voltage in this test was 2.229%, and the RMS value of none of the harmonics exceeded 1% of that of the fundamental harmonic.



(a)



(b)

FIGURE 25. Waveforms of the inverter and load voltages (a) and results of harmonic analysis of the load voltage (values of harmonics are related to the fundamental harmonic and the result is presented in logarithmic scale). RMS value of the load voltage is 110 V and its THD is 2.229%.

To verify the dynamics of the converter in transient states, inverter operation tests were performed using closed-loop control. The tests were performed for an inverter with an *LC* filter and resistive load. Fig. 26 presents a block diagram of the closed-loop control system in which the tests were performed. This concept assumes that the reference output voltage signal (U_{LOAD_ref}) is constant, which can reflect the requirements of backup power supply systems. At the start of the system, the signal increased with the ramp-on. The theoretical value of the modulation index m_{est} was calculated from the reference output voltage signal and the measured value of the input voltage (u_{in}). If the output voltage differs

from the voltage based on the theoretical modulation index, then the voltage controller corrects the reference voltage signal to the PWM generator.

The waveforms shown in Fig. 27 demonstrate the behavior of the system that controls the load voltage in a closed-loop control system. From the waveforms presented in Fig. 27, it can be observed that the load voltage remains constant when the input voltage decreases by ΔU_{in}. A change in the input voltage also results in a change in the maximum value of the modulated voltage at the inverter output. However, the RMS value of the load voltage was maintained by a change in the modulation index of the control system. From this case of closed-loop control regulation, it can be observed that the system can operate stably using this control system, and the detailed selection of the controller parameters depends on the application parameters of the system in which the inverter is used.

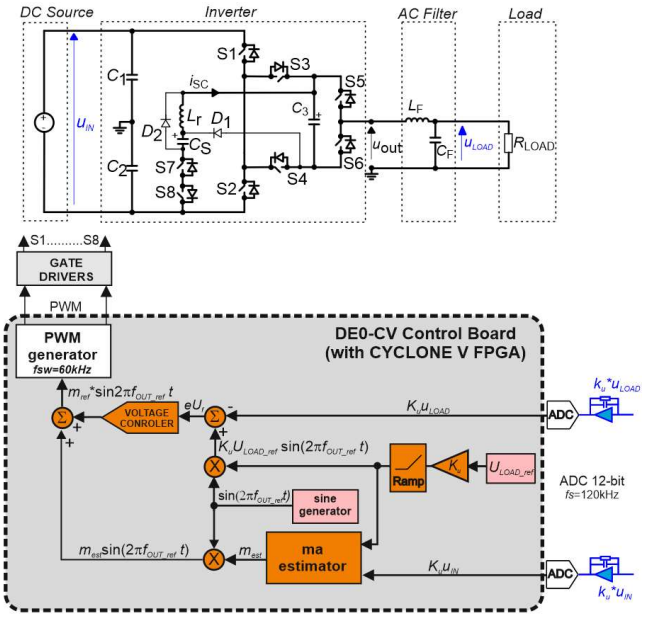


FIGURE 26. Block diagram of the inverter closed-loop control system based on the FPGA Cyclone V controller.

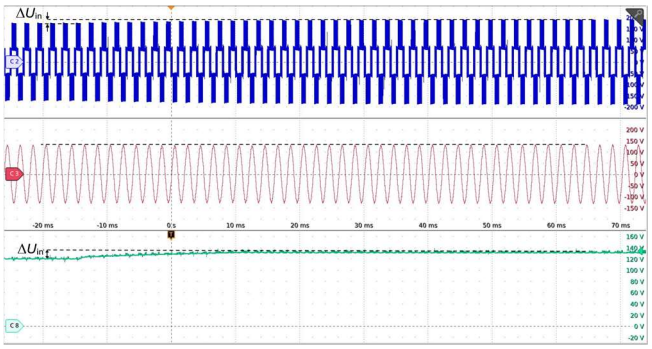


FIGURE 27. Waveforms of the inverter and load voltages during transient-state operation in a closed load voltage control system. C2 - inverter output voltage (u_{OUT}), C3 – load voltage (u_{LOAD}), C8 – DC input voltage (u_{IN}).

V. COMPARISON

Table III provides data to compare the proposed inverter with a DC-AC system with a DC link, a DC-DC converter, and a 3-level NPC inverter. The proposed inverter has a significant advantage in this comparison because it operates at a DC voltage that is three times lower, which reduces the voltage stress of the transistors.

One of the applications of the proposed boost-inverter topology may be in photovoltaic systems. In [29], a review of step-up transformerless photovoltaic DC-AC topologies is presented. The efficiency of single-phase single-stage topologies is in the range of 80-94.5%. The boost-inverter proposed in this study (Fig. 1) achieves a comparable efficiency level (Fig. 21). Numerous DC-AC boost-inverter topologies are also presented in [29].

TABLE III
BASIC PARAMETERS OF THE PROPOSED BOOST-INVERTER COMPARED TO CASCADE SYSTEMS WITH A DC-DC BOOST CONVERTER AND AN INVERTER

System Parameters	DC-DC boost and 2-level inverter	DC-DC boost and 3-level NPC inverter	Proposed
Number of phase-to-phase output voltage levels	3	5	7
DC-link voltage	$V_{\text{p-pmax}}$	$V_{\text{p-pmax}}$	$V_{\text{p-pmax}}/3$
Voltage stress across devices	$V_{\text{p-pmax}}$ for all devices	$V_{\text{p-pmax}}$ for boost parts, and $V_{\text{p-pmax}}/2$ for inverter parts	S1-S6: $V_{\text{p-pmax}}/3$ S7-S8: $2V_{\text{p-pmax}}/3$
Processed power for boosting	100%	100%	Part (boosting is not implemented at the medium modulation level)
Choke for boosting	Typical power choke for DC-DC	Typical power choke for DC-DC	Resonant (low volume, low energy)

Another class of boost inverters is that of systems that operate on the principle of a switched-mode converter with an input choke and an output capacitor. Reference [30] presents an inverter with buck-boost characteristics, for which the maximum efficiency is 97.4%. Reference [31] shows a grid-connected inverter based on the buck-boost topology and demonstrates results at the input voltage 110 V DC, the output voltage 110 V rms, and a current equal to 5 A. This inverter achieves 5 levels using 10 transistors, two flying capacitors, and two chokes, reaching a peak efficiency of 95.1%. Reference [32] presents the concept of a split-source high-boost inverter with an input cell containing two inductors, a capacitor, and two diodes, which is connected to the branches of the two-level inverter by diodes. Its efficiency demonstrated is 91%. A T-type boost-inverter with a switched-capacitor-based input circuit is shown in [33]. This results in a three-phase bidirectional converter that amplifies the voltage by adding a circuit of three transistors and two capacitors, but without the use of chokes. A system

TABLE IV
PARAMETERS COMPARISON BETWEEN THE PROPOSED INVERTER AND ANPC-BASED BOOST INVERTERS

	Ref. [16]	Ref. [17]	Ref. [18]	Ref. [19]	Ref. [20]	Ref. [21]	Ref. [22]	Ref. [23] Fig. 1c	Ref. [24]	Ref. [25]	Proposed
No. of levels (per phase)	7	7	7	7	11	5	5	5	5	5	4
Count of transistors (N_T)	9	10	8	10	12	8	6*	10	9	8	8
Count of diodes in power circuit (N_D)	0	0	0	0	0	0	2*	0	**2**	0	0**
Count of auxiliary capacitors per phase	1x DC	1x DC	2x flying	2x flying	2x flying	1x DC	1x flying	1x flying	1x DC 1x switched	1x DC	1x DC 1x switched
Auxiliary inductors	no	no	no	no	no	no	no	no	1x resonant	no	1x resonant
Voltage stress across transistor (per V_{DC})	*****	8x1 2x($^1/_2$)	2x($^1/_2$) 2x($^3/_8$) 2x($^1/_4$) 2x($^1/_8$)	6x1 2x2 2x($^1/_2$)	4x2 6x1 2x($^1/_2$)	6x($^1/_2$) 2x1	4x($^1/_2$) 2x($^1/_4$)	8x($^1/_2$) 2x1	9x($^1/_2$) 2x($^1/_2$)	6x($^1/_2$) 2x1	6x1 2x2
Capacitors switched in parallel	yes	yes	yes	yes	yes	yes	yes	yes	no	yes	no
Inrush current mitigation	no	no	no	no	no	no	no	no	low inrush current	low inrush current	yes (in resonant circuit)
Maximum current of transistors ***	-	2x: $I_{o,m}+I_{C,m}$ 6x: $I_{o,m}$ 2x: ($I_{o,m}$ or $I_{C,m}$)	2x****: $I_{o,m}+I_{C,m}$ 6x: $I_{o,m}$	4x: $I_{o,m}+I_{C,m}$ 6x: $I_{o,m}$	-	-	-	4x: $I_{o,m}+I_{C,m}$ 4x: $I_{o,m}$	-	-	4x: $I_{o,m}+I_{C,m}$ 2x: $I_{o,m}$ 2x: $I_{C,m}$
Phase gain (per V_{DC})	1.5	1.5	2	1.5	2	2	2.5	1	1	1	1.5
Efficiency (DC input voltage and power)	-	-	98.2% (400 V, 1.4 kVA)	98.3% (100 V, ca. 52W)	96.67% (100 V)	-	99% (400 V, 1.5 kW)	98.2% (400 V, 2.2 kW)	>97% (800 W)	ca. 98.6% (400 V, 1.5 kW)	93.2% (130 V, ca. 90 W)
THD of load current	0.92	-	2.15	-	-	-	-	-	-	-	2.29
TSV(xV_{DC})	8	9	2.5	11	15	5	2.5	5	5.5	5	10
TCV(xV_{DC})	1	1	1.25	2	2	1	1	1	0.5	1	1
Cost function CF (42): for $\alpha = 1, \beta = 1$	2.7	3.0	2.0	3.6	2.8	3.0	2.5	3.4	3.6	3.0	5.0
for $\alpha = 0.5, \beta = 1$	2.1	2.4	1.8	2.8	2.1	2.5	2.3	2.9	3.1	2.5	3.8
Cost function $CF2$ (43): for $\alpha = 1, \beta = 1$	1.8	2.0	1.0	2.4	1.4	1,5	1.0	3.4	3.6	3.0	3.3

Note: Empty cells indicate that the data presented in the literature are insufficient for comparison.
* The inverter contains two RB IGBTs with two body diodes.
** The proposed converter uses diodes, but only for protection against the open circuit of the choke.
*** The current contains the maximum values of the output component $I_{o,m}$ and the component required for auxiliary capacitors charging $I_{C,m}$.
**** Switches in a bipolar voltage-blocking structure.
***** The reference provides Total Voltage Stress (TVS) parameter TVS = $16 \cdot V_{step}$.

based on an ANPC inverter with 5 levels is shown in [34]. It is a converter with a double boost circuit at the input common for all phases (composed of two 300 µH chokes and two transistors) so that the gain is greater than one and regulated by duty cycle. The layout demonstrated in [34] also uses 8 transistors per phase and achieves an efficiency of 97%. The Y-inverter presented in [35], which is made up of buck and boost bridges, demonstrates an efficiency of 97.2%. The prototype was compared with a conventional boost VSI, with an efficiency of 95.5%. In [36], a phase-modular converter with buck-boost cells also exhibits high efficiency (>98.5%), and in [37], a concept with 97% efficiency is demonstrated in the DC-AC mode of operation.

Inverter systems with impedance source (IS) networks are also a solution for the implementation of a single-stage DC-AC transformation. Reference [38] presents a comparison of selected multilevel buck-boost inverters with IS networks, with a detailed reference to the energy stored in capacitors and diodes, as well as the voltage stresses across the devices. An example of an inverter of this type is the 3-level quasi-switched boost F-type inverter shown in [39] using a circuit with a switched capacitor. At V_{DC} = 130 V the inverter efficiency reported in [39] was 93.7 %.

The boost-inverter proposed in this paper is not a concept based on buck-boost cell derivatives but an inverter topology based on the concept of the ANPC system. Therefore, it is also important to compare them with the systems presented in [16]–[25]. Table IV summarizes the parameters of the referenced boost inverters and the proposed inverter (Fig. 1).

The cost function CF presented in Table IV uses the definition as in [24]:

$$CF = \frac{N_T + N_D + N_C + \alpha \cdot TSV + \beta \cdot TCV}{N_L} \quad (42)$$

where TSV and TCV are the total standing voltage of the transistors and the total capacitor voltage related to V_{DC}, α

and β are numerical coefficients, while N_L, N_T, N_D and N_C indicate the number of levels, transistors, diodes, and capacitors (excluding input capacitors) of the inverter.

The cost function can also be proposed as considering the gain of the inverter, which is an important parameter in this class of converters:

$$CF2 = \frac{N_T+N_D+N_C+\alpha \cdot TSV+\beta \cdot TCV}{N_L \cdot G_U} \quad (43)$$

where G_U is the voltage phase gain per V_{DC} (Table IV).

From the comparison in Table IV, it appears that the proposed inverter is advantageous due to the limited charging current of the floating capacitors. In converters in which the floating capacitor is connected in parallel with the DC with link capacitors, it is difficult to predict the value and effects of inrush currents (e.g., for the EMC emission level of the target system, the current stress of the semiconductor components, or reliability). The proposed inverter has more transistors in relation to the number of levels in the topology than those presented in [16]–[25], but it has a limited inrush current that occurs when the capacitors are loaded in parallel connections.

VI. CONCLUSION

From the analysis presented of the new inverter concept, the results of its operation and the design of the experimental system, the following conclusions were drawn:

1) The inverter achieves an output voltage at a level that is three times higher than that of a two-level inverter.
2) The inverter gains voltage without the use of a DC-DC converter, which reduces the volume of the converter, as the DC-DC converter chokes and the transistor and diode designed for higher voltage stress values are eliminated.
3) Compared to the DC-AC system with a DC link and a DC-DC converter, the proposed inverter operates at a three-time lower DC voltage, which can significantly reduce the cost of the elements. This is summarized in Table III.
4) The system uses an additional floating capacitor that is recharged by a switched-capacitor-based balancing circuit with control synchronized with the inverter transistors.
5) The method of voltage control across the auxiliary capacitor does not require measuring its voltage.
6) The balancing circuit converts only part of the converter energy because a floating capacitor is not used in all operating states of the inverter. The balancing circuit utilizes a very low-volume resonant choke, and energy is mainly transferred by the switched capacitor.
7) The proposed converter can operate as a boost-inverter and buck-rectifier.
8) In the proposed system topology and the use of a resonant circuit with a switched capacitor, the occurrence of an inrush current in the switched capacitor is avoided.
9) An efficiency greater than 93% was achieved in the inverter efficiency measurement. The tests were performed at a low input voltage (130 V) in a MOSFET-based circuit and were implemented on a typical PCB laminate. The theoretical efficiency of the inverter, calculated based on the losses in the system components, is significantly higher. An efficiency higher than that demonstrated in this study can be achieved in systems with improved parasitic parameters, such as multilayer PCBs.

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