Three-Phase Diode-Clamped Four-Level PWM Inverter with Offset Voltage Injection

MIN-SUP SONG[1], JAEWON KIM[1], AND HWAN-HEE CHO[1]

[1]Electrification System Research Department, Smart Electrical & Signaling Division, Korea Railroad Research Institute, Uiwang-si 16105, Korea

Corresponding author: Min-Sup Song (e-mail: mssong@ krri.re.kr).

ABSTRACT In this paper, a three-phase diode-clamped four-level PWM inverter with offset voltage injection is proposed. The proposed inverter is based on multi-neighboring reference vector (discontinuous) pulse-width modulation (MNRV (D)PWM), where multiple adjacent reference vectors with different charging/discharging characteristics of the capacitors are selected depending on the location of the command voltage. These reference vectors are evenly utilized, and the duty ratio of the remaining reference vector as a degree of freedom is adjusted to satisfy the *volt·time* product. Additionally, the proposed MNRV (D)PWM can generate various (D)PWM forms by applying the offset voltage injection method. By extending the methodology applied to the four-level inverter, a general MNRV (D)PWM method applicable to general high-dimensional multilevel multiphase PWM inverters is also proposed. It is demonstrated that MNRV (D)PWM can be applied not only to dc/ac but also to dc/dc topologies. The ripple component of the dc-link voltage has been confirmed to be related to the three-phase summation of the product of the duty of the E voltage level vector and the phase current. Through various simulations and prototype experiments, the steady-state operating characteristics have been confirmed, demonstrating reduced average switching frequency and superior THD performance compared to conventional methods. Furthermore, proficient management of fluctuations in the dc-link voltage reference and sustained voltage equilibrium are exemplified.

INDEX TERMS three-phase PWM inverter, diode-clamped, four-level, dc-link voltage balancing, offset voltage injection, multi-neighboring reference vector discontinuous PWM

I. INTRODUCTION

Multilevel converters, including diode-clamped, flying capacitor, cascaded H-bridge topologies, and modular multilevel converters (MMC), are widely used in medium to high-power applications like renewable energy systems, motor drives, and high voltage direct current (HVDC) transmission systems. These converters provide benefits such as improved voltage/current quality, reduced switching losses, enhanced power handling, modularity, scalability, and high reliability [1]−[7].

The diode-clamped method is especially popular due to its simple power stage configuration. However, maintaining balanced voltages across dc-link capacitors, particularly in higher levels like four-level or above, is challenging but essential for stable operation and enhanced performance [8]−[12]. Extensive research has focused on addressing this voltage balancing issue over the past few decades.

Common methods for voltage balancing in diode-clamped circuits include active voltage balancing circuits [13]−[15], model predictive control (MPC) [16]−[18], and artificial intelligence (AI)-based control [19]−[21]. Active voltage balancing circuits use additional power electronics components like choppers or active switches to transfer energy between dc-link capacitors, ensuring stable operation by real-time monitoring and precise adjustments. However, this method involves complex implementation, additional power consumption, and limited effectiveness during rapid load changes. MPC predicts future system behavior and optimizes control inputs to achieve voltage balance, offering high performance, flexibility, and fast transient responses. Despite its advantages, MPC faces challenges like computational complexity, implementation difficulties, and model accuracy issues. AI-based methods utilize techniques such as neural networks, fuzzy logic, and genetic algorithms to optimize voltage levels by leveraging

system data. Trained on historical data and simulations, these models enhance performance, efficiency, and reliability. However, AI methods present challenges including training complexity, interpretability, and hardware implementation difficulties.

Meanwhile, two widely recognized methods in the industry to address voltage balancing issues are virtual-vector PWM (VVPWM) [22]−[26] and carrier-overlapped PWM (COPWM) [27]−[30]. VVPWM uses virtual reference vectors to ensure that the sum of related currents is zero, effectively eliminating voltage imbalances within the carrier cycle. It is easy to implement with carrier-based equivalent PWM methods [26]. However, VVPWM has high total harmonic distortion (THD) at high amplitude modulation indexes (m) and incurs relatively high switching losses due to the narrow clamping region of the outermost vectors within a 120° interval. COPWM achieves voltage balancing using intricately designed overlapping carriers with a single command voltage. This method ensures uniform duty ratios of intermediate voltage levels, naturally satisfying the *volt·time* product. However, COPWM suffers from low power quality at low m due to frequent transitions between clamp and normal modes, leading to potential noise. Additionally, it involves complex processes like calculating zero-sequence voltage for dc-link control. Both VVPWM and COPWM ideally calculate the duty ratios of reference voltage vectors, sometimes failing to satisfy the *volt·time* product during transient periods.

On the other hand, another new modulation technique, the multi-neighboring reference vector discontinuous PWM (MNRV DPWM), was introduced to address the dc-link voltage imbalance in a four-level diode-clamped ac/dc converter [31]. This method selects multiple adjacent reference vectors based on the command voltage's location, with different capacitor charging characteristics. This method achieves voltage balancing naturally by evenly utilizing the duty ratios of these vectors and integrating duty compensators to reflect the capacitors' charging characteristics. A remaining degree of freedom outmost reference vector is selected to satisfy the *volt·time* product.

MNRV DPWM has been extended to various dc/dc converters, including the full-bridge (FB) diode-clamped four-level *LLC* resonant converter [32], FB symmetric switching converter [33], FB three-level *LLC* resonant converter [34], and a half-bridge (HB) four-level *LLC* resonant converter [35]. Specifically, in the four-level symmetric switching converter, this method successfully implements a modulation technique that injects an offset voltage using the extreme values of the reference voltage into the FB topology composed of two symmetric HBs. This indicates the potential scalability of MNRV DPWM to future multiphase multilevel converter topologies.

This paper introduces a three-phase diode-clamped four-level PWM inverter utilizing an offset voltage injection-based

TABLE 1. COMPARISON OF PROS AND CONS OF THE PROPOSED METHOD AND EXISTING METHODS

	VVPWM [22]−[26]	COPWM [27]−[30]	Proposed Method
Pros	·Easy implementation ·Ensures minimal dc-link voltage deviation	·Natural voltage balance ·Fast dc-link voltage dynamics	·Generality (various DPWM types are possible depending on applied offset voltage, applicable not only to inverter but also to dc/dc, easy to extend to high-dimensional multilevel multiphase systems) ·Superior reference voltage tracking performance ·Satisfactory THD in wide range of m
Cons	·High average switching frequency (Large switching loss) ·Low THD in high m	·Somewhat complex control (calculation of zero sequence voltage) ·Low THD in low m	·Requires somewhat large capacitance ·High dc-link voltage deviation

MNRV (D)PWM method. Originally developed for single-phase FB systems, it's now adapted to three-phase systems. This approach employs the offset voltage injection method, commonly used in traditional two-level inverters, to generate various continuous/discontinuous switching modulation schemes [36]−[38].

The proposed MNRV (D)PWM-based multilevel PWM inverter offers several advantages over conventional methods.

 - By incorporating the duty compensation parameters into the duty cycle calculation of the reference step voltage in real-time to address the voltage deviations in dc-link capacitors, the *volt·time* product is maintained without errors even during transient conditions.
 - The versatility of this approach allows for the generation of various DPWM types using miscellaneous offset voltages based on the extremes of the command voltage. Additionally, the application of intuitive modulation techniques makes it easy to extend to high-dimensional multilevel multiphase systems. It can also be applied in a similar way to both inverter and dc/dc converter topologies.
 - The presence of a wide discontinuous switching region can lower the average switching frequency, thereby reducing switching losses.
 - Additionally, it has been demonstrated to provide excellent THD performance in output current and line voltage across a wide range of modulation indices.

However, a higher capacitance value is needed for stable operation, as the proposed method permits a certain level of voltage deviation compared to conventional approaches. Table 1 compares the advantages and disadvantages of conventional methods and the proposed method.

Section II outlines the design principles for offset voltage injection-based MNRV DPWM, tailored for three-phase diode-clamped four-level PWM inverters, and extends the methodology to high-dimensional multilevel multiphase systems. It also confirms the universality of the proposed

modulation method by demonstrating its applicability to both dc/ac and dc/dc topologies. In Section III, a thorough analysis of the dc-link voltage ripple component is conducted using fast Fourier transform (FFT) analysis of the product of the duty of the E vector and the phase current. Section IV presents simulation results, including verification of steady-state operating characteristics, comparison of THD, analysis of average switching frequency, and validation of dynamic response to dc-link voltage fluctuations. Finally, Section V confirms steady-state operation and transient behavior through prototype circuit experiments, along with verification of dc-link voltage balancing control.

II. MNRV (D)PWM FOR THREE-PHASE FOUR-LEVEL PWM INVERTER WITH OFFSET VOLTAGE INJECTION

The circuit of the proposed three-phase diode-clamped four-level PWM inverter is illustrated in Fig. 1. The dc-link stage, composed of three capacitors connected in series (C_{dc1}, C_{dc2}, and C_{dc3}), interfaces with the voltage source V_{dc}. Meanwhile, the three-phase switching stage consists of three switch groups, labeled Q_{x1} to Q_{x6} (where $x = a$, b, c), along with clamping diodes that connect each step voltage of the dc-link stage to the switching nodes. The output of each phase is then connected to either a delta- or wye-connected load. Here, the output voltage of each phase is denoted as V_{xn}, while the output current of each phase is represented as i_x.
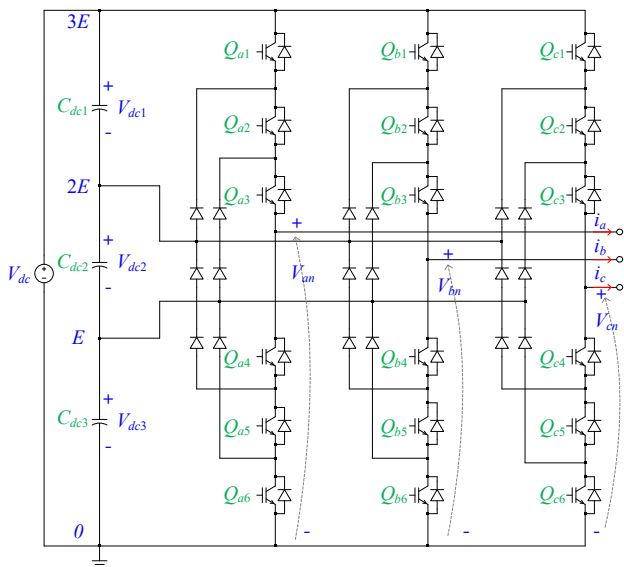

FIGURE 1. Three-phase diode-clamped four-level PWM inverter.

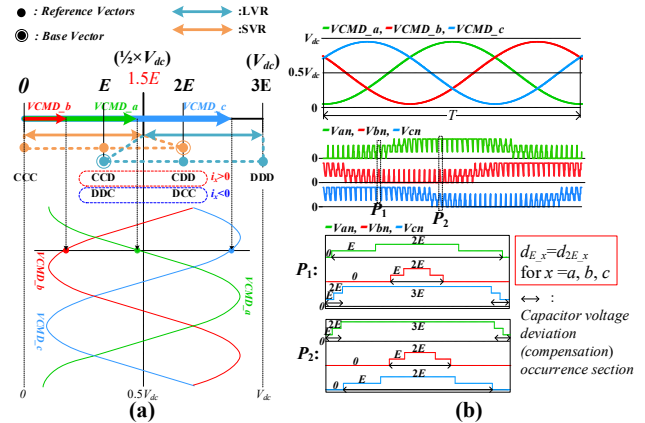## A. OPERATION PRINCIPLES OF MNRV (D)PWM FOR THREE-PHASE DIODE-CLAMPED FOUR-LEVEL PWM INVERTER

FIGURE 2. Operation principles of MNRV (D)PWM for a four-level PWM inverter applying SPWM (Voffset = 0): (a) selection of MNRVs according to the VCMD_x position and (b) switching patterns with equal durations of intermediate-levels (dE_x = d2E_x).

In a three-phase system, the command voltages v_{cmd_x} have a phase difference of 120° from each other, as shown in (1) ($x = a$, b, c). The phase angle θ can be expressed as 2π times the product of the base frequency f_s of the power system and the time t. V_{CMD_x} used in MNRV (D)PWM has the value of v_{cmd_x} plus the injected offset voltage V_{offset} and normalization voltage of $0.5V_{dc}$, as shown in (2). V_{offset} takes various forms depending on the modulation methods.

$$\begin{cases} v_{cmd\_a} = m\dfrac{V_{dc}}{2}\sin\theta, \\[2mm] v_{cmd\_b} = m\dfrac{V_{dc}}{2}\sin\left(\theta - \dfrac{2\pi}{3}\right), \\[2mm] v_{cmd\_c} = m\dfrac{V_{dc}}{2}\sin\left(\theta + \dfrac{2\pi}{3}\right). \end{cases} \quad (1)$$

$$V_{CMD\_x} = v_{cmd\_x} + V_{offset} + 0.5V_{dc} \quad (2)$$

Fig. 2 illustrates the implementation example of MNRV (D)PWM for a three-phase diode-clamped four-level PWM inverter applying sinusoidal PWM (SPWM). In MNRV (D)PWM, symmetry is maintained with respect to the virtual center vector, which corresponds to the 1.5E vector here [35]. Depending on the magnitude of V_{CMD_x}, it is primarily divided into two regions: a large vector region (LVR) when $V_{CMD\_x} \geq 0.5V_{dc}$ and a small vector region (SVR) when $V_{CMD\_x} < 0.5V_{dc}$. In other words, v_{cmd_x} is positive in LVR and negative in SVR. To ensure uniform control of the dc-link capacitor voltages, it is crucial to evenly utilize all reference voltage vectors capable of influencing the state of charge of the capacitors. This entails utilizing voltage vectors corresponding to all intermediate levels except for the outermost voltage levels, namely 0 and 3E. Furthermore, to uphold the *volt·time* product, another voltage vector with a degree of freedom must be included. Therefore, to incorporate all reference vectors with distinct capacitor charging/discharging characteristics and one voltage vector

for adjusting the *volt·time* product, MNRVs become E, $2E$, and $3E$ when V_{CMD_x} is in LVR, and 0, E, and $2E$ when V_{CMD_x} belongs to SVR. Here, 0, E, $2E$, and $3E$ refer V_0, V_E, V_{2E}, and V_{3E}, which are 0, $V_{dc}/3$, $V_{dc} \times 2/3$, and V_{dc}, respectively. C or D expressed under each step voltage indicates the charging/discharging state of the capacitors in the dc-link stage. For example, the capacitor charging state at $2E$ is CDD for positive current ($i_x > 0$), which implies that C_{dc1} is charged with $2/3 \times i_x$ and C_{dc2}, C_{dc3} are discharged with $1/3 \times i_x$.

Since the *a*, *b*, and *c* phases can be operated independently, this method offers the advantage of linear implementation on a straight line, unlike conventional space-vector PWM (SVPWM), which considers both the magnitude and phase of the command voltage and is implemented on a two-dimensional plane. The key to maintaining capacitor voltage balance, regardless of the position of the V_{CMD_x}, is to set the duty ratios of the intermediate-level voltage vectors to be equal to each other, i.e. $d_{E\_x} = d_{2E\_x}$. This method effectively minimizes voltage imbalances on average by evenly utilizing all factors influencing capacitor charging and discharging.

To define other PWM types, we first need to define maximum and minimum values as in (3). Here, V_{max} and V_{min} refer to the maximum and minimum values of v_{cmd_x}, respectively, and $V_{max(min)\_\pm\pi/6}$ refer to the maximum and minimum values of v_{cmd_x} phase shifted by (+)π/6 and (−)π/6, respectively.

By utilizing the previously defined maximum and minimum values to set V_{offset} as (4), it becomes possible to define SPWM, SVPWM, 60°DPWM, 30°DPWM, 60°(+30°)DPWM, 60°(−30°)DPWM, and DPWMMAXorMIN.

Next, the parameters d_{compx} are established as in (5) to finely adjust each reference voltage vector. The d_{compx} represent values that are proportional to the difference between the average voltages on the left and right sides of the subscript underscore. For instance, d_{comp12_3} represents the proportional integral control output of the difference between $(V_{dc1}+V_{dc2})/2$ on the left side and V_{dc3} on the right side of the subscript underscore. Here, V_{dc1}, V_{dc2}, V_{dc3} denote the terminal voltages of C_{dc1}, C_{dc2}, C_{dc3}, respectively. K_p and K_I represent the proportional and integral gains of PI controller.

$$
\begin{cases}
V_{\max} = \max(v_{cmd\_a}, v_{cmd\_b}, v_{cmd\_c}), \\
V_{\min} = \min(v_{cmd\_a}, v_{cmd\_b}, v_{cmd\_c}), \\
V_{\max\_+\pi/6} = \max(v_{cmd\_a}(\theta+\frac{\pi}{6}), v_{cmd\_b}(\theta+\frac{\pi}{6}), v_{cmd\_c}(\theta+\frac{\pi}{6})), \\
V_{\min\_+\pi/6} = \min(v_{cmd\_a}(\theta+\frac{\pi}{6}), v_{cmd\_b}(\theta+\frac{\pi}{6}), v_{cmd\_c}(\theta+\frac{\pi}{6})), \\
V_{\max\_-\pi/6} = \max(v_{cmd\_a}(\theta-\frac{\pi}{6}), v_{cmd\_b}(\theta-\frac{\pi}{6}), v_{cmd\_c}(\theta-\frac{\pi}{6})), \\
V_{\min\_-\pi/6} = \min(v_{cmd\_a}(\theta-\frac{\pi}{6}), v_{cmd\_b}(\theta-\frac{\pi}{6}), v_{cmd\_c}(\theta-\frac{\pi}{6})).
\end{cases}
\tag{3}
$$

V_{offset}
$$
= \begin{cases}
SPWM : 0 \\
SVPWM : -0.5(V_{\max}+V_{\min}) \\
60°DPWM : \begin{cases} 0.5V_{dc}-V_{\max}, for\ V_{\max}+V_{\min} \geq 0 \\ -0.5V_{dc}-V_{\min}, for\ V_{\max}+V_{\min} < 0 \end{cases} \\
30°DPWM : \begin{cases} -0.5V_{dc}-V_{\min}, for\ V_{\max}+V_{\min} \geq 0 \\ 0.5V_{dc}-V_{\max}, for\ V_{\max}+V_{\min} < 0 \end{cases} \\
60°(+30°)DPWM : \begin{cases} 0.5V_{dc}-V_{\max}, for\ V_{\max\_-\pi/6}+V_{\min\_-\pi/6} \geq 0 \\ -0.5V_{dc}-V_{\min}, for\ V_{\max\_-\pi/6}+V_{\min\_-\pi/6} < 0 \end{cases} \\
60°(-30°)DPWM : \begin{cases} 0.5V_{dc}-V_{\max}, for\ V_{\max\_+\pi/6}+V_{\min\_+\pi/6} \geq 0 \\ -0.5V_{dc}-V_{\min}, for\ V_{\max\_+\pi/6}+V_{\min\_+\pi/6} < 0 \end{cases} \\
DPWMMAXorMIN : \begin{cases} 0.5V_{dc}-V_{\max}, for\ CM=1(V_{dc1}>V_{dc3}) \\ -0.5V_{dc}-V_{\min}, for\ CM=-1(V_{dc1}<V_{dc3}) \end{cases}
\end{cases}
\tag{4}
$$

$$
\begin{aligned}
d_{comp12\_3} &= K_P(\frac{V_{dc1}+V_{dc2}}{2}-V_{dc3}) + K_I \int_0^t (\frac{V_{dc1}+V_{dc2}}{2}-V_{dc3})dt, \\
d_{comp1\_23} &= K_P(V_{dc1}-\frac{V_{dc2}+V_{dc3}}{2}) + K_I \int_0^t (V_{dc1}-\frac{V_{dc2}+V_{dc3}}{2})dt.
\end{aligned}
\tag{5}
$$

To maintain capacitor voltage balance, the duty cycles of intermediate-level voltage vectors are initially set to be equal. Then, the d_{comp} parameters, which are proportional to small voltage deviations occurring during actual operation, are inserted. This allows for fine adjustments to the duty ratios of each reference voltage vector during closed-loop control, ensuring precise regulation even during transient intervals.

In this manner, depending on the magnitude of V_{CMD_x}, the duty ratios of each reference voltage vector and the PWM command voltages compared to the actual carrier are expressed as shown in (6) and (7). In LVR, d_{E_x} is treated as the base vector, while in SVR, d_{2E_x} serves as the base vector. The duty ratios of the remaining intermediate-level vectors are primarily set to match that of the base vector, incorporating the d_{comp} values for precise voltage balance control. Additionally, the duty ratios of the remaining outermost voltage vectors are adjusted to fulfill the *volt·time* product requirement.

The values of d_{0_x}, d_{E_x}, d_{2E_x}, and d_{3E_x} represent the duty ratios of reference vectors 0, E, $2E$, and $3E$ for x phase, respectively. *PWM_CMD_x*1, *PWM_CMD_x*2, and *PWM_CMD_x*3 denote the PWM command voltages corresponding to the upper switches of phase x, namely Q_{x1}, Q_{x2}, and Q_{x3}, respectively. These values are compared with the carrier signal to generate the PWM output signal. N_{max} denotes period value of the carrier. To modulate the effect of the d_{comp} based on the sign of the output current i_x, the sgn() function, which outputs the polarity of the input variable, is defined as shown in (8). The definition of i_x is provided in (9) along with the amplitude of I_m, and δ is related to the power factor *pf* according to (10).

Fig. 3 depicts the PWM command voltages, output voltage of *a* phase, duty ratio of the E-level voltage vector for *a* phase, the product of phase current and the duty ratio of the

corresponding phase's E voltage vector, and their FFT results for SPWM, SVPWM, and various DPWMs.

The command voltage patterns for widely known offset voltage injection-based (D)PWM are observed across all modulation methods [36]−[38]. Additionally, in DPWMs, we can observe that switching actions halt during discontinuous modulation intervals. Furthermore, in LVR, the output phase voltage takes on values of E, $2E$, and $3E$, while in SVR, it takes on values of 0, E, and $2E$. The duty cycles of the intermediate voltage levels (E or $2E$) vectors are closely related to the capacitor voltage deviation, which will be elaborated on in Section III.

$$\underline{For\ V_{CMD\_x} \geq 0.5 V_{dc}\,(@\,LVR)}$$

$$if\ (V_{CMD\_x} == V_{dc})$$

$$\{$$

$$\begin{pmatrix} d_{0\_x} \\ d_{E\_x} \\ d_{2E\_x} \\ d_{3E\_x} \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 1 \end{pmatrix},$$

$$\begin{pmatrix} PWM\_CMD\_x1 \\ PWM\_CMD\_x2 \\ PWM\_CMD\_x3 \end{pmatrix} = N_{max} \begin{pmatrix} 1 \\ 1 \\ 1 \end{pmatrix},$$

$$\}$$

$$else$$

$$\{$$

$$\begin{pmatrix} d_{0\_x} \\ d_{E\_x} \\ d_{2E\_x} \\ d_{3E\_x} \end{pmatrix} = \begin{pmatrix} 0 \\ -\dfrac{V_{CMD\_x}}{V_{dc}} + \dfrac{1}{3}\text{sgn}(i_x)d_{comp1\_23} + 1 \\ -\dfrac{V_{CMD\_x}}{V_{dc}} - \dfrac{2}{3}\text{sgn}(i_x)d_{comp1\_23} + 1 \\ -1 + 2\dfrac{V_{CMD\_x}}{V_{dc}} + \dfrac{1}{3}\text{sgn}(i_x)d_{comp1\_23} \end{pmatrix}, \quad (6)$$

$$\begin{pmatrix} PWM\_CMD\_x1 \\ PWM\_CMD\_x2 \\ PWM\_CMD\_x3 \end{pmatrix} = N_{max} \begin{pmatrix} d_{3E\_x} \\ d_{2E\_x} + d_{3E\_x} \\ 1 \end{pmatrix}.$$

$$\}$$

B. EXTENTION TO MULTI-PHASE AND HIGH-LEVEL TOPOLOGIES

The proposed modulation method can be easily extended to multi-phase, high-dimensional multilevel topologies. Fig. 4 illustrates the implementation example of MNRV (D)PWM for a typical high-dimensional N-level power system with p phases. Depending on whether V_{CMD_x} falls above or below the virtual center point $(N−1)/2 \cdot E$ vector, it belongs to LVR or SVR. When in LVR, MNRVs cover the switching range of E, $2E$, ..., $(N−1) \cdot E$ vectors, while in SVR, MNRVs operate within

0, E, ..., $(N−2) \cdot E$ vectors. The duty cycles of all intermediate voltage levels, excluding the outermost voltage levels of 0 and $(N−1) \cdot E$ vectors, are initially set to be equal, and fine adjustments are made by d_{comp}. The switches' duty ratios and PWM command values are expressed as shown in (11) and (12). The duty compensation parameter $d_{comp12...k\_(k+1)(k+2)...(N-1)}$ in a general N-level case is given by (13) for $1 \leq k \leq N−2$. This parameter is proportional to the voltage difference between the average voltages on the left and right sides of the subscript underscore.

$$\underline{For\ V_{CMD\_x} < 0.5 V_{dc}\,(@\,SVR)}$$

$$if\ (V_{CMD\_x} == 0)$$

$$\{$$

$$\begin{pmatrix} d_{0\_x} \\ d_{E\_x} \\ d_{2E\_x} \\ d_{3E\_x} \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix},$$

$$\begin{pmatrix} PWM\_CMD\_x1 \\ PWM\_CMD\_x2 \\ PWM\_CMD\_x3 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix},$$

$$\}$$

$$else$$

$$\{$$

$$\begin{pmatrix} d_{0\_x} \\ d_{E\_x} \\ d_{2E\_x} \\ d_{3E\_x} \end{pmatrix} = \begin{pmatrix} 1 - 2\dfrac{V_{CMD\_x}}{V_{dc}} + \dfrac{1}{3}\text{sgn}(i_x)d_{comp12\_3} \\ \dfrac{V_{CMD\_x}}{V_{dc}} - \dfrac{2}{3}\text{sgn}(i_x)d_{comp12\_3} \\ \dfrac{V_{CMD\_x}}{V_{dc}} + \dfrac{1}{3}\text{sgn}(i_x)d_{comp12\_3} \\ 0 \end{pmatrix}, \quad (7)$$

$$\begin{pmatrix} PWM\_CMD\_x1 \\ PWM\_CMD\_x2 \\ PWM\_CMD\_x3 \end{pmatrix} = N_{max} \begin{pmatrix} 0 \\ d_{2E\_x} \\ d_{E\_x} + d_{2E\_x} \end{pmatrix}.$$

$$\}$$

$$\text{sgn}(x) = \begin{cases} +1, for\ x \geq 0 \\ -1, for\ x < 0 \end{cases} \quad (8)$$

$$\begin{cases} i_a = I_m \sin(\theta - \delta), \\ i_b = I_m \sin(\theta - \dfrac{2\pi}{3} - \delta), \\ i_c = I_m \sin(\theta + \dfrac{2\pi}{3} - \delta). \end{cases} \quad (9)$$
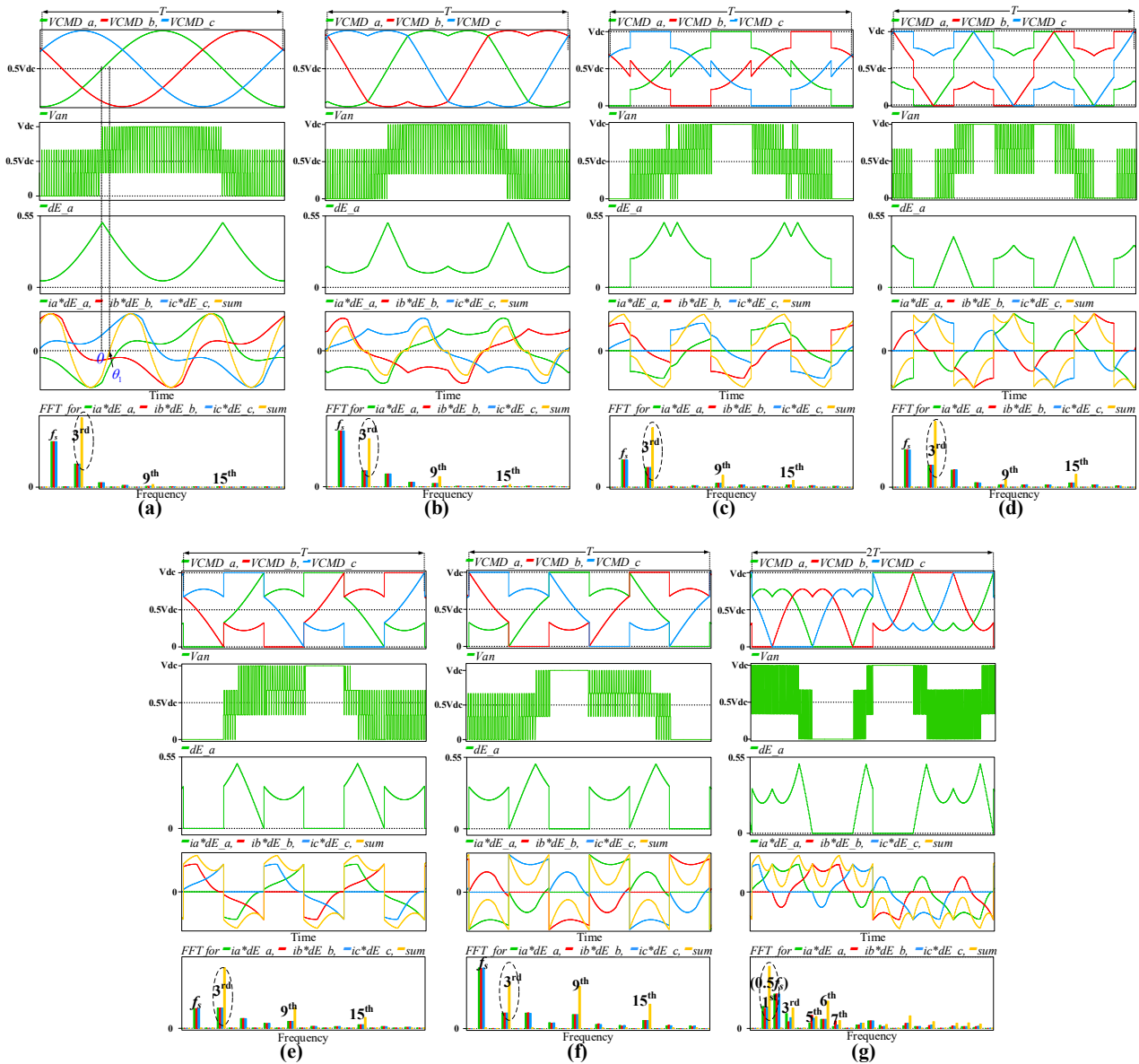
$$\cos \delta = pf \quad (10)$$

FIGURE 3. Various MNRV (D)PWM forms according to injected offset voltage types: (a) SPWM, (b) SVPWM, (c) 60°DPWM, (d) 30°DPWM, (e) 60° (+30°)DPWM, (f) 60°(-30°)DPWM, and (g) DPWMMAXorMIN.
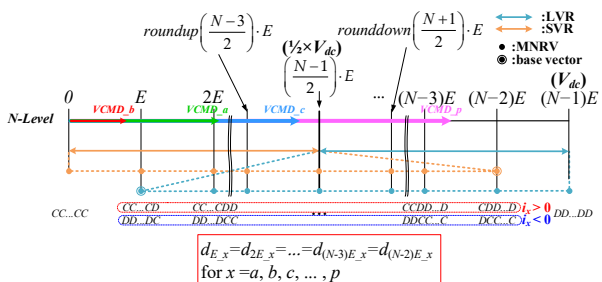

FIGURE 4. Extension of proposed offset voltage injection-based MNRV (D)PWM to multi-phase (p) multilevel (N) topologies.

C. APPLICATION OF THE PROPOSED MNRV DPWM TO DC/DC CONVERTER TOPOLOGIES

Fig. 5a depicts the PWM command voltage and output phase voltage of a three-phase four-level PWM inverter with SPWM using MNRV PWM. To maintain high-quality voltage and current waveforms in PWM inverters, relatively high-frequency modulation factors (m_f) are employed, along with sinusoidal reference voltages. When applying this to dc/dc converters, it is necessary to first reduce the frequency modulation index to $m_f = 2$ to minimize switching losses. Then, the reference voltage should be transformed into a square waveform to improve input voltage utilization. Furthermore, achieving specific waveform outputs requires careful synchronization of the reference voltage and carrier wave, as well as attention to the direction of carrier counting [32]–[35].
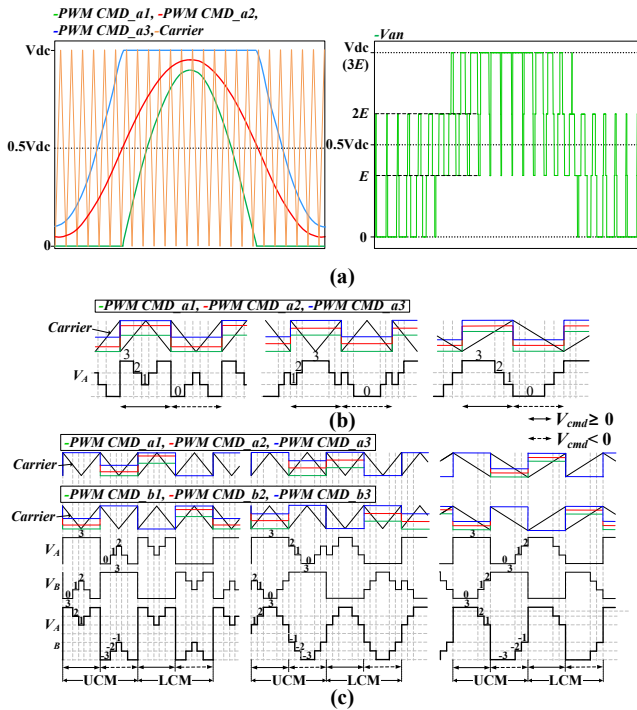
FIGURE 5. Relationship between MNRV (D)PWM based dc/ac inverter and dc/dc converter: (a) dc/ac inverter (SPWM), (b) HB dc/dc converter, and (c) FB dc/dc converter.

Figs. 5(b) and (c) illustrate the forms of MNRV DPWM applied to HB and FB dc/dc topologies, respectively, with reduced $m_f = 2$.

To achieve symmetric voltage output in dc/dc converters, adjustments to the phase of the carrier wave may be necessary in HB configurations when there are changes in the polarity of the reference voltage [35], while in FB configurations, modulation of the carrier wave phase may be required when changing the clamp mode (CM). In the case of a FB configuration, utilizing CM can further reduce the switching losses [32, 33].

III. ΔVdc ANALYSIS

When defining the voltage ripple of the dc-link capacitor C_{dcn}, denoted as ΔV_{dcn_x}, attributed to i_x during the sampling time $T_{smpl} (= T/m_f)$, it becomes evident that this satisfies (14), where T represents the fundamental period of the power system.

When considering the influence of current in all phases, ΔV_{dcn} satisfies (15), where $n = 1, 2, 3$. Here, it was assumed that $d_{E\_x} = d_{2E\_x}$, ignoring the small d_{comp} values in the steady-state. The voltage variation ΔV_{dc2} across the middle capacitor C_{dc2} remains at zero throughout the carrier period, while the voltage variations ΔV_{dc1} and ΔV_{dc3} across the upper and lower capacitors C_{dc1} and C_{dc3}, respectively, are related to the summation of $d_{E\_x} \cdot i_x$ for all phases and observed to have opposite signs.

Referring to the third rows in Fig. 3, in SPWM, SVPWM, 60°DPWM, 30°DPWM, 60°(+30°)DPWM, and

$60°(-30°)$DPWM methods, d_{E_x} is observed to have a period of $0.5T$ with dc bias.

Therefore, $d_{E\_x} \cdot i_x$ contains harmonics of $(2k\pm1)$th order in the fundamental frequency f_s (where $k = 0, 1, 2, 3, \ldots$). However, in a three-phase power system, the term "$\sin(n\omega t) + \sin(n\omega t - 2n\pi/3) + \sin(n\omega t + 2n\pi/3)$" cancels out when $n = 1, 2, 4, 5, 7, 8, \ldots$. Consequently, the total sum of $d_{E\_x} \cdot i_x$ (yellow line in the fourth rows of Fig. 3) ultimately exhibits 3rd, 9th, 15th, … order harmonics. As observed from the FFT analysis results, the lowest harmonic is the 3rd harmonic, indicating that ΔV_{dc} becomes a periodic function with a frequency of $3f_s$.

$$For\ V_{CMD\_x} \ge 0.5V_{dc}\,(@\,LVR)$$

$$if\ (V_{CMD\_x} == V_{dc})$$

$$\{$$

$$\begin{pmatrix} d_{0\_x} \\ d_{E\_x} \\ \ldots \\ d_{(N-2)E\_x} \\ d_{(N-1)E\_x} \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ \ldots \\ 0 \\ 1 \end{pmatrix},$$

$$\begin{pmatrix} PWM\_CMD\_x1 \\ PWM\_CMD\_x2 \\ \ldots \\ PWM\_CMD\_x(N-1) \end{pmatrix} = N_{max}\begin{pmatrix} 1 \\ 1 \\ \ldots \\ 1 \end{pmatrix},$$

$$\}$$

$$else$$

$$\{$$

$$d_{E\_x} =$$

$$\begin{cases} -\dfrac{2V_{CMD\_x}}{(N-2\,V_{dc})} + (\text{sgn}(i_x)d_{comp12\ldots(N-3)\_(N-2)(N-1)}) \cdot \dfrac{2(N-3)}{(N-1)(N-2)}, \\ + (\text{sgn}(i_x)d_{comp12\ldots(N-4)\_(N-3)(N-2)(N-1)}) \cdot \dfrac{2(N-4)}{(N-1)(N-2)} + \ldots \\ + (\text{sgn}(i_x)d_{comp1\_23\ldots(N-1)}) \cdot \dfrac{2}{(N-1)(N-2)} + \dfrac{2}{N-2} \end{cases}$$

$$\begin{pmatrix} d_{0\_x} \\ d_{E\_x} \\ d_{2E\_x} \\ \ldots \\ d_{(N-2)E\_x} \\ d_{(N-1)E\_x} \end{pmatrix} = \begin{pmatrix} 0 \\ d_{E\_x} \\ d_{E\_x} - \text{sgn}(i_x) \cdot d_{comp12\ldots(N-3)\_(N-2)(N-1)} \\ \ldots \\ d_{E\_x} - \text{sgn}(i_x) \cdot d_{comp1\_23\ldots(N-1)} \\ 1 - d_{E\_x} - d_{2E\_x} - \ldots - d_{(N-2)E\_x} \end{pmatrix},$$

$$\begin{pmatrix} PWM\_CMD\_x1 \\ PWM\_CMD\_x2 \\ \ldots \\ PWM\_CMD\_x(N-2) \\ PWM\_CMD\_x(N-1) \end{pmatrix} = N_{max}\begin{pmatrix} d_{(N-1)E\_x} \\ d_{(N-2)E\_x} + d_{(N-1)E\_x} \\ \ldots \\ d_{2E\_x} + d_{3E\_x} + \ldots + d_{(N-1)E\_x} \\ 1 \end{pmatrix}.$$

$$\}$$

(11)

In the DPWMMAXorMIN method, d_{E_x} has a period of $2T$. Thus, $d_{E\_x} \cdot i_x$ exhibits harmonics of $(0.5k \pm 1)$th order. As mentioned earlier, the total sum of $d_{E\_x} \cdot i_x$ includes harmonics of 1st, 3rd, 5th, 6th, … orders at the base frequency of $0.5f_s$. Since the lowest harmonics is the 1st order harmonic, it means that ΔV_{dc} becomes a periodic function with a frequency of $0.5f_s$.

$$For\ V_{CMD\_x} < 0.5V_{dc}\ (@\ SVR)$$

$$if\ (V_{CMD\_x} == 0)$$

$$\{$$

$$\begin{pmatrix} d_{0\_x} \\ d_{E\_x} \\ ... \\ d_{(N-2)E\_x} \\ d_{(N-1)E\_x} \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ ... \\ 0 \\ 0 \end{pmatrix},$$

$$\begin{pmatrix} PWM\_CMD\_x1 \\ PWM\_CMD\_x2 \\ ... \\ PWM\_CMD\_x(N-1) \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ ... \\ 0 \end{pmatrix},$$

$$\}$$

$$else$$

$$\{$$

$$d_{(N-2)E\_x} =$$

$$\left\{ \begin{array}{l} \dfrac{2V_{CMD\_x}}{(N-2)V_{dc}} + (\mathrm{sgn}(i_x)d_{comp12...(N-2)\_(N-1)}) \cdot \dfrac{2}{(N-1)(N-2)}, \\ +(\mathrm{sgn}(i_x)d_{comp12...(N-3)\_(N-2)(N-1)}) \cdot \dfrac{4}{(N-1)(N-2)} + ... \\ +(\mathrm{sgn}(i_x)d_{comp12\_34..(N-1)}) \cdot \dfrac{2(N-3)}{(N-1)(N-2)} \end{array} \right\}$$

$$\begin{pmatrix} d_{0\_x} \\ d_{E\_x} \\ ... \\ d_{(N-3)E\_x} \\ d_{(N-2)E\_x} \\ d_{(N-1)E\_x} \end{pmatrix} = \begin{pmatrix} 1 - d_{E\_x} - d_{2E\_x} - ... - d_{(N-2)E\_x} \\ d_{(N-2)E\_x} - \mathrm{sgn}(i_x) \cdot d_{comp12...(N-2)\_(N-1)} \\ ... \\ d_{(N-2)E\_x} - \mathrm{sgn}(i_x) \cdot d_{comp12\_34..(N-1)} \\ d_{(N-2)E\_x} \\ 0 \end{pmatrix},$$

$$\begin{pmatrix} PWM\_CMD\_x1 \\ PWM\_CMD\_x2 \\ ... \\ PWM\_CMD\_x(N-2) \\ PWM\_CMD\_x(N-1) \end{pmatrix} = N_{\max} \begin{pmatrix} 0 \\ d_{(N-2)E\_x} \\ ... \\ d_{2E\_x} + ... + d_{(N-2)E\_x} \\ d_{E\_x} + d_{2E\_x} + ... + d_{(N-2)E\_x} \end{pmatrix}.$$

$$\}$$

$$(12)$$

$$d_{comp12...k\_(k+1)(k+2)...(N-1)} =$$

$$K_P \left(\dfrac{\sum_{n=1}^{k} V_{dcn}}{k} - \dfrac{\sum_{n=k+1}^{N-1} V_{dcn}}{N-k-1} \right) + K_I \int_0^t \left(\dfrac{\sum_{n=1}^{k} V_{dcn}}{k} - \dfrac{\sum_{n=k+1}^{N-1} V_{dcn}}{N-k-1} \right) dt. \quad (13)$$

On the other hand, in VVPWM, d_{E_x} has a period of $T/6$, resulting in sum of $d_{E\_x} \cdot i_x$ includes harmonics of $(6k \pm 1)$th orders. However, as previously mentioned, harmonics of orders when $k = 0, 1, 2, 4, 5, 7, 8, ...$ are naturally canceled in a three-phase system. Therefore, ΔV_{dc} naturally becomes 0 in VVPWM.

The voltage ripple ΔV_{dc1} is determined by the sum of $d_{E\_x} \cdot i_x$ for each phase over half of the voltage ripple period. For instance, in the case of SPWM, the duty ratios of the E voltage vector for each phase during the $T/6$ period are described by (16). Therefore, ΔV_{dc1} is determined as the integral sum of $d_{E\_x} \cdot i_x$ during $\pi/3$ period, divided by the product of the capacitance C_{dc} and the angular frequency ω as presented in (17). As illustrated earlier in Fig. 3(a), the summation function of $d_{E\_x} \cdot i_x$ exhibits periodicity of $3f_s$ delayed by θ_1 from the zero-crossing point of V_{CMD_a}. Here, θ_1 indicates the point where the sum of $d_{E\_x} \cdot i_x$ becomes 0 and it is obtained as outlined in (18).

$$\begin{cases} \Delta V_{dc1\_x} = \dfrac{T_{smpl}}{C_{dc}} (d_{2E\_x} \dfrac{2}{3} i_x + d_{E\_x} \dfrac{1}{3} i_x) = \dfrac{T_{smpl}}{C_{dc}} d_{E\_x} i_x \\ \Delta V_{dc2\_x} = \dfrac{T_{smpl}}{C_{dc}} (-d_{2E\_x} \dfrac{1}{3} i_x + d_{E\_x} \dfrac{1}{3} i_x) = 0 \\ \Delta V_{dc3\_x} = \dfrac{T_{smpl}}{C_{dc}} (-d_{2E\_x} \dfrac{1}{3} i_x - d_{E\_x} \dfrac{2}{3} i_x) = -\dfrac{T_{smpl}}{C_{dc}} d_{E\_x} i_x \end{cases} \quad (14)$$

$$\begin{cases} \Delta V_{dc1} = \dfrac{T_{smpl}}{C_{dc}} \sum_{x=a,b,c} d_{E\_x} i_x, \\ \Delta V_{dc2} = 0, \\ \Delta V_{dc3} = -\dfrac{T_{smpl}}{C_{dc}} \sum_{x=a,b,c} d_{E\_x} i_x, \\ \Delta V_{dc} = \Delta V_{dc1} - \Delta V_{dc3} = \dfrac{2T_{smpl}}{C_{dc}} \sum_{x=a,b,c} d_{E\_x} i_x. \end{cases} \quad (15)$$

$$\theta : [0, \pi/3]$$

$$\begin{cases} d_{E\_a} = -\dfrac{V_{CMD\_a}}{V_{dc}} + 1 = \dfrac{1}{2} - \dfrac{1}{2} m \sin\theta \\ d_{E\_b} = \dfrac{V_{CMD\_b}}{V_{dc}} = \dfrac{1}{2} + \dfrac{1}{2} m \sin(\theta - \dfrac{2\pi}{3}) \\ d_{E\_c} = -\dfrac{V_{CMD\_c}}{V_{dc}} + 1 = \dfrac{1}{2} - \dfrac{1}{2} m \sin(\theta + \dfrac{2\pi}{3}) \end{cases} \quad (16)$$

$$\Delta V_{dc1} = \dfrac{1}{C_{dc}} \int_{<T/6>} \sum_{x=a,b,c} d_{E\_x} i_x dt$$

$$= \dfrac{T}{2\pi C_{dc}} \left[-\int_0^{\theta_1} \sum_{x=a,b,c} d_{E\_x} i_x d\theta + \int_{\theta_1}^{\pi/3} \sum_{x=a,b,c} d_{E\_x} i_x d\theta \right] \quad (17)$$

$$\theta_1 = 0.5 \times \left\{ \dfrac{\pi}{3} + \delta - \cos^{-1}\left(\dfrac{\cos\delta}{2} \right) \right\} \quad (18)$$

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For SPWM,

$$\Delta V_{dc1} = \frac{mI_mT}{8\pi C_{dc}} \cdot \begin{bmatrix} -\sin\delta + \left\{ \delta - \cos^{-1}(\frac{\cos\delta}{2}) \right\} \cdot \cos\delta \\ +\sqrt{4 - \cos^2\delta} \end{bmatrix} \quad (19)$$

For SVPWM,

$$\Delta V_{dc1} = \begin{cases} \dfrac{mI_mT}{16\pi C_{dc}} \cdot \begin{Bmatrix} (-6 + 2\sqrt{3}\delta)\sin\delta \\ +(2\sqrt{3} - \pi + 6\delta)\cos\delta \end{Bmatrix}, for\ \delta \le \dfrac{\pi}{6} \\ \dfrac{\sqrt{3}mI_mT\sin\delta}{48C_{dc}}, for\ \delta > \dfrac{\pi}{6} \end{cases} \quad (20)$$

For DPWMs,

$$\Delta V_{dc1} = \frac{mI_mT\cos\delta}{8C_{dc}} for\ m < 0.57735 \quad (21)$$

Consequently, the determination of ΔV_{dc1} for SPWM is elucidated by (19). Applying a similar approach, ΔV_{dc1} for SVPWM can be derived as shown in (20). In SVPWM, it can be observed that ΔV_{dc1} is divided into two parts depending on the magnitude of the phase delay δ between the output phase current and the reference command voltage phase.

Except for DPWMMAXorMIN, the remaining DPWMs satisfy (21) when $m < 0.57735$. However, due to the variability in scenarios based on the values of m and δ, analytical investigation is required for the remaining DPWM methods rather than explicit equations. Fig. 6 illustrates ΔV_{dc1} for SPWM, SVPWM, and various DPWM methods. Here, the horizontal and vertical axes represent m and δ. ΔV_{dc1} is depicted using contour lines, reflecting changes in values across the axes. The darker shades of blue represent lower values of ΔV_{dc1}, while the darker shades of yellow indicate higher values.
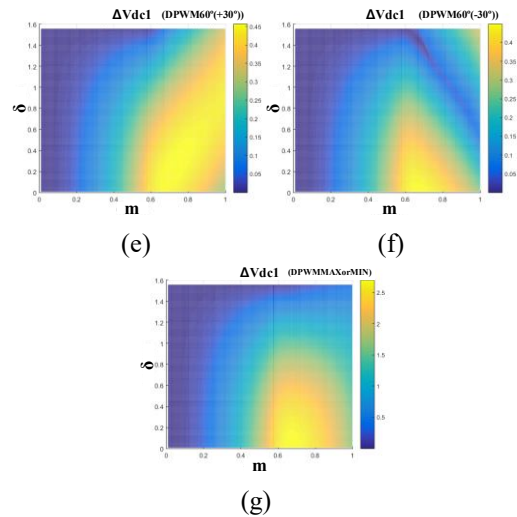

(e)　　　　　　(f)

(g)

FIGURE 6. Numerical analysis results of ΔVdc1 according to m and δ for (a) SPWM, (b) SVPWM, (c) 60°DPWM, (d) 30°DPWM, (e) 60° (+30°)DPWM, (f) 60°(-30°)DPWM, and (g) DPWMMAXorMIN.

Fig. 7 directly compares the ΔV_{dc1} values for various modulations under the conditions of V_{dc} = 200V, load impedance of 22.71Ω, C_{dc} = 7.5mF, and f_s = 60Hz. Generally, an increase in m leads to an increase in ΔV_{dc1}, while a decrease in the *pf* results in a decrease in ΔV_{dc1}. For all DPWM methods, when $m < 0.57735$, ΔV_{dc1} is expressed as given in (21). However, beyond this threshold, there exists a region where ΔV_{dc1} decreases as m increases. Therefore, at lower *pf* and higher values of m, DPWM methods such as 30°DPWM or 60°(−30°)DPWM exhibit smaller ΔV_{dc1} regions compared to SPWM or SVPWM. DPWMMAXorMIN, which utilizes CM, tends to maintain continuous charging or discharging of V_{dc1} over one fundamental cycle, resulting in higher ΔV_{dc1} values compared to other methods. However, as the *pf* decreases, the difference between DPWMMAXorMIN and other methods gradually diminishes.
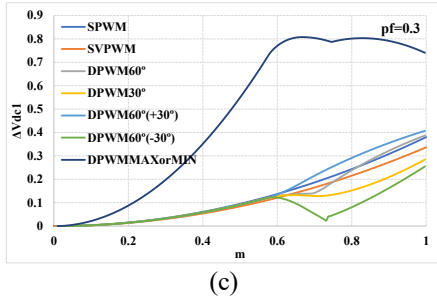

(a)　　(b)

(c)　　(d)

(a)

(b)

(c)
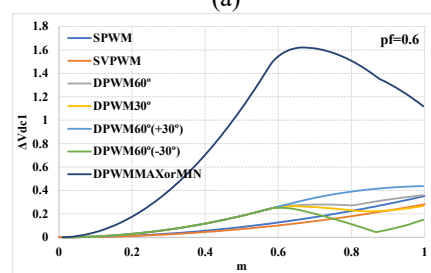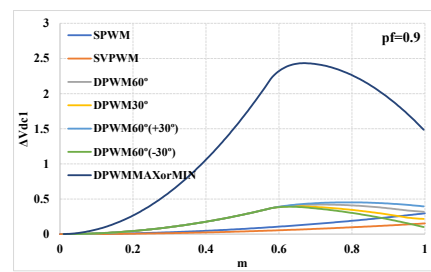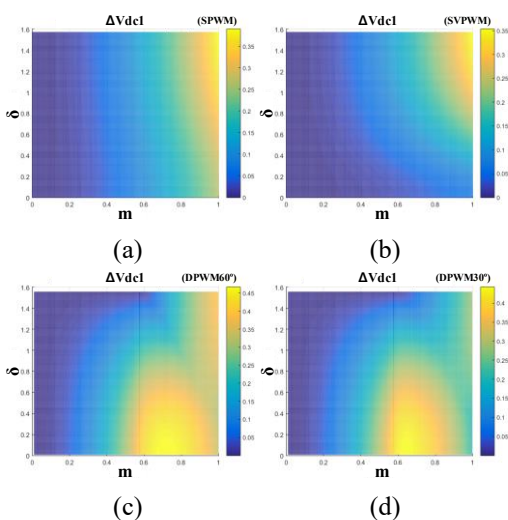
FIGURE 7. ΔVdc1 comparisons of various MNRV (D)PWMs for (a) pf = 0.9, (b) pf = 0.6, and (c) pf = 0.3.

IV. SIMULATIONS

A. OPERATING WAVEFORM

The main operation of the proposed offset voltage injection-based MNRV (D)PWM is illustrated in Fig. 8 along with simulation results. Under the simulation conditions of V_{dc} = 200V, load impedance of 22.71Ω, $m = 0.9$, $m_f = 100$, $pf = 0.9$, $C_{dc} = 7.5$mF, and $f_s = 60$Hz, unique characteristics of seven different MNRV (D)PWM methods were observed based on various offset voltage injection methods as described in (4).
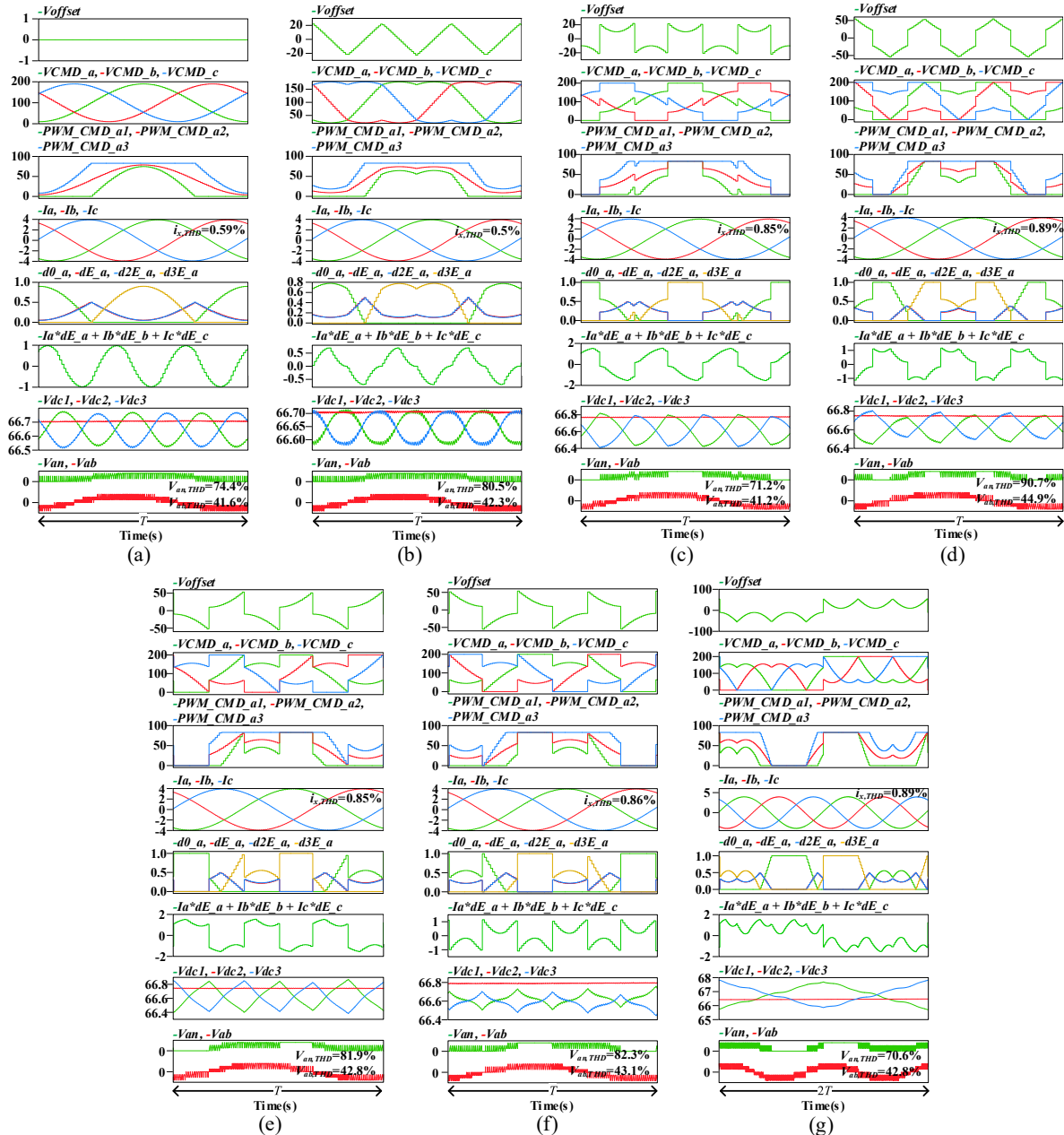
FIGURE 8. Steady-operating waveforms for the proposed offset voltage injection-based MNRV(D)PWM for (a) SPWM, (b) SVPWM, (c) 60°DPWM, (d) 30° DPWM, (e) 60°(+30°)DPWM, (f) 60°(-30°)DPWM, and (g) DPWMMAXorMIN

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Unlike VVPWM, the clamp interval of the outermost vectors is observed to be 180°, indicating lower switching losses. THD in the output current was lowest in SVPWM at 0.5%, slightly higher in SPWM at 0.59%, and approximately 0.85~0.89% in the remaining DPWMs.

The THD in the output phase voltage was lowest in DPWMMAXorMIN at 70.6% and highest in 30°DPWM at 90.7%. The THD in the line voltage ranged from 41.2% to 44.9%. As observed earlier, the sum of $d_{E\_x} \cdot i_x$ appears to be closely related to the charging and discharging profiles of V_{dc1} or V_{dc3}. In fifth rows, the values of d_{E_a} and d_{2E_a} are nearly identical, indicating a very small value of d_{comp}.

Under the same simulation conditions, simulations for VVPWM and COPWM were conducted for comparison (see Fig. 9). Unlike MNRV (D)PWM methods where the clamp interval of the outermost vectors is 180°, VVPWM exhibits a 120° interval. As a result, while VVPWM endures more switching losses, significantly reduced dc-link voltage ripple is observed under steady-state conditions due to the broader active switching intervals. Additionally, COPWM, by segmenting the switching regions around $0.5V_{dc}$ and maintaining consistent duty ratios for intermediate voltage levels, demonstrates operation characteristics almost similar to the proposed MNRV (D)PWM, except for zero-sequence voltage injection. However, in COPWM, frequent transitions between clamp and non-clamp regions are observed due to the update of the zero-sequence voltage to its optimal value for dc-link voltage balance in every control cycle. While this approach minimizes capacitor voltage imbalances, the high-frequency distortion components included in the PWM command may adversely affect current or voltage components. The THD in the output current for both VVPWM and COPWM was approximately 0.85%. However, due to the higher switching frequency in VVPWM, relatively higher THD values were observed in the output voltage and line voltage.
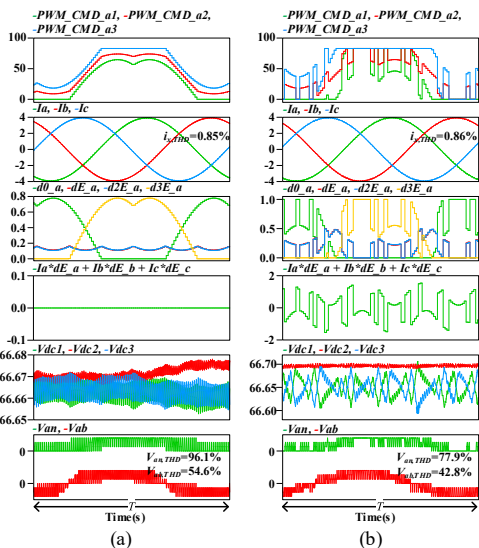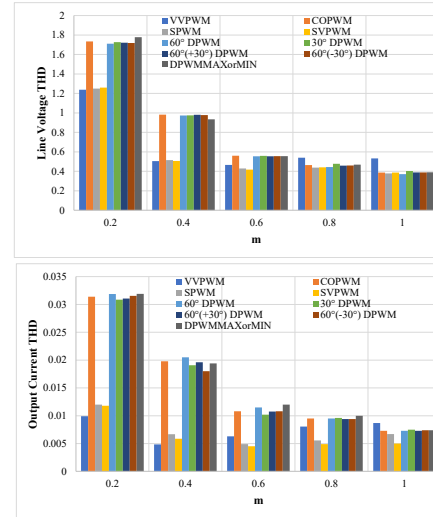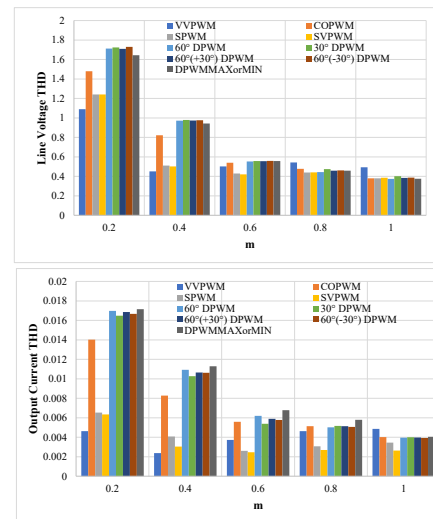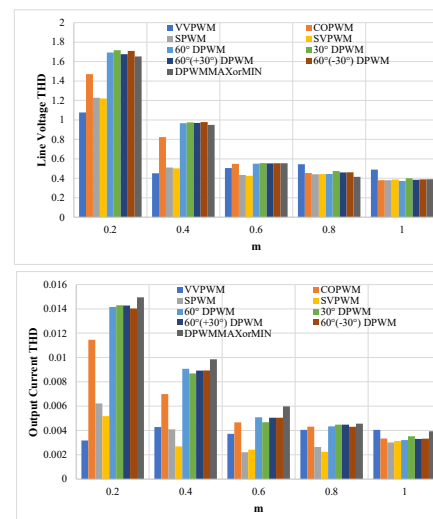

FIGURE 9. Steady-state operating waveforms for the existing (a) VVPWM and (b) COPWM.

FIGURE 10. Comparative analysis of total harmonic distortions for line voltage and output current at (a) pf = 0.9, (b) pf = 0.6, and (c) pf = 0.3.

B. THD ANALYSIS

A comprehensive analysis of THD on the output line voltage and output phase current for VVPWM, COPWM, and proposed MNRV (D)PWM schemes is presented in Fig. 10. The THD comparison results for $pf = 0.9$, $pf = 0.6$, and $pf = 0.3$ are illustrated in Figs. 10(a), (b), and (c), respectively. It is observed that VVPWM exhibits outstanding THD performance for both line voltage and output current at low m. However, as m increases, the THD performance of MNRV(D)PWM methods gradually improves. Especially for the line voltage, satisfactory THD performance of the proposed MNRV (D)PWM is observed at $m > 0.8$, while for the output current, SPWM and SVPWM exhibit superior characteristics compared to VVPWM at $m > 0.6$. Moreover, as m approaches 1, all MNRV (D)PWM methods demonstrate commendable THD performance. Furthermore, COPWM shows lower THD performance compared to continuous MNRV PWM methods (SPWM, SVPWM), while demonstrating similar performance to MNRV DPWMs.

C. AVERAGE SWITCHING FREQUENCY

Under the conditions of $f_s = 60$Hz, $m_f = 100$, and $m = 0.9$, the average switching frequencies for VVPWM, COPWM, and the proposed MNRV (D)PWM were compared in Fig. 11. For VVPWM, PWM_CMD_a1 and PWM_CMD_a3 each have a switching pause period of 120°. As a result, the individual switching frequencies for Q_{a1} and Q_{a3} are calculated to be 4kHz (6kHz×2/3), resulting in an average switching frequency of 4.6kHz ((4+6+4)/3). On the other hand, for MNRV-based SPWM and SVPWM, PWM_CMD_a1 and PWM_CMD_a3 have a switching pause period of 180°. Therefore, the individual switching frequencies of Q_{a1} and Q_{a3} are calculated to be 3kHz (6kHz×1/2), resulting in an average switching frequency of 4kHz ((3+6+3)/3). For MNRV DPWMs, there is an additional 60° clamp period in addition to the 180° switching rest period. As a result, the average switching frequency is calculated to be 2.6kHz ((2+4+2)/3). COPWM shares similarities with MNRV DPWM in that it has a clamp period, but its actual switching frequency is slightly higher due to frequent movement between clamp intervals and continuous intervals. Therefore, the actual average switching frequency is slightly higher than 2.6 kHz. In conclusion, for MNRV DPWM, as m approaches 1, the average switching frequency decreases while the THD performance of the phase current is superior to that of VVPWM.

D. DYNAMICS OF DC-LINK VOLTAGE STEP CHANGES

The comparison of dynamic characteristics in response to sudden voltage fluctuations of the dc-link voltage reference is illustrated in Fig. 12.

Initially, the dc-link voltages are set as $V_{dc1} = V_{dc2} = V_{dc3} = 66.6$V. At $t = 0.15$s, these voltages are stepped to $V_{dc1} =$
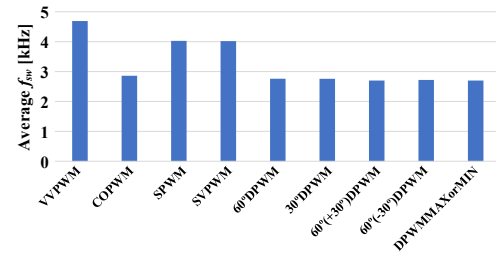

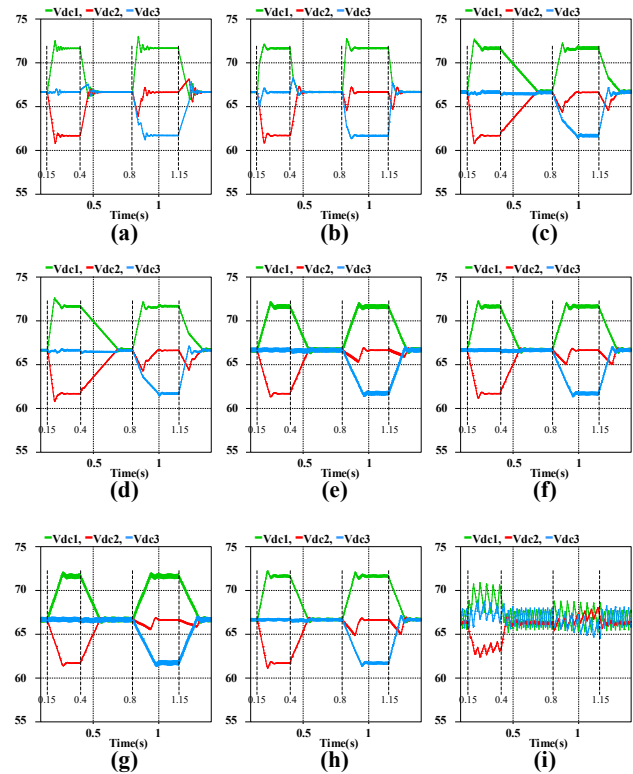**FIGURE 11. Comparison for average switching frequency.**

FIGURE 12. Comparison of dynamic characteristics for step changes in dc-link voltage for (a) VVPWM, (b) COPWM, (c) SPWM, (d) SVPWM, (e) 60°DPWM, (f) 30°DPWM, (g) 60°(+30°)DPWM, (h) 60°(-30°)DPWM, and (i) DPWMMAXorMIN.

71.6V, $V_{dc2} = 61.6$V, $V_{dc3} = 66.6$V. After a certain stabilization period, at $t = 0.4$s, they revert to $V_{dc1} = V_{dc2} = V_{dc3} = 66.6$V. At $t = 0.8$s, the voltages are stepped to $V_{dc1} = 71.6$V, $V_{dc2} = 66.6$V, $V_{dc3} = 61.6$V. Finally, at $t = 1.15$s, they return to $V_{dc1} = V_{dc2} = V_{dc3} = 66.6$V.

For closed-loop control, the d_{comp} parameters have been integrated not only into MNRV (D)PWM but also into VVPWM and COPWM. Stable operational characteristics are confirmed across all modulation methods, responding well to step changes in the dc-link voltages. Overall, VVPWM and COPWM demonstrate relatively rapid dynamic responses compared to MNRV (D)PWM. Furthermore, it can be observed that the voltage variations in the values of V_{dc1} and V_{dc3} in VVPWM or COPWM are

relatively smaller compared to MNRV (D)PWM. This is probably because VVPWM and COPWM tightly control the voltage deviations at each control cycle, while in MNRV (D)PWM, some degree of voltage deviation is allowed, controlling the voltage deviations every $T/3$ period. An intriguing observation is that in the DPWMMAXorMIN method, there are control efforts to overcome forced voltage variations and mitigate voltage imbalances by utilizing clamp mode based on dc-link voltage deviations.
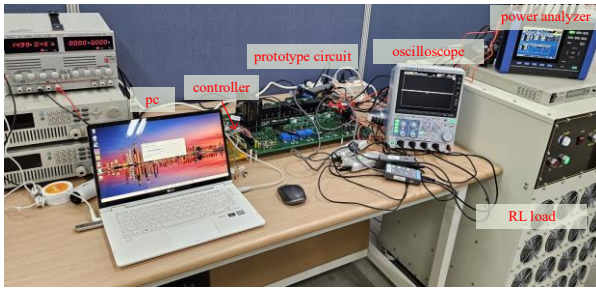
V. EXPERIMENTS

To verify the feasibility of proposed three-phase diode-clamped four-level PWM inverter with offset voltage injection, several experiments were performed under the specified conditions with $V_{dc} = 200V$, $C_{dc} = 7.5mF$, $f_s = 60Hz$, $m_f = 100$, while varying m between 0.3 and 0.9, and varying pf between 0.2 and 0.9.

Fig. 13 illustrates the experimental setup utilized in the prototype test. It encompasses a laptop computer serving as the control unit, the prototype circuit, an oscilloscope, a power analyzer, and an RL load.

Fig. 14 illustrates the main operational waveforms such as V_{an}, V_{ab}, I_a, and I_b under steady-state conditions with a load impedance of 24.3 Ω having a $pf = 0.9$ ($R = 21.87$ Ω, $L = 28.096mH$ per phase) at $m = 0.9$. Additionally, it includes the FFT results for line voltage (V_{ab}) and phase current (I_a). For comparison, experiments under the same conditions were conducted for conventional VVPWM and COPWM methods. From Figs. 14(a) to (i), each figure exhibits distinctive modulation characteristics derived from the V_{an} waveform. In the case of VVPWM, the THD of V_{ab} is 57.9%, and for I_a, it is 3.98%. The observed higher THD for I_a compared to simulation results is attributed to nonlinear circuit elements and side effects such as dead-time and switching noise, including CM mode noise, which are not dealt with in this paper [39, 40]. In COPWM, intermittent clamping to the maximum (V_{dc}) or minimum (0) occurs in the V_{an} waveform, and it exhibits a more natural stepped waveform shape compared to VVPWM when the polarity of V_{ab} changes. The THD for V_{ab} is 45.5%, and for I_a, it is 2.55%, indicating better performance for both components compared to VVPWM when m is high. Figs. 14(c) to (i) represent the proposed MNRV (D)PWM. The characteristics of MNRV (D)PWM,

as outlined in the simulation section, are uniquely observed in the V_{an} waveform. Overall, the THD for V_{ab} ranges from 39.1% to 47.2%, comparable to or lower than COPWM, while the THD for I_a ranges from 2.52% to 3.16%, slightly higher or similar to COPWM.

Fig. 15 depicts the main operational waveforms under steady-state conditions with a $pf = 0.9$ and $m = 0.3$. For VVPWM, the THD of V_{ab} is 94%, and for I_a, it is 11.2%. In contrast, for COPWM, the THD for V_{ab} is 147%, and for I_a, it is 8.61%. It is observed that when m is low, the THD performance of V_{ab} in COPWM deteriorates compared to VVPWM, whereas THD of I_a is superior. Figs. 15(c) to (i) represent the proposed MNRV (D)PWM. Overall, the THD performance of V_{ab} and I_a seems to degrade compared to when m is high. Specifically, the THD for V_{ab} ranges from 72.7% to 160%, while the THD for I_a ranges from 4.52% to 12.1%. This indicates that in 30°DPWM, 60°(−30°)DPWM, and DPWMMAXorMIN, higher THD is observed compared to COPWM, whereas in the remaining SPWM, SVPWM, 60°DPWM, and 60°(+30°)DPWM, lower THD is observed compared to COPWM. This trend generally aligns with the simulation results.

Figs. 16 and 17 illustrate the experimental results under the conditions of $pf = 0.2$ ($R = 4.86$ Ω, $L = 63.156mH$ per phase) for $m = 0.9$ and $m = 0.3$, respectively. Comparing with the results from Figs. 14 and 15, where pf is higher, it appears that overall THD performance of V_{ab} and I_a is better when pf is lower. However, due to the presence of side effects in the circuit, the THD for I_a remains higher compared to simulation values. For $m = 0.9$, in VVPWM, the THD value for V_{ab} was 52.8%, and for I_a, it was 2.26%. In COPWM, the THD values were 44.7% and 2.12% for V_{ab} and I_a respectively. In MNRV (D)PWM, the THD ranged from 37.9% to 44.4% for V_{ab} and from 2.07% to 2.37% for I_a. Meanwhile, for $m = 0.3$, in VVPWM, the THD value for V_{ab} was 81.7%, and for I_a, it was 5.26%. In COPWM, the THD values were 128% and 6.83% for V_{ab} and I_a respectively, showing a significant increase in V_{ab}'s THD compared to VVPWM. In MNRV (D)PWM, the THD for V_{ab} ranged from 64.6% to 139%, while the THD for I_a ranged from 3.03% to 5.27%, showing superior performance compared to VVPWM and COPWM.

Overall, waveform quality analysis of line voltage and phase current for $pf = 0.2/0.9$ and $m = 0.3/0.9$ shows that MNRV (D)PWM outperforms existing methods in terms of power quality.

Figs. 18 and 19 depict the transient characteristics observed when m suddenly transitions from 0.3 to 0.9 under conditions of $pf = 0.9$ and $pf = 0.2$ respectively. Due to the limitation of the oscilloscope's simultaneous measurement channels, V_{dc1}, V_{dc2}, V_{dc3}, and I_a were initially measured during the m transition condition. Subsequently, I_a, V_{an}, and V_{offset} were measured again under the same conditions, and the waveforms were overlaid to compare. The MNRV (D)PWM methods used in the experiments can be

distinguished from the V_{an} and V_{offset} waveforms. It is evident that the dc-link voltages are well balanced and regulated when m undergoes sudden changes under all experimental conditions. Moreover, the current exhibits stable operation with minimal distortion during transient periods.
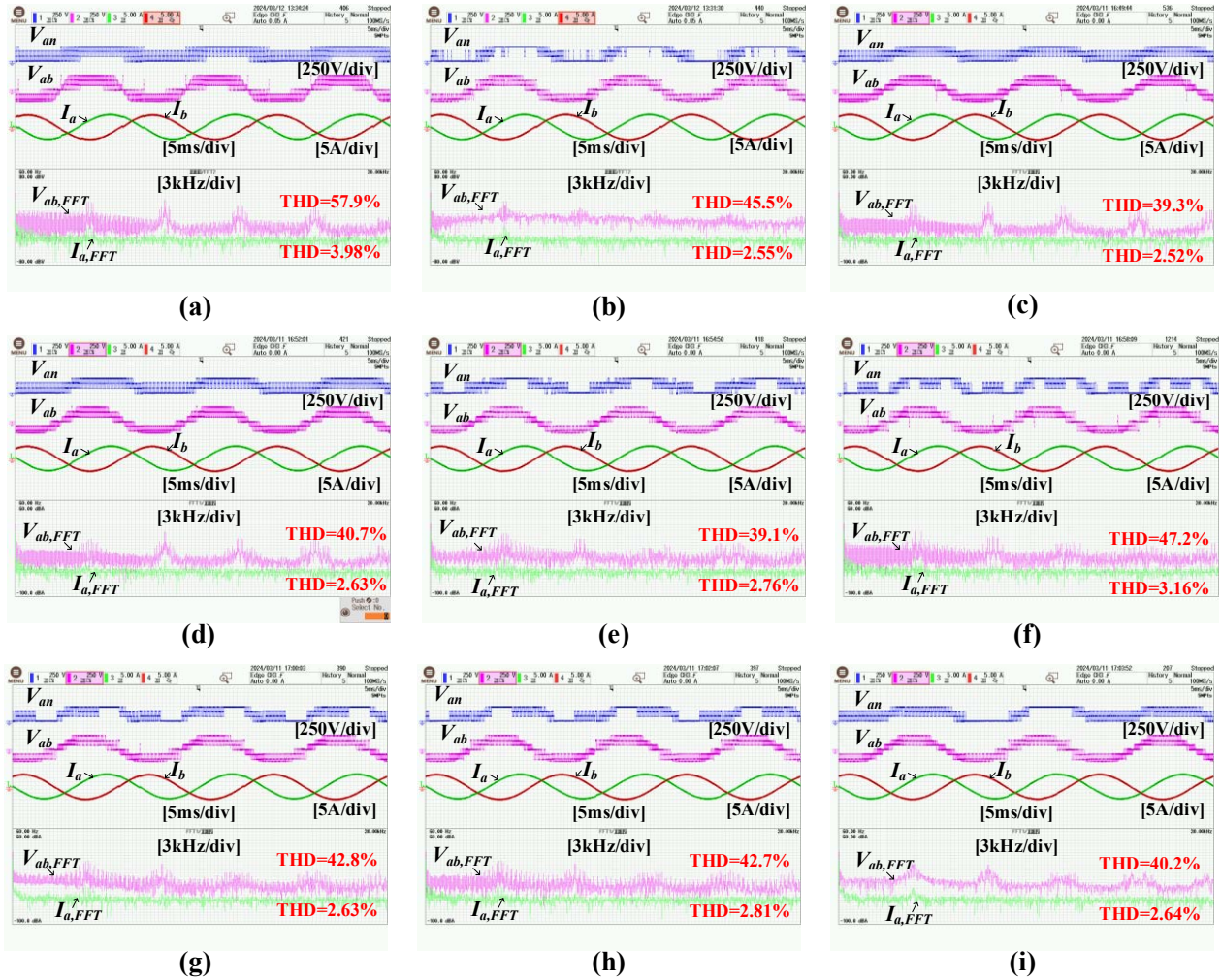

FIGURE 14. Steady state operational waveforms (V_{an}, V_{ab}, I_a, I_b) and harmonics spectrum of V_{ab} and I_a for (a) VVPWM, (b) COPWM, (c) SPWM, (d) SVPWM, (e) 60°DPWM, (f) 30°DPWM, (g) 60°(+30°)DPWM, (h) 60°(-30°)DPWM, and (i) DPWMMAXorMIN when m = 0.9 and pf = 0.9.
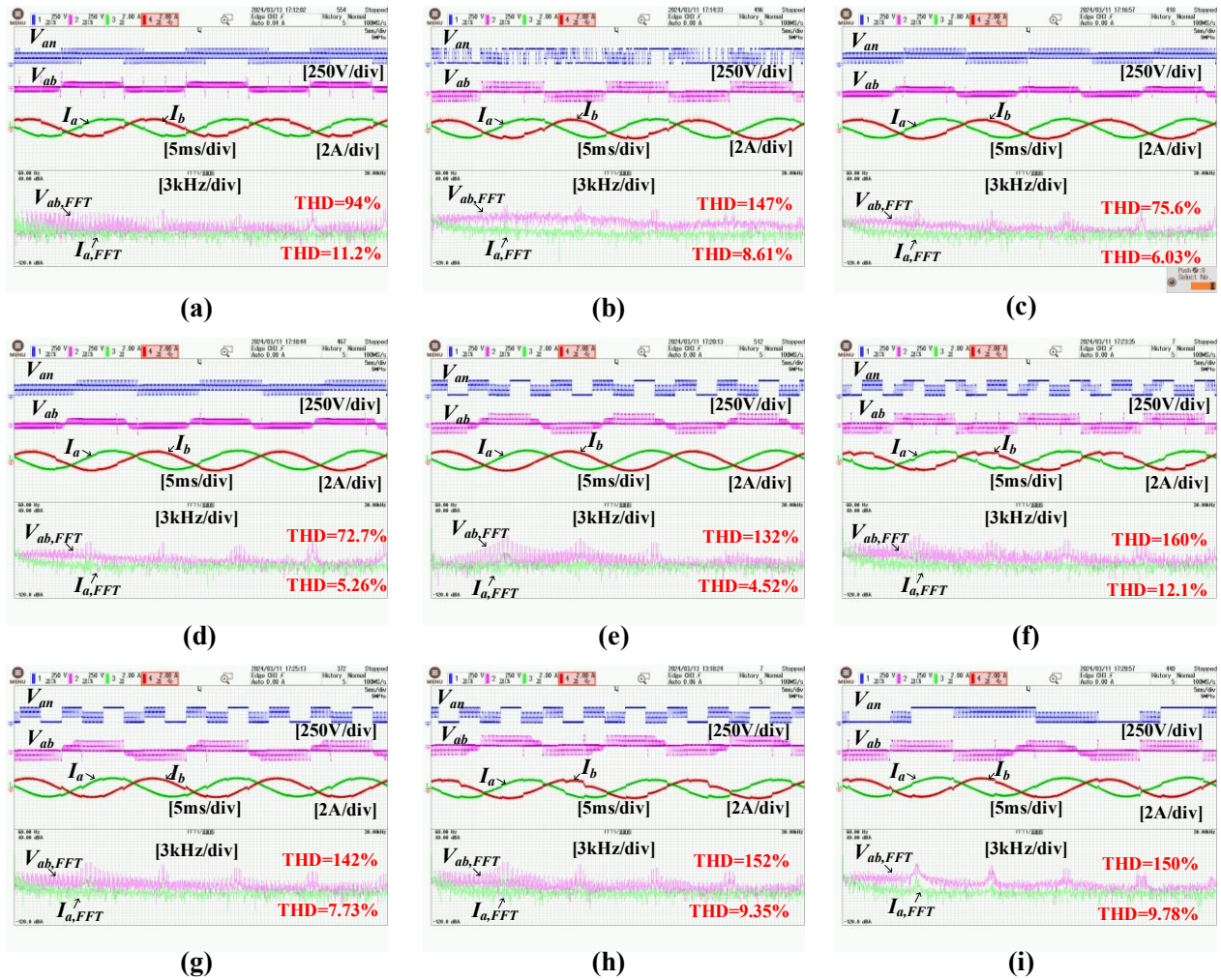
FIGURE 15. Steady state operational waveforms (V_{an}, V_{ab}, I_a, I_b) and harmonics spectrum of V_{ab} and I_a for (a) VVPWM, (b) COPWM, (c) SPWM, (d) SVPWM, (e) 60°DPWM, (f) 30°DPWM, (g) 60°(+30°)DPWM, (h) 60°(-30°)DPWM, and (i) DPWMMAXorMIN when m = 0.3 and pf = 0.9.
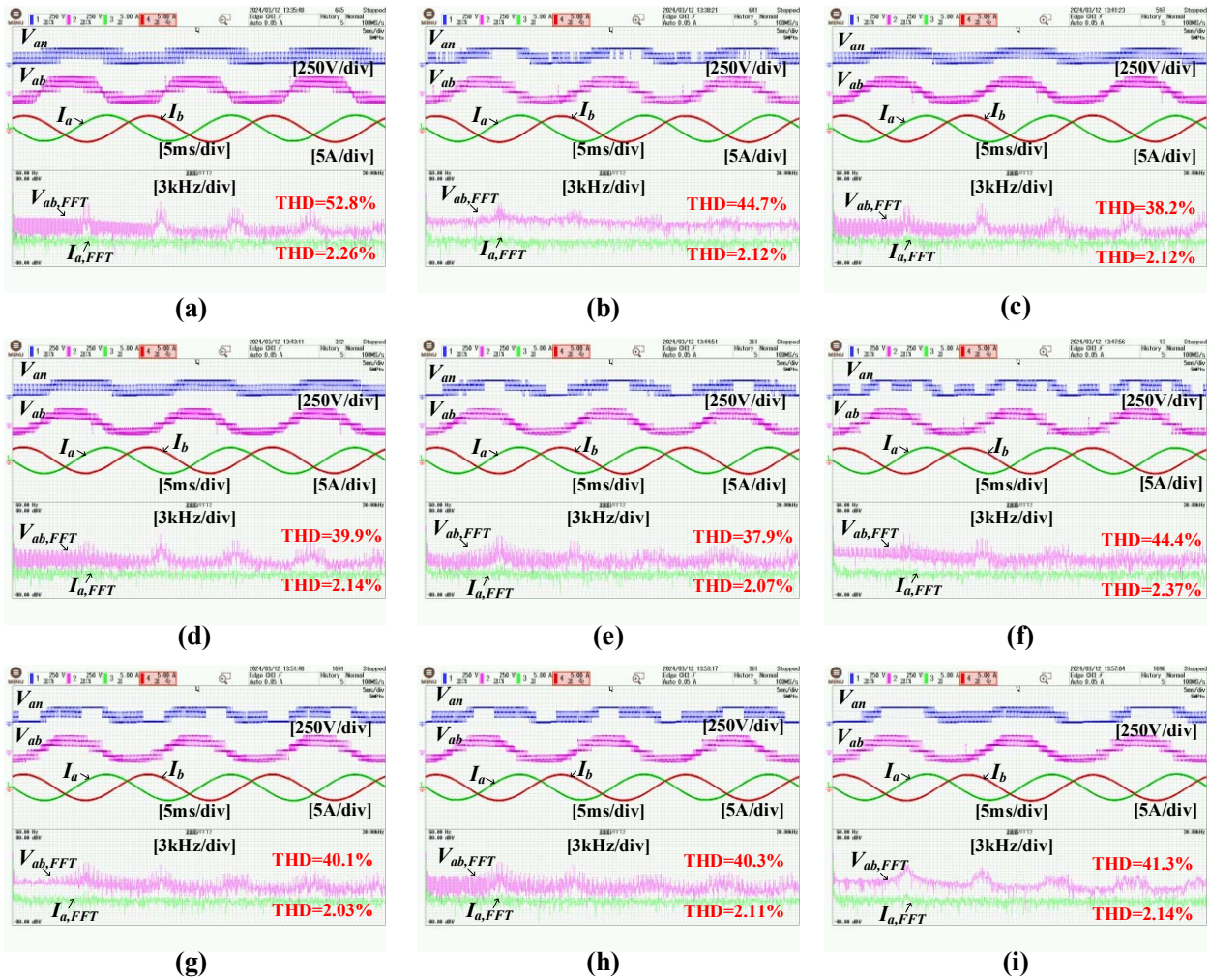
FIGURE 16. Steady state operational waveforms (V$_{an}$, V$_{ab}$, I$_a$, I$_b$) and harmonics spectrum of V$_{ab}$ and I$_a$ for (a) VVPWM, (b) COPWM, (c) SPWM, (d) SVPWM, (e) 60°DPWM, (f) 30°DPWM, (g) 60°(+30°)DPWM, (h) 60°(-30°)DPWM, and (i) DPWMMAXorMIN when m = 0.9 and pf = 0.2.

FIGURE 17. Steady state operational waveforms (V_{an}, V_{ab}, I_a, I_b) and harmonics spectrum of V_{ab} and I_a for (a) VVPWM, (b) COPWM, (c) SPWM, (d) SVPWM, (e) 60°DPWM, (f) 30°DPWM, (g) 60°(+30°)DPWM, (h) 60°(-30°)DPWM, and (i) DPWMMAXorMIN when m = 0.3 and pf = 0.2.
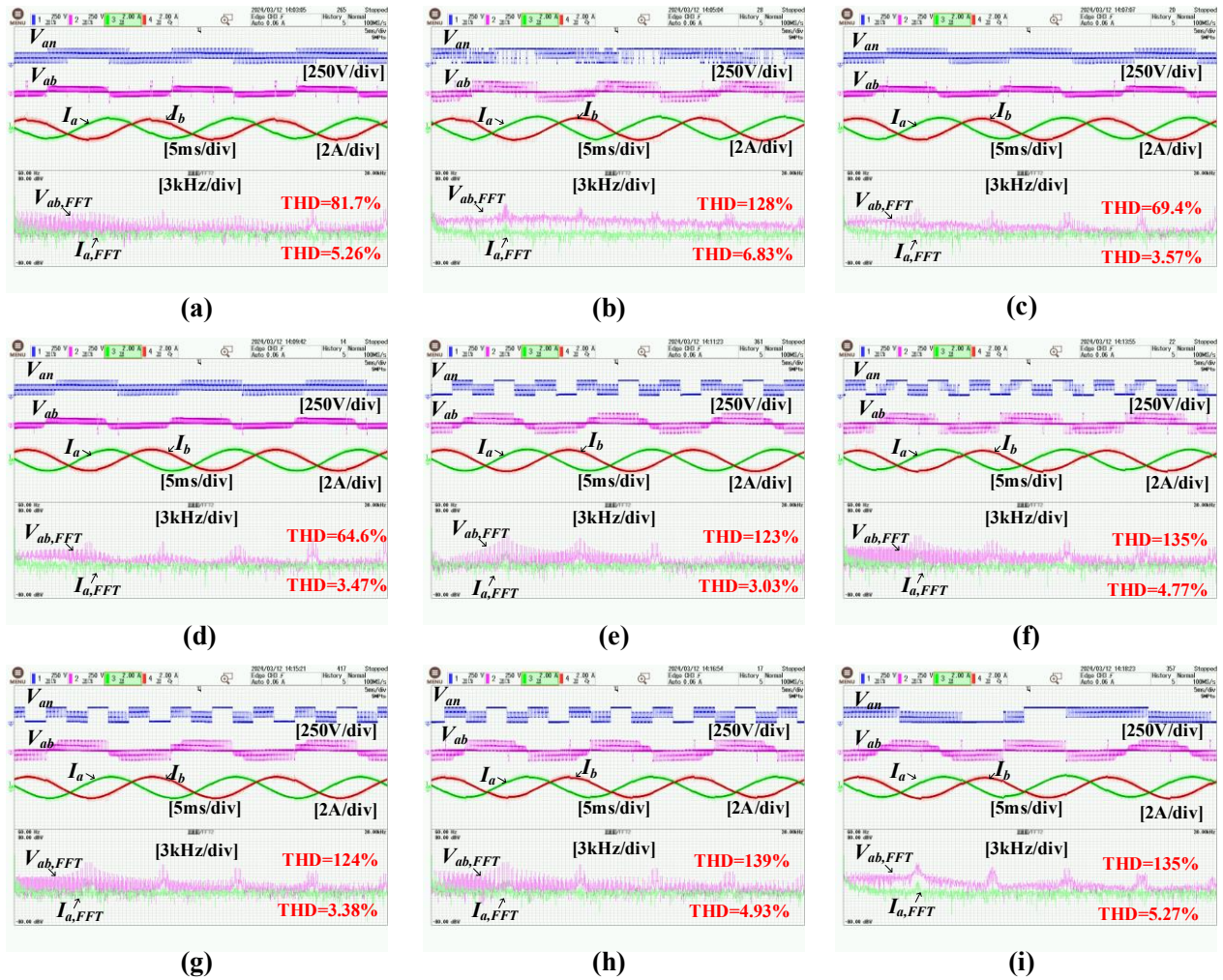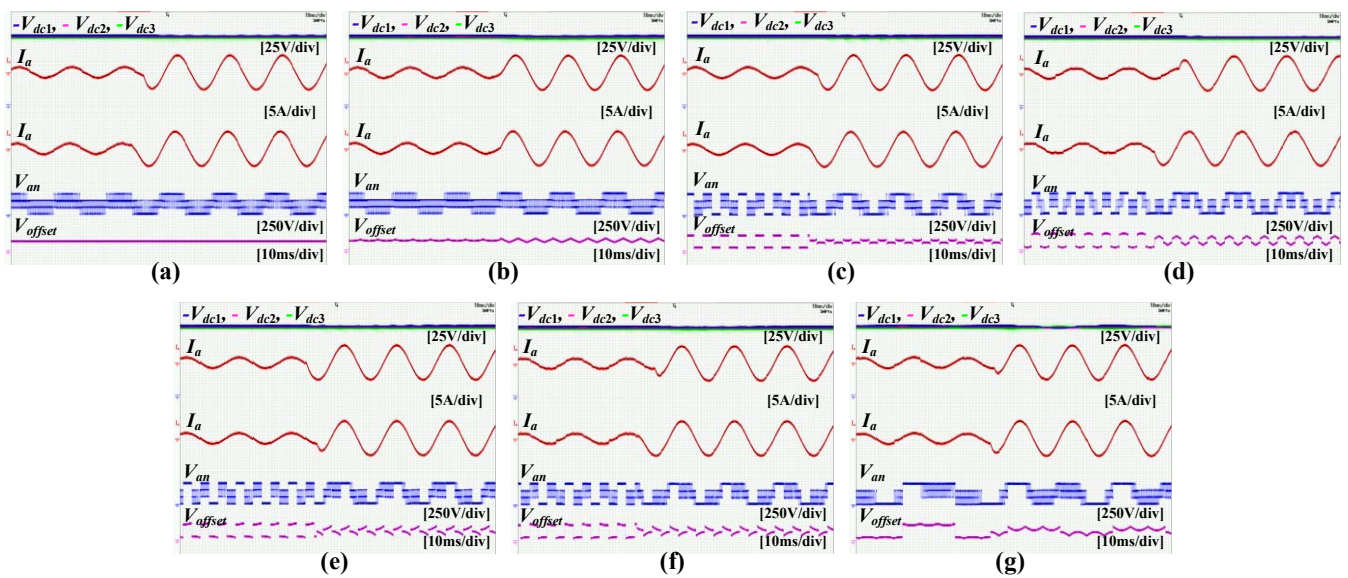

FIGURE 18. Dynamic performance of (a) SPWM, (b) SVPWM, (c) 60°DPWM, (d) 30°DPWM, (e) 60°(+30°)DPWM, (f) 60°(-30°)DPWM, and (g) DPWMMAXorMIN when m suddenly changes from 0.3 to 0.9 with pf = 0.9.
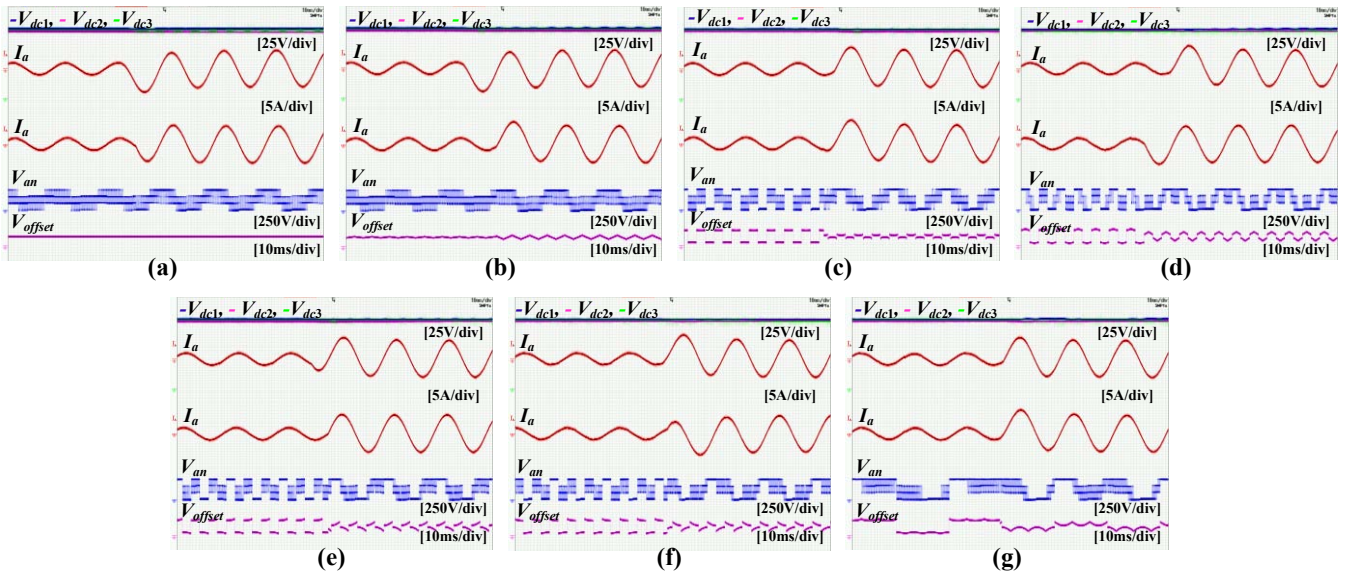
FIGURE 19. Dynamic performance of (a) SPWM, (b) SVPWM, (c) 60°DPWM, (d) 30°DPWM, (e) 60°(+30°)DPWM, (f) 60°(-30°)DPWM, and (g) DPWMMAXorMIN when m suddenly changes from 0.3 to 0.9 with pf = 0.2.

Figs. 20 and 21 demonstrate the dynamic behavior observed when the dc-link reference voltages fluctuate under the conditions of $m = 0.9$, $pf = 0.9$, and $m = 0.9$, $pf = 0.2$, respectively. Similar to Fig. 12, all dc-link voltage references were initially fixed at 66.6V. However, subsequently, they were adjusted to $V_{dc1} = 71.6$V, $V_{dc2} = 61.6$V, and $V_{dc3} = 66.6$V. After a stabilization period, all reference voltages reverted to 66.6V. Subsequently, following another stabilization period,

the reference voltages were adjusted to $V_{dc1} = 71.6$V, $V_{dc2} = 66.6$V, and $V_{dc3} = 61.6$V, before being readjusted back to 66.6V. To distinguish between the applied modulation methods, the DAC output values for d_{E_a} were included.

Despite slight differences in stabilization time compared to simulations, the system demonstrates stable transient characteristics and maintains a balanced dc-link voltage after fluctuations under all conditions, indicating well-controlled behavior.
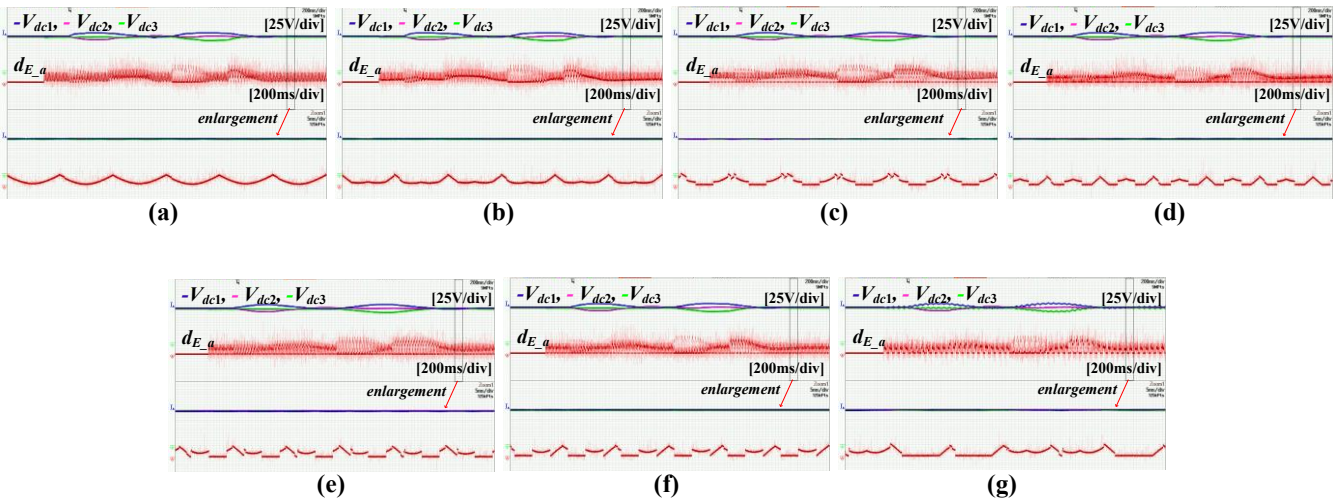

FIGURE 20. Dynamics of dc-link voltage step changes for (a) SPWM, (b) SVPWM, (c) 60°DPWM, (d) 30°DPWM, (e) 60°(+30°)DPWM, (f) 60°(-30°)DPWM, and (g) DPWMMAXorMIN when m = 0.9 and pf = 0.9.
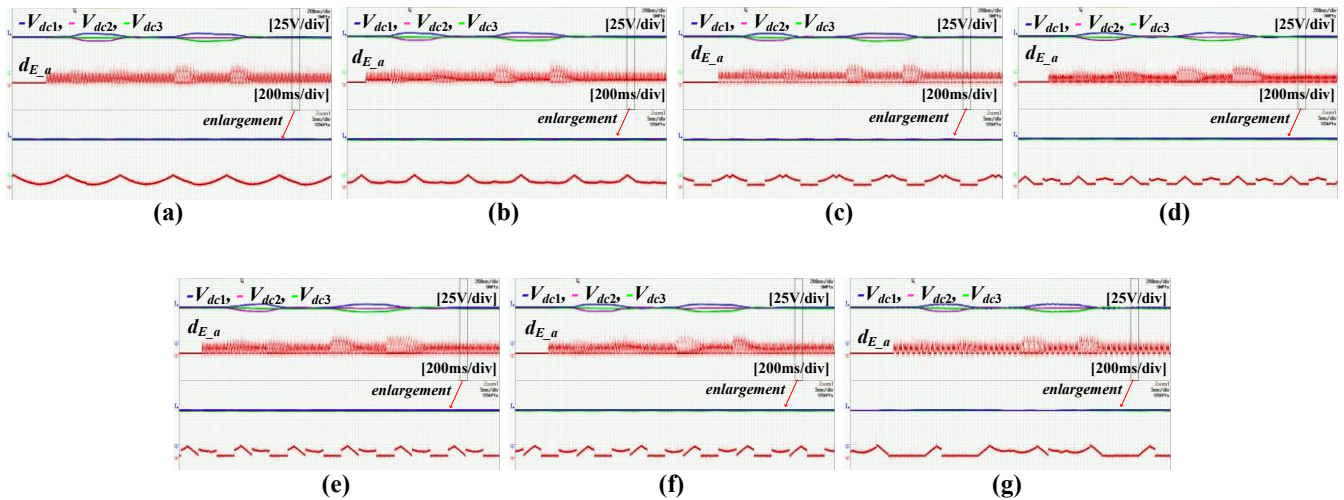
FIGURE 21. Dynamics of dc-link voltage step changes for (a) SPWM, (b) SVPWM, (c) 60°DPWM, (d) 30°DPWM, (e) 60°(+30°)DPWM, (f) 60°(-30°)DPWM, and (g) DPWMMAXorMIN when m = 0.9 and pf = 0.2.

Based on the characteristics observed under both normal and transient conditions, it has been confirmed that the proposed offset voltage injection-based MNRV (D)PWM operates effectively. The analysis of THD in line voltage and phase current indicates superior performance compared to conventional methods such as VVPWM and COPWM. Additionally, it has been observed that the system exhibits stable operational characteristics even when m varies or dc-link reference voltages fluctuate.

VI. CONCLUSION

In this paper, a three-phase diode-clamped four-level PWM inverter based on offset voltage injection utilizing the MNRV (D)PWM methods was proposed. MNRV(D)PWM evenly utilizes multiple adjacent vectors to adjust the charge/discharge characteristics of the dc-link capacitors and fine-tune the duty ratios of the reference vectors to satisfy the *volt·time* product. Additionally, duty compensators proportional to the dc-link voltage deviations are designed to balance the dc-link voltage while facilitating easy closed-loop control. Furthermore, various (D)PWM methods based on the offset voltage injection methods were presented.

By extending the methodology applied to the four-level inverter, a general MNRV (D)PWM method applicable to general high-dimensional multilevel multiphase PWM inverters was also proposed. Additionally, while discussing the characteristics and differences between dc/dc converters and dc/ac inverters using the MNRV (D)PWM method, the generality of MNRV (D)PWM applicable not only to dc/ac but also to dc/dc was demonstrated. Through ΔV_{dc} analysis, it was confirmed that the ripple component of the dc-link voltage generated by the offset voltage injection method is related to the three-phase summation of the product of the duty of the E voltage level vector and the phase current.

Various simulations and experiments have confirmed the efficacy of the proposed method compared to well-established multilevel inverter schemes such as VVPWM and COPWM. While exhibiting a lower average switching frequency, the proposed method demonstrates superior performance in terms of THD for line-to-line voltages and phase currents, particularly at higher m values. Effective control over fluctuations in the dc-link voltage reference and maintenance of voltage balancing were also verified.

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MIN-SUP SONG received the B.S., M.S., and Ph.D. degrees, in 2005, 2007 and 2011, respectively, from the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang, South Korea. He was a Senior Researcher with LG Display, Samsung Electro-Mechanics, and Hyundai-Rotem, South Korea, from 2011 to 2016. He is currently a Senior Researcher with the Smart Electrical & Signaling Division, Korea Railroad Research Institute, Uiwang, South Korea. His research interests include the development of novel circuit topologies and suitable switching modulation techniques for high-power and high-voltage power conversion systems.
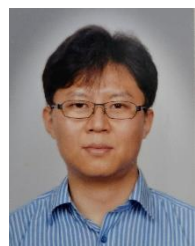
JAEWON KIM received the B.S., M.S and Ph.D. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2006, 2008, and 2018, respectively. He is currently a Principal Researcher with Korea Railroad Research Institute, Uiwang, South Korea. His research interests include onboard energy storage system for railway trains, traction power supply system analysis, and railway electric components reliability analysis.

HWAN-HEE CHO received the B.S. degree from the school of Electrical Engineering at Dankook University, Yongin, Korea, in 2014 and M.S. and Ph.D. degrees in electrical engineering from Korea University, Seoul, Korea, in 2020. He is currently a senior researcher with the Smart Electrical & Signaling Division, Korea Railroad Research Institute, Uiwang, Korea.