IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 25 November 2024, accepted 14 December 2024, date of publication 23 December 2024,
date of current version 31 December 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3521810

RESEARCH ARTICLE

Hierarchical Control Design of a Modular Integrated OBC for Dual-Motor Electric Vehicle Applications

FATEMEH NASR ESFAHANI[1], (Member, IEEE), AHMED DARWISH[1], (Member, IEEE), SAUD ALOTAIBI[2], AND FELICIAN CAMPEAN[3], (Member, IEEE)

[1]School of Engineering, Lancaster University, LA1 4YW Lancaster, U.K.
[2]Department of Electrical Engineering, Engineering College, Shaqra University, Riyadh 11911, Saudi Arabia
[3]School of Engineering, Faculty of Engineering and Digital Technologies, University of Bradford, BD7 1DP Bradford, U.K.

Corresponding author: Ahmed Darwish (a.badawy@lancaster.ac.uk)

This work was supported by Lancaster University.

ABSTRACT This paper presents a novel modular integrated on-board charger (MIOBC) topology and control scheme for dual-motor electric vehicle (EV) applications. Designed for effective power management across various operational states (driving, regenerative braking, and charging), the MIOBC modularises the HV battery and converters, improving fault ride-through (FRT) capability, system flexibility, safety, and efficiency. The architecture features a single-stage bidirectional isolated Cuk converter as its submodule (SM), providing inherent power factor correction (PFC), reduced current ripple, and enhanced power quality. The control strategy integrates finite control set model predictive control (FCS-MPC) with classical proportional-integral (PI) controllers in a hierarchical multi-loop framework. The FCS-MPC dynamically predicts and regulates switching states, minimising a defined cost function to achieve real-time current and voltage tracking while suppressing second-order harmonic components through an innovative capacitor-based energy buffering technique. The paper further explores the impact of the prediction horizon on stability, employing state-space modelling to analyse robustness under parameter variations. Experimental validation is conducted on a 20 kW dual-motor system controlled by a TMS28335fezdsp, demonstrating robust performance under normal and fault conditions, including mode switching and second-order harmonic suppression.

INDEX TERMS Electric vehicles (EVs), on-board battery charger (OBC), model predictive control (MPC), Cuk converter, integrated OBC, modular topology.

I. INTRODUCTION

The number of electric vehicles (EVs) available in the market has been growing rapidly [1], [2]. Their pivotal role in reducing greenhouse gas (GHG) emissions and gasoline consumption, combined with economically advantageous features such as lower operating costs and vehicle-to-grid (V2G) technology, has established EVs as a cornerstone of future transportation systems [3], [4], [5]. EVs can be categorised into four main types: battery electric vehicles (BEVs), hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEVs), and fuel cell electric vehicles (FCEVs). Assured to dominate the market due to their superior design and functionality, BEVs rely exclusively on electricity for operation [6].

Fig. 1 illustrates the detailed schematic of a conventional EV charger system, highlighting key components such as the electric propulsion system, the battery charger, and the low-voltage (LV) battery. The electric propulsion system itself contains electric motor(s), traction inverter (motor drive), and high-voltage (HV) battery.

The battery charger typically consists of a diode bridge converting the AC input voltage to DC, followed by an active power factor correction (PFC) stage and a step-up power converter topology [7]. EV chargers can be implemented either externally (off-board) or within the EV (on-board) [8].

The associate editor coordinating the review of this manuscript and approving it for publication was Dinesh Kumar.

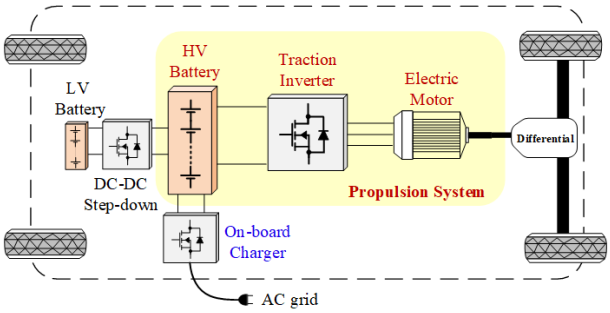


FIGURE 1. Schematic of the conventional EV system with OBC.

While off-board chargers are less constrained by volume, size, and weight, the existing charging infrastructure often falls short of meeting demand, particularly in emergency charging scenarios [9]. Conversely, an on-board charger (OBC) enables EV owners to charge their vehicles wherever a suitable power supply is available. Moreover, new high-power OBC topologies rated at 6.6 kW, 7.4 kW, and 11 kW are gradually replacing traditional 3.3 kW systems [10]. OBCs are further categorised into two main types: integrated and non-integrated battery chargers. In integrated OBCs, specific power electronics components are shared between the propulsion system and the battery charger, reducing the EV drive's weight, volume, and cost.

Traditional EVs typically rely on a single HV battery and motor controller to propel the vehicle. The voltage level at the HV battery terminal must align with the DC-link voltage of the drive system. High voltages, typically 400-800 V, are preferred to minimise electric currents, reducing the size and weight of the required copper cables within the EV. To achieve these voltage levels, multiple battery packs are connected in series. Although this approach increases the voltage at the motor drive terminals, it can introduce challenges, such as shortened battery lifespan and added complexity in balancing battery cells concerning temperature, state of charge (SoC), and voltage [11]. Additionally, operating at high DC-link voltages poses safety risks, creating hazardous working conditions for maintenance personnel and consumers. Another significant drawback of a single HV battery system is the potential shutdown of the entire battery system if a single cell fails. To address these challenges, modularising the HV battery [12], [13] and employing two-wheel-drive architectures [14], [15] have emerged as promising solutions.

Fig. 2 illustrates a dual-motor architecture, where two motors are connected to the wheels via fixed reduction gears. This configuration offers several advantages for EV manufacturing, including reduced weight by utilising smaller reduction gears, increased space for battery placement, and the ability to use smaller electric motors compared to a single large central motor and transmission system [16]. Additionally, using smaller motors necessitates lower battery voltage, which mitigates issues associated with several series-connected batteries, such as prolonged charging times and hazardous working conditions.

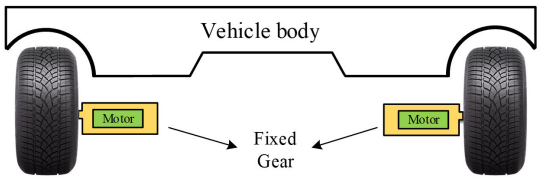


FIGURE 2. Dual-motor EV architecture with fixed reduction gearing.

In a modularised HV battery system, the battery management system (BMS) plays a critical role in improving the EV's reliability and performance by isolating and disconnecting faulty cells, thereby enabling continued operation at reduced power until the fault is resolved [17], [18], [19]. Modular topologies provide a range of benefits that contribute to the overall efficiency and resilience of the EV system [10]:

- **Enhanced safety:** Dividing the HV battery packs into multiple groups ensures that the voltage in each group remains lower than that of a single large HV battery system, thereby reducing potential electrical hazards [9].
- **Reduced stress on semiconductor devices:** Operating multiple power converters at lower voltages and currents minimises stress on semiconductor components, allowing for higher switching frequencies and improved performance [20].
- **Improved power density and efficiency:** Modularisation, while increasing system complexity, allows the power capacity of the converter to expand beyond 100 kW. Utilising semiconductor devices with lower on-resistances and forward voltages further enhances efficiency and power density [9].
- **Flexibility and scalability:** The modular design enables straightforward upgrades and scalability compared to centralised systems. Additional modules can be integrated, or existing ones replaced, without extensive reconfiguration, thereby accommodating evolving technological and energy demands [9], [21].
- **Enhanced battery monitoring and controllability:** Modularisation allows the BMS to independently monitor and control the SoC and state of health (SoH) of each battery group. This leads to more precise performance optimisation and balanced charge/discharge cycles [9], [10], [21].
- **Faster fault detection:** Modular systems simplify the implementation of fault detection algorithms, enabling rapid isolation and disconnection of unhealthy battery cells or faulty semiconductor devices through the BMS. This facilitates easier maintenance and troubleshooting [21].
- **Improved fault ride-through (FRT) capability:** The modular structure enhances FRT performance by maintaining system operation even when a battery module or semiconductor device fails. For instance, a faulty battery module can be bypassed, allowing current to flow

through a switch and maintaining power delivery to the output load. This prevents a complete system shutdown, enhances reliability, and reduces driver anxiety [22].

To ensure user safety, galvanic isolation must comply with the safety standards outlined in the IEC 60950 regulations when the EV enters charging mode [9]. This galvanic isolation can also boost the voltage level at the battery terminals.

Several modular OBC topologies were proposed in the literature, enabling the output sides of power modules to be paralleled to increase voltage levels at the HV battery pack terminals [23], [24]. The dual-active bridge (DAB) DC-DC converter has been a popular choice for high-power modular architectures in EV applications due to its compact size, minimal passive component requirements, zero-voltage switching (ZVS) capability, and fully bidirectional power flow, which supports both regenerative braking and V2G operations.

In [23], three single-phase AC-DC converters were paralleled to form a modular converter delivering 10.5 kW from the AC grid to the HV battery. Each SM featured a two-stage AC-DC configuration comprising a PFC stage and a DAB converter. The integrated OBC achieved high power conversion efficiency and power density across various load conditions. Similarly, [24] described a modularised fast OBC where two DAB converters were series-connected on the primary side and parallel-connected on the secondary side, delivering 20 kW.

A modular OBC architecture was introduced in [25], combining a single-phase/three-phase bidirectional AC-DC rectifier and a DAB DC-DC converter to achieve universal operation across wide input and output voltage ranges. The front-end rectifier utilised a modular buck-boost Y-rectifier design, where each phase integrated a buck-boost converter connected to a shared DC-link, enabling single- and three-phase operation without additional components. This design achieved sinusoidal grid current and unity power factor while ensuring comparable voltage and current stress across phases. The back-end DAB converter provided high-frequency isolation, bidirectional power transfer, and ZVS soft-switching, adapting to battery voltages from 550 V to 850 V. This architecture delivered a peak efficiency exceeding 98% and a power density of 3.7 kW/L, offering a compact, high-performance solution.

The full-bridge (FB) converter is another viable candidate for the galvanically isolated DC-DC converter required in a modularised battery system, as it offers a higher conversion ratio and power level. In [26], an interleaved ZVS FB converter with a voltage doubler was proposed to reduce voltage stress and output ripple current. However, significant reverse recovery losses were identified as a notable drawback.

Alternatively, a modular single-stage topology was proposed in [27], featuring a three-phase isolated AC-DC converter with three electrolytic capacitor-less interleaved totem-pole SMs. Each SM integrated PFC and DC-DC functionalities in a simplified design, with high-frequency isolation provided by transformers. The interleaved topology minimised filter inductor size and eliminated the unfolding bridge, reducing component count and enhancing efficiency. The SMs were paralleled to provide a stable DC charging current under unbalanced grid conditions, achieving a peak efficiency of 96.3% at 11 kW and a power density of 5.5 kW/L.

Similarly, [28] presented a modular single-stage topology using interleaved totem-pole converters with high-frequency isolation for three-phase AC-DC conversion. Each SM operated independently, processing phase-to-neutral voltage and ensuring ripple-free grid current through sinusoidal modulation. A reconfiguration of one SM into an integrated power decoupling circuit (IPDC) facilitated single-phase operation by suppressing second-order harmonic ripple in the charging current. This design achieved a volumetric power density of 5.25 kW/L and a peak efficiency of 97.01% at 11 kW, offering compatibility with global single- and three-phase grid standards.

The modular topology in [29] employed a single-stage interleaved bridgeless AC-DC converter. Each SM integrated a bridgeless boost PFC stage with interleaved control and a CLL resonant circuit for high-frequency isolation and soft-switching. The stacked switch configuration reduces voltage stress on switches to half the DC-link voltage, enhancing reliability for 800 V systems. This topology achieved ZVS turn-on and zero-current switching (ZCS) turn-off for all components, delivering a peak efficiency of 97.9% at 2.4 kW. It offered a compact, efficient solution for high-power EV charging applications without the drawbacks of traditional DAB designs.

Existing power conversion systems in EV applications face several critical challenges, including significant energy losses, limited voltage flexibility, and substantial issues with input and output current ripple. Additionally, many traditional designs, such as DAB-based topologies, experience efficiency degradation at low to medium power levels and involve complex control requirements. Furthermore, while these modular topologies have enhanced power and voltage levels through parallelised converters, they often lack consideration for modularising the HV battery system.

To address these shortcomings, the MIOBC design proposed in this paper modularises both the HV battery and its associated power electronic converters. It also incorporates an isolated, bidirectional, single-stage Cuk-based converter.

Table 1 summarises the specific advantages of the Cuk-based converter topology compared to other DC-DC converter designs used in EV applications, focusing on aspects such as bidirectional power flow, power PFC, current ripple reduction, efficiency, electromagnetic interference (EMI), and overall performance. This innovative topology enhances system efficiency, ensures galvanic isolation for improved safety, offers flexible output voltage adaptation, and maintains continuous input and output currents, effectively mitigating current ripple issues.

TABLE 1. Comparison of DC-DC converter topologies for EV applications [23], [24], [25], [26], [27], [28], [29].

Feature	Cuk-based topology (proposed)	DAB	Resonant DAB	Interleaved FB	Interleaved Totem Pole	Interleaved Bridgeless AC-DC
Bidirectional	Yes	Yes	Yes	Yes	No	No
PFC	Inherent	Can be designed for PFC	Can be designed for PFC	Can be designed for PFC	Inherent	Inherent
Output voltage regulation	Higher and lower outputs	Excellent	Excellent	Excellent	Excellent	Excellent
Current ripple	Lower	Low	Very low	Very low	Moderate	Reduced
Component count	Low	Moderate to high	Moderate to high	Moderate to high	Low	Moderate
Efficiency	High	High efficiency, suitable for high power	Very high efficiency, reduced losses	High efficiency due to interleaving	High efficiency	Very high efficiency
Control complexity	More manageable	More complex	More complex	Moderate complexity	Moderate complexity	Moderate to high complexity
EMI	Low	Moderate	Moderate	Moderate	Low	Low
Thermal performance	Excellent	Good	Good	Moderate	Excellent	Good

The proposed MIOBC requires multiple control loops to effectively manage its decentralised structure and ensure precise voltage and current tracking. A further significant contribution of this paper is the design and validation of a model predictive control (MPC) strategy implemented in the inner loops of individual Cuk-based SMs. This approach is particularly advantageous due to MPC's ability to handle finite control sets (FCS), offering superior disturbance rejection and faster tracking capabilities [30], [31], [32]. The application of MPC is especially beneficial in single-phase charging mode, where it efficiently eliminates second-order harmonics [33].

While other nonlinear control strategies, such as sliding mode control (SMC) [34], [35], hysteresis control (HC) [36], [37], and feedback linearisation control (FLC) [38], have been widely applied to power converters, MPC offers distinct advantages. SMC provides inherent robustness and a fast response but suffers from steady-state chattering and a limited ability to handle multi-objective optimisation or system constraints. Similarly, HC is straightforward to implement and offers rapid response but lacks flexibility for advanced harmonic suppression and incurs high switching losses. Conversely, FLC provides precise linearization of nonlinear systems but requires detailed modelling and is less robust to parameter variations.

In contrast, MPC excels in multi-objective optimisation, constraint handling, and adaptability to system dynamics. These strengths make MPC particularly effective for power converters operating under complex conditions. Table 2 summarises the advantages of MPC compared to other nonlinear controllers.

In [39], an MPC scheme was presented for a single-phase integrated OBC. This scheme introduced a double-prediction algorithm to minimise switching frequency, thereby reducing switching losses compared to conventional sinusoidal pulse-width modulation (SPWM). The active power decoupling technique effectively mitigated the inherent 100 Hz second-order harmonic ripple on the DC link by using the third motor winding, ensuring safe and efficient battery charging. The design achieved sinusoidal grid current at unity power factor and enabled the zero-torque operation of the motor during charging. Despite these advantages, the approach increased control complexity, requiring precise modelling and significant computational effort for the double-prediction MPC algorithm. Furthermore, while the second-order harmonic ripple was significantly reduced, the decoupling process heavily depended on tuning motor parameters, potentially impacting efficiency under certain load conditions.

In [40], predictive current control (PCC), a form of MPC, and proportional-resonant (PR) controllers were employed to achieve efficient and reliable operation of a non-isolated pseudo-six-phase (P6P) integrated OBC. The PCC approach simplified control design by avoiding the need for gain tuning and dynamically managing nonlinear constraints, while the PR controller provided excellent current quality and fault tolerance. Although PCC offered a simpler design and better dynamic performance, it had a higher computational burden. The system's charging capacity was also limited to 52.36% under faulty conditions, which could present challenges in high-power applications.

An enhanced dual-vector model predictive current integrated control (MPCIC) strategy was introduced in [30]. This enhanced MPCIC utilised virtual voltage vectors to effectively suppress harmonic currents, achieving total harmonic distortion (THD) as low as 5.24% in driving mode and 14.7% in in-motion charging mode. The approach also enabled seamless mode switching between driving, DC charging, and in-motion charging, ensuring flexibility and reliability.

TABLE 2. Comparison of MPC and other nonlinear control strategies for EV Applications [30], [31], [32], [33], [34], [35], [36], [37], [38].

Feature	MPC (proposed)	SMC	HC	FLC
Robustness to uncertainties	Moderate (model-dependent)	High	Moderate	Moderate
Harmonic suppression	Directly addressed via cost function	Limited	Limited	Requires compensators
Chattering effect	None (smooth control)	Present	None	None
Constraint handling	Excellent (explicitly incorporated)	Limited	None	None
Dynamic optimization	Multi-objective over prediction horizon	Not optimized	Not optimized	Not optimized
Implementation complexity	High (requires optimization solver)	Moderate	Low	High
Switching losses	Low (optimized switching)	Moderate to High	High	Moderate
Response speed	High (predictive behavior)	High	Moderate	High
Adaptability to EV dynamics	High (flexible cost function design)	Limited (fixed structure)	Limited	Moderate

Experimental results demonstrated robust performance under parameter uncertainties, superior current tracking, and fast dynamic response. However, the method increased design complexity, requiring precise tuning of virtual voltage vectors and cost functions.

The MPC strategy proposed in this paper introduces several enhancements to improve system performance. It dynamically predicts and regulates the converter's switching states to achieve two primary objectives. Firstly, it proactively suppresses second-order harmonic components (at twice the grid frequency). Secondly, it employs a custom-designed cost function incorporating weight factors to balance multiple objectives, including output current regulation, voltage tracking, second-order harmonic suppression, and robustness against parameter variations. This innovative MPC design offers significant advantages over existing methods. It enhances power quality and system stability by minimising second-order harmonic ripple through cost function optimisation. Furthermore, the algorithm reduces chattering and ensures seamless transitions between operational modes (driving, charging, and regenerative braking).

By modularising the battery and power converters, the MIOBC simplifies control as each SM is managed independently through its state-space representation. This modularisation reduces computational load, as each SM operates based on localised dynamics rather than requiring a comprehensive global model. This approach facilitates the efficient management of nonlinear behaviours and dynamic responses. The inner-loop MPC provides precise voltage and current regulation without constant model updates, alleviating the complexity of maintaining a detailed system-wide model. Simultaneously, classical proportional-integral (PI) controllers are employed in the outer loops to generate reference signals for the inner-loop controllers, ensuring overall system stability and coordination among the SMs. This dual-layered control strategy enhances the robustness of the MIOBC and offers a scalable solution adaptable to future modular charger designs, optimising performance across various operational modes.

The main contributions of this paper are summarised as follows:

- **Novel topology design**: The proposed topology modularises both the battery and power converters, significantly enhancing flexibility, fault tolerance, battery balancing, safety, and overall efficiency in the EV's power management system. Cuk-based SMs were specifically selected for their inherent advantages, including built-in PFC and reduced current ripple. While modular OBCs have been previously explored for benefits like flexibility and efficiency, integrating Cuk-based SMs enables the proposed design to address the complexities of multi-mode EV operations, delivering superior power quality and reduced ripple.
- **Development, implementation, and validation of advanced control architecture**: The proposed topology is supported by an innovative control strategy that combines loop shaping with MPC to manage the complex dynamics of the Cuk-based MIOBC. Loop shaping stabilises the outer loop by adjusting the system's frequency response, effectively balancing stability and performance despite the second-order harmonic distortion introduced by the AC grid and Cuk converter. In the inner loop, MPC provides adaptive, real-time control to mitigate these harmonics actively. This dual-layered approach compensates for variations in load and input, ensuring precise voltage and current regulation across the modular system. While loop shaping ensures system-level stability, MPC delivers the precision required at the SM level, resulting in a robust and efficient control framework under normal and fault conditions without compromising performance or stability.

The remainder of this paper is organised as follows: Section II provides an overview of the proposed MIOBC and its key components. Section III details the switching

principles of the MIOBC and presents an in-depth discussion of the proposed FCS-MPC, including its stability analysis. This section also discusses the system-level (outer-loop) control loops. Section IV presents the main experimental results, demonstrating the performance of the proposed MIOBC and its control system across various scenarios, including normal and faulty conditions, mode switching, second-order harmonic suppression, and the impact of outer-loop control gains. Finally, Section V discusses the findings, and conclusions are drawn in Section VI.

II. THE PROPOSED MIOBC DESIGN TOPOLOGY

Fig. 3 illustrates the single-phase layout of the proposed MIOBC. As shown in Fig. 3a, a single-stage isolated Cuk-based topology is employed as the SM. The single-stage configuration of the Cuk converter is particularly suited for this application as it enhances overall system efficiency by minimising energy losses associated with multiple conversion stages. As previously discussed, the Cuk converter offers inherent PFC, bidirectional energy flow capability, and reduced current ripple, improving power quality and system reliability. Its ability to handle wide input voltage variations makes it ideal for integrating modular battery segments and ensures smooth operation across different modes.

The Cuk-based topology comprises the following key components:

- **Input Inductor** (L_1): Designed to handle high peak currents while minimizing ripple.
- **Capacitors** (C_1 **and** C_2): High-frequency capacitors selected for efficient energy storage and transfer; they serve as energy transfer elements, ensuring smooth current and voltage waveforms, reducing EMI, and minimising ripple.
- **High-Frequency Transformer**: Operates in the kHz range with an optimised turn ratio ($N_P : N_S$), providing galvanic isolation between input and output, enabling flexible voltage transformation while blocking DC components and matching voltage levels between the battery and load.
- **Switching Network**: Includes S_P on the input side and an FB converter (S_1, S_2, S_3, S_4) on the output side, enabling bidirectional power flow and efficient energy transfer. The MOSFET-based switches are rated for high current, feature low on-state resistance to minimise conduction losses, and ensure optimal efficiency and performance.
- **Output Filter** (L_o, C_o): Refines the output voltage v_o, ensuring stability and compliance with load requirements. It is designed to achieve low harmonic distortion and smooth voltage regulation, which is critical for motor drive applications.

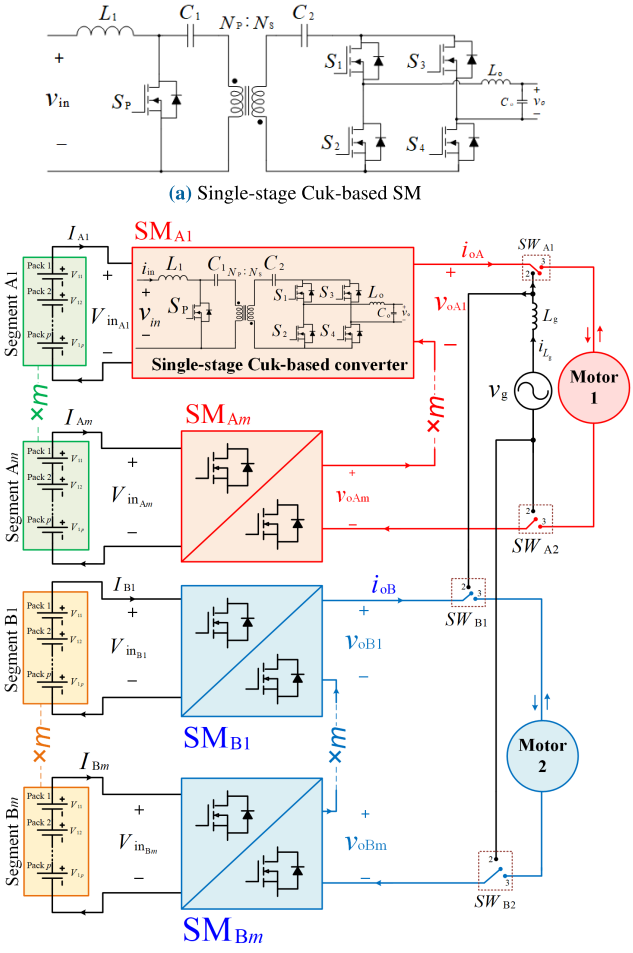
The layout is based on the dual-motor propulsion architecture shown in Fig. 2, with each motor connected to a dedicated set of battery segments and cascaded SMs. Each battery segment consists of "p" series-connected battery packs and "c" parallel-connected battery cells. The total number of battery packs is:

$$n = 2 \times p \times m, \tag{1}$$

where "m" is the number of battery segments. The total number of cells is:

$$n_t = 2 \times p \times m \times c, \tag{2}$$

The traction inverter is integrated into the OBC, enabling three operational modes: driving, charging, and regenerative braking. Single-phase single-pole double-throw (SPDT) switches (SW_{A_h} and SW_{B_h}, where $X = A, B$ and $h = 1, 2$) are used to connect the modular charger to either the AC grid in charging mode or the motors during driving and regenerative braking.



(a) Single-stage Cuk-based SM

(b) Single-phase layout

FIGURE 3. Schematic diagram of the proposed MIOBC.

The output voltage of the cascaded SMs for each motor is:

$$V_X = \sum_{i=1}^{m} v_{o_{X_i}}, \tag{3}$$

where $v_{o_{X_i}}$ is the output voltage of the i^{th} SM ($i = 1, 2, \ldots, m$). The output current of the i^{th} battery segment

is estimated as:

$$I_{\mathrm{i}} \cong \frac{V_o I_o}{m \eta_{SM} V_{in_i}}, \tag{4}$$

where η_{SM} is the efficiency of the i^{th} SM, and V_o and I_o are the root-mean-square (RMS) values of the output voltage and current, respectively.

III. CONTROL DESIGN

The proposed modular OBC and other EV components are depicted in Fig. 4. The modular OBC is designed to operate in three modes: regenerative braking (deceleration), charging, and driving (acceleration). In regenerative braking mode (blue arrows), kinetic energy is redirected to the HV battery segments, with the currents flowing through the HV battery packs ($I_1, \ldots, I_m$) reversing their direction. During charging mode (brown arrows), current flows from the AC grid to the HV battery packs. In driving mode (red arrows), power flows from the HV battery packs to the motors.

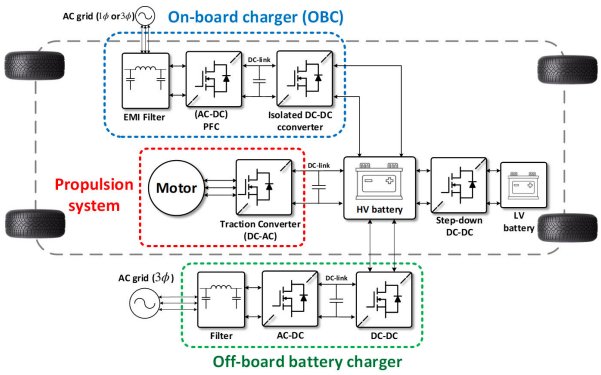


FIGURE 4. Dual-motor EV equipped with charging, driving, and regenerative braking modes.

Two sets of controllers are employed to effectively control the modular OBC. The first is the SM-level controller (inner loop), which manages the operation of individual SMs connected to specific battery segments. The second is the system-level controller (outer loop), which establishes the SM-level controllers' overall output voltage and current references. Notably, the inner loop operates at a significantly higher speed to respond to dynamic changes and executes control actions based on reference values provided by the outer loop.

A. SM-LEVEL (INNER LOOP) CONTROL DESIGN

This section outlines the switching principles of the Cuk-based SM converter and derives the necessary equations for control design. Each SM must maintain specific voltage and current levels, operating as a DC-DC converter during normal driving and regenerative braking modes or an AC-DC rectifier during charging mode. The driver's velocity profile dictates the mode of operation and the control system requirements.

1) SWITCHING PRINCIPLES

The Cuk-based SM operates in three distinct switching states (S_T). The equivalent circuits for these states are illustrated in Fig. 5.

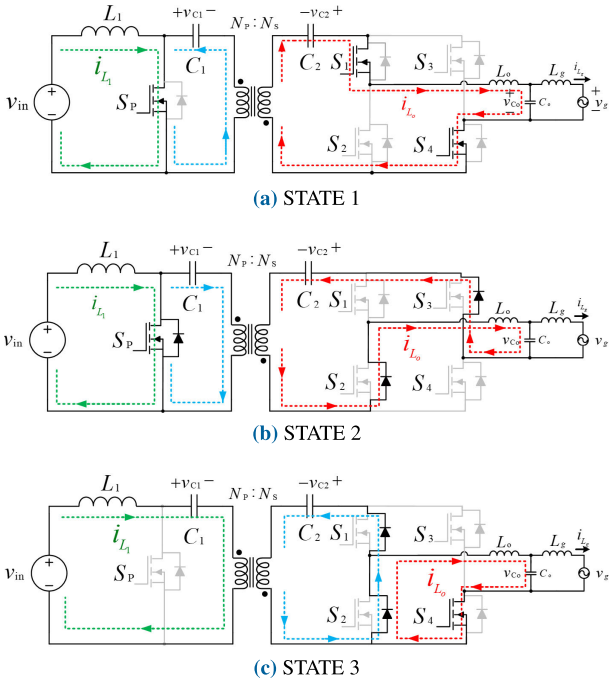


FIGURE 5. Operating modes of the Cuk-based SM.

STATE 1 ($S_T = 1, 0 \leq t < t_1$)**:** As shown in Fig. 5a, switch S_P is in the ON state, charging the input inductor L_1 from the input voltage source v_{in}, resulting in an increase in the input current i_{L_1}. Additionally, switches S_1 and S_4 are turned ON, discharging capacitors C_1 and C_2 into inductor L_o, boosting the output current i_{L_o}.

The state-space equation for this continuous-time system is:

$$\dot{x}(t) = Ax(t) + Bu(t), \tag{5}$$

where $x(t) = [i_{L_1}(t)\ v_{C_{eq}}(t)\ i_{L_o}(t)\ v_{C_o}(t)\ i_{L_g}(t)]^T$, $u(t) = [v_{in}(t)\ v_g(t)]^T$, and $y(t) = [i_{L_o}(t)]$. The governing differential equations for this state are:

$$\begin{cases} \dot{i}_{L_1}(t) = \dfrac{1}{L_1} v_{in}(t) \\ \dot{v}_{C_{eq}}(t) = \dfrac{1}{NC_{eq}} i_{L_o}(t) \\ \dot{i}_{L_o}(t) = \dfrac{1}{L_o} v_{C_{eq}}(t) - \dfrac{1}{L_o} v_{C_o}(t) \\ \dot{v}_{C_o}(t) = \dfrac{1}{C_o} i_{L_o}(t) - \dfrac{1}{C_o} i_{L_g}(t) \\ \dot{i}_{L_g}(t) = \dfrac{1}{L_g} v_{C_o}(t) - \dfrac{1}{L_g} v_g(t). \end{cases} \tag{6}$$

The equivalent capacitor C_{eq} and voltage $v_{C_{eq}}(t)$ are defined as:

$$\begin{cases} C_{eq} = \dfrac{C_1 C_2}{C_1 + N^2 C_2} \\ v_{C_{eq}}(t) = N v_{C_1}(t) + v_{C_2}(t). \end{cases} \tag{7}$$

STATE 2 ($S_T = 2$, $t_1 \leq t < t_2$)**:** As shown in Fig. 5b, switch S_P remains ON, while switches S_1 and S_4 are turned OFF. Consequently, the input inductor L_1 continues charging from v_{in}, increasing i_{L_1}. The output current i_{L_o} flows through diodes D_2 and D_3, discharging inductor L_o into capacitors C_1 and C_2.

The governing differential equations for this state are:

$$\begin{cases} \dot{i}_{L_1}(t) = \dfrac{1}{L_1} v_{in}(t) \\ \dot{v}_{C_{eq}}(t) = \dfrac{1}{N C_{eq}} i_{L_o}(t) \\ \dot{i}_{L_o}(t) = -\dfrac{1}{L_o} v_{C_{eq}}(t) - \dfrac{1}{L_o} v_{C_o}(t) \\ \dot{v}_{C_o}(t) = \dfrac{1}{C_o} i_{L_o}(t) - \dfrac{1}{C_o} i_{L_g}(t) \\ \dot{i}_{L_g}(t) = \dfrac{1}{L_g} v_{C_o}(t) - \dfrac{1}{L_g} v_g(t). \end{cases} \tag{8}$$

This state introduces a subinterval designed to trap second-order harmonic components within the SM's passive components, specifically C_1 and C_2, decoupling the input and output currents. During this interval, i_{L_1} increases while i_{L_o} decreases, effectively mitigating second-order harmonics.

STATE 3 ($S_T = 3$, $t_2 \leq t < t_s$)**:** In this state, as shown in Fig. 5c, switch S_P turns OFF, causing L_1 to discharge into C_1 and C_2. Switch S_4 remains ON, discharging L_o and reducing i_{L_o}.

The differential equations governing this state are:

$$\begin{cases} \dot{i}_{L_1}(t) = -\dfrac{1}{N L_1} v_{C_{eq}}(t) + \dfrac{1}{L_1} v_{in}(t) \\ \dot{v}_{C_{eq}}(t) = \dfrac{1}{N C_{eq}} i_{L_1}(t) \\ \dot{i}_{L_o}(t) = -\dfrac{1}{L_o} v_{C_o}(t) \\ \dot{v}_{C_o}(t) = \dfrac{1}{C_o} i_{L_o}(t) - \dfrac{1}{C_o} i_{L_g}(t) \\ \dot{i}_{L_g}(t) = \dfrac{1}{L_g} v_{C_o}(t) - \dfrac{1}{L_g} v_g(t). \end{cases} \tag{9}$$

The primary waveforms of the SM during these three states are illustrated in Fig. 6.

2) THE PROPOSED FCS-MPC CONTROL STRATEGY

Fig. 7 illustrates the integration of MPC within the control framework for regulating the voltages and currents of individual SMs across all operational modes. In this framework, the MPC controller uses the desired input and output current signals ($i_{L_1}{}^*(t)$, $i_{L_o}{}^*(t)$, and $v^*_{C_{eq}}(t)$) provided by the system-level control (outer loop) as inputs. These inputs are processed to generate gate signals for the power switches (S_P, S_1, S_2, S_3, S_4) within each SM.

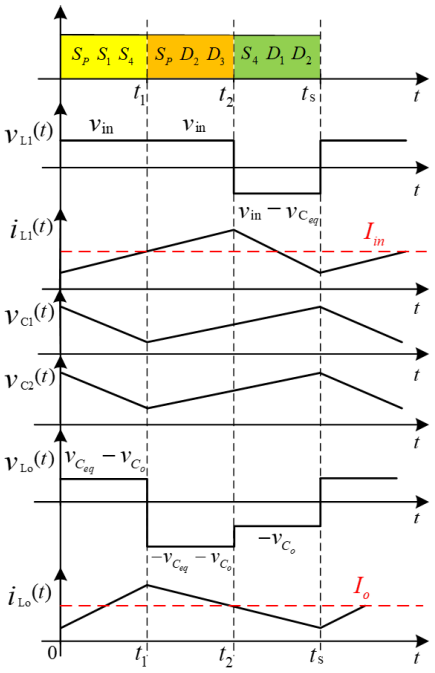


FIGURE 6. Key waveforms of the Cuk-based SM (for the positive half-cycle).

MPC offers several advantages that make it particularly effective in this framework. Firstly, its capability to handle multiple variables, including input currents, output currents, and capacitor voltages, facilitates seamless control of the system's dynamics (an aspect that can be significantly more challenging with classical PI controllers). Secondly, the FCS-MPC approach allows for dynamic adaptation, enabling online modifications of the control logic to correct errors or respond to changing operating conditions. Thirdly, MPC excels in multi-objective optimisation, balancing competing system requirements such as harmonic suppression, current tracking, and voltage regulation. Fourthly, it inherently manages system constraints and nonlinearity, ensuring robust and efficient performance even under complex dynamics. Furthermore, using MPC in this design addresses specific challenges, such as zero-crossing spikes, providing smooth operation and minimising disturbances during transitions [41]. Since the inner loop receives its reference values from the outer loop control, it must operate significantly faster. This demand suits MPC well due to its predictive capabilities and fast response.

The main steps of the FCS-MPC are depicted in the block diagram shown in Fig. 8 and can be outlined as follows:

1) Measure or estimate the voltages and currents of the SM during the switching period k using sensing boards or mathematical equations.
2) Apply all possible switching states, denoted as S_j where $j = 1, \ldots, s$, for any power electronic converter.
3) Predict voltages and currents for the next period $(k + 1)$ based on the switching states from the previous step.

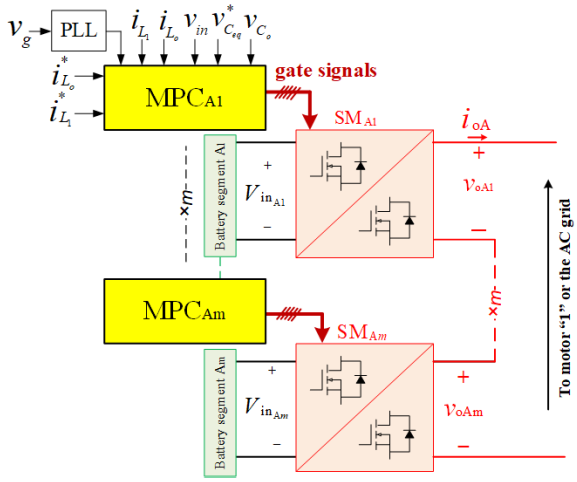


FIGURE 7. Block diagram of the proposed FCS-MPC used at SM-level (inner loop controller).

4) Evaluate the cost function J_j for each switching state in step (2) using the predicted values from step (3). The cost function is typically chosen to minimise the error of specific voltages or currents, expressed as $J = \left|x^*_{k+1} - x_{k+1}\right|^2$.
5) Select the optimal cost function to identify the switching state that minimises the error of the desired voltage or current determined in step (4).
6) Store the computed values in the micro-controller for utilisation in the subsequent period.

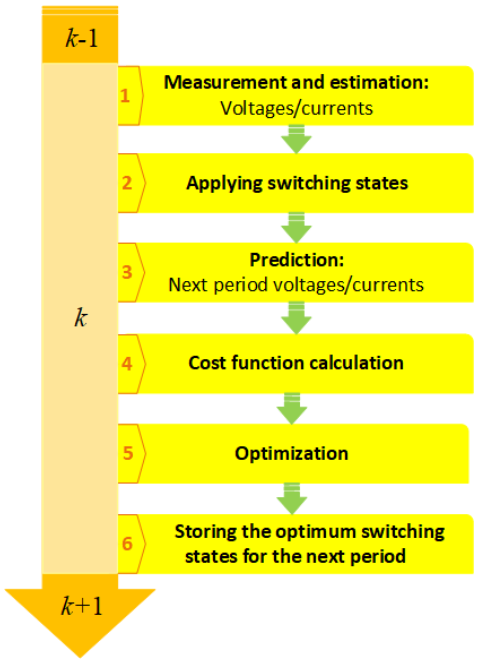


FIGURE 8. Pipeline for the proposed FCS-MPC.

The proposed FCS-MPC requires information about v_{in}, i_{L_1}, $v_{C_{eq}}$, v_{C_o}, and i_{L_o}. The differential equations for these state variables can be expressed as functions of the switching state S_T as follows:

$$\begin{cases} \dot{i}_{L_1}(t) = \dfrac{1}{L_1} v_{in}(t) - \dfrac{M_1}{2NL_1} v_{C_{eq}}(t) \\ \dot{v}_{C_{eq}}(t) = \dfrac{M_2}{2NC_{eq}} i_{L_o}(t) + \dfrac{M_1}{2NC_{eq}} i_{L_1}(t) \\ \dot{i}_{L_o}(t) = \dfrac{-M_2}{2L_o} v_{C_{eq}}(t) - \dfrac{1}{L_o} v_{C_o}(t). \end{cases} \tag{10}$$

where $M_1 = (S_T - 1)(S_T - 2)$ and $M_2 = (-3S_T^2 + 13S_T - 12)$.

The Euler forward method provides a straightforward and efficient approach to approximating the state values at the next time step (i.e., $k+1$). This method assumes the derivative remains constant over the sampling interval t_s. By applying the Euler forward method in the discrete-time domain, the state update can be expressed as:

$$x(k+1) \approx x(k) + t_s \dot{x}(k), \tag{11}$$

Therefore,

$$\begin{cases} i_{L_1}(k+1) = \dfrac{t_s}{L_1} v_{in}(k) - \dfrac{M_1 t_s}{2NL_1} v_{C_{eq}}(k) + i_{L_1}(k) \\ v_{C_{eq}}(k+1) = \dfrac{M_2 t_s}{2NC_{eq}} i_{L_o}(k) + \dfrac{M_1 t_s}{2NC_{eq}} i_{L_1}(k) + v_{C_{eq}}(k) \\ i_{L_o}(k+1) = \dfrac{-M_2 t_s}{2L_o} v_{C_{eq}}(k) - \dfrac{t_s}{L_o} v_{C_o}(k) + i_{L_o}(k). \end{cases} \tag{12}$$

The FCS-MPC algorithm predicts the system's behaviour for each potential switching state and selects the optimal state to minimise the cost function J. This process aids in regulating the input and output currents of the SM, thereby ensuring adequate power quality.

3) SECOND-ORDER HARMONIC SUPPRESSION USING THE PROPOSED FCS-MPC

As mentioned before, an additional subinterval is introduced in the Cuk-based SM to trap the second-order harmonic component within the system's passive components, specifically the coupling capacitors (C_1 and C_2). These capacitors act as buffers, storing the harmonic energy and preventing it from propagating to the output. This supports maintaining a stable input current and generating sinusoidal output voltages and currents. To achieve this, the amplitude and phase of the second-order harmonic component must be estimated.

The apparent power S_g generated by a single-phase AC grid is expressed as:

$$S_g = P_g + jQ_g. \tag{13}$$

The grid current and voltage are defined as:

$$\begin{cases} i_{L_g}(t) = I_{L_g} \sin(\omega t + \phi) \\ v_g(t) = V_g \sin(\omega t). \end{cases} \tag{14}$$

Thus, P_g and Q_g are given by:

$$\begin{cases} P_g = \dfrac{V_g I_{L_g}}{2} \cos(\phi) \\ Q_g = -\dfrac{V_g I_{L_g}}{2} \cos(2\omega t + \phi). \end{cases} \tag{15}$$

To trap the oscillating power containing the second-order harmonic Q_g within the capacitors (C_1 and C_2), the following relationship must hold:

$$Q_g + Q_{C_{eq}} = 0. \tag{16}$$

Substituting into this equation yields:

$$\frac{V_g I_{L_g}}{2}\cos(2\omega t + \phi) = C_{eq}\frac{dv_{C_{eq}}}{dt}v_{C_{eq}}(t). \tag{17}$$

Assuming that the voltage across the capacitor $v_{C_{eq}}(t)$ includes a DC component and an AC component at 2ω:

$$v_{C_{eq}}(t) = \underbrace{V_{C_{eq}}}_{\text{DC component}} + \underbrace{V_{2\omega}\sin(2\omega t + \phi_{2\omega})}_{\text{AC component}}, \tag{18}$$

where $V_{2\omega}$ and $\phi_{2\omega}$ represent the amplitude and phase of the second-order harmonic component. Substituting (18) into (17) results in:

$$\frac{V_g I_{L_g}}{2}\cos(2\omega t + \phi) = 2\omega C_{eq} V_{C_{eq}} V_{2\omega}\cos(2\omega t + \phi_{2\omega}) + \omega C_{eq} V_{2\omega}^2 \sin(4\omega t + 2\phi_{2\omega}). \tag{19}$$

For small-signal analysis, the term $\omega C_{eq} V_{2\omega}^2 \sin(4\omega t + 2\phi_{2\omega})$ can be considered negligible, therefore:

$$\frac{V_g I_{L_g}}{2}\cos(2\omega t + \phi) \approx 2\omega C_{eq} V_{C_{eq}} V_{2\omega}\cos(2\omega t + \phi_{2\omega}). \tag{20}$$

Equating the coefficients, we obtain the amplitude:

$$V_{2\omega} = \frac{V_g I_{L_g}\sin(\phi)}{4\omega C_{eq} V_{C_{eq}}}. \tag{21}$$

The phase relationship:

$$\phi_{2\omega} = \phi. \tag{22}$$

For effective harmonic suppression, the capacitor must follow the $v_{C_{eq}}(t)$ in (18). In addition, the coupling capacitors must be sized to store the required harmonic energy without reaching voltage limits or saturation. This ensures that the second-order harmonic is trapped effectively within the coupling capacitors, resulting in steady output and high power quality.

The Cuk-based SM converter operates in three S_T to control the input and output energy transfer. The MPC method is designed to dynamically predict and manage these states, thereby suppressing the second-order harmonic components at twice the grid frequency (2ω) that can arise during operation. The primary objectives of the MPC in this context are precise current and voltage tracking, minimised harmonic distortion, and efficient overall operation. The FCS-MPC achieves these through the following key mechanisms:

(i) **Predictive regulation**: Using real-time data, the MPC predicts future state variables (i_{L_1}, i_{L_o}, and $v_{C_{eq}}$). By anticipating the occurrence of second-order harmonic components within these variables, the MPC dynamically adjusts the switching states to suppress their impact effectively.

(ii) **Cost function design for harmonic suppression**: The MPC employs a cost function J specifically tailored to target second-order harmonics. This design ensures an optimal balance between accurate voltage/current tracking and the suppression of harmonic content. The cost function J, evaluated over the prediction horizon N_{PH}, is defined as:

$$\begin{aligned} J = \sum_{y=1}^{N_{\text{PH}}} \Big[& \left| i_{L_1}^*(k+y) - i_{L_1}(k+y) \right|^2 \\ & + W_f \left| i_{L_o}^*(k+y) - i_{L_o}(k+y) \right|^2 \\ & + W_h \left| v_{C_{eq}}^*(k+y) - v_{C_{eq}}(k+y) \right|^2 \Big] \\ & + \sum_{\rho} W_\rho \Delta_\rho(k+y), \end{aligned} \tag{23}$$

where y represents the index for the prediction step within the horizon N_{PH}, denoting the number of future time steps considered. The term $W_h \left| v_{C_{eq}}^*(k+y) - v_{C_{eq}}(k+y) \right|^2$ ensures that the voltage across the decoupling capacitors $v_{C_{eq}}(t)$ tracks its desired value, effectively confining the second-order harmonic components within the coupling capacitors rather than allowing them to propagate to the output. This is critical for maintaining high power quality and system stability.

The weight factors W_f, W_h, and W_ρ play a crucial role in prioritising specific control objectives and enhancing system robustness. For example, setting $W_f > 1$ emphasises output current tracking more, which is essential for motor control applications where precise torque regulation is required. This ensures effective current regulation during driving modes while allowing for less stringent tracking of battery current. Similarly, increasing W_h prioritises capacitor voltage tracking, vital for suppressing harmonic content and preserving system stability.

Robustness is further incorporated into the cost function through the additional term $\sum_\rho W_\rho \Delta_\rho(k+y)$, where $\Delta_\rho(k+y)$ represents deviations in predictions due to parameter variations, such as changes in L_1, C_{eq}, and L_o. These deviations can shift the system's eigenvalues and potentially impact stability. By assigning appropriate weights W_ρ, the MPC algorithm penalises such deviations, enabling it to anticipate potential instabilities and proactively adjust its control strategy to maintain reliable performance.

Algorithm 1 is implemented within the micro-controller to determine the optimal S_T. These states are then used to generate the pulse-width modulation (PWM) gate signals for the five switches of each SM, ensuring precise control and efficient operation of the system.

A detailed breakdown of the FCS-MPC algorithm is as follows:

- **Function inputs:** The algorithm takes as inputs the actual and reference currents (i_{L_1}, $i_{L_1}^*$, i_{L_o}, $i_{L_o}^*$), actual

Algorithm 1 FCS-MPC Algorithm

function FCS-MPC(i_{L_1}, $i^*_{L_1}$, i_{L_o}, $i^*_{L_o}$, v_{in}, $v_{C_{eq}}$, $v^*_{C_{eq}}$, v_{C_o}, W_f, W_h, W_ρ)
  Outputs: S_P, S_1, S_2, S_3, S_4
  Initialize: $J_{opt} \leftarrow \infty$
  Define possible states:
    States $= \begin{bmatrix} 1 & 0 & 1 & 1 & 0 \\ 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 \end{bmatrix}$
  for $S_T = 1$ to 3 **do**
    Predict: $i_{L_1}(k+1)$, $v_{C_{eq}}(k+1)$, $i_{L_o}(k+1)$
  end for
  for $S_T = 1$ to 3 **do**
    Compute cost function:
      $J_{st} = \sum_{y=1}^{N_{\text{PH}}} \Big[\left| i^*_{L_1}(k+y) - i_{L_1}(k+y) \right|^2$
      $+W_f \left| i^*_{L_o}(k+y) - i_{L_o}(k+y) \right|^2$
      $+W_h \left| v^*_{C_{eq}}(k+y) - v_{C_{eq}}(k+y) \right|^2 \Big]$
      $+ \sum_\rho W_\rho \Delta_\rho(k+y)$
    if $J_{st} < J_{opt}$ **then**
      $J_{opt} \leftarrow J_{st}$
      $S_{T_{opt}} \leftarrow S_T$
    end if
  end for
  Return: $S_{T_{opt}}$
end function

and reference capacitor voltages ($v_{C_{eq}}$, $v^*_{C_{eq}}$), voltages (v_{in} and v_{C_o}), and weight factors (W_f, W_h, and W_ρ).

- **Initialisation:** The optimal cost, J_{opt}, is initialised to infinity to ensure that any calculated cost during the iteration will be smaller.
- **Defining possible states:** The algorithm defines a set of potential S_T in a matrix format, representing all valid combinations of switch positions.
- **Prediction loop:** For each switching state S_T, the algorithm predicts the future values of key variables, including $i_{L_1}(k+1)$, $v_{C_{eq}}(k+1)$, and $i_{L_o}(k+1)$. These predictions are based on the dynamic model of the system and the influence of the specific switching state over the prediction horizon N_{PH}.
- **Cost calculation:** The algorithm evaluates the cost function J_{st} for each switching state by computing the squared differences between the predicted and reference values of currents and voltages. Weight factors W_f, W_h, and W_ρ are applied to prioritise specific objectives.
- **Optimal state selection:** If the calculated cost J_{st} for an S_T is lower than the current J_{opt}, the algorithm updates J_{opt} and assigns S_T as optimal switching state $S_{T_{opt}}$.
- **Output:** The algorithm outputs the optimal switching state $S_{T_{opt}}$. This state is then used to generate PWM signals for the system's switches, ensuring the desired performance objectives are met.

4) EVALUATION OF PREDICTION HORIZON N_{PH} IMPACT ON STABILITY IN THE PROPOSED MPC METHOD

The linearised system dynamics are used in state-space form for stability and robustness analysis. Using (10), the nonlinear function $f(x, u)$, which defines the system dynamics, is expressed as:

$$f(x,u) = \begin{bmatrix} \dot{i}_{L_1} = \frac{1}{L_1} v_{in} - \frac{M_1}{2NL_1} v_{C_{eq}} \\ \dot{v}_{C_{eq}} = \frac{M_2}{2NC_{eq}} i_{L_o} + \frac{M_1}{2NC_{eq}} i_{L_1} \\ \dot{i}_{L_o} = -\frac{M_2}{2L_o} v_{C_{eq}} - \frac{1}{L_o} v_{C_o} \end{bmatrix}. \tag{24}$$

The continuous-time Jacobian matrices A and B are derived as:

$$A = \left.\frac{\partial f}{\partial x}\right|_{(x^*,u^*)} = \begin{bmatrix} 0 & -\frac{M_1}{2NL_1} & 0 \\ \frac{M_1}{2NC_{eq}} & 0 & \frac{M_2}{2NC_{eq}} \\ 0 & -\frac{M_2}{2L_o} & 0 \end{bmatrix}. \tag{25}$$

$$B = \left.\frac{\partial f}{\partial u}\right|_{(x^*,u^*)} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \end{bmatrix}. \tag{26}$$

Substituting $\dot{x}(k) = Ax(k) + Bu(k)$ from the continuous-time model into (11) gives:

$$\begin{aligned} x(k+1) &= x(k) + t_s(Ax(k) + Bu(k)) \\ &= (I + t_s A)x(k) + t_s Bu(k), \end{aligned} \tag{27}$$

where I is the identity matrix of the same size as A. The discrete-time linearised system is represented as:

$$x(k+1) = A_d x(k) + B_d u(k), \tag{28}$$

where the discrete-time state transition matrices are extracted as:

$$A_d = I + t_s A = \begin{bmatrix} 1 & -\frac{M_1 t_s}{2L_1 N} & 0 \\ \frac{M_1 t_s}{2C_{eq} N} & 1 & \frac{M_2 t_s}{2C_{eq} N} \\ 0 & -\frac{M_2 t_s}{2L_o} & 1 \end{bmatrix}. \tag{29}$$

$$B_d = t_s B = \begin{bmatrix} \frac{t_s}{L_1} \\ 0 \\ 0 \end{bmatrix}. \tag{30}$$

The prediction horizon N_{PH} in MPC plays a crucial role in determining the stability of the system. The system's stability over the prediction horizon can be analysed by studying the eigenvalues of the matrix $A_d^{N_{\text{PH}}}$, which represents the effect of the state transition over N_{PH} steps:

$$x(k + N_{\text{PH}}) = A_d^{N_{\text{PH}}} x(k). \tag{31}$$

The eigenvalues of $A_d^{N_{\text{PH}}}$ are given by $\lambda_\alpha(A_d^{N_{\text{PH}}})$. For stability over N_{PH} steps, the following condition must be satisfied:

$$\max_{\alpha} |\lambda_\alpha(A_d^{N_{\text{PH}}})| < 1, \quad \forall\alpha \tag{32}$$

where α is the index for the eigenvalues. The impact of N_{PH} on stability is verified by simulating the eigenvalue behaviour of $A_d^{N_{\text{PH}}}$ for different prediction horizons. The analysis involves computing the eigenvalues for various N_{PH} values and plotting their maximum real part (i.e., $|\lambda_\alpha(A_d^{N_{\text{PH}}})|$) to observe trends.

As shown in Fig. 9, the maximum real part of the eigenvalues decreases as the prediction horizon N_{PH} increases from 1 to 20. Initially, at $N_{\text{PH}} = 1$, the maximum real part is approximately 0.9, indicating that the system is stable but close to the instability threshold. As N_{PH} grows, the maximum real part steadily decreases, reaching a value of around 0.3 at $N_{\text{PH}} = 20$. This trend suggests that increasing the prediction horizon enhances system stability by ensuring the control strategy accounts for a longer-term view of the system dynamics. However, this comes at the cost of control and computational complexities. Therefore, while a longer prediction horizon can improve stability and robustness, balancing the computational load associated with larger N_{PH} values is essential.

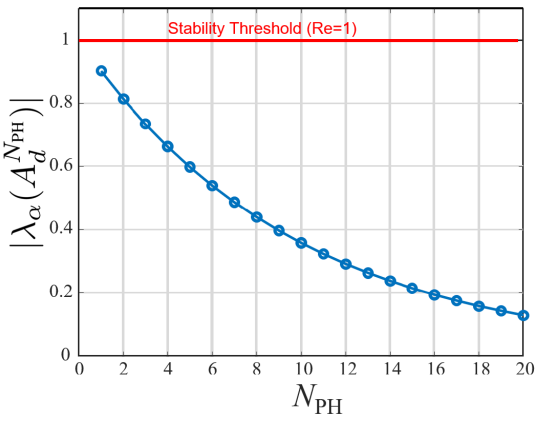


FIGURE 9. Maximum Real Part of Eigenvalues as a Function of Prediction Horizon N_{PH}.

B. SYSTEM-LEVEL (OUTER LOOP) CONTROL DESIGN

The outer loop control determines the reference values for the inner loop FCS-MPC controller. PI controllers are implemented for the outer loop controllers. The primary consideration for utilising PI controllers is their computational efficiency and speed, critical for maintaining real-time performance in highly dynamic systems. The outer loop's primary function is to ensure stability and reference tracking, where PI controllers excel due to their simplicity and robust performance across varying operating conditions. While FCS-MPC offers precise control capabilities, its computational demands are undesirable in the outer control layer. By employing a hybrid approach, the strengths of both control strategies are leveraged: PI controllers manage the overall system's stability and performance, while FCS-MPC is applied in the inner loop for fast and precise control of individual SMs.

Fig. 10 illustrates the control system for driving and regenerative braking modes. The driver-defined reference linear velocity profile v^* is converted to the rotational reference speed $\omega_m{}^*$ by multiplying by the gear ratio G and dividing by the wheel radius r. To track $\omega_m{}^*$, a PI controller $G_{PI}(s)$ is employed. This controller generates the reference electromagnetic torque $T_e{}^*$ necessary to compensate for mechanical load torque. $T_e{}^*$ in a DC motor is directly proportional to the armature current $i_a{}^*$ and the magnetic field ϕ_f as [42]:

$$T_e^* = k_f \phi_f i_a^* = k_{f_1} i_a^*. \tag{33}$$

The same current passes through all the series-connected SMs, therefore $i_a{}^* = i_{L_o}^*$. Since a PM brushed DC motor is utilised, the magnetic field ϕ_f remains constant. This results in the DC motors operating within a constant torque region.

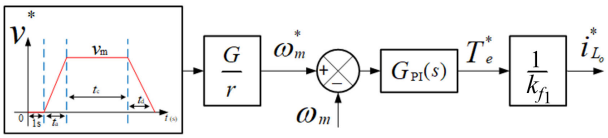


FIGURE 10. Outer-loop controller for Driving/braking mode.

The gains of the PI controllers (k_P and k_I) can be selected to ensure adequate phase margin (PM) and gain margin (GM), thereby stabilising the system. The small-signal transfer function of the Cuk-based SM can be represented as:

$$G_d(s) \cong {V_o}^2/V_{in} \frac{\left(1-\frac{s}{\omega_{Z_1}}\right)\left(1-\frac{s}{\omega_{Z_2}}\right)}{\left(1+\frac{s}{\omega_{P_1}}\right)\left(1+\frac{s}{\omega_{P_2}}\right)\left(1+\frac{s}{\omega_{P_3}}\right)}. \tag{34}$$

Here, ω_{Z_1} and ω_{Z_2} denote the frequencies of the two right-half-plane (RHP) zeros, which typically contribute phase lag to the system. On the other hand, ω_{P_1}, ω_{P_2}, and ω_{P_3} represent the frequencies of the three left-half-plane (LHP) poles, which influence the system's stability and frequency response.

The loop's bandwidth (BW) is determined by the frequency at which the Bode plots of the SM small-signal transfer function $G_d(s)$ and the inverse of the PI controller $1/G_{PI}(s)$ intersect, as depicted in Fig. 11. The gains of the PI controller $G_{PI}(s)$ are tuned such that its Bode plot intersects with $G_d(s)$ at the desired BW frequency, ensuring stable operation with sufficient margins for stability and performance.

Fig. 12 illustrates the outer loop controller during the charging mode. A PI controller is employed to produce the

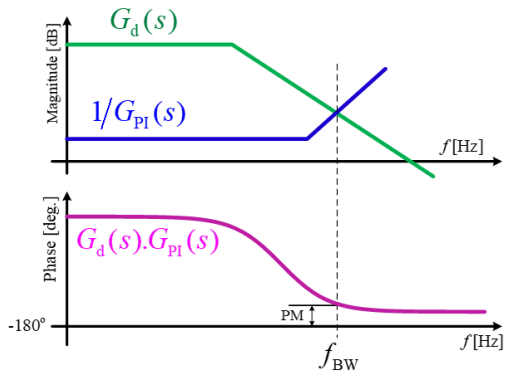


FIGURE 11. Bode diagram for loop shaping method using a PI controller $G_{PI}(s)$.

reference signal for the input current $i^*_{L_1}$ (the single-phase grid current) based on the desired charging power.

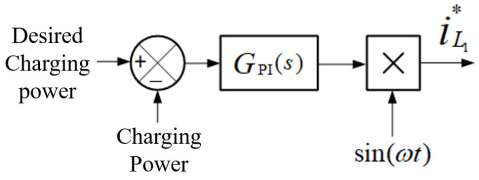


FIGURE 12. Outer-loop controller for charging mode.

IV. MIOBC CONTROL SYSTEM EXPERIMENTAL VERIFICATION

This section details the experimental setup and results obtained to evaluate the proposed MIOBC's performance and control system.

Information regarding the parameters for the Cuk-based SMs and the DC motors are presented in Table 3. The passive components of the Cuk-based SMs are carefully selected to maintain voltage and current ripples within 10% of peak voltage and current at the operating switching frequency.

A. VERIFICATION PLAN

The primary objective of this verification plan is to evaluate the performance and reliability of the proposed MIOBC and its control system across various operational scenarios. The plan outlines the testing procedures and expected outcomes as follows:

- **Operational scenarios:**
  - **Driving mode:** Assess torque and speed tracking, as well as the system's ability to recover from sudden changes in the reference speed profile.
  - **Regenerative braking mode:** Test energy recovery performance during braking events.
  - **Fault scenarios:** Simulate partial and complete faults to verify FRT capability.
  - **Mode switching:** Validate seamless transitions between driving, braking, and charging modes.

TABLE 3. System parameter values.

Systems	Parameters	Values
Cuk-based SMs	Switching frequency	$f_s = 20\ kHz$
	Inductors	$L_1 = L_o = 1\ mH$
	Capacitors	$C_1 = C_2 = 20\ \mu F$
	Turns' ratio	$N = 2$
	Output capacitor	$C_o = 1\ \mu F$
Motor system	Motor type	PM brushed DC
	Peak power	20 kW
	Maximum current	200 A (2min.)
	Maximum speed	6000 rpm
	Maximum torque	140 N.m
	Efficiency	98%
	Armature resistance	$R_a = 0.5\ \Omega$
	Armature inductance	$L_a = 10\ mH$
	Field resistance	$R_f = 0.5\ \Omega$
	Field inductance	$L_f = 10\ mH$
	Field voltage	$V_f = 300\ V$
	Wheel radius	$30\ cm$
	Gearbox ratio	2.5

  - **Outer-loop control gains:** Analyse the impact of outer-loop gains on system stability and fault recovery.
  - **Second-order harmonic suppression:** Verify harmonic suppression effectiveness using MPC under grid-connected operation in the charging mode.

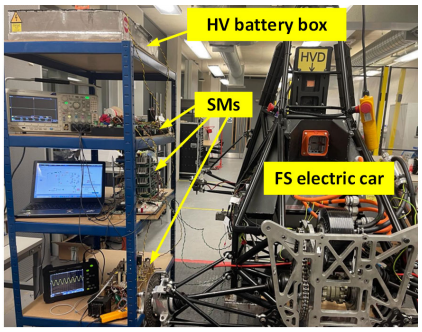
B. EXPERIMENTAL SETUP

The overall layout of the experimental setup is depicted in Fig. 13a. As shown in Fig. 13b, two DC motors are mounted on the rear wheels using two sets of fixed gears, forming a dual-motor configuration. The MIOBC, the control and measurement circuits, and the HV box are mounted outside the vehicle. These components are connected to the DC motors via lengthy HV cables to facilitate testing.

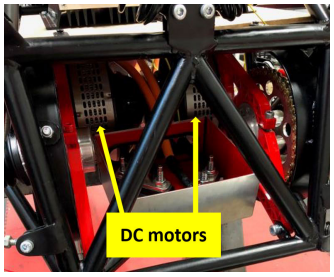
The experiments were conducted at Lancaster University using one of the Formula Student (FS) project electric racing cars under various operating conditions [43]. During testing, the vehicle's rear wheels were elevated off the ground, allowing data collection using an oscilloscope without requiring the vehicle to be in motion. Additionally, the vehicle's mechanical brakes were employed to simulate load torque, replicating the effects of friction and air drag forces.

Fig. 13c illustrates one of the isolated Cuk SM converters used in the MIOBC topology. The Cuk SM incorporates two capacitors connected in series with the primary and secondary sides of the HF transformer, effectively blocking DC currents. The HF transformer used in the experimental setup is compact, thanks to the modularised structure of the proposed MIOBC.

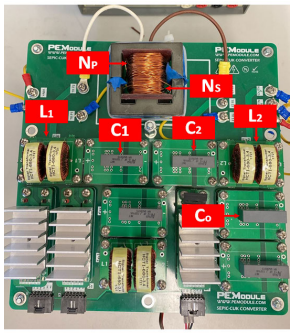
The physical layout of the battery box is displayed in Fig. 14a. Each battery pack (3.6 V, 20.4 Ah) consists of 8 parallel-connected Li-ion cells (Li8P25RT), and 22 such packs are connected in series to form each battery segment,



(a) Overal layout



(b) Dual-motor configuration



(c) Isolated Cuk-based SM

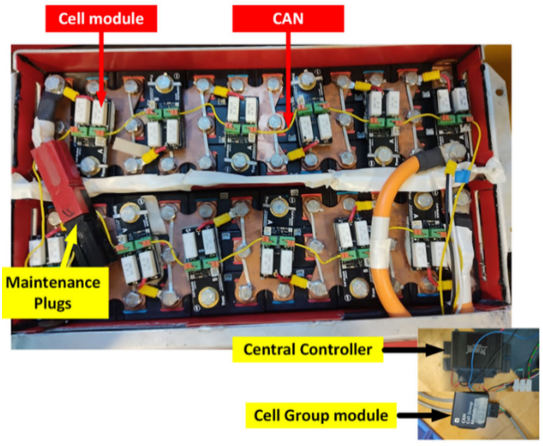
FIGURE 13. Experimental set-up.

resulting in 4 battery segments. For safety, 160 A EET protection fuses are employed throughout the experiments.

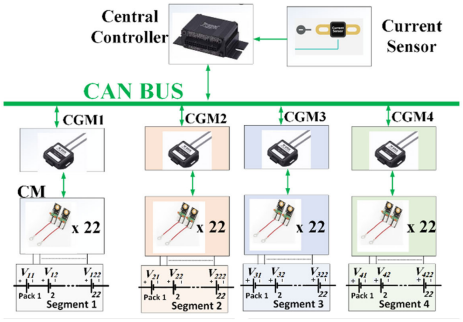
The experimental setup incorporates a comprehensive BMS and advanced measurement and control units. Fig. 14b illustrates the BMS architecture, which includes a central controller (EMUS G1), 4 Cell Group Modules (CGMs), 4 × 22 individual Cell Modules (CMs), and a current sensor. The CGMs gather data from the CMs connected to the battery segments, monitoring voltage, temperature, and current. This data is transmitted to the central controller via a core Controller Area Network (CAN) bus. The central controller continuously monitors all parameters, ensuring they remain within safe operating limits. Any anomalies trigger alerts to the driver or can initiate system shutdown via the LV control circuits. These circuits also manage car ON/OFF operations, pedal signal processing, dashboard displays, and safety routines.

To enable precise voltage measurements, LEM25-P sensors are employed, providing a measurement range of 10-500 V and high-frequency bandwidth suitable for both AC and DC signals. These sensors meet the fast-response requirements of the inner MPC loop. Current sensing is achieved using LEM LA55-P sensors, which offer galvanic isolation and a BW of up to 200 kHz, enabling accurate capture of rapid current changes critical for effective feedback control.

The control system is powered by the TMS320F28335 DSP, a 150 MHz floating-point processor capable of generating high-frequency PWM signals for the inner loop. The DSP interfaces directly with gate drive circuits, suppressing the need for additional interfacing electronics. This configuration supports real-time monitoring and control, with data visualised through Code Composer Studio. Additionally, the DSP's compatibility with the CAN communication protocol ensures seamless integration with the BMS, enabling efficient and coordinated EV system operation while maintaining high safety standards.



(a) Physical layout



(b) BMS schematic

FIGURE 14. HV Battery box.

In the experimental setup, the control system of the proposed MIOBC is designed with two distinct loops: (i) an inner loop utilising MPC, as detailed in Algorithm 1, and (ii) an outer loop employing PI controllers, as depicted in Fig. 10 and Fig. 12. The inner loop operates at a high frequency of approximately 10 kHz with a sampling time of 10 microseconds, tailored to the fast dynamics required for precise, real-time current control. This high-speed inner loop rapidly adjusts control actions. It generates gate signals for the switches in each SM, ensuring adaptive current regulation and addressing non-linearities inherent in the Cuk converter topology. In contrast, the outer loop operates at a lower frequency of around 1 kHz, which is suitable for managing system-level tasks such as speed and charging power control. It provides reference currents ($i^*_{L_1}$ and $i^*_{L_o}$) to the inner loop. The control frequencies and sampling rate are chosen to prevent aliasing, ensuring the high-speed updates of

the inner loop effectively translate into system performance. In contrast, the outer loop supports consistent and stable operation across all modes.

The dual-loop control strategy enables the outer loop to maintain system stability and regulate overall power flow, while the inner loop ensures localised precision and rapid responsiveness to dynamic changes. The design minimises latency by focusing on high-frequency updates in the inner loop, which could otherwise degrade EV performance by slowing system responses during fast transitions and compromising current and voltage regulation. This dual-loop approach reduces stress on components and enhances the lifespan of batteries and power electronics. The two loops facilitate smooth transitions between driving, charging, and regenerative braking modes.

C. EXPERIMENTAL RESULTS

To evaluate the effectiveness of the control systems, including the inner loop MPC and the outer loop controller, experiments were conducted under normal and faulty conditions across different operational modes: driving (acceleration), constant speed, regenerative braking (deceleration), and charging.

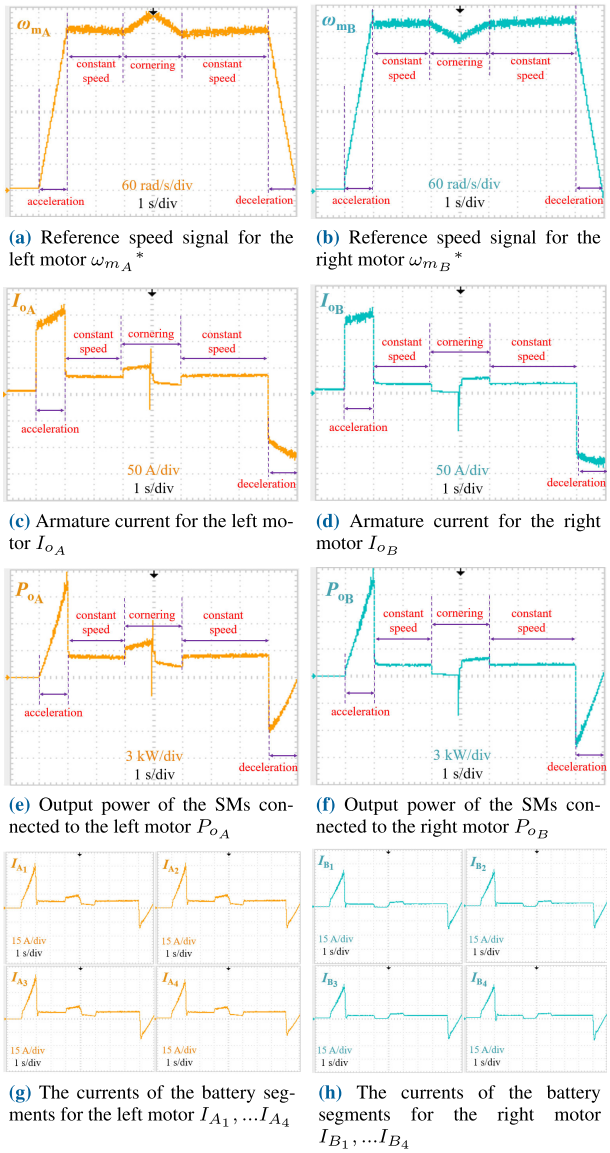
1) NORMAL CONDITION

The reference speed signals for the left motor $\omega_{m_A}{}^*$ and the right motor $\omega_{m_B}{}^*$ are illustrated in Fig. 15a and Fig. 15b, respectively. In practice, the wheels of a car turn at different speeds to ensure smooth and efficient handling while navigating turns or curves. To mimic this behaviour and demonstrate the control system's effectiveness in tracking changes in reference speed signals, the left and right rear motors' speeds were intentionally increased and decreased at $t = 4$ s, respectively. These speeds were communicated to the DSP via the accelerator pedal.

Fig. 15c and Fig. 15d show the armature currents I_{o_A} and I_{o_B}. Initially, these currents rise from zero to a peak of approximately 160 A following changes in the reference speed signals. During constant-speed operation, the currents decrease and stabilise as the EV maintains its momentum. Between $t = 4$ s and $t = 6$ s, the armature current I_{o_A} for the left motor increases, while I_{o_B} for the right motor decreases in response to variations in speed signals. During deceleration (regenerative braking), the armature currents reverse direction, becoming negative, which indicates energy transfer from the motors back to the HV battery.

Fig. 15e and Fig. 15f present the total output power of the SMs connected to the left and right motors, respectively. As shown, the output powers P_{o_A} and P_{o_B} are zero during the first second because the rotor speeds $\omega_{m_A}{}^*$ and $\omega_{m_B}{}^*$ are zero, and the EV is stationary. During acceleration, both output powers increase accordingly. During constant-speed periods, P_{o_A} and P_{o_B} stabilise at values lower than their peaks as the EV maintains its momentum. Similar to the armature currents, the output powers respond to changes in the reference speed signals between $t = 4$ s and $t = 6$ s. During deceleration or regenerative braking, the output powers become negative, indicating that the motors function as generators, recharging the HV battery.

Fig. 15g and Fig. 15h display the currents through the battery segments ($I_{A_1}, \ldots, I_{A_4}$ and $I_{B_1}, \ldots, I_{B_4}$). These currents increase from zero to their maximum values during the acceleration phase, corresponding to the rise in the motor's back electromotive force (emf) with speed. Once the DC motors reach their desired speeds, the currents in the battery segments decrease to their rated values. During regenerative braking, the currents in the battery segments become negative, indicating that the batteries are being recharged in this mode.



(a) Reference speed signal for the left motor $\omega_{m_A}{}^*$

(b) Reference speed signal for the right motor $\omega_{m_B}{}^*$

(c) Armature current for the left motor I_{o_A}

(d) Armature current for the right motor I_{o_B}

(e) Output power of the SMs connected to the left motor P_{o_A}

(f) Output power of the SMs connected to the right motor P_{o_B}

(g) The currents of the battery segments for the left motor $I_{A_1}, \ldots I_{A_4}$

(h) The currents of the battery segments for the right motor $I_{B_1}, \ldots I_{B_4}$

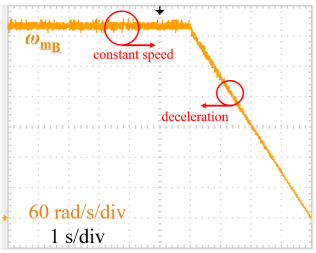
FIGURE 15. Experimental results: MIOBC performance under normal conditions (acceleration, constant speed, and deceleration modes).

2) MODE SWITCHING

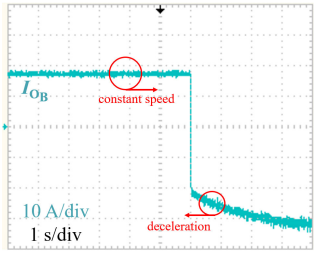
The high-speed inner loop control, utilising MPC, ensures immediate adjustments to sudden fluctuations, while the

outer loop provides stable reference currents to support seamless mode transitions. The experimental results presented in Fig. 16 demonstrate the dynamic capabilities of the proposed MIOBC control scheme, particularly during regenerative braking.

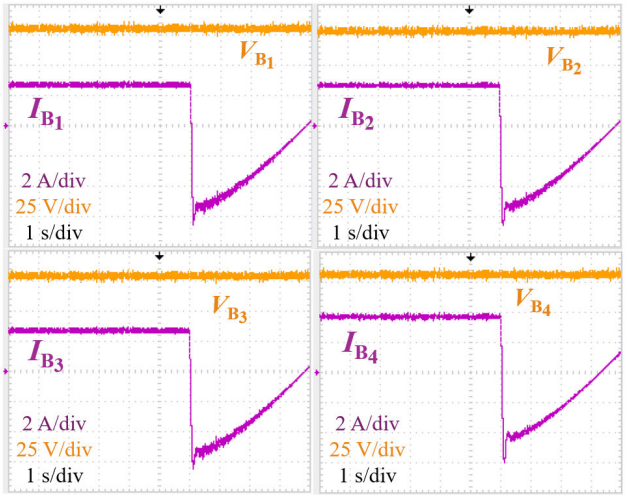
In this mode, the control system enables rapid response to reverse power flow, capturing energy from the propulsion system and redirecting it to the battery. As shown in Fig. 16a, the motor speed reduces effectively during regenerative braking, where the converter applies negative torque to decelerate the motor and facilitate energy recovery. This is further confirmed by the armature current in Fig. 16b, where a reversal in the current direction indicates the regenerative charging process. Fig. 16c highlights the performance of individual SMs in response to battery segment voltages, showcasing the bidirectional flow of current and validating the MIOBC's ability to ensure seamless power transfer across various operating conditions.



(a) Motor's speed during regenerative braking for the right motor $\omega_{m_B}{}^*$



(b) Armature current for the right motor I_{o_B}



(c) The currents of the battery segments for the right motor $I_{B_1}, \ldots I_{B_4}$

FIGURE 16. Experimental results: MIOBC performance during mode switching (from constant speed to regenerative braking (deceleration)).

3) FAULTY CONDITION

A fault scenario was introduced to evaluate the robustness of the control system. Specifically, the fault condition involved disconnecting the first and third battery segments connected to the SMs associated with the left and right motors, respectively. This fault was simulated at approximately $t = 7$ s for the left motor and $t = 4$ s for the right motor.

In this scenario, the disconnection of these battery segments caused the current from these segments to drop nearly to zero. The controller increased the currents from the remaining battery segments to compensate for this loss and maintain consistent output power.

The reference signals for the speeds of the left and right rear wheels ($\omega_{m_A}{}^*$ and $\omega_{m_B}{}^*$) are depicted in Fig. 17a and Fig. 17b, respectively. It is assumed that both wheels operate at identical speeds.

The impact of this fault on system performance is illustrated through the measured armature currents I_{o_A} and I_{o_B}, as shown in Fig. 17c and Fig. 17d, respectively. These currents exhibit disturbances and slight increases around $t = 7$ s and $t = 4$ s, corresponding to the fault events. However, the control system effectively compensates for these faults, with the currents returning to their nominal values within one second.

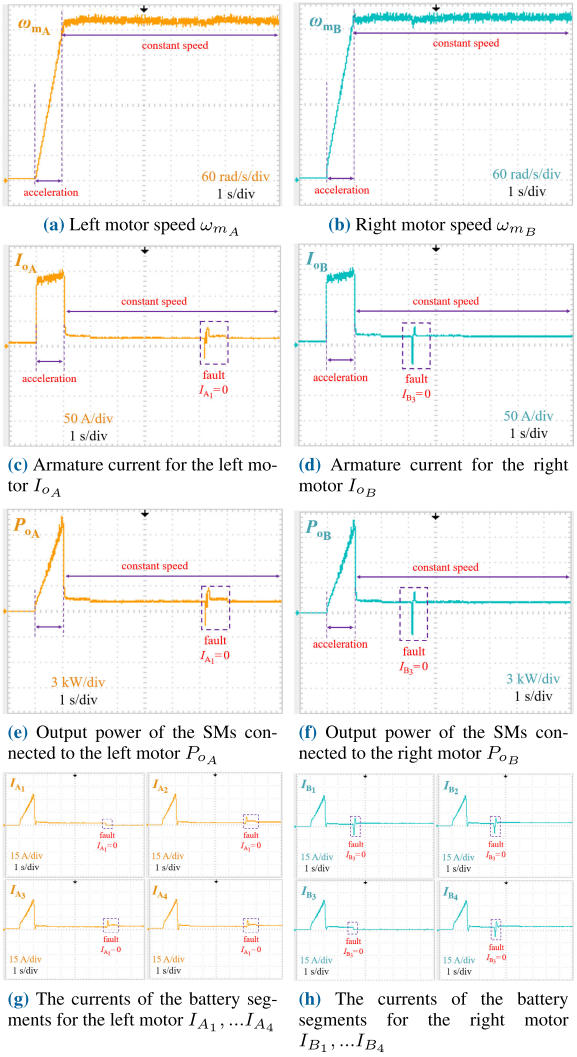
A similar response is observed in the output powers P_{o_A} and P_{o_B}, as depicted in Fig. 17e and Fig. 17f. The powers show transient disturbances but quickly stabilise, demonstrating the system's fault tolerance and ability to maintain performance under adverse conditions.

4) THE EFFECT OF THE OUTER LOOP (SYSTEM-LEVEL) GAINS DURING PARTIAL FAULT

To evaluate the performance of the PI controllers during a partial fault in the driving mode, experiments were conducted with the first battery segment disconnected at approximately $t = 2.4$ s for the left motor and the third battery segment disconnected at approximately $t = 8.4$ s for the right motor. The armature and battery currents were examined for both motors, with the left motor controlled by $G_{PI_1}(s)$, which uses $k_P = 2$ and $k_I = 5$, targeting a PM of 32Â° and a BW of approximately 1 kHz. The right motor was controlled by $G_{PI_2}(s)$, with $k_P = 0.1$ and $k_I = 8$, designed for a PM of 58Â° and a BW of 250 Hz.

The experimental results indicate that the left motor managed by the $G_{PI_1}(s)$ controller, with its higher BW but lower PM, exhibits a faster response to the disconnection event with relatively low overshoot, as shown in Fig. 18a and Fig. 18c. The higher BW enables quicker current adjustments, facilitating rapid recovery from the fault condition. In contrast, the $G_{PI_2}(s)$ controller, designed with a higher PM and lower BW, provides a more stable but slower response, as illustrated in Fig. 18b and Fig. 18d. While this stability ensures that the current through the right motor's armature I_{oB} and battery segments eventually return to their desired levels, the lower BW results in a delayed current recovery following the fault.

This analysis highlights the trade-offs between responsiveness and stability inherent in loop-shaping controller design. A higher BW is associated with faster response times and quicker recovery from dynamic changes, while a higher PM promotes system stability at the expense of slower response.



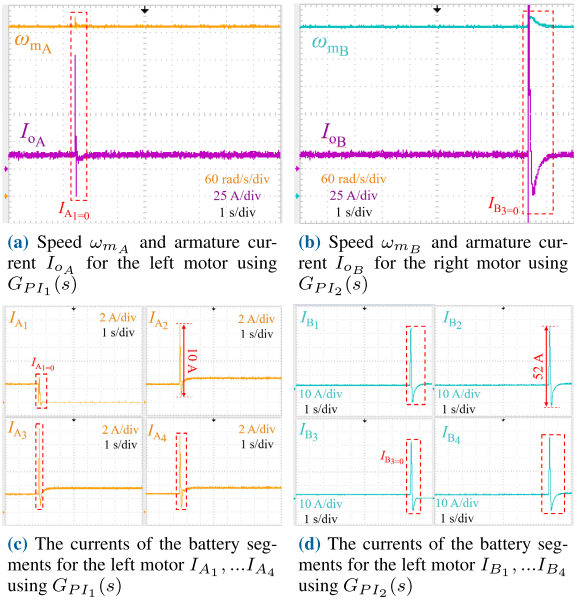
(a) Left motor speed ω_{m_A} (b) Right motor speed ω_{m_B}

(c) Armature current for the left motor I_{o_A} (d) Armature current for the right motor I_{o_B}

(e) Output power of the SMs connected to the left motor P_{o_A} (f) Output power of the SMs connected to the right motor P_{o_B}

(g) The currents of the battery segments for the left motor $I_{A_1}, ...I_{A_4}$ (h) The currents of the battery segments for the right motor $I_{B_1}, ...I_{B_4}$

FIGURE 17. Experimental results: MIOBC performance under faulty condition (acceleration and constant speed modes).



(a) Speed ω_{m_A} and armature current I_{o_A} for the left motor using $G_{PI_1}(s)$ (b) Speed ω_{m_B} and armature current I_{o_B} for the right motor using $G_{PI_2}(s)$

(c) The currents of the battery segments for the left motor $I_{A_1}, ...I_{A_4}$ using $G_{PI_1}(s)$ (d) The currents of the battery segments for the left motor $I_{B_1}, ...I_{B_4}$ using $G_{PI_2}(s)$

FIGURE 18. Experimental results: the effect of the outer loop (system-level) controller's gains under partial fault (driving mode.

These results underscore the importance of selecting and tuning controller parameters (k_P and k_I) based on specific performance criteria and operational constraints, balancing dynamic performance and stability to meet the desired system objectives.

5) SECOND-ORDER HARMONIC SUPPRESSION

Fig. 19a shows the input voltage waveform supplied to the first SM, v_{oA1}, and the grid current, i_{L_g}, over five cycles at a fundamental frequency of 50 Hz. The input voltage maintains a smooth sinusoidal profile, while the grid current exhibits minimal distortion. Fig. 19b presents the equivalent voltage across the coupling capacitors (C_1 and C_2), which contains second-order harmonic components at 100 Hz. These capacitors are critical in filtering out these harmonics and maintaining steady voltage levels.

Fig. 19c illustrates the output current directed to the battery -I_{A_1} which exhibits a stable and consistent waveform, confirming the effective reduction of second-order harmonics at 100 Hz and ensuring efficient power delivery. Fig. 19d highlights the grid charging power P_g, demonstrating the presence of second-order harmonic components at 100 Hz. Additionally, the charging power for the first SM's battery segments P_{A_1} is shown in this figure, featuring a stable waveform with minimised harmonic content. Fig. 19e displays the stored power in the coupling capacitors (C_1 and C_2), again indicating the presence of second-order harmonics at 100 Hz.

These results demonstrate that the second-order harmonic components are effectively trapped within the SM's coupling capacitors, resulting in a high-quality output current to the battery with minimal harmonic distortion.

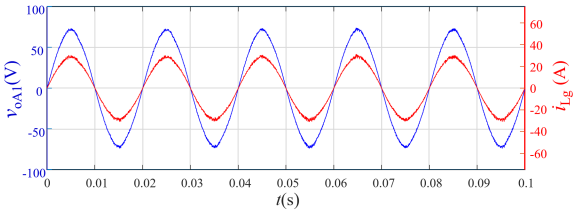
V. DISCUSSION

The experimental results validate the effectiveness and robustness of the proposed MIOBC and control system under various operational and fault conditions. This section discusses the implications of these results in the context of EV operation and compares the proposed solution with existing power conversion systems.

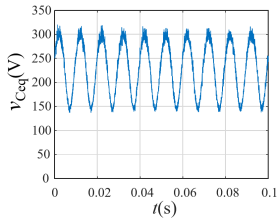
A. ANALYSIS OF EXPERIMENTAL RESULTS

The performance of the MIOBC system was thoroughly evaluated under normal and fault conditions. During normal operation, the system effectively managed power distribution across driving, constant speed, and regenerative braking modes. Stable armature currents and consistent output power verified the control system's ability to track changes in reference speed signals.

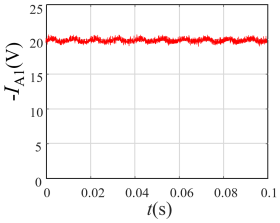
The robustness of the MIOBC system was further demonstrated by simulating fault scenarios, such as disconnecting battery segments. The system successfully compensated for the loss of battery segments by increasing the current supplied



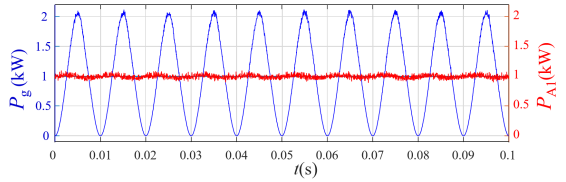
(a) The first SM voltage v_{oA1} and grid current i_{L_g} over five cycles (f_o=50 Hz)



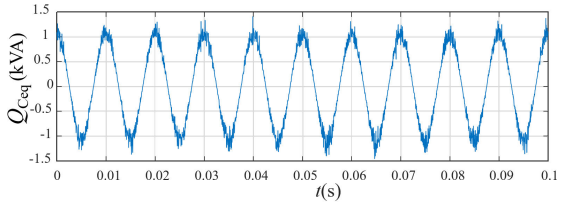
(b) The voltage across the coupling capacitors (C_1 and C_2)



(c) Current to the battery in the first SM



(d) Grid power P_g containing the second-order harmonic component at 100 Hz and first SM charging power P_{A_1}



(e) The stored reactive power in the coupling capacitors (C_1 and C_2) containing the second-order harmonic at 100 Hz

FIGURE 19. Experimental results: the suppression of the second-order harmonic components in the charging mode.

by the remaining segments. This validated the efficacy of the inner-loop MPC, which adapted rapidly to changes, maintaining system stability and minimising disturbances under dynamic fault conditions.

The high-speed inner-loop control, utilising MPC, facilitated immediate adjustments to sudden fluctuations, while the outer-loop control maintained stable reference currents, ensuring seamless mode transitions. For example, during regenerative braking, the control system enabled rapid reverse power flow, efficiently redirecting energy from the propulsion system back to the battery.

The experimental results revealed that the controller with higher BW and lower PM delivered a faster response but exhibited lower stability. Conversely, the controller with a lower BW and higher PM provided greater stability but slower response times. These findings highlight the inherent trade-offs between responsiveness and stability, emphasising the need to carefully tune controller gains to balance dynamic performance and system stability.

Additionally, the experimental results validated the effectiveness of the harmonic suppression strategy. The input voltage maintained a smooth sinusoidal waveform, while the grid current displayed minimal distortion, confirming the system's ability to preserve power quality. The equivalent voltage across the coupling capacitors, which contained second-order harmonic components at 100 Hz, demonstrated their critical role in filtering these harmonics.

B. COMPARISON WITH EXISTING SOLUTIONS

The proposed MIOBC addresses several challenges commonly faced by existing power conversion systems:

- **Cuk-based SMs:** The single-stage isolated bidirectional design enhances efficiency and safety, providing galvanic isolation, inherent PFC, and flexible voltage adaptation while minimising energy losses.
- **Integration:** Integrating the OBC with the traction inverter reduces the system's physical size and weight, improving power density and simplifying the EV design.
- **Modularity:** The modular approach improves scalability, controllability, and FRT capability, making the system robust against component failures.
- **Advanced control:** The dual-loop control strategy, incorporating MPC in the inner loop, ensures rapid response, effective disturbance rejection, and harmonic suppression, outperforming traditional control methods in single-phase charging and other scenarios.

Despite its effectiveness, the proposed MIOBC's practical implementation will need to overcome challenges associated with complexity, cost, and space constraints, as well as fully validate its robustness within a vehicle installation and under real-world conditions.

Future research will address these challenges to optimise further the MIOBC design for improved scalability, cost-effectiveness, and seamless integration into various EV applications.

VI. CONCLUSION

This paper presented the design and experimental validation of an MIOBC for dual-motor EV applications. The proposed MIOBC addresses critical challenges in EV power management, including rapid dynamic changes, efficient harmonic suppression, and FRT capability. The modular design enhances flexibility, scalability, and reliability by enabling the system to operate effectively even during battery segment or semiconductor failures. A dual-loop control strategy was implemented to manage the complex dynamics of the Cuk-based MIOBC. The high-speed inner loop, utilising MPC, operates at 10 kHz to provide precise real-time control of currents and voltages, ensuring rapid responsiveness to dynamic changes. The outer loop, employing classical PI controllers, operates at 1 kHz to manage system-level tasks, including speed control, charging power regulation, and the seamless transitions between driving, regenerative braking, and charging. Experimental results validated the MIOBC's effectiveness under normal and fault conditions. In normal operation, the system effectively tracked reference speed profiles, demonstrated stable power distribution, and

maintained high efficiency across all operational modes. During a simulated partial fault scenario, where battery segments were disconnected, the decentralised control system successfully compensated by increasing currents from intact segments, maintaining stable output power with minimal disturbances. In single-phase charging mode, the inner loop's MPC eliminated second-order harmonics at 100 Hz, as confirmed by harmonic-free output currents and sinusoidal grid voltage and current waveforms. The MIOBC also showcased advanced capabilities during mode switching. The high-speed inner loop enabled immediate adjustments to dynamic changes, such as reverse power flow during braking, redirecting energy efficiently to the battery. The dual-loop design minimised latency ensured smooth operation, and mitigated the impact of rapid transitions, resulting in consistent system performance across all modes.

APPENDIX
POWER LOSS ANALYSIS AND EFFICIENCY EVALUATION

To accurately evaluate the efficiency of the proposed MIOBC, which consists of m number of SMs per motor (with two sets for dual-motor configuration), a detailed mathematical analysis of power losses is performed. Each SM is a bidirectional, isolated Cuk converter with five semiconductor switches and a high-frequency transformer. The total power loss P_{total} can be approximated by:

$$P_{\text{loss}_{\text{total}}} \approx P_{\text{Conduction}} + P_{\text{Switching}} + P_{\text{Copper}} + P_{\text{Core}}. \tag{A.1}$$

A. CONDUCTION LOSSES

The conduction losses in the semiconductor switches and diodes for all SMs are calculated as:

$$P_{\text{Conduction}} = \sum_{z=1}^{5} mR_{\text{ON}} I^2_{S_{z(\text{rms})}} + \sum_{w=1}^{4} m\bar{I}_{D_w} V_{DF}, \tag{A.2}$$

where:

- m is the number of SMs in each motor's set,
- R_{ON} is the on-resistance of the switches,
- $I_{S_{z(\text{rms})}}$ is the RMS current through the z^{th} switch,
- $\bar{I}_{D_w}$ is the average current through the w^{th} diode,
- V_{DF} is the forward voltage drop of the diodes.

B. SWITCHING LOSSES

Switching losses for the semiconductor switches across all SMs are given by:

$$P_{\text{Switching}} = \sum_{z=1}^{5} m \frac{V_{in}\bar{I}_{S_z}}{2}(t_{\text{on}} + t_{\text{off}}), \tag{A.3}$$

where:

- V_{in} is the input voltage of the Cuk converter,
- $\bar{I}_{S_z}$ is the average current through the z^{th} switch,
- t_{on} and t_{off} are the turn-on and turn-off times of the switches.

C. COPPER LOSSES IN INDUCTORS

Copper losses due to the parasitic resistance in the inductors of each SM are calculated by:

$$P_{\text{Copper}} = \sum_{j=1}^{2} mr_j I^2_{L_{j(\text{rms})}}, \tag{A.4}$$

where:

- r_j is the parasitic resistance of the j^{th} inductor,
- $I_{L_{j(\text{rms})}}$ is the RMS current through the j^{th} inductor.

D. CORE LOSSES

Core losses in the high-frequency transformers and magnetic components of each SM are expressed as:

$$P_{\text{Core}} = k_F B^2_{\text{peak}} f_s^2 V_{\text{core}}, \tag{A.5}$$

where:

- k_F is a loss coefficient dependent on the core material,
- B_{peak} is the peak flux density in the core,
- f_s is the switching frequency of the converter,
- V_{core} is the volume of the magnetic core.

E. CURRENT WAVEFORM ANALYSIS

To accurately estimate the root-mean-square (RMS) and average values of currents flowing through each semiconductor device, detailed current waveform analysis is essential. This subsection presents the current envelopes for each switching state, as obtained from MATLAB simulations. The parameters used in the simulations are listed in Table 3, ensuring consistency with the system's specifications. The analysis presented here focuses on the positive half cycle of the operation in accordance with the switching principles discussed in Section III-A. Fig. 20 illustrates the current waveforms for the primary side switch S_P, the secondary side switches S_1 and S_4, and diodes D_1, D_2, and D_3.

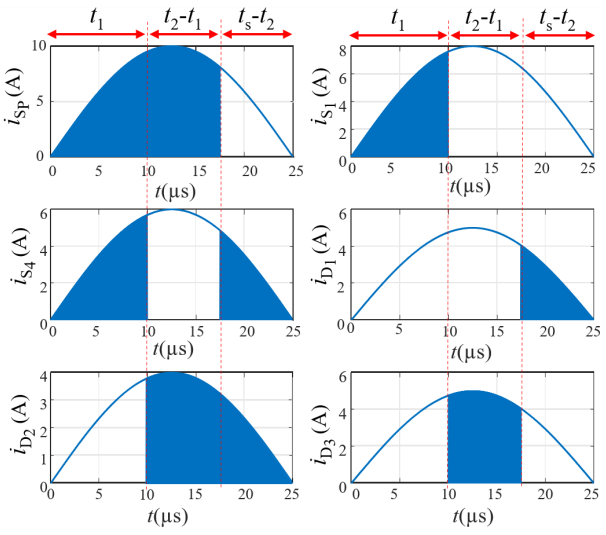


FIGURE 20. Simulated current waveforms for primary and secondary side switches and diodes in the positive half-cycle.

1) PRIMARY SIDE CURRENT ANALYSIS (S_P)

The current i_{L_1} on the primary side varies throughout the switching states as follows:

- **STATE 1** ($0 \leq t < t_1$): Switch S_P is conducting, charging the input inductor L_1. The current envelope during this state is approximated by:

$$i_{env_{L_1}}(t) = I_{L_1,\text{peak}} \sin\left(\frac{\pi t}{t_1}\right). \tag{A.6}$$

- **STATE 2** ($t_1 \leq t < t_2$): S_P remains ON, continuing to charge L_1. The envelope is:

$$i_{env_{L_1}}(t) = I_{L_1,\text{peak}} \sin\left(\frac{\pi(t-t_1)}{t_2-t_1}\right). \tag{A.7}$$

- **STATE 3** ($t_2 \leq t < t_s$): S_P is OFF, and L_1 discharges into the capacitors C_1 and C_2. The current decreases as:

$$i_{env_{L_1}}(t) = I_{L_1,\text{peak}} \sin\left(\frac{\pi(t-t_2)}{t_s-t_2}\right). \tag{A.8}$$

The RMS value for the primary current i_{L_1} over a complete switching cycle t_s is calculated by:

$$I_{L_1(\text{rms})} = \sqrt{\frac{1}{t_s}\sum_{q=1}^{3}\int_{t_{q-1}}^{t_q} I_{L_1,\text{peak}}^2 \sin^2\left(\frac{\pi(t-t_{q-1})}{t_q-t_{q-1}}\right) \mathrm{d}t}, \tag{A.9}$$

where $t_0 = 0$, t_1, t_2, and $t_3 = t_s$ correspond to the time boundaries of each state.

The average current for i_{L_1} is:

$$\bar{I}_{L_1} = \frac{1}{t_s}\sum_{q=1}^{3}\int_{t_{q-1}}^{t_q} I_{L_1,\text{peak}} \sin\left(\frac{\pi(t-t_{q-1})}{t_q-t_{q-1}}\right) \mathrm{d}t. \tag{A.10}$$

2) SECONDARY SIDE CURRENT ANALYSIS (S_1, S_4)

The output current i_{L_o} on the secondary side flows as follows:

- **STATE 1** ($0 \leq t < t_1$): S_1 and S_4 conduct, transferring energy to the output inductor. The envelope is:

$$i_{env_{L_o}}(t) = I_{L_o,\text{peak}} \sin\left(\frac{\pi t}{t_1}\right). \tag{A.11}$$

- **STATE 3** ($t_2 \leq t < t_s$): S_4 conducts, and the output inductor discharges. The envelope is:

$$i_{env_{L_o}}(t) = I_{L_o,\text{peak}} \sin\left(\frac{\pi(t-t_2)}{t_s-t_2}\right). \tag{A.12}$$

The RMS value for i_{L_o} is:

$$I_{L_o(\text{rms})} = \sqrt{\frac{1}{t_s}\sum_{q=1,3}\int_{t_{q-1}}^{t_q} I_{L_o,\text{peak}}^2 \sin^2\left(\frac{\pi(t-t_{q-1})}{t_q-t_{q-1}}\right) \mathrm{d}t}, \tag{A.13}$$

where $t_0 = 0$, t_1, t_2, and $t_3 = t_s$ represent the boundaries of the switching states where i_{L_o} is relevant.

The average current for i_{L_o} is:

$$\bar{I}_{L_o} = \frac{1}{t_s}\sum_{q=1,3}\int_{t_{q-1}}^{t_q} I_{L_o,\text{peak}} \sin\left(\frac{\pi(t-t_{q-1})}{t_q-t_{q-1}}\right) \mathrm{d}t. \tag{A.14}$$

3) DIODE CURRENT ANALYSIS (D_2, D_3, D_1)

During the different switching states, the diode current behaviour varies as follows:

- **STATE 2** ($t_1 \leq t < t_2$): Diodes D_2 and D_3 conduct as the output inductor L_o discharges into the capacitors C_1 and C_2. The current envelope for diode D_2 is:

$$i_{env_{D_2}}(t) = I_{D_2,\text{peak}} \sin\left(\frac{\pi(t-t_1)}{t_2-t_1}\right). \tag{A.15}$$

The envelope for D_3 is similar:

$$i_{env_{D_3}}(t) = I_{D_3,\text{peak}} \sin\left(\frac{\pi(t-t_1)}{t_2-t_1}\right). \tag{A.16}$$

The RMS currents for D_2 and D_3 are:

$$I_{D_2(\text{rms})} = \sqrt{\frac{1}{t_s}\int_{t_1}^{t_2} I_{D_2,\text{peak}}^2 \sin^2\left(\frac{\pi(t-t_1)}{t_2-t_1}\right) \mathrm{d}t}. \tag{A.17}$$

$$I_{D_3(\text{rms})} = \sqrt{\frac{1}{t_s}\int_{t_1}^{t_2} I_{D_3,\text{peak}}^2 \sin^2\left(\frac{\pi(t-t_1)}{t_2-t_1}\right) \mathrm{d}t}. \tag{A.18}$$

- **STATE 3** ($t_2 \leq t < t_s$): Diodes D_1 and D_2 conduct as S_P is OFF, allowing the input inductor L_1 and the output inductor L_o to discharge. The current envelope for diode D_1 is:

$$i_{env_{D1}}(t) = I_{D1,\text{peak}} \sin\left(\frac{\pi(t-t_2)}{t_s-t_2}\right). \tag{A.19}$$

The envelope for D_2 in this state can be expressed as:

$$i_{env_{D_2}}(t) = I_{D_2,\text{peak}} \sin\left(\frac{\pi(t-t_2)}{t_s-t_2}\right). \tag{A.20}$$

The RMS currents for D_1 and D_2 are:

$$I_{D1(\text{rms})} = \sqrt{\frac{1}{t_s}\int_{t_2}^{t_s} I_{D1,\text{peak}}^2 \sin^2\left(\frac{\pi(t-t_2)}{t_s-t_2}\right) \mathrm{d}t}. \tag{A.21}$$

$$I_{D_2(\text{rms})} = \sqrt{\frac{1}{t_s}\int_{t_2}^{t_s} I_{D_2,\text{peak}}^2 \sin^2\left(\frac{\pi(t-t_2)}{t_s-t_2}\right) \mathrm{d}t}. \tag{A.22}$$

It must be mentioned that the same approach applies to the negative half cycle, with the following state changes:

- STATE 1: S_P, S_2, and S_3 are ON
- STATE 2: S_P, D_1, and D_4 are ON
- STATE 3: S_2, D_3, and D_4 are ON

F. EFFICIENCY ESTIMATION

The overall efficiency η of the MIOBC is defined as the ratio of the output power P_{out} to the input power P_{in}. It can be approximated by considering the total power loss $P_{\text{loss}_{\text{total}}}$ as follows:

$$\eta \approx \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}_{\text{total}}}}, \tag{A.23}$$

where $P_{\text{out}} \approx V_o I_o$ and $P_{\text{loss}_{\text{total}}}$ is extracted from (A.1).

The MATLAB simulation results depicted in Fig. 21 illustrate the efficiency η trends of the MIOBC under various conditions, specifically focusing on the number of segments and the continuous power range. The analysis is conducted using system parameters detailed in Table 3.

For the purpose of these simulations, core and copper losses have been neglected. The highlighted points in Fig. 21 illustrate specific conditions, such as low power with few segments (point P_1), optimal performance with moderate power and segment count (point P_2), and reduced efficiency at high power with excessive segments (point P_3).

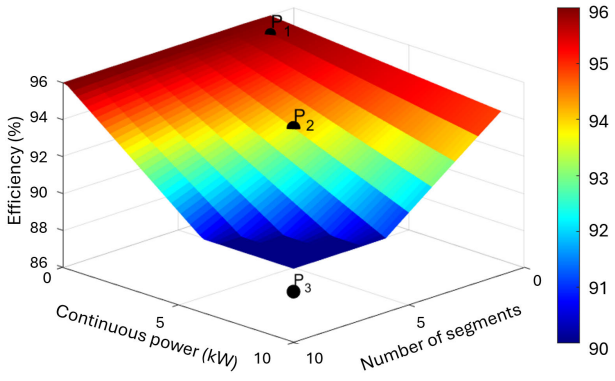


FIGURE 21. Simulation results of MIOBC efficiency for different numbers of segments and a range of continuous power.

The results reveal that as the number of segments increases, the efficiency initially improves due to better power distribution and reduced strain on individual devices. However, the efficiency begins to decline beyond a certain threshold (in this case, more than four segments), primarily due to the increased complexity and the associated switching and conduction losses. The efficiency decreases as the continuous output power increases, reflecting higher conduction and switching losses at elevated power levels.

ACKNOWLEDGMENT

The authors extend their appreciation to the Deanship of Scientific Research at Shaqra University for supporting this research work.

REFERENCES

[1] Int. Energy Agency. *Global EV Outlook 2024: Moving Towards Increased Affordability*. Accessed: Nov. 5, 2024. [Online]. Available: https://iea.blob.core.windows.net/assets/a9e3544b-0b12-4e15-b407-65f5c8ce1b5f/GlobalEVOutlook2024.pdf

[2] Y. Guan and Q. Hou, "Dynamic strategy of power battery closed-loop supply chain considering cascade utilization," *IEEE Access*, vol. 10, pp. 21486–21496, 2022.

[3] S. P. Sathiyan, C. B. Pratap, A. A. Stonier, G. Peter, A. Sherine, K. Praghash, and V. Ganji, "Comprehensive assessment of electric vehicle development, deployment, and policy initiatives to reduce GHG emissions: Opportunities and challenges," *IEEE Access*, vol. 10, pp. 53614–53639, 2022.

[4] T. Yuvaraj, K. R. Devabalaji, J. A. Kumar, S. B. Thanikanti, and N. I. Nwulu, "A comprehensive review and analysis of the allocation of electric vehicle charging stations in distribution networks," *IEEE Access*, vol. 12, pp. 5404–5461, 2024.

[5] S. M. Dawoud, F. Selim, X. Lin, and A. A. Zaky, "Techno-economic and sensitivity investigation of a novel perovskite solar cells based high efficient hybrid electric sources for off-shore oil ships," *IEEE Access*, vol. 11, pp. 41635–41643, 2023.

[6] S. Shafiq, U. B. Irshad, M. Al-Muhaini, S. Z. Djokic, and U. Akram, "Reliability evaluation of composite power systems: Evaluating the impact of full and plug-in hybrid electric vehicles," *IEEE Access*, vol. 8, pp. 114305–114314, 2020.

[7] S. S. G. Acharige, Md. E. Haque, M. T. Arif, N. Hosseinzadeh, K. N. Hasan, and A. M. T. Oo, "Review of electric vehicle charging technologies, standards, architectures, and converter configurations," *IEEE Access*, vol. 11, pp. 41218–41255, 2023.

[8] P. Pescetto, M. F. T. Cruz, F. Stella, and G. Pellegrino, "Galvanically isolated on-board charger fully integrated with 6-Phase traction motor drives," *IEEE Access*, vol. 11, pp. 26059–26069, 2023.

[9] J. Schmenger, S. Endres, S. Zeltner, and M. März, "A 22 kW on-board charger for automotive applications based on a modular design," in *Proc. IEEE Conf. Energy Convers. (CENCON)*, Johor Bahru, Malaysia, Oct. 2014, pp. 1–6.

[10] A. Khaligh and M. D'Antonio, "Global trends in high-power on-board chargers for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 68, no. 4, pp. 3306–3324, Apr. 2019.

[11] J. Becker, C. Schaeper, S. Rothgang, and D. U. Sauer, "Development and validation of an energy management system for an electric vehicle with a split battery storage system," *J. Electr. Eng. Technol.*, vol. 8, no. 4, pp. 920–929, Jul. 2013.

[12] A. Stippich, C. H. Van Der Broeck, A. Sewergin, A. H. Wienhausen, M. Neubert, P. Schülting, S. Taraborrelli, H. van Hoek, and R. W. De Doncker, "Key components of modular propulsion systems for next generation electric vehicles," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 4, pp. 249–258, Dec. 2017.

[13] S. Rothgang, T. Baumhöfer, H. van Hoek, T. Lange, R. W. De Doncker, and D. U. Sauer, "Modular battery design for reliable, flexible and multi-technology energy storage systems," *Appl. Energy*, vol. 137, pp. 931–937, Jan. 2015.

[14] F. Tahami, R. Kazemi, and S. Farhanghi, "A novel driver assist stability system for all-wheel-drive electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 52, no. 3, pp. 683–692, May 2003.

[15] A. Fraser, "In-wheel electric motors," in *Proc. 10th Int. CTI Symp.*, 2016, pp. 12–23.

[16] S. Zou, J. Zhang, Y. Liu, Y. Yang, Y. Zhou, J. Wang, J. Peng, and G. Wang, "Design and analysis of a novel multimode powertrain for a PHEV using two electric machines," *IEEE Access*, vol. 12, pp. 76442–76457, 2024.

[17] H. Budde-Meiwes, J. Drillkens, B. Lunz, J. Muennix, S. Rothgang, J. Kowal, and D. U. Sauer, "A review of current automotive battery technology and future prospects," *Proc. Inst. Mech. Eng., D, J. Automobile Eng.*, vol. 227, no. 5, pp. 761–776, May 2013.

[18] N. Hartmann and E. D. Özdemir, "Impact of different utilization scenarios of electric vehicles on the German grid in 2030," *J. Power Sources*, vol. 196, no. 4, pp. 2311–2318, Feb. 2011.

[19] F. Nasr Esfahani, A. Darwish, and X. Ma, "Design and control of a modular integrated on-board battery charger for EV applications with cell balancing," *Batteries*, vol. 10, no. 1, p. 17, Jan. 2024.

[20] J. Lu, K. Bai, A. R. Taylor, G. Liu, A. Brown, P. M. Johnson, and M. McAmmond, "A modular-designed three-phase high-efficiency high-power-density EV battery charger using dual/triple-phase-shift control," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8091–8100, Sep. 2018.

[21] S. E. Schulz, "Exploring the high-power inverter: Reviewing critical design elements for electric vehicle applications," *IEEE Electrific. Mag.*, vol. 5, no. 1, pp. 28–35, Mar. 2017.

[22] A. Darwish, D. Holliday, and S. Finney, "Operation and control design of an input-series–input-parallel–output-series conversion scheme for offshore DC wind systems," *IET Power Electron.*, vol. 10, no. 15, pp. 2092–2103, Dec. 2017.
[23] G. Yang, E. Draugedalen, T. Sorsdahl, H. Liu, and R. Lindseth, "Design of high-efficiency high power density 10.5 kW three-phase onboard charger for electric/hybrid vehicles," in *Proc. PCIM Eur., Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, Nuremberg, Germany, 2016, pp. 1–7.
[24] P. M. Johnson and K. H. Bai, "A dual-DSP controlled SiC MOSFET based 96%-efficiency 20kW EV on-board battery charger using LLC resonance technology," in *Proc. IEEE Symp. Ser. Comput. Intell. (SSCI)*, Honolulu, HI, USA, Nov. 2017, pp. 1–5.
[25] H. Sarnago and Ó. Lucía, "Design and experimental verification of a bidirectional EV on-board charger featuring multiphase operation in full power/voltage ranges," *IEEE Open J. Ind. Electron. Soc.*, vol. 5, pp. 458–467, 2024.
[26] S. S. Williamson, A. K. Rathore, and F. Musavi, "Industrial electronics for electric transportation: Current state-of-the-art and future challenges," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3021–3032, May 2015.
[27] H. Kim, H. Belkamel, J. Park, R. M. Hakim, and S. Choi, "Modular three-phase single-stage isolated AC-DC converter for electrolytic capacitor-less EV DC charging," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf. (IPEMC-ECCE Asia)*, Nanjing, China, Nov. 2020, pp. 1573–1578.
[28] H. Kim, J. Park, S. Kim, R. M. Hakim, H. Belkamel, and S. Choi, "A single-stage electrolytic capacitor-less EV charger with single- and three-phase compatibility," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6780–6791, Jun. 2022.
[29] M. Abbasi, K. Kanathipan, and J. Lam, "An interleaved bridgeless single-stage AC/DC converter with stacked switches configurations and soft-switching operation for high-voltage EV battery systems," *IEEE Trans. Ind. Appl.*, vol. 58, no. 5, pp. 5533–5545, Sep./Oct. 2022.
[30] F. Yu, Q. Yin, L. Luo, and Y. Zhang, "Enhanced dual-vector model predictive current integrated control for electric-drive- reconstructed onboard chargers," *IEEE Access*, vol. 12, pp. 86917–86927, 2024.
[31] C. Zhang, P. Gao, J. Wang, M. Dang, X. Yang, and Y. Feng, "Research on active rear-wheel steering control method with sliding mode control optimized by model predictive," *IEEE Access*, vol. 11, pp. 57228–57239, 2023.
[32] M. Rezaei Larijani, S. Hedayati Kia, M. Zolghadri, A. El Hajjaji, and A. Taghavipour, "Linear parameter-varying model predictive control for intelligent energy management in battery/supercapacitor electric vehicles," *IEEE Access*, vol. 12, pp. 51026–51040, 2024.
[33] A. Darwish, A. Massoud, D. Holliday, S. Ahmed, and B. Williams, "Generation, performance evaluation and control design of single-phase differential-mode buck–boost current-source inverters," *IET Renew. Power Gener.*, vol. 10, no. 7, pp. 916–927, Aug. 2016.
[34] X. Shen, J. Liu, Z. Liu, Y. Gao, J. I. Leon, S. Vazquez, L. Wu, and L. G. Franquelo, "Sliding-mode control of neutral-point-clamped power converters with gain adaptation," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9189–9201, Aug. 2024.
[35] Z. Liu, X. Lin, Y. Gao, R. Xu, J. Wang, Y. Wang, and J. Liu, "Fixed-time sliding mode control for DC/DC buck converters with mismatched uncertainties," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 1, pp. 472–480, Jan. 2023.
[36] Z. Liu, B. Li, F. C. Lee, and Q. Li, "High-efficiency high-density critical mode rectifier/inverter for WBG-device-based on-board charger," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9114–9123, Nov. 2017.
[37] M. Kumar, P. M. Barbosa, and J. M. Ruiz, "Light-load and cross-load control of integrated OBC and APM for electric vehicle applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Orlando, FL, USA, Mar. 2023, pp. 1915–1921.
[38] S.-G. Jeong, J.-M. Kwon, and B.-H. Kwon, "High-efficiency bridgeless single-power-conversion battery charger for light electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 215–222, Jan. 2019.
[39] D. Bhule and R. Sudharshan Kaarthik, "A model predictive control scheme for a single-phase integrated battery charger with active power decoupling for EV application," *IEEE Trans. Power Electron.*, vol. 39, no. 4, pp. 4117–4126, Apr. 2024.
[40] M. S. Abdel-Majeed, A. Shawier, A. Habib, A. S. Abdel-Khalik, M. S. Hamad, S. Ahmed, and N. A. Elmalhy, "A three-phase nonisolated pseudo-six-phase-based integrated onboard battery charger for electric vehicles," *IEEE Trans. Transport. Electrific.*, vol. 9, no. 1, pp. 1300–1310, Mar. 2023.
[41] O. Matiushkin, O. Husev, J. Rodriguez, H. Young, and I. Roasto, "Feasibility study of model predictive control for grid-connected twisted buck–boost inverter," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2488–2499, Mar. 2022.
[42] I. P. Wiltuschnig, A. F. F. Filho, B. H. B. Boff, and P. R. Eckert, "Design and analysis of a novel axial variable-flux reluctance machine with DC-excited field and modular double rotor," *IEEE Trans. Energy Convers.*, vol. 39, no. 3, pp. 1478–1487, Sep. 2024.
[43] *Formula Student Project by IMechE*. Accessed: Jan. 1, 2024. [Online]. Available: https://www.formulastudent.de/fileadmin/user_upload/all/2020/rules/FS-Rules_2020_V1.0.pdf

FATEMEH NASR ESFAHANI (Member, IEEE) received the B.Sc. degree in electrical engineering from the Amirkabir University of Technology, in 2015, the M.Sc. degree in electrical engineering from the University of Isfahan, in 2018, and the Ph.D. degree in electrical engineering from Lancaster University, Lancaster, U.K., in 2024. She is currently a Postdoctoral Researcher with the School of Engineering, Lancaster University. Her research interests include power electronics, electric vehicles, wireless power transfer, renewable energy, hardware-in-the-loop, machine learning, and cyber-physical power systems (CPPS).

AHMED DARWISH (Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the Faculty of Engineering, Alexandria University, Egypt, and the Ph.D. degree in electrical engineering from the Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, U.K., in 2016. He is currently an Assistant Professor (Lecturer) in electrical engineering with the School of Engineering, Lancaster University. He previously was a Research Assistant with Texas A&M University, Qatar, a Postdoctoral Research Associate with the PEDEC Group, University of Strathclyde, and a Faculty Member with the Faculty of Engineering and Digital Technologies, University of Bradford. His research interests include power electronic converters, electric machines, digital control, energy conversion, renewable energy, power quality, and electric vehicles.

SAUD ALOTAIBI received the B.Sc. degree in electrical engineering from the University of Taif, the M.Sc. degree in electrical engineering from the University of Nottingham, and the Ph.D. degree in electrical and electronic engineering from the University of Lancaster, in 2023. He is currently an Assistant Professor with the Department of Electrical Engineering, Shaqra University. His research interests include power electronics, dc-dc converters, multilevel converters, energy conversion, and power quality.

FELICIAN CAMPEAN (Member, IEEE) received the Ph.D. degree in reliability from Brunel University, U.K. He is currently a Professor of reliability engineering with the University of Bradford, U.K., where he is the Associate Dean of research and innovation with the Faculty of Engineering and Digital Technologies. His research interests revolve around model-based and data-centric approaches for the reliability and resilience of complex multidisciplinary systems within a whole systems lifecycle approach, with a strong track record of collaboration with the automotive industry. He is a fellow of the Royal Statistical Society.