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RESEARCH ARTICLE

Weight-Update Characteristics Dependent on Carrier Densities of Hf-ZnO Charge-Trap Layers in Sub-Threshold Synaptic Transistors

KUNHEE TAE, DANYOUNG CHA, GYOUNGYEOP DO, NAYEONG LEE, AND SUNGSIK LEE
Department of Electronics Engineering, Pusan National University, Busan 46241, South Korea

Corresponding author: Sungsik Lee (sungsiklee@pusan.ac.kr)

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ABSTRACT We present a study on a weight-update characteristics dependent on electron densities of Hf-ZnO charge-trap layers (CTLs) in a low-power synaptic thin-film transistor (Syn-TFT) operating in the sub-threshold region. For a memory function of Syn-TFTs, electrons in the Hf-ZnO CTL are de-trapped toward a channel layer with applying negative programming-pulses (PPs) to a gate terminal. Here, the Hf-ZnO CTL with a lack of electrons is insufficient to get the electron de-trapping. So, as increasing the electron density in the CTL, it is expected that the number of de-trapped electrons are also increased, which leads to a faster weight-update of the Syn-TFT compared to a lower electron density of the Hf-ZnO CTL with applying the same number of the negative PPs. Due to this phenomenon, a weight-update characteristics (i.e. a synaptic facilitation) is to be improved, which can lead to an increase of a dynamic ratio (dr_w) as a measure of that. To check this, the pulsed characteristics of fabricated Syn-TFTs are monitored with respect to different electron densities in the Hf-ZnO CTL. Here, the electron densities in the CTL are controlled by the growth temperature of an atomic-layer-deposition (ALD) process. From experimental results, as increasing of electron carrier densities in the Hf-ZnO CTL, it is confirmed that the weight-update of the Hf-ZnO CTL with more electron carrier density is faster than that with fewer electrons. Also, for higher carrier densities, the relaxation time is quicker through paired-pulse facilitation compared to the case of lower carrier densities.

INDEX TERMS Carrier density, charge-trap layer, dynamic ratio, hafnium-doped zinc oxide, maximum static-power consumption, relaxation time, synaptic facilitation, synaptic thin-film transistor, atomic layer deposition.

I. INTRODUCTION

Synaptic devices, such as memristors as a passive type and synaptic transistors as an active type, have been intensively investigated for neuromorphic systems [1], [2], [3], [4]. Among them, as an active type, a synaptic transistor is more attractive because it has a higher controllability associated with multiple terminals unlike memristors with two terminals [5], [6]. Recently, a synaptic thin-film transistor (i.e., Syn-TFT), one of the forms of synaptic transistors, has been based on a low-cost emerging material, such as an amorphous oxide (e.g., InGaZnO, HfZnO, HfO, ZnO) [7], [8]. In the Syn-TFT, a synaptic functionality (i.e. memory functionality) can usually be implemented within gate insulator systems, such as a charge-trap layer (CTL) or ferro-electric oxide layer [9], [10].

As a typical structure, the Syn-TFT with a non-conductive CTL (e.g., HfO, Al_2O_3) is usually operating with a high read-voltage corresponding to a high drain-current level (i.e., a synaptic facilitation state) [11]. Starting with this initial state, the electron trapping into this CTL occurs while applying positive programming pulses (PPs), leading to a positive threshold-voltage shift of the Syn-TFT, thus a reduction of the drain current at the read voltage (i.e., a synaptic

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depression process). After arriving at the full synaptic depression, the drain current can be recovered with applying negative PPs (i.e. a synaptic facilitation). However, with this non-conductive CTL, the Syn-TFT is initially difficult to start with a depression state [12]. In other words, an electron de-trapping phenomenon cannot ideally be induced for the synaptic facilitation because the non-conductive CTL has no electrons at its initial state [13], [14]. This limitation of this kind of the CTL can eventually lead to a narrow memory window [15], [16]. To overcome these limitations, the conductive CTL can be suggested, which can be realized with amorphous oxide semiconductors. Indeed, it has been reported that a ZnO can be used as a conductive CTL [17]. Here, the ZnO layer has electrons initially. So, electrons in the ZnO CTL can be de-trapped initially when a negative PP is applied to the gate terminal, which leads to a negative threshold-voltage shift and gradually an increase of the drain current (i.e., a synaptic facilitation). Since the ZnO layer usually has metastable defects, such as oxygen vacancies, metal cations (e.g., Ga, In, Hf) can be added for a higher stability [18], [19], [20]. Although this approach with the ZnO-based CTL can be a solution to overcome the limitations of the Syn-TFT with the non-conductive CTL, a static power consumption of the Syn-TFT can be relatively high since it is operating in the above-threshold region rather than the sub-threshold region. This aspect is not consistent with a biological synapse with an ultra-low power characteristics [21]. Thus, the weight-update characteristics in the sub-threshold operating Syn-TFT with the Hf-ZnO CTL is needed to be studied.

In this paper, we present a weight-update characteristics of synaptic thin-film transistors (Syn-TFTs) depending on carrier densities of Hf-ZnO in charge-trap layers (CTLs), while operating in the sub-threshold region for an ultra-low power consumption. Here, this carrier density of the Hf-ZnO CTL is controlled by the growth temperature of the atomic-layer deposition (ALD). For a synaptic functionality of Syn-TFTs, when negative programming pulses (PPs) are applied to the gate terminal, electrons in the Hf-ZnO CTL are de-trapped toward a channel layer. Assuming that the Hf-ZnO CTL has a low carrier density, electrons should be difficult to get an electron de-trapping phenomenon. On the other hand, as the electron density in the CTL is increased, it is expected that the number of de-trapped electrons is also increase, leading to a faster weight-update of the Syn-TFT in comparison with a lower electron density of the Hf-ZnO CTL with a series of the same number of the negative PPs. Therefore, this phenomenon is expected to improve the weight-update characteristics (i.e., a synaptic facilitation), leading to the increase of a dynamic ratio (dr_w) as a measure of that. To verify this, the pulsed characteristics of the fabricated Syn-TFTs are monitored in relation to different electron densities of the Hf-ZnO CTL. According to experimental results, the Hf-ZnO CTL with a higher carrier density shows a quicker weight-update than that with a lower carrier density, and this process is operated in a sub-threshold region for a low power consumption.

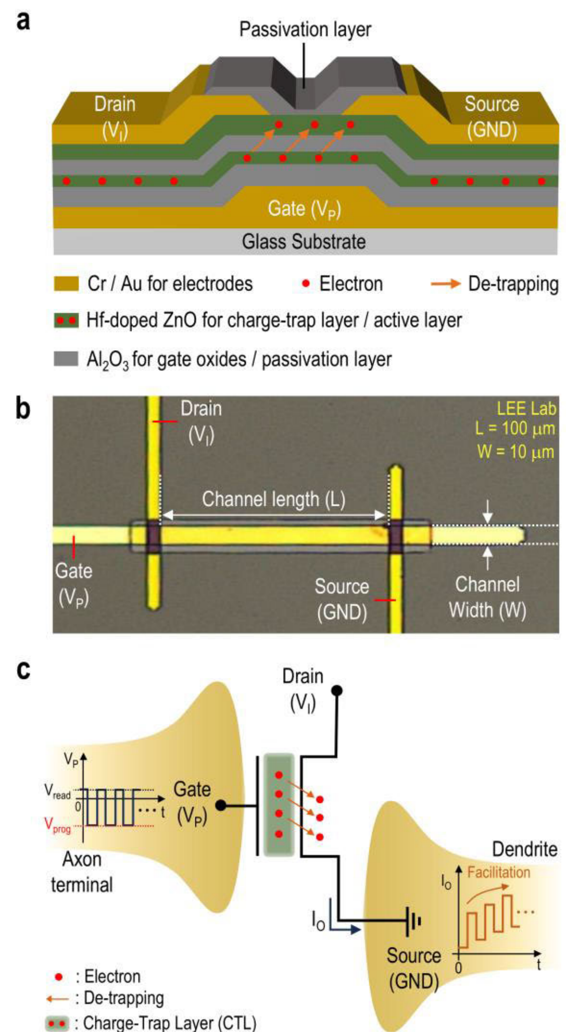

FIGURE 1. (a) Cross-sectional view of the Syn-TFT with a charge-trap layer (CTL) based on a Hf-doped ZnO (i.e. a Hf-ZnO CTL) and (b) optical microscope image of the fabricated Syn-TFT. (c) Schematic of the equivalent circuit with a Syn-TFT based on the Hf-ZnO CTL.

II. SYN-TFT WITH THE CTL AND RELATED THEORIES

Figs. 1(a) and (b) show a cross-sectional view and the captured optical microscope image of fabricated synaptic thin-film transistors (Syn-TFTs), respectively. A memory function of the Syn-TFT can be implemented with a charge-trap layer (CTL) which has a difference of an energy band gap in the gate insulator stacks [22]. Here, the CTL is based on a Hf-doped ZnO (Hf-ZnO) which has a higher carrier density (e.g., the electron density) than a dielectric CTL (e.g., HfO). Note that, the Hf-ZnO is combined with the ZnO as a base and a metal material (i.e., Hf), which is relatively improved for stable synaptic characteristics [23], [24], [25]. With the high carrier density in the CTL can be expected that a synaptic weight-update (e.g., the synaptic facilitation) is improved. Especially, the electrons in the Hf-ZnO CTL are more de-trapped into a channel layer for applying negative PPs to the gate terminal (V_P) (see Fig. 1(c)). Due to the

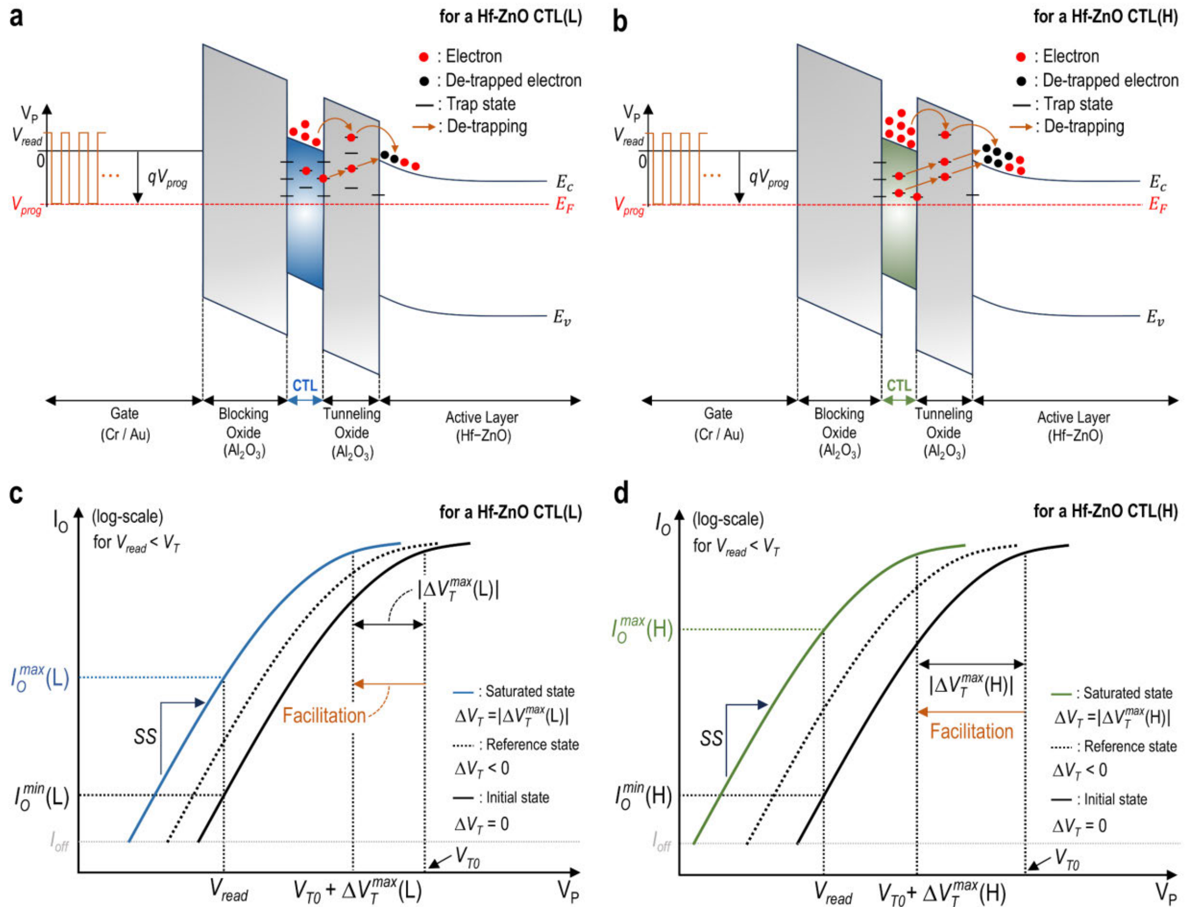

FIGURE 2. Band diagrams to describe the electron de-trapping with applying continuously negative programming pulses for (a) a lower electron carrier density and (b) higher electron carrier density, respectively. After multiple negative programming pulses, for the extreme cases (i.e. the initial and saturated state), the conceptual plot of the transfer characteristics for (c) a lower electron carrier density and (d) higher electron carrier density in the sub-threshold region, respectively.

de-trapped electrons, the threshold voltage shift (ΔV_T) can be changed and it is expressed as follows,

$$\Delta V_T = -\frac{\Delta Q_e^{dt}}{C_{ox}}, \quad (1)$$

where ΔQ_e^{dt} is the variation of a de-trapped negative charge density per area in the gate oxide and C_{ox} is the gate insulator capacitance per area. Here, ΔQ_e^{dt} is related to the number of de-trapped electrons per cubic (i.e., the negative carrier density, n_e^{dt}), which is expressed as follows,

$$\Delta Q_e^{dt} = q\Delta n_e^{dt} t_{CTL}, \quad (2)$$

where the Δn_e^{dt} is the variation of n_e^{dt} for applying negative PPs to the V_P and t_{CTL} is the thickness of the Hf-ZnO CTL. Based on (1), the ΔV_T is rewritten with (2), as follows,

$$\Delta V_T = -\frac{q\Delta n_e^{dt} t_{CTL}}{C_{ox}}. \quad (3)$$

Here, the increase of Δn_e^{dt} leads to the negative shift of the ΔV_T (see (3)). Therefore, with the varied ΔV_T, the threshold voltage (V_T) can also be changed and represented as follows,

$$V_T = V_{T0} + \Delta V_T, \quad (4)$$

where the V_{T0} is the initial value. From the (4), the V_T is defined with (3), as follows,

$$V_T = V_{T0} - \frac{q\Delta n_e^{dt} t_{CTL}}{C_{ox}}. \quad (5)$$

Assuming that the Hf-ZnO CTL is deposited for a higher temperature, the V_T can be a more negative shift compared to a lower deposition temperature, since the Δn_e^{dt} of Hf-ZnO in the CTL can be increased by a relatively higher growth temperature for a series of negative PPs to the V_P. Therefore, it needs to specifically be analyzed with respect to each electron carrier density (i.e., lower and higher electron carrier densities).

As mentioned in the previous section, the Hf-ZnO CTL has a higher negative carrier density (i.e., the number of electrons per cubic, n_e) compared to the dielectric CTL, and it can be improved to the weight-update characteristics (e.g., dr_w). Here, the n_e of the Hf-ZnO CTL can be dependent on the

TABLE 1. Process conditions for a Hf-ZnO CTL (L) and Hf-ZnO CTL (H) in the ALD systems (Lucida 100, NCD Co. Ltd). In the Table 1, for deposition temperature of 90 °C and 200 °C, the growth rate of ZnO is approximately to be 1.6 Å per cycle, and the HfO is about 1Å per cycle [26], [27], [28].

Order	Precursors / Reactant	Hf-ZnO CTL(L) (Depo-Temp : 90 ℃)	Hf-ZnO CTL(H) (Depo-Temp : 200 ℃)	Materials	Growth rate
1	TEMAHf / H_2O	1 cycle	1 cycle	HfO	≈ 1 Å $(cycle)^{-1}$
2	DEZ / H_2O	12 cycles	12 cycles	ZnO	≈ 1.6 Å $(cycle)^{-1}$
3	TEMAHf / H_2O	1 cycle	1 cycle	HfO	≈ 1 Å $(cycle)^{-1}$
4	DEZ / H_2O	12 cycles	12 cycles	ZnO	≈ 1.6 Å $(cycle)^{-1}$

deposition temperature for the atomic layer deposition (ALD) process [26], [27], [28]. Therefore, it needs to be monitored for the two different electron carrier densities (i.e., relatively lower and higher carrier densities). When the Hf-ZnO CTL is deposited at a high temperature, the electrons of the Hf-ZnO CTL can be more effectively de-trapped through the trap states toward the channel layer by multiple negative PPs to the V_P compared to a low electron carrier density (see Figs. 2(a) and (b)). With these de-trapped electrons, the ΔV_T is reduced, which leads to the increase of the output current (I_O) (see (3)). This process is called the synaptic facilitation. Note that, when applying positive PPs to the V_P, the I_O is decreased due to an increase of the I_O, which is called a synaptic depression. Here, the I_O is operated in a sub-threshold region for a low-power consumption, and I_O can be expressed, as follows [7], [21],

$$I_O = \frac{W}{L} K_{sub} exp\left(\frac{V_{read} - V_{T0} - \Delta V_T}{n_t kT/q}\right) V_I, \quad (6)$$

where the W is a channel width, L is a channel length, K_{sub} is a constant for the sub-threshold region, q is the elementary charge, V_I is a fixed voltage at the drain electrode, n_t is the ideality factor related to interface states, and kT is the thermal energy. Here, the I_O is rewritten with (4), as follows,

$$I_O = \frac{W}{L} K_{sub} exp\left(\frac{V_P - V_T}{n_t kT/q}\right) V_I. \quad (7)$$

With (3), the I_O can be represented based on (7), as follows,

$$I_O = \frac{W}{L} K_{sub} exp\left(\frac{V_{read} - V_{T0}}{n_t kT/q}\right) exp\left(\frac{q\Delta n_e^{dt} t_{CTL}}{n_t kT/q} \frac{1}{C_{ox}}\right) V_I. \quad (8)$$

For the initial state, assuming that the number of de-trapped electrons is zero (i.e., $\Delta n_e^{dt} = 0$), the ΔV_T is to be zero (i.e., $\Delta V_T = 0$) (see (3)), thus the I_O is expected to be a minimum value (I_O^{min}) as follows,

$$I_O^{min} = \frac{W}{L} K_{sub} exp\left(\frac{V_{read} - V_{T0}}{n_t kT/q}\right) V_I. \quad (9)$$

As mentioned earlier, for applying negative PPs to the V_P, the I_O is increased by the de-trapped electrons into the channel layer (i.e., the synaptic facilitation). Especially, after applying negative PPs, the ΔV_T can be saturated as a maximum value (i.e., $|\Delta V_T^{max}|$) due to the saturated Δn_e^{dt} (i.e., maximized Δn_e^{dt}, $\Delta n_e^{dt}(max)$), so the I_O is to be a maximum value (i.e., I_O^{max}) (see Figs. 2(c) and (d)), and it is expressed as follows,

$$I_O^{max} = \frac{W}{L} K_{sub} exp\left(\frac{V_{read} - V_{T0}}{n_t kT/q}\right) \times exp\left(\frac{q\Delta n_e^{dt}(max) t_{CTL}}{n_t kT/q} \frac{1}{C_{ox}}\right) V_I. \quad (10)$$

From (8), the I_O is rewritten with (9) as follows,

$$I_O = I_O^{min} exp\left(\frac{q\Delta n_e^{dt} t_{CTL}}{n_t kT/q} \frac{1}{C_{ox}}\right). \quad (11)$$

With the (11), the I_O is a function of Δn_e^{dt} (i.e., $I_O = f(\Delta n_e^{dt})$). Here, with a ratio between the I_O^{max} and I_O, the normalized synaptic weight ($\overline{w_G}$) which has a range from 0 to 1, is defined as follows [8],

$$\overline{w_G} \equiv \frac{I_O}{I_O^{max}}. \quad (12)$$

Based on (12), the minimum and maximum value of the $\overline{w_G}$ (i.e., $\overline{w_G^{min}}$ and $\overline{w_G^{max}}$) can be expressed with the I_O^{min} and I_O^{max} at the fixed V_{read}, respectively, as follows,

$$\overline{w_G^{min}} = \frac{I_O^{min}}{I_O^{max}}, \quad (13)$$

$$\overline{w_G^{max}} = 1. \quad (14)$$

With (13) and (14), the characteristics of weight-update (e.g., dr_w) can be defined, as follows [7], [8],

$$dr_w \equiv \frac{\overline{w_G^{max}}}{\overline{w_G^{min}}}. \quad (15)$$

For the Hf-ZnO CTL of a higher n_e (i.e., the Hf-ZnO CTL(H)), the dr_w can be given to be a larger value because the $\overline{w_G^{min}}$ is decreased by the increase of I_O^{max}(see (13)). On the other hand, a relatively small I_O^{max} for the Hf-ZnO

CTL having a low n_e (i.e., the Hf-ZnO CTL(L)) leads to the increase of the w_G^{min}, resulting in a lower dr_w(see (13)). Note that, for the increase of the dr_w, the synaptic resolution can be improved. Additionally, a static power consumption (i.e., P_{static}) at V_P=V_{read} is significant for the neuromorphic system as another synaptic characteristics, so it is to be reduced. This P_{static} is explained as a product of between the I_O and constant V_I (i.e., P_{static}=$V_I I_O$). Here, the maximum value of the P_{static} (i.e., P_{static}^{max}) is expressed as follows [8],

$$P_{static}^{max} = V_I I_O^{max}. \quad (16)$$

It is expected that the Syn-TFT with the Hf-ZnO CTL(H) can be required to the larger power dissipation compared to the Hf-ZnO CTL(L) suggesting the trade-off relation between the dr_w and P_{static}^{max} dependent on the electron carrier density of the Hf-ZnO CTL. Therefore, to verify these, it is needed to be monitored experimentally.

III. RESULTS AND DISCUSSION

A. DEVICE PREPARATION

The Syn-TFTs with the Hf-ZnO are fabricated as follows. Firstly, to remove organic contaminants on the glass wafer, the wafer is cleaned with an acetone and de-ionized water (D.I water) for each 30 minutes, using an ultrasonic cleaning. After that, for the gate electrode, the patterning and metal deposition are performed with a mask aligner and thermal evaporation on the glass wafer, respectively. After these processes, the lift-off process is carried out for the gate electrode patterning with a Cr-based photomask, which was designed with AutoCad™. Here, the total thickness of the gate electrode is 105 nm consistent with Cr of 5 nm and Au of 100 nm. Note that, Au has a poorer adhesion compared to other metals (e.g., Al), so Cr is used to enhance the adhesion capability between glass substrate and Au [29], [30]. And then, the wafer with the deposited gate electrode is annealed at 200 °C for 30 minutes. Afterward, to make the hydrophilicity on the glass substrate, the UV-Ozone is implemented for 15 minutes [31], [32]. Following this, for the blocking oxide (B-Ox), the Al_2O_3 films is grown by the thermal ALD at 200 °C, using both trimethyl aluminum (TMA) precursor and water vapor (H_2O) reactant of 650 cycles. In the following step, to deposit a charge-trap layer (CTL), a 4 nm thick Hf-doped ZnO (Hf-ZnO) is deposited with the thermal ALD using tetrakis hafnium (TEMAHf), diethylzinc (DEZ) precursor, and H_2O reactant. Here, concerning different electron carrier densities of CTL by the deposition temperature (a relatively lower and higher carrier density), the detailed process conditions are presented in Table 1. Then, for the tunneling oxide (T-Ox), the Al_2O_3 films is deposited by thermal ALD utilizing TMA and H_2O precursors of 150 cycles. Subsequently, the active layer (i.e., Hf-ZnO) is achieved using DEZ, TEMAHf, and H_2O which is a thickness of 10.1 nm with a ratio of 100:1 between ZnO and HfO through the ALD at 150 °C, and the annealing is proceeded at 200 °C for 2 hours. After this process, for an active region, the device needs to be wet etching. Firstly, using a hydrochloric acid (HCl), the channel layer and Hf-ZnO are etched. And then, for T-Ox and B-Ox etching, buffered oxide etch (BOE) is used. Afterward, with the mask aligner and thermal evaporation, based on the lift-off process, the source and drain electrodes are deposited to 105 nm (i.e., Cr of 5 nm and Au of 100 nm). Finally, through the ALD, the passivation process is proceeded with TMA precursors and H_2O reactant, and the vacuum annealing is performed at 200 °C for 30 mins (see Fig. 1(a)).

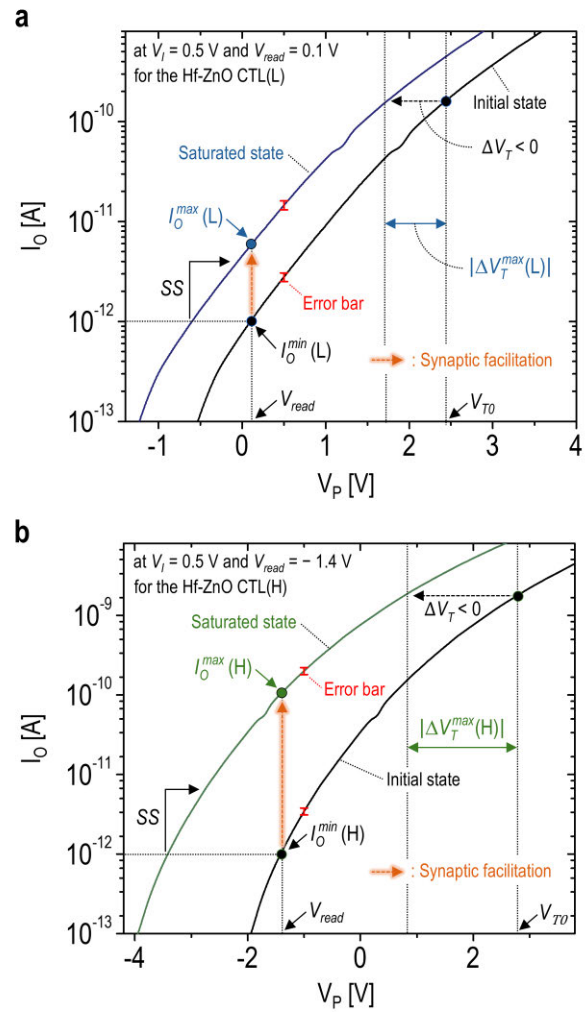

FIGURE 3. Transfer characteristics of fabricated Syn-TFTs with two different electron carrier density in the Hf-ZnO CTL, which are the deposited temperatures at (a) 90°C and (b) 200°C for V_I= 0.5 V (fixed), respectively. In addition, error bars of 10% are shown for the I_O at the saturated and initial state, respectively.

B. STATIC CHARACTERISTICS OF SYN-TFTS

Figs. 3(a) and (b) show the static characteristics of fabricated Syn-TFTs with the Hf-ZnO CTL having different n_e for two extreme states (i.e., the initial and saturated states) at $V_I = 0.5$V, respectively. As can be seen, to fairly compare the Syn-TFTs, the I_O^{min} is commonly set as 10^{-12} A, so the V_{read} for the Hf-ZnO CTL(L) and Hf-ZnO CTL(H) are set as 0.1 V and – 1.4 V, respectively. For the initial state (i.e., $V_T = V_{T0}$), after negative PPs of 20 cycles are applied to

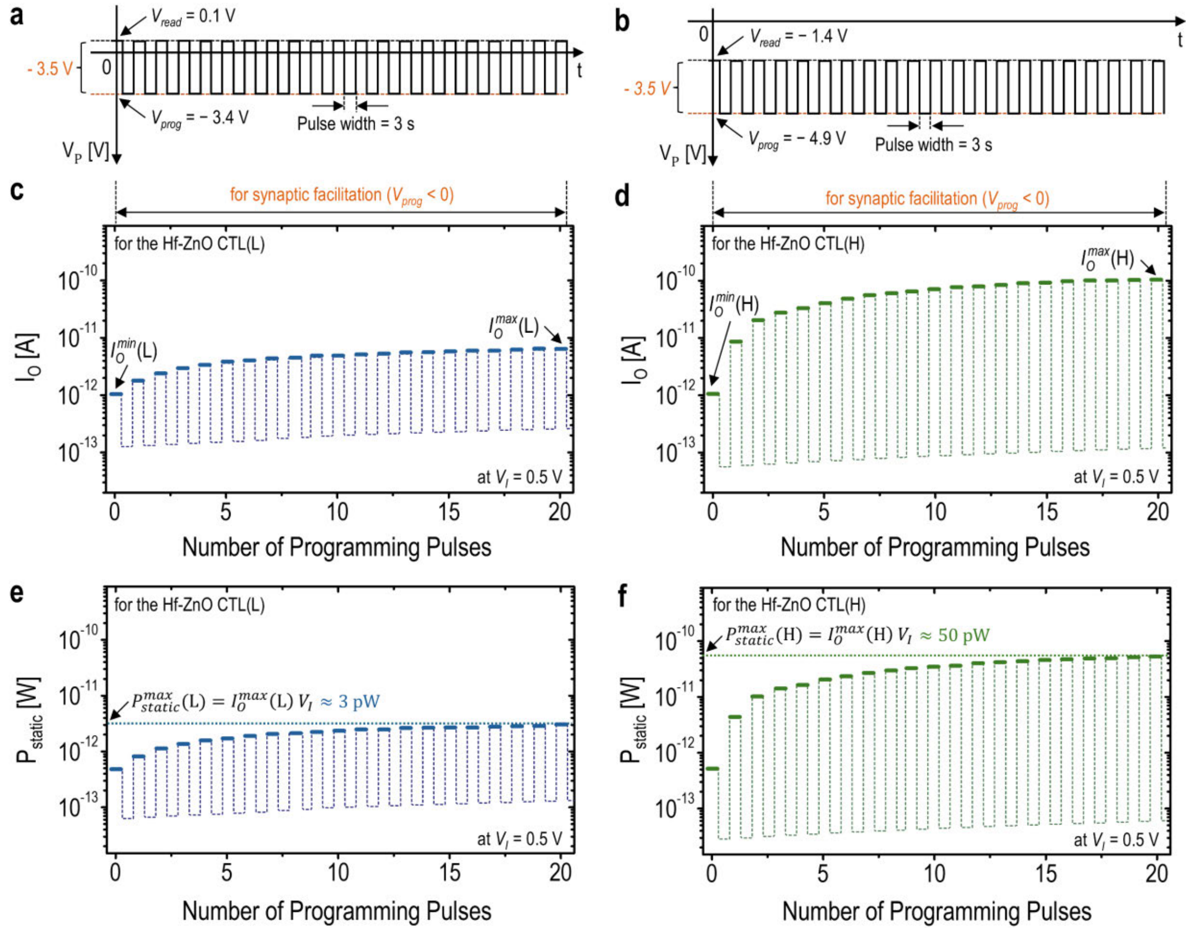

FIGURE 4. Waveform of the negative programming pulses (PPs) for the synaptic facilitation of the (a) Hf-ZnO CTL(L) and (b) Hf-ZnO CTL(H) which are different deposition temperatures as 90 °C and 200°C, respectively. The varied output current (I_O) of the (c) Hf-ZnO CTL(L) and (d) Hf-ZnO CTL(H) for the synaptic facilitation of the Syn-TFT with the negative PP train, respectively. Here, the negative PPs of 20 cycles for both Hf-ZnO CTL(L) and (H) are applied to the V_P. The change of the static power consumption (P_{static}) of Hf-ZnO CTL grown for (e) 90 °C and (f) 200 °C for the synaptic facilitation, indicating the maximum value of the static power consumption (P_{static}^{max}), respectively.

the V_P, it is observed that the I_O arrives at the saturated state with $\Delta V_T = |\Delta V_T^{max}|$ because of the electron de-trapping (see Figs. 2(a) and (b)). As can be seen, for the Syn-TFT with the Hf-ZnO CTL(H), the $|\Delta V_T^{max}(\text{H})|$ (≈2 V) is bigger than the $|\Delta V_T^{max}(\text{L})|$ (≈0.7 V) for the Hf-ZnO CTL(L). This result $|\Delta V_T^{max}(\text{H})| > |\Delta V_T^{max}(\text{L})|$ because the $\Delta n_e^{dt}(\text{H}) > \Delta n_e^{dt}(\text{L})$, which is explained as (3). From each $|\Delta V_T^{max}|$ ($|\Delta V_T^{max}(\text{L})|$ and $|\Delta V_T^{max}(\text{H})|$), the I_O^{max} is determined as I_O^{max} (L) ≈ 6 pA and I_O^{max} (H) ≈100 pA, respectively. Note that, the sub-threshold slope (*SS*) of Syn-TFT, for the Hf-ZnO CTL(L) and Hf-ZnO CTL(H), is determined to be approximate 0.9 V / dec, commonly. Based on the static characteristics of Syn-TFTs with two cases of the Hf-ZnO CTL (i.e., the Hf-ZnO CTL(L) and Hf-ZnO CTL(H)) in the previous section, the detailed synaptic process (i.e., the synaptic facilitation) needs to be checked in terms of the weight-update characteristics and power consumption.

C. PULSED CHARACTERISTICS OF SYN-TFTS

Based on the analysis related to the static characteristics of fabricated Syn-TFTs with the Hf-ZnO CTL at different carrier densities, the pulsed characteristics of the Syn-TFTs need to be monitored. Figs. 4(a) and (b) show the pulse specification for the synaptic facilitation in each graph. As can be seen, for the Hf-ZnO CTL(L), the V_{read} and V_{prog} are set as each 0.1 V and – 3.4 V. On the other hand, the V_{read} and V_{prog} of Hf-ZnO CTL (H) are to be – 1.4 V and – 4.9 V, respectively. Additionally, the pulse width for both the Hf-ZnO CTL(L) and Hf-ZnO CTL(H) is commonly 3 s. Also, the number of cycles and duty cycle equally is set as 20 and 50 % for two cases, respectively.

With these pulse conditions, Figs. 4(c) and (d) show the changed I_O for the synaptic facilitation at two growth temperatures. As can be seen, with these cases (i.e., the Hf-ZnO CTL(L) and Hf-ZnO CTL(H)), the I_O is gradually increased with multiple negative PPs for the synaptic facilitation (see Fig. 1(b)). This is because the electrons are de-trapped into the channel layer (i.e., the increase of Δn_e^{dt}), resulting in the decrease of ΔV_T (see (3) and (7)). After the synaptic facilitation (i.e., 20 cycles of negative PPs), the I_O for both Hf-ZnO CTL(L) and Hf-ZnO CTL(H) are saturated with $|\Delta V_T^{max}|$(L) ≈ 0.7 V and $|\Delta V_T^{max}|$(H) ≈ 2 V, due to the

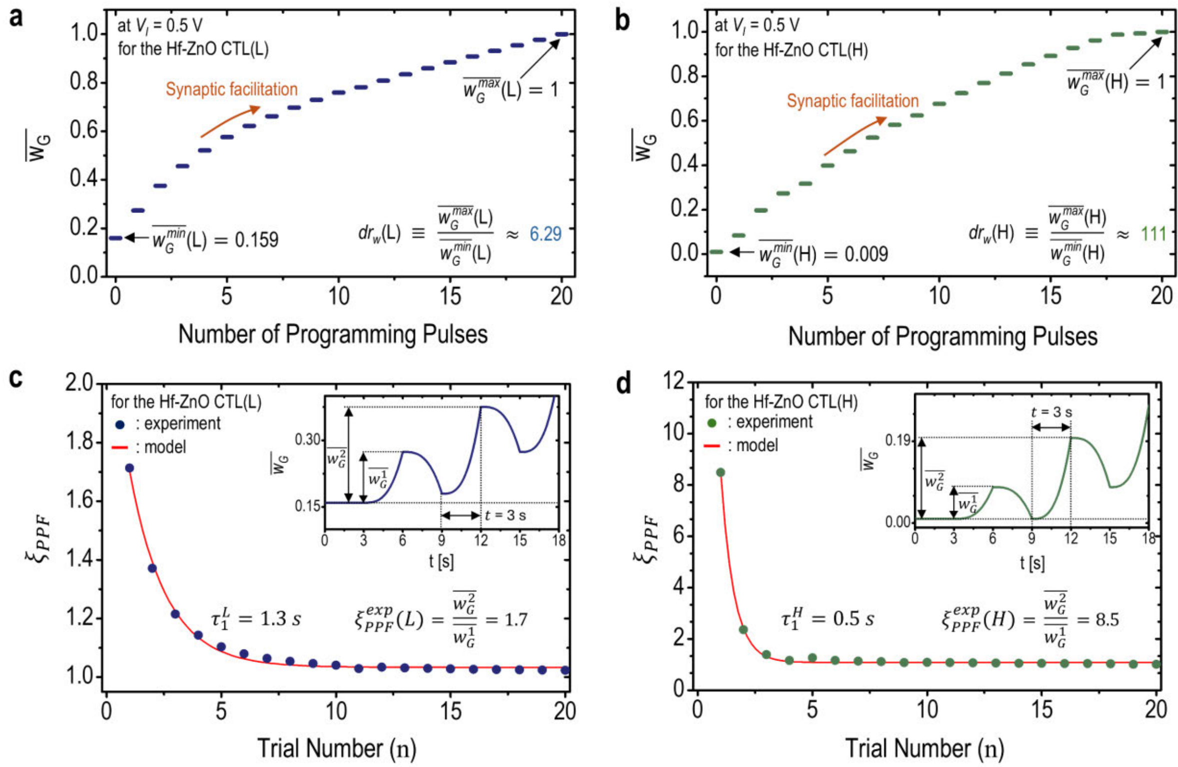

FIGURE 5. The normalized synaptic weight ($\overline{w_G}$) versus the number of PPs for the Syn-TFTs with the (a) Hf-ZnO CTL(L) and (b) Hf-ZnO CTL(H), respectively. A paired pulse facilitation (PPF) as a function of trial number for the (c) Hf-ZnO CTL(L) and (d) Hf-ZnO CTL(H), respectively. Here, the PPF can be explained as ratio between $\overline{w_G^{n+1}}$ and $\overline{w_G^{n}}$, and it is symbolized as ξ_{PPF}, where the $\overline{w_G^{n+1}}$ and $\overline{w_G^{n}}$ are the $\overline{w_G}$ at n+1- and n-th number of negative PPs for the synaptic facilitation, respectively. Inset: Plots of the $\overline{w_G}$ versus the time for the first and second pulse number.

TABLE 2. Summary of extracted parameters for fabricated Syn-TFTs with the different n_e of the Hf-ZnO CTL.

Parameters	$\lvert\Delta V_T^{max}\rvert$	I_O^{max}	P_{static}^{max}	dr_w	ξ_{PPF}^{exp} (n = 1)
Hf-ZnO CTL (L) (Deposited at 90 °C)	0.7 V	6 pA	3 pW	6.29	1.7
Hf-ZnO CTL (H) (Deposited at 200 °C)	2 V	100 pA	50 pW	111	8.5

higher relative Δn_e^{dt}(max) at Hf-ZnO CTL (H) compared to the Δn_e^{dt}(max) of Hf-ZnO CTL (L). At the $\lvert\Delta V_T^{max}\rvert$, the I_O is to be the I_O^{max} which is leading to the I_O^{max} (H) ≈100 pA and I_O^{max} (L) ≈6 pA for each growth temperature, respectively, and it is explained as (10). With the increased I_O, the P_{static} can be monitored for applying a series of negative PPs. Figs. 4(e) and (f) are shown that the P_{static} is gradually increased by the increase of I_O for two cases, respectively. Afterward, at the saturated state, the P_{static} nearly arrives to the P_{static}^{max} of 3 pW for the Hf-ZnO CTL(L) and 50 pW for the Hf-ZnO CTL(H), using (16) respectively, showing P_{static}^{max}(H) > P_{static}^{max}(L), since I_O^{max}(H) (≈100 pA) > I_O^{max}(L) (≈6 pA), which is also explained as (16).

Based on the waveform of multiple negative PPs for the synaptic facilitation, the weight-update characteristics (e.g., dr_w and paired pulse facilitation (*PPF*)) can be verified. Note that, the *PPF* is a phenomenon that the post-synaptic weight induced by the stimulus is increased when the second stimulus closely follows the prior stimulus [33].

In order to check the weight-update characteristics (e.g., dr_w and *PPF*) for different n_e in the Hf-ZnO CTL (i.e., Hf-ZnO CTL(L) and Hf-ZnO CTL(H)), it firstly needs to be monitored the $\overline{w_G}$ for the synaptic process (e.g., synaptic facilitation). Figs. 5(a) and (b) show the modulation of the $\overline{w_G}$ for the synaptic facilitation at different n_e, respectively. As can be seen, the $\overline{w_G}$ is increased from $\overline{w_G^{min}}$ to $\overline{w_G^{max}}$ for

applying a series of negative PPs because of the increase of the I_O (see Figs. 4(c) and (d)), resulting in the same $\overline{w_G^{max}}$ regardless of growth temperatures (i.e., $\overline{w_G^{max}} = 1$). Here, with (13), the $\overline{w_G^{min}}$ is calculated as 0.159 for the Hf-ZnO CTL (L) and 0.009 for the Hf-ZnO CTL(H), respectively, which leads to $\overline{w_G^{min}}(\mathrm{H}) < \overline{w_G^{min}}(\mathrm{L})$. This is because the I_O^{max} (≈100 pA) for the Hf-ZnO CTL(H) is bigger than the I_O^{max} of Hf-ZnO CTL (L) (≈6 pA) where I_O^{min} is commonly set as 10^{-12} A in two cases. With both the determined $\overline{w_G^{max}}$ and $\overline{w_G^{min}}$, dr_w is to be calculated as approximately 6.29 for the Hf-ZnO CTL(L) and 111 for the Hf-ZnO CTL(H), respectively, resulting in $dr_w(\mathrm{H}) > dr_w(\mathrm{L})$ (see Figs. 5(a) and (b)). It is because $\overline{w_G^{min}}(\mathrm{H}) < \overline{w_G^{min}}(\mathrm{L})$, which is explained as (15). Additionally, through the process of $\overline{w_G}$, the synaptic plasticity (e.g., the *PPF*) can be monitored as shown in Figs. 5(c) and (d). Here, the *PPF* is re-constructed as the ratio of the peak amplitudes of the first and second $\overline{w_G}$ response, which is symbolized as ξ_{PPF}, and it is expressed as ratio between $\overline{w_G^{n+1}}$ and $\overline{w_G^{n}}$ as follows,

$$\xi_{PPF}^{exp} = \frac{\overline{w_G^{n+1}}}{\overline{w_G^{n}}}\ (\mathrm{n} \geq 1)\,, \tag{17}$$

where the $\overline{w_G^{n}}$ and $\overline{w_G^{n+1}}$ are the $\overline{w_G}$ at n- and n+1-th negative PPs for the synaptic facilitation, respectively. With this, for the Syn-TFT with the Hf-ZnO CTL at a relatively higher and lower n_e, ξ_{PPF}^{exp} is calculated to be 8.5 and 1.7 for n = 1, respectively, where the ξ_{PPF}^{exp} for the Hf-ZnO CTL (H) (i.e., $\xi_{PPF}^{exp}(\mathrm{H})$) is bigger than the ξ_{PPF}^{exp} of Hf-ZnO CTL (L) (i.e., $\xi_{PPF}^{exp}(\mathrm{L})$). This is because the n_e of Hf-ZnO CTL is increased by the deposition temperature of ALD, leading to the $\Delta n_e^{dt}(\mathrm{H}) > \Delta n_e^{dt}(\mathrm{L})$ for applying multiple negative PPs. Also, to analysis the performance of biological synapse (e.g., relaxation time, τ), the ξ_{PPF} can be fitted by a double exponential decay function as follows, [34],

$$\xi_{PPF}^{mod} = 1 + A_1 exp\left(\frac{-\mathrm{n}}{\tau_1}\right) + A_2 exp\left(\frac{-\mathrm{n}}{\tau_2}\right). \tag{18}$$

Here, n is the trial number of the presynaptic pulse, the A_1 and A_2 are the initial facilitation magnitudes of the rapid and slow phases. The τ_1 and τ_2 are the characteristic relaxation times of the rapid and slow phases, respectively [35]. As shown in Figs. 5(c) and (d), ξ_{PPF}^{exp} show a good agreement with ξ_{PPF}^{mod} for the case of each carrier density (i.e., the Hf-ZnO CTL(L) and Hf-ZnO CTL(H)). From (18), all these parameters are extracted: $A_1^L = 1.3$ %, $A_2^L = 0.1$ %, $\tau_1^L = 1.3$ s, and $\tau_2^L = 11.02$ s for the Hf-ZnO CTL(L).In the other hand, for the Hf-ZnO CTL(H), $A_1^H = 47$ %, $A_2^H = 0.3$ %, $\tau_1^H = 0.5$ s, and $\tau_2^H = 7.05$ s. For the two cases of n_e in the Hf-ZnO CTL, $\tau_1^H (= 0.5\ \mathrm{s}) < \tau_1^L\ (= 1.3\ \mathrm{s})$. These results can be explained as a sensitivity (s_i), which is defined as follows,

$$s_i = \frac{I_O^{max}}{I_O^{min}} \frac{1}{N_P}. \tag{19}$$

In (19), the N_P is the number of negative PPs, and I_O^{min} is commonly set as 10^{-12} A for two cases (i.e., the Hf-ZnO CTL(L) and Hf-ZnO CTL(H)). Thus, the s_i is dependent on the I_O^{max}, and it is related to the $\Delta n_e^{dt}(\max)$ which is explained as (10). As mentioned earlier, $\Delta n_e^{dt}(\max)$ in the Hf-ZnO CTL(H) is higher than the $\Delta n_e^{dt}(\max)$ of Hf-ZnO CTL(L), resulting in $I_O^{max}(\mathrm{L}) < I_O^{max}(\mathrm{H})$. Therefore, for the Hf-ZnO CTL-given a higher n_e, s_i is larger than Hf-ZnO CTL(L), leading to $\tau_1^L\ (= 1.3\ \mathrm{s}) > \tau_1^H (= 0.5\ \mathrm{s})$. Note that the main parameters (e.g., dr_w and P_{static}^{max}) are summarized in Table 2 for the case of different n_e.

These results indicate that the increase of an electron carrier density for the Hf-ZnO CTL can lead to an improvement of the weight-update characteristics (e.g., dr_w and *PPF*) as shown in Fig. 4. However, in terms of power consumption, when the Hf-ZnO CTL has a high electron carrier density, the P_{static}^{max} is a relatively larger compared to the Hf-ZnO CTL(L) (see Figs. 4(e), (f), and Table 2), thus the trade-off relation between dr_w and P_{static}^{max} which can be affected by the $\Delta n_e^{dt}(\max)$ for the synaptic facilitation.

IV. CONCLUSION

In this study, we have discussed that the experimental framework on a carrier density of the CTL-dependent weight-update characteristics of the Syn-TFT based on the Hf-ZnO CTL has been shown for the low-power synaptic thin-film transistors. Here, the number of electrons per cubic of Hf-ZnO in the CTL is dependent on the growth temperature in the atomic layer deposition. As increasing the electron carrier density in the Hf-ZnO CTL, the weight-update characteristics (e.g., dynamic ratio) for the number of negative programming pulses can be improved. To verify this, the static and pulsed characteristics have been monitored for the Hf-ZnO CTL-deposited at two different temperatures (i.e., 90°C and 200°C), which are given lower and higher electron carrier densities, respectively. From the fabricated two Syn-TFTs with Hf-ZnO CTL having different carrier densities, it has been observed that the dynamic ratio in the CTL for a relatively higher and lower carrier density are 111 and 6.29 for applying negative programming pulses to the gate terminal, respectively. As shown in Table 2, the dynamic ratio is larger than the Hf-ZnO CTL for a low electron carrier density. Additionally, the relaxation time (i.e., τ) of CTL-grown at 90 °C (≈1.3 s) is longer compared to 200 °C (≈0.5 s) because s_i of the Hf-ZnO CTL(H) is larger than the Hf-ZnO CTL(L). From these results, the Hf-ZnO CTL with the high electron density is similarly shown as biological synapse. Consequently, we are believed that the increase of the programming speed due to the higher carrier density leads to improve data processing efficiency in the neuromorphic system. Furthermore, if the optimized growth temperature of the Hf-ZnO CTL can determined for a large dynamic ratio and synaptic plasticity in terms of the device level, it can be believed to achieve a superior high-level intelligence of the neuromorphic system which is composed of Syn-TFTs.

AUTHOR CONTRIBUTION

(Kunhee Tae and Danyoung Cha contributed equally to this work.) Kunhee Tae performed the fabrication process with Gyoungyeop Do and Nayeoung Lee. Kunhee Tae performed the measurement and characterization of the fabricated devices with Gyoungyeop Do. Kunhee Tae did the synaptic analysis with Danyoung Cha. Kunhee Tae drew all figures. All the authors discussed together and contributed to writing the manuscript.

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KUNHEE TAE is currently pursuing the master's degree with the Department of Electronics, Pusan National University, South Korea. His research interests include synaptic devices and physics for the low power operation of neuromorphic circuits and systems.

DANYOUNG CHA received the bachelor's degree from the Department of Electronics, Pusan National University, South Korea, in 2019, where he is currently pursuing the combined master's and Ph.D. degrees. His research interests include synaptic devices and physics for the low power operation of neuromorphic circuits and systems.

GYOUNGYEOP DO received the bachelor's degree from the Department of Electronics, Pusan National University, South Korea, in 2020, where he is currently pursuing the master's degree. His research interests include synaptic devices, device fabrications, and device measurements for the low power operation of neuromorphic circuits and systems.

NAYEONG LEE is currently pursuing the master's degree with the Department of Electronics, Pusan National University, South Korea. Her research interests include synaptic devices and physics for the low power operation of neuromorphic circuits and systems.

SUNGSIK LEE received the Ph.D. degree from University College London (UCL), London, U.K., in 2013. From 2013 to 2017, he worked as a Research Associate with the University of Cambridge, Cambridge, U.K. He has been a Professor with the Department of Electronics, Pusan National University (PNU), Pusan, Republic of Korea, since 2017. His area of expertise is semiconductor devices and physics for futuristic electronics. So far, he has published over 80 articles in the related field, including the prestigious journal 'Science' as the first author. In 2017, he was awarded the Best Teaching Prize 2017 from the Korean Society for Engineering Education (KSEE), Republic of Korea. He is currently the Director of the Inter-university Semiconductor Research Center (PNU-ISRC, called Ban-Gong-Yeon) for the regional semiconductor education and services.