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RESEARCH ARTICLE

Retention Characteristics Dependent on High-κ Gate-Insulator Stack in Hf-ZnO Synaptic Thin-Film Transistors

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ABSTRACT In this paper, we present a study on a retention characteristics dependent on a high-κ gate insulator stack in synaptic thin-film transistors (Syn-TFTs) with a Hf-ZnO channel layer. A memory function of Syn-TFTs can be implemented in a gate insulator, where electrons are trapped with applying positive programming pulses to a gate terminal. This is usually realized in a flash memory structure with the tunneling oxide (T-Ox). As a simple structure, the gate insulator without the T-Ox can also be used, where traps associated with defects are intentionally playing the role as charge trapping sites. Here, depending on the presence or absence of the T-Ox in the gate insulator, it is anticipated that both the weigh-update characteristics (e.g., a programming speed) and retention characteristics (e.g., a retention time) of the Syn-TFTs are varied. To verify this, the pulsed characteristics of the fabricated Syn-TFTs with different gate-insulator structure (i.e., the fabricated Syn-TFTs with and without the T-Ox) are monitored experimentally. From experimental results, it is found that the programming speed of the Syn-TFT without the T-Ox is faster compared to the Syn-TFT with the T-Ox, meaning a higher sensitivity. On the other hand, the extracted retention time of the Syn-TFT with the T-Ox is longer than that without the T-Ox. These suggest a trade-off relation between the sensitivity and retention time depending on whether the T-Ox exists in the gate insulator stack.

INDEX TERMS Synaptic thin-film transistor, high-κ gate-insulator stack, hafnium-doped zinc oxide, tunneling oxide, retention time, sensitivity.

I. INTRODUCTION

Amorphous oxide material-based synaptic thin-film transistors (Syn-TFTs) have attracted a significant research interest for neuromorphic applications due to their low-temperature processability and low power consumption, enabled by their wide bandgap [1], [2], [3], [4], [5]. The ZnO, compensated with metal cations like Ga, In, or Hf, is widely employed for the channel layer [6], [7], [8], [9]. And a synaptic functionality can be implemented within a high-k amorphous oxide gate insulator stack, such as Al_2O_3, HfO_2, or ZrO_2, incorporating a charge-trap layer (CTL) with a tunneling oxide (T-Ox) [10], [11], [12], [13]. With a Syn-TFT based on the CTL structure, when the positive programming pulse is applied to the gate terminal, channel electrons are trapped into the CTL through the T-Ox [12], [13], [14], [15]. Here, it is difficult for electrons trapped in the CTL to be de-trapped toward the channel because the T-Ox can play the role as an energy barrier for the trapped electrons, thus a good retention characteristics [16]. At the same time, depending on the thickness of the T-Ox, the electron trapping for a positive programming process can be suppressed, especially with a thick T-Ox, which can lead to a poor weight-updates characteristics (e.g., a slow programming

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speed) [17], [18]. As another approach, the gate insulator without the T-Ox can also be considered as the synaptic gate insulator, where defects are intentionally used as trap states for electrons [12], [13], [19], [20]. With these defective oxides, the Syn-TFT can be anticipated to easily accomplish the synaptic weight-updates characteristics due to the absence of the T-Ox as an energy barrier [12], [13], [21], [22]. On the other hand, since there is no energy barrier, trapped electrons can easily be de-trapped toward the channel layer, thus a short retention time (τ_{ret}) [23]. In this vein, a trade-off relation between the weight update and retention characteristics needs to be specifically analyzed for a dependence on whether the T-Ox exists in the gate insulator stack.

In this paper, a study on the retention characteristics depending on a high-κ gate insulator stack in the Syn-TFT with a Hf-doped ZnO (Hf-ZnO) active layer is shown. In the Syn-TFT, a memory functionality can be achieved in the gate insulator through electron trapping, utilizing either the gate insulator with or without the T-Ox. Here, in the Syn-TFT with the T-Ox, which is playing the role as an energy barrier by a wide bandgap, tends to suppress an electron trapping and de-trapping phenomena, respectively. So, the Syn-TFT with the T-Ox exhibits the improved retention characteristics, while having a slow programming speed, such as a low sensitivity of an output current with respect to the programming pulse (a low s_i). In contrast, the Syn-TFT without the T-Ox are more susceptible to electron trapping and de-trapping phenomena due to the absence of the T-Ox, resulting in a higher s_i and shorter τ_{ret}. With the respect to the T-Ox in the gate-insulator structure, it is suggested that the s_i and τ_{ret} are in a trade-off relation. To check this relation, the Syn-TFTs with $Al_2O_3/HfO_x/Al_2O_3$ (A/H/A) and Al_2O_3/HfO_x (A/H) stacks are fabricated. With two types of the fabricated Syn-TFTs, the synaptic and retention characteristics of are monitored, respectively. From observational results, it is found that the fabricated Syn-TFT with the A/H/A stack (i.e., with the T-Ox) is to be a relatively longer τ_{ret} and smaller s_i. In contrast, in the fabricated Syn-TFT with the A/H stack (i.e., without the T-Ox), the shorter τ_{ret} and higher s_i are also observed, respectively. In addition, to enhance the retention characteristics of the fabricated Syn-TFT with A/H stack, repeated programming and retention processes can be considered. With programming and retention cycles, electrons in the CTL can be trapped in the deeper energy state. As a result, it is found that the τ_{ret} of the Syn-TFT with A/H stack is exponentially increased as a function of the number of these cycles.

II. SYN-TFT AND RELATED THEORIES

A. DEVICE PREPARATION

The fabrication process of the Syn-TFT is as follows. Firstly, the glass wafer is prepared for the substrate. Afterward, for the deposition of a gate electrode, the patterning and thermal evaporation are performed. Here, a Cr-based photomask is used for patterning the gate electrode, which

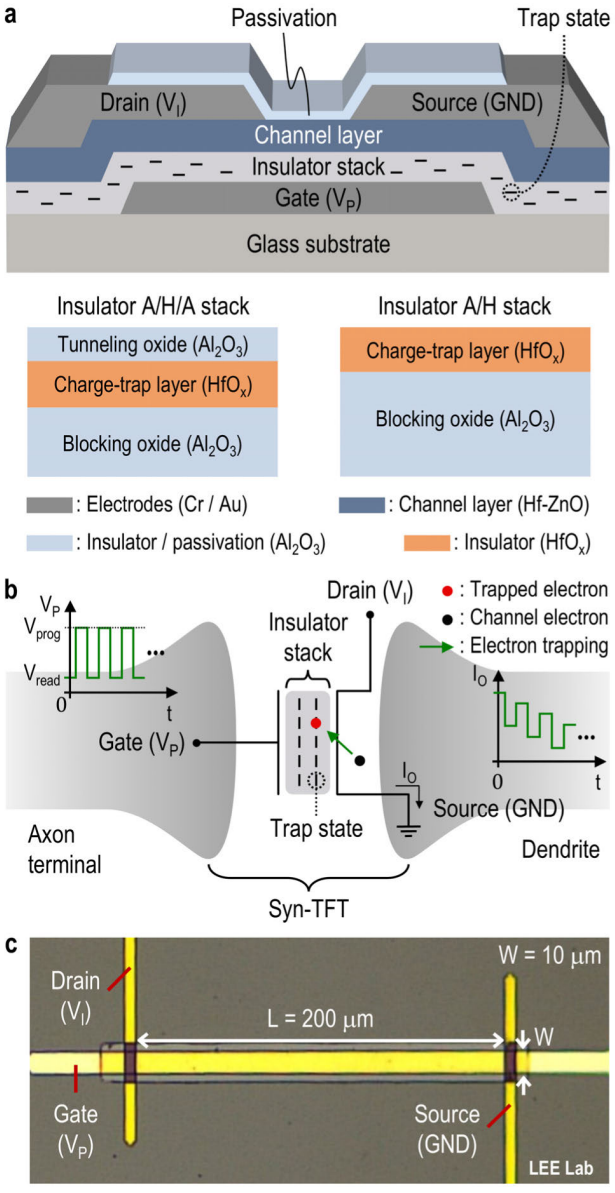

FIGURE 1. (a) Schematic cross-sectional view of the fabricated synaptic thin-film transistors (Syn-TFTs) with A/H/A and A/H stacks (i.e., with and without a tunneling oxide (T-Ox)) (b) Equivalent circuit and (c) microscopic image of the fabricated Syn-TFT.

was designed with AutoCad^{TM}. After these, the lift-off process is carried out, and the total thickness of the gate electrode is 105 nm, consisting of Cr of 5 nm and Au of 100 nm, respectively. Note that Cr is plated to enhance adhesion between the glass substrate and Au [24], [25]. Following this, it is annealed at 200 °C for 30 mins. And then, UV-Ozone treatment is carried out for 15 mins for making the surface hydrophilic [26], [27]. And then, two cases of gate oxides are deposited to the total thickness of 80 nm at 200 °C by the atomic layer deposition (ALD) with trimethyl aluminum (TMA), tetrakis hafnium (TEMAHf), and H_2O, which is used as a reactant source, respectively. Note that the

total thickness of Al_2O_3 and HfO_x is set as 65 nm and 15 nm for maintaining the overall oxide capacitance, respectively. Here, the gate insulator with the T-Ox is constituted by Al_2O_3 of 55 nm, HfO_x of 15 nm, and Al_2O_3 of 10 nm (i.e., the A/H/A stack), whereas the gate insulator without the T-Ox (i.e., A/H stack) are composed of Al_2O_3 (=65 nm) and HfO_x (=15 nm), respectively. In the following step, the thickness of the active layer (i.e., Hf-doped ZnO) is 20.2 nm with a ratio of 100:1 between ZnO (i.e., diethylzinc, DEZ) and HfO_x, which is deposited at 150 °C using ALD. Note that, to check the structural and chemical properties of the thin film, a transmission-electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) are performed, and these analyses are shown in Section S5. After the deposition of the active layer, the annealing is performed at 200 °C for 2 hours. Afterward, to define a single synaptic device, the wet etching needs to be carried out. Here, the channel layer is etched using hydrochloric acid (HCl), and buffered oxide etch (BOE) is used for the insulator etching, respectively. After that, the patterning of the source and drain electrodes is performed, and these electrodes are deposited to 105 nm (i.e., Cr of 5 nm and Au of 100 nm) by the thermal evaporation, similarly. Following this, the lift-off process is performed, and it is annealed at 200 °C for 30 mins. Finally, the channel layer of the Syn-TFT is passivated with Al_2O_3 of 50 nm with the ALD at 200 °C, and the thermal annealing is processed at 200 °C for 30 mins. Note that, the thermal annealing processes are carried out on a hot plate at atmospheric pressure to evaporate etchants or solvents and enhance the thin-film quality, maintaining a constant room temperature of approximately 25 °C.

B. BASIC OPERATING PRINCPLE

Fig. 1(a), (b) and (c) show a cross-sectional view, equivalent circuit, and micro image of the fabricated Syn-TFT, respectively. Here, the memory functionalities of the Syn-TFT are embedded in the gate insulator. This synaptic gate insulator is usually consisted of the blocking oxide, CTL, and T-Ox, such as the $Al_2O_3/HfO_x/Al_2O_3$ stack (the A/H/A stack) [9], [10]. Also, this structure without the T-Ox (e.g., the Al_2O_3/HfO_x stack (the A/H stack)) can be considered as a synaptic gate insulator, where defects are performed the role as the electron trap [19], [20]. Note that these defects are deposited with a low temperature process of the Syn-TFT. With two types of the insulator stacks (e.g., the A/H/A and A/H stacks), when positive programming pulses are applied to the gate terminal (V_P), charges (e.g., electrons) in the channel layer are continuously trapped into the gate insulator. These trapped electrons can gradually reduce an output current (I_O), which is called a synaptic depression. Note that, trapped electrons are also de-trapped toward the active layer with applying negative programming pulse train to the gate terminal, leading to the increase of the I_O (i.e., a synaptic facilitation). After the synaptic depression, the I_O is naturally recovered with applying a constant read voltage to the gate terminal (i.e., the retention process). Here, the retention characteristics of the Syn-TFT can be influenced by the presence or absence of the T-Ox in the gate insulator.

Before theoretically confirming the retention characteristics, it is essential to first check band diagrams of the Syn-TFTs, which have a structural difference of the gate-insulator stack, for the synaptic process (e.g., the synaptic depression) (see Figs. 2(a) and (b)). As can be seen, when series of positive programming pulses are applied to the V_P, electrons in the ground state of channel layer can be trapped into the trap state of the gate insulator. With trapped electrons, a negative charge density shift per area in the oxide (ΔQ_{ox}) is decreased, and this can be expressed as $\Delta Q_{ox} = q(N_{de-trap} - N_{trap})$. Here, $N_{de-trap}$ and N_{trap} are the number of de-trapped electrons to the channel per area and trapped electrons in the gate insulator per area, respectively. The decreased ΔQ_{ox} leads to the positive threshold voltage shift (ΔV_T), which is explained with the following,

$$\Delta V_T = -\frac{\Delta Q_{ox}}{C_{ox}}. \tag{1}$$

Here, the C_{ox} is a capacitance per area of the total gate-insulator stack. Note that, (1) is considered valid in typical cases, but it can be varied when considering the oxide thickness between the gate electrode and average trapped charge position (see Section S3) [28], [29]. With the positive shift of the ΔV_T, the threshold voltage (V_T) can also be increased and expressed as follows,

$$V_T = V_{T0} + \Delta V_T, \tag{2}$$

in (2), the V_{T0} is an initial value of the V_T. Here, since a low power consumption in the Syn-TFT is the essential requirement for a high intelligence of a neuromorphic computing system, the Syn-TFT can be operated in the sub-threshold region [10], [30]. So, the I_O in the sub-threshold region can be expressed as follows,

$$I_O = K_{sub}\frac{W}{L}\exp\left[\frac{q\,(V_P - V_T)}{n_t kT}\right]\left[1 - \exp\left(-\frac{qV_I}{n_c kT}\right)\right]. \tag{3}$$

As can be seen in (3), the K_{sub} is a constant for the sub-threshold regime, W is a channel width, L is a channel length, q is an elementary charge, n_t is a factor related to interface states, kT is a thermal energy, n_c is a contact ideality factor, and V_I is a fixed input voltage for the sub-threshold region. Note that, the subthreshold swing (SS) can be expressed as $ln10(kT/q)n_t$ [31]. Here, assuming the read voltage (V_{read}) is applied to the gate terminal (i.e. $V_P \approx V_{read}$), the I_O can also be rewritten based on the Taylor series with a condition of $(qV_I/n_c kT) \ll 1$ and $V_T = V_{T0} + \Delta V_T$ (see (2) and Section S4), as follows,

$$I_O = K'_{sub}\frac{W}{L}exp\left[\frac{q\,(V_{read} - V_{T0} - \Delta V_T)}{n_t kT}\right]V_I, \tag{4}$$

where the K'_{sub} is represented as $(qK_{sub})/(n_c kT)$. In addition, assuming that the initial state is no electrons into the gate insulator (i.e., $\Delta V_T = 0$), the I_O becomes a maximum value (i.e., I_O^{max}). On the other hand, the I_O arrives at the minimum

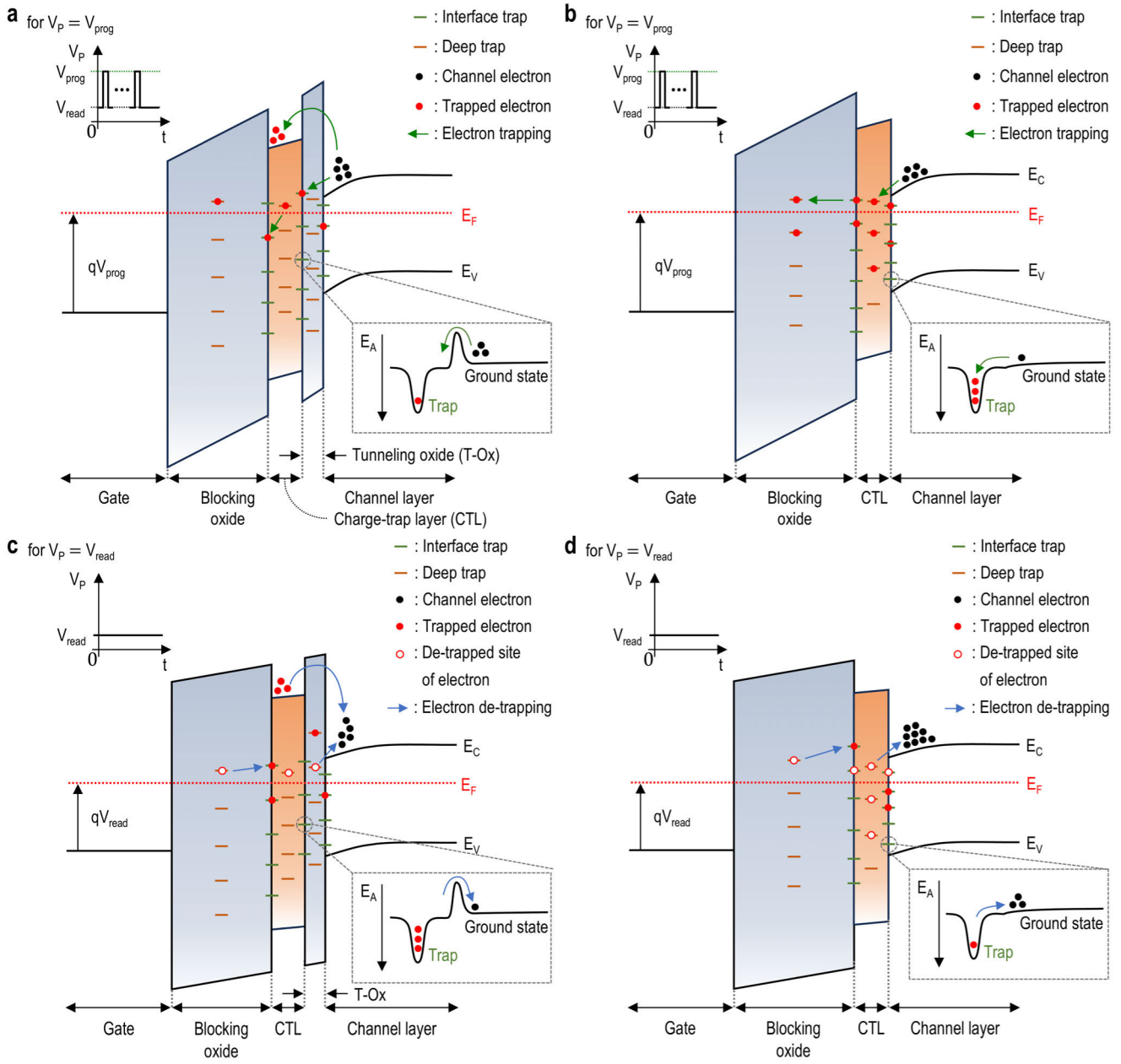

FIGURE 2. Schematic of the energy band diagram of Syn-TFTs with (a) the A/H/A and (b) A/H stacks to describe the electron trapping for applying a positive programming voltage (V_{prog}). Note that trap states in the gate insulator are composed of deep trap and interface trap states. The energy band structure of Syn-TFTs with (c) the A/H/A and (d) A/H stacks for the retention process. Here, the trapped electron can be de-trapped with a read voltage (V_{read}) in the retention process.

value (i.e., I_O^{min}) for applying multiple positive programming pulses, leading to a depressed state (i.e., $\Delta V_T = \Delta V_T^{max}$). Note that the depressed state means to the point at which the ΔV_T saturates despite a further increase of the ΔV_T. For these extreme states (i.e., the initial and depressed states), the I_O^{max} and I_O^{min} can be rewritten with (4), respectively, as follows,

$$I_O^{max} = K_{sub}^{'} \frac{W}{L} \exp\left[\frac{q\left(V_{read} - V_{T0}\right)}{n_t kT}\right] V_I, \tag{5}$$

$$I_O^{min} = K_{sub}^{'} \frac{W}{L} \exp\left[\frac{q\left(V_{read} - V_{T0} - \Delta V_T^{max}\right)}{n_t kT}\right] V_I. \tag{6}$$

After the synaptic depression (D) process, the retention (R) process can be performed. For this R process, it is expected that the retention characteristics (e.g., the τ_{ret}) can be different each other depending on the type of the gate-insulator stack. To specifically explain this, it is employed to two band diagrams for the R process. Figs. 2(c) and (d) show the electron de-trapping from a different oxide stack

for the R process, respectively. As can be seen in Fig. 2(d), the electron de-trapping can easily occur since there is no T-Ox (i.e., Al_2O_3), where the T-Ox is carried out as a high energy barrier due to a wide band gap, between the CTL (i.e., HfO_x) and the channel layer (i.e., Hf-ZnO) [21]. Note that electrons in the gate insulator can be de-trapped in the channel layer through tunneling mechanisms (e.g., a direct tunneling and trap-assisted tunneling) [32], [33]. In contrast, because the T-Ox with a wide energy band gap suppresses the electron de-trapping for the R process, de-trapped electrons from the gate insulator are reduced. With a reduction of de-trapped electrons, it is anticipated that the τ_{ret} of the Syn-TFT with the A/H/A stack (i.e., with the T-Ox) can be longer compared to that with the A/H stack (i.e., without the T-Ox) [12], [13]. Therefore, based on the theory related to the Syn-TFT, the retention characteristics of fabricated Syn-TFTs with different gate oxides needs to be observed experimentally.

III. RESULTS AND DISCUSSION

Based on the theoretical analysis associated with the Syn-TFT in the previous section, it is expected that the retention characteristics is different with respect to the gate insulator stack. To verify this, the static characteristics of fabricated Syn-TFTs needs to be checked firstly. The static characteristics of fabricated Syn-TFTs with for two cases of the gate insulator stack (i.e., the A/H/A and A/H stacks) are described in "Part A of Section III". In this "Part A of Section III", the V_{read} is commonly determined as the same I_O for two cases of gate oxides. To specifically compare for each case with the selected V_{read}, the pulsed characteristics of the A/H/A and A/H devices need to be monitored during the synaptic D and R processes, respectively. These detailed processes are analyzed in "Part B of Section III", respectively. Furthermore, as another approach to improve the retention characteristics (e.g., the τ_{ret}), repeated D and R cycles can be implemented in the fabricated Syn-TFTs with the A/H/A and A/H stacks, and this is given in the following "Part C of Section III". Here, the experimental framework is performed with a standard semiconductor analyzer, called Keithley^{TM} 4200A.

A. STATIC CHARACTERISTICS OF FABRICATED SYN-TFTS

To verify the retention characteristics of fabricated Syn-TFTs, the static characteristics of fabricated Syn- TFTs needs to be monitored. Figs. 3(a) and (b) show the static characteristics of fabricated Syn-TFTs with the A/H/A and A/H stacks at two extreme states (i.e., the initial and depressed states) for $V_I = 0.1$ V. As can be seen, the V_{read} is commonly determined as 1 V with almost the same I_O^{max} (≈ 5 pA) in each graph. Note that, the V_{read} is set within the sub-threshold region, considering the synaptic and retention characteristics, and the measured V_{T0} is 2 V for each case. With the V_{read}, the I_O is reduced by 1-order for applying positive programming pulses continuously, resulting in approximately $I_O^{min} = 0.5$ pA. (see Section S6) This is because the V_T is increased by

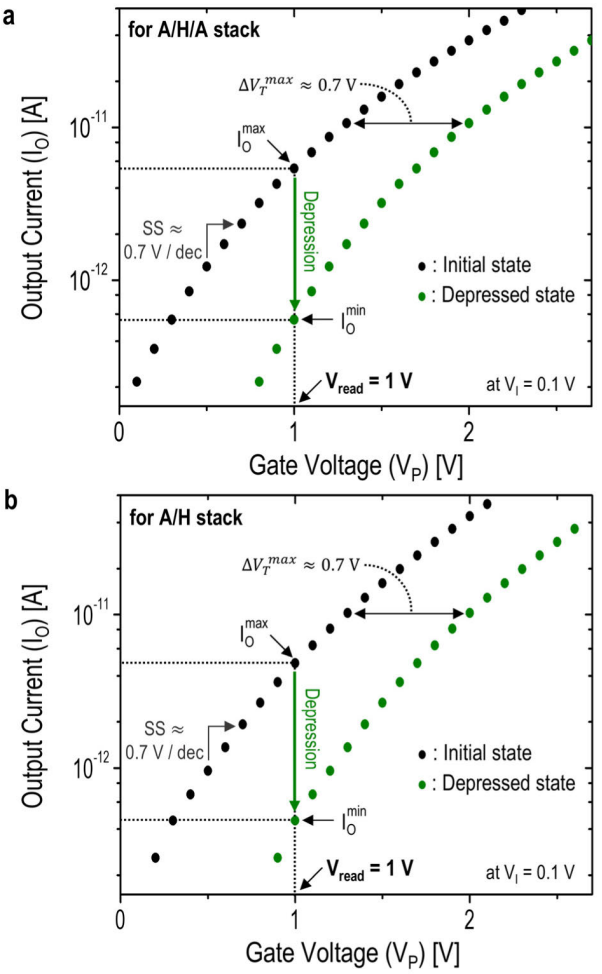

FIGURE 3. Measured transfer characteristics of fabricated Syn-TFTs with (a) the A/H/A and (b) A/H stacks for $V_I = 0.1$ V. Here, after applying multiple positive programming pulses, the initial state (i.e., I_O=I_O^{max}) arrives at the depressed state (i.e., I_O=I_O^{min}) with a V_{read}. Here, the V_{read} is commonly set as same I_O^{max} (i.e., $I_O^{max} = 10$ pA) for two cases. Note that the level of I_O^{max} is decreased by 1-order for a fair observation of the retention characteristics.

the electron trapping, and it leads to the decrease of the I_O, as mentioned earlier. Note that the subthreshold swing (SS) and ΔV_T^{max} are measured as 0.7 V / dec and 0.7 V, respectively. With the reduced I_O, the initial state arrives at the depressed state. For a fixed V_{read}, after the depressed state, because the retention characteristics with respect to two cases are expected to be different each other, both detailed synaptic D and R processes are shown in the following section.

B. PULSED CHARACTERISTICS OF FABRICATED SYN-TFTS

With the determined V_{read} in the previous section, since the retention characteristics of fabricated Syn-TFTs are expected to be different with respect to gate oxides, it needs to be observed. For checking this, the synaptic processes (e.g., the synaptic D process) are monitored firstly. Figs. 4 (a) and (b) show the pulse specification for the D process and constant

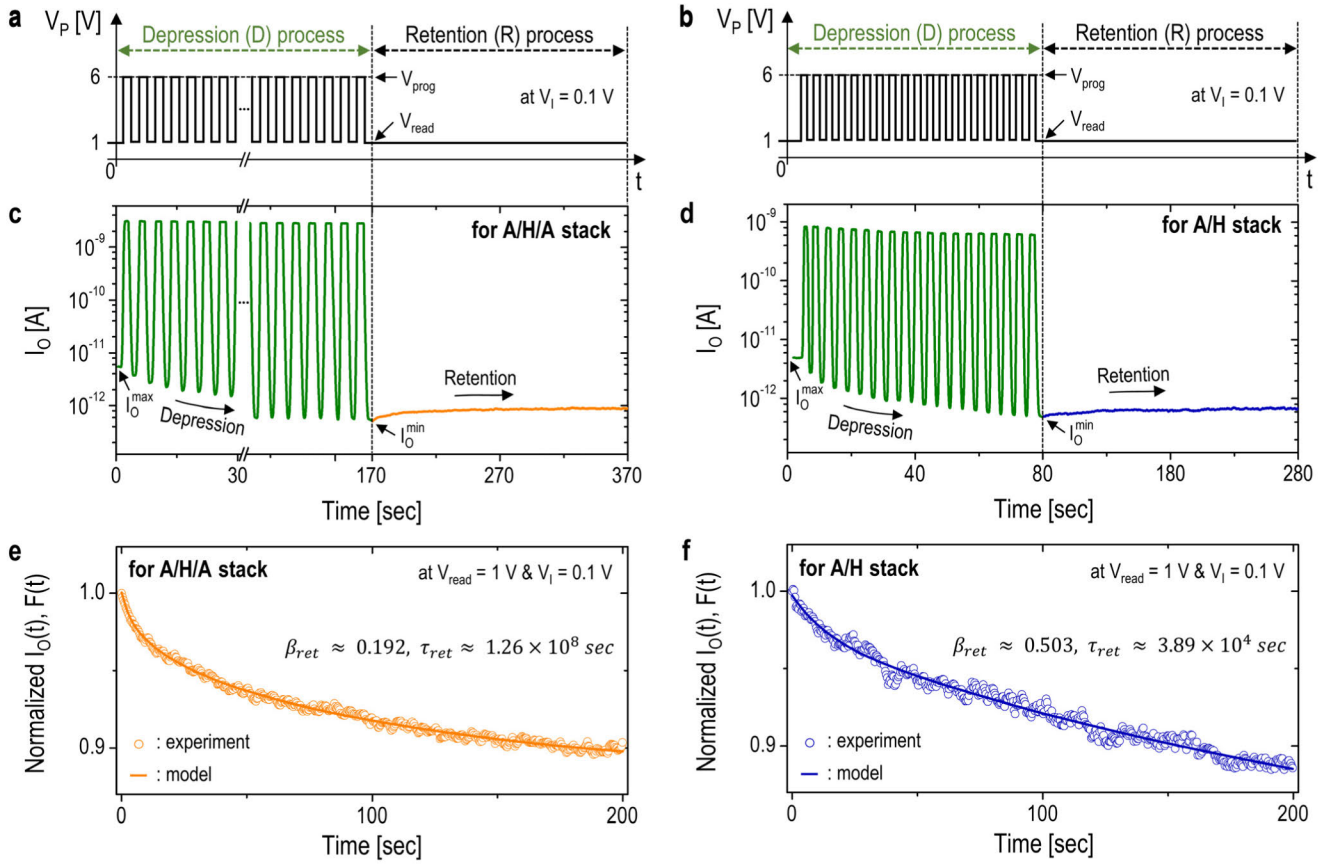

FIGURE 4. Waveform of positive programming pulses for the synaptic D process and the constant bias voltage (i.e.,V_{read}) for the R process of fabricated Syn-TFTs with (a) the A/H/A and (b) A/H stacks for $V_I = 0.1$ V. Here, the V_{read} related to the I_O^{max} is determined as 1 V. The changed I_O of (c) the A/H/A and (d) A/H devices for the synaptic D and R processes with the V_{read}, respectively. Normalized stretched exponential function ($\overline{F(t)}$) and output current ($\overline{I_O(t)}$) of fabricated Syn-TFTs with (e) the A/H/A and (f) A/H stacks for the R process, respectively. Note that, for the fair comparison of the τ_{ret}, the R process is observed for 200 seconds.

V_{read} for checking the R process. As can be seen, the V_{prog} is commonly as 6 V for the synaptic D process. In addition, the pulse width and duty cycle for two cases of the gate insulator stacks are commonly set to 2 sec and 50 %, respectively. Here, to reduce the I_O by the 1-order, for case of the A/H/A stack, the number of cycles is 42 whereas, for the case of A/H stack, the number of cycles is 19, respectively (see Figs. 4 (a) and (b)).

Based on these wave conditions of programming pulses, Figs. 4 (c) and (d) show each changed I_O for two cases of the gate insulator stack during the synaptic D and R processes, respectively. Note that, to fairly compare the retention characteristics (i.e., the τ_{ret}) of fabricated Syn-TFTs for each case, the I_O is decreased by only 1-order. It is shown that the overall trend of the I_O is gradually decreased with applying a series of positive programming pulses to the gate terminal (i.e., the synaptic Depression), regardless of the gate insulator stack. This is because the electron trapping leads to the increase of the ΔV_T, which is explained with (1) and (4). Here, it is also found that, for decreasing the I_O by 1-order, more programming pulses are required for the A/H/A device (i.e., with the T-Ox) than the A/H device (i.e., without the T-Ox). It is because the T-Ox, which is carried out as a high energy barrier for channel electrons, suppresses the electron trapping during the Depression process. To specifically explain this phenomenon, a sensitivity of the I_O variation dependent on the number of programming pulses (s_i) can be employed, as follows [34],

$$s_i = \frac{\Delta I_O}{n_p}. \tag{7}$$

where the n_p is the number of programming pulses for the decreasing I_O and ΔI_O is a difference of the I_O between before and after the synaptic Depression (i.e., $I_O^{max} - I_O^{min}$). As mentioned earlier, during the D process, the $I_O$of the Syn-TFT is reduced by increasing the ΔV_T (see (4)). This is because the ΔQ_{ox} is decreased by the electron trapping in the gate oxides (i.e., the increase of the N_{trap}), in which the measured C_{ox} is equal value at approximately 15 μF / cm^2 for two cases of the gate insulator (see Section S3). Here, for the synaptic Depression process, the N_{trap} is the same because the ΔI_O of fabricated Syn-TFTs with two cases of gate insulator

is commonly 4.5 pA. On the other hand, the n_p required to decrease the I_O varies depending on the gate insulator. Therefore, the s_i can be determined by the n_p, where s_i of fabricated Syn-TFT with the A/H stack is higher compared to that with the A/H/A stack. Consequently, the measured s_i of the A/H/A and A/H devices are 0.107 and 0.237 pA, respectively. Note that, a high s_i can imply more N_{trap} per the programming pulse, and applying a higher programming height can be considered as another approach to a faster programming speed [35], [36].

After the synaptic D process, the I_O is naturally recovered due to the electron de-trapping for applying a V_{read} (see Figs. 4(c) and (d)). For a fair comparison of this natural recovery, the I_O for the R process with two cases of gate oxides is normalized with the following equation,

$$\overline{I_O(t)} = \frac{I_O^{max} - I_O(t)}{I_O^{max} - I_O^{min}}. \tag{8}$$

Here, the I_O^{max} and I_O^{min} for each case are 5 pA and 0.5 pA, respectively. And the $I_O(t)$ is the measured for the R process. From experimental results, to extract and specifically compare the τ_{ret} of fabricated Syn-TFTs, the stretched exponential function ($F(t)$) can be applied [23], [37]. The general form of the F(t) is presented as follows,

$$F(t) = F_0 \exp\left(-\left(\frac{t}{\tau_{ret}}\right)^{\beta_{ret}}\right), \tag{9}$$

where the F_0 is the initial value at t = 0, τ_{ret} is a retention time, and β_{ret} is a stretched exponent. Note that, the β_{ret} value reflects the degree of the saturation in the modeled function, and a lower β_{ret} value indicates a higher level of the saturation. Based on (9), the normalized $F(t)$ (i.e., $F(t)/F_0$) can be defined as [23] and [37],

$$\overline{F(t)} = \exp\left(-\left(\frac{t}{\tau_{ret}}\right)^{\beta_{ret}}\right). \tag{10}$$

For applying (8) and (10), Figs. 4(e) and (f) show the $\overline{I_O(t)}$ and $\overline{F(t)}$ for two cases of gate insulator during the retention process with the V_{read}, and also indicate a good agreement between the experiment and model results (i.e., the $\overline{I_O(t)}$ and $\overline{F(t)}$). As shown in Figs. 4(e) and (f), the τ_{ret} of the Syn-TFT with the A/H/A stack is longer than that with the A/H stack (see (10)). As a result, it is observed that the τ_{ret} of the A/H/A and A/H devices are 1.26×10^8 seconds and 3.89×10^4 seconds, respectively. It is because the T-Ox can be performed as a role of a high energy barrier for trapped electrons in the gate oxides. And this τ_{ret} as a measure of the retention characteristics of the synaptic device than 10^4 times can be considered as its improvement, but it doesn't mean that the retention characteristics is enhanced by 10^4 times. Also, it is found that the I_O of the A/H/A device is faster recovered compared to the A/H device for the initial R process. This is because of the rapid de-trapping of the electrons at the interface between the T-Ox and channel layer, suggesting a higher electron density at the interface. With this respect to the fast retention loss for the early R process, the β_{ret} values are different, and the extracted τ_{ret} can be considered valid [6], [38]. Based on these results, it is found that the T-Ox can enhance the retention characteristics (e.g., the τ_{ret}) whereas it leads to the reduction of the s_i, thus meaning the trade-off relation between the τ_{ret} and s_i depending on the presence of the T-Ox in the gate insulator stack. Also, this trade-off relation needs to be checked at different bias voltages, so the weight-updates and retention characteristics of two fabricated Syn-TFTs with respect to a high V_{read} are shown in Section S1 and S2. Note that the endurance characteristics of the devices related to the repeated cycles are shown in Section S7. In addition, as another approach to enhance the retention characteristics of the A/H Syn-TFT with a high s_i, repeated D and R processes can be considered. Therefore, the pulsed characteristics with respect to the repeated D and R processes are shown in the follow sections.

C. PULSED CHARACTERISTICS WITH REPEATED D AND R PROCESSES

To investigate the impact of the repeated D and R processes on the retention characteristics, 4 sets of the D and R processes are sequentially applied to the gate terminal of the A/H Syn-TFT. Fig. 5(a) shows the measured I_O as a function of time for the D and R processes. Here, in the first process, the initial I_O of 5 pA (i.e., the I_O^{max}) reaches the I_O^{min} ($\approx$ 0.5pA) during D1 process, whereas the I_O^{min} is increased to the recovered the I_O (I_O^{rec}) of 0.7 pA for R1 process. Note that, the I_O^{rec} is set to 0.7 pA, which corresponds to the saturation level rather than the I_O^{max} of 5 pA, considering the limitations of the measurement equipment. Once the I_O is decreased the I_O^{rec}, the D2 and R2 stage is processed until the I_O arrives at the I_O^{rec}. Note that the I_O^{rec} level can be considered sufficient for observing the retention characteristics. As can be seen, after the D1 and R1 processes, the I_O quickly approaches to the I_O^{min}. On the other hand, the I_O is slowly recovered for the R2 process. This can be explained that electrons at the interface trap states are trapped into the deep trap states in the CTL. In other words, some electrons are de-trapped toward the channel nearby the CTL interface during the R1, and these electrons are trapped into deeper states of the gate insulator for the D2. With trapped electron in the deep state, it is more difficult to occur the electron de-trapping phenomena during R2 process than R1 process. In this respect, electrons trapped in deeper states require higher activation energy to escape. This suggests that the synaptic stimulation is accumulated by the repeated D and R processes, resulting in the improvement of the retention characteristics [23]. To verify the accumulated effects, the τ_{ret} for each R process is extracted with the $\overline{F(t)}$. Figs. 5 (b), (c), (d), and (e) show the plot of the $\overline{I_O(t)}$ and $\overline{F(t)}$ as a function of the time. As can be seen, the time required to reach the same level of the $\overline{I_O(t)}$ is observed to be 145 seconds for R1, 309 seconds for R2, 410 seconds for R3, and 504 seconds for R4, respectively. This is because electrons are more trapped

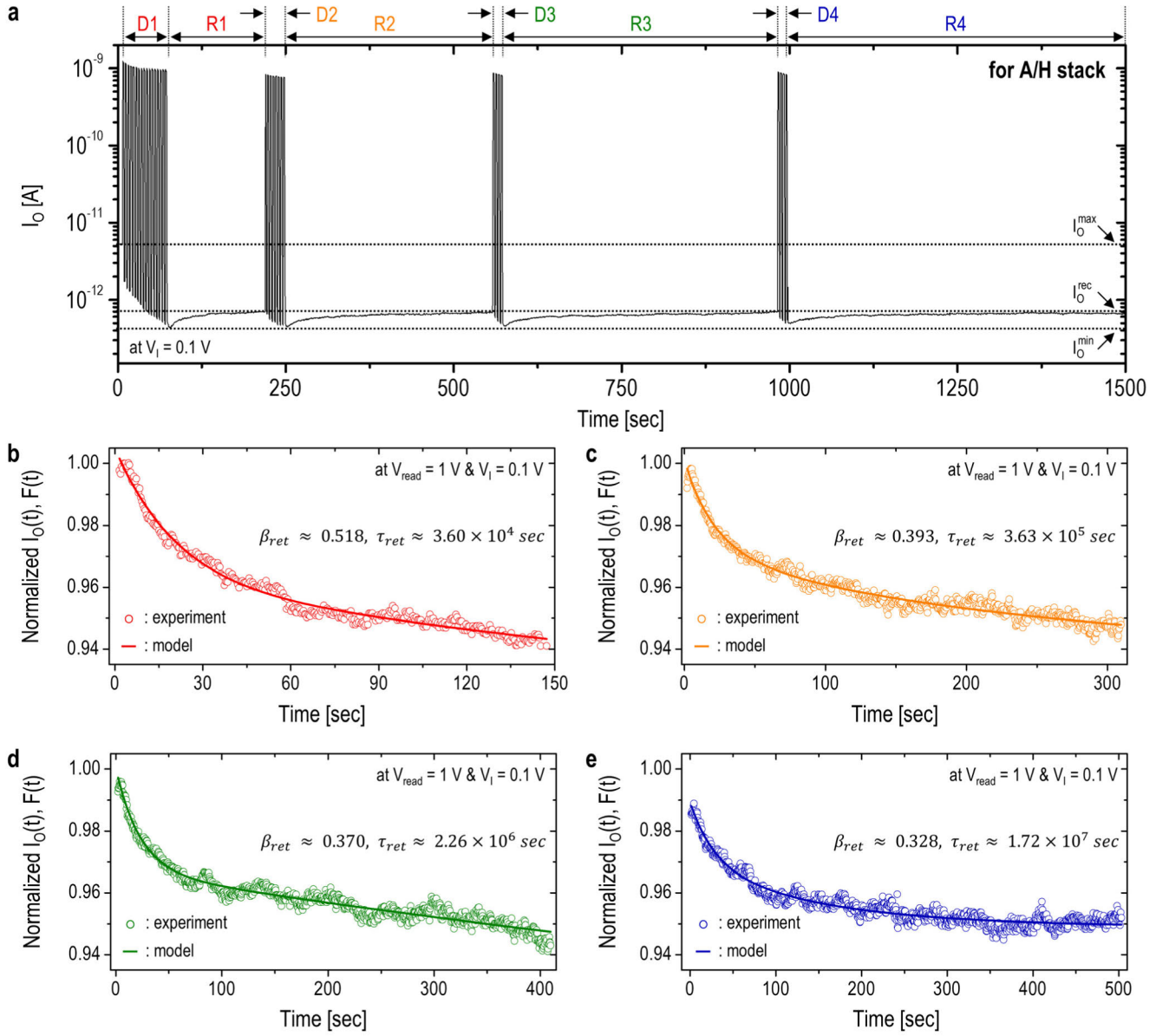

FIGURE 5. (a) Measured I_O of the A/H Syn-TFT with the repeated D and R processes as a function of time. Here, the repeated D and R processes are 4 cycles. Normalized stretched exponential function ($\overline{F(t)}$) and output current ($\overline{I_O(t)}$) of fabricated Syn-TFTs for (b) D1 and R1, (c) D2 and R2, (d) D3 and R3, and (e) D4 and R4 processes, respectively. Note that, for the fair comparison of the τ_{ret}, the I_O is decreased from the I_O^{max} to the I_O^{min} during each D process, and the I_O^{min} is increased to the same level of the recovered I_O (I_O^{rec}) during each R process.

into deeper states as the D and R processes are repeated. With these experiments, the data analyses are performed, and the proposed models also give a good agreement. From the prosed models, it is found that the extracted τ_{ret} for R1, R2, R3, and R4 are 3.60×10^4seconds, 3.63×10^5seconds, 2.26×10^6seconds, and 1.72×10^7seconds, respectively. These results are summarized in Table 1. Also, it is observed that these values are increased exponentially as repeating the D and R process.

To confirm the exponential increase of the τ_{ret}, Fig. 6 show the plot of the τ_{ret} depending on the number of the D and R processes on a log-scale. As illustrated in Fig. 6, The linear extrapolation suggests that the estimated τ_{ret} can be substantially extended to about 10^8 seconds after 5 D and R processes. Note that further can be limited by the capacity of deeper states. Additionally, multiple repeated processes can result in either a high gate-leakage current or insulator breakdown. Despite these potential drawbacks, the Syn-TFT with the A/H stack can still be used for a long-term device if it has sufficient deep trap states. Consequently, these results suggest that repeated D and R processes lead to an exponential increase of the τ_{ret}.

TABLE 1. Summary of the extracted τ_{ret} of the fabricated Syn-TFT with the A/H stack.

Parameters	The Syn-TFT with the A/H stack			
D-R process	1	2	3	4
β_{ret}	0.518	0.393	0.370	0.328
τ_{ret} [sec]	3.60×10^4	3.63×10^5	2.26×10^6	1.72×10^7

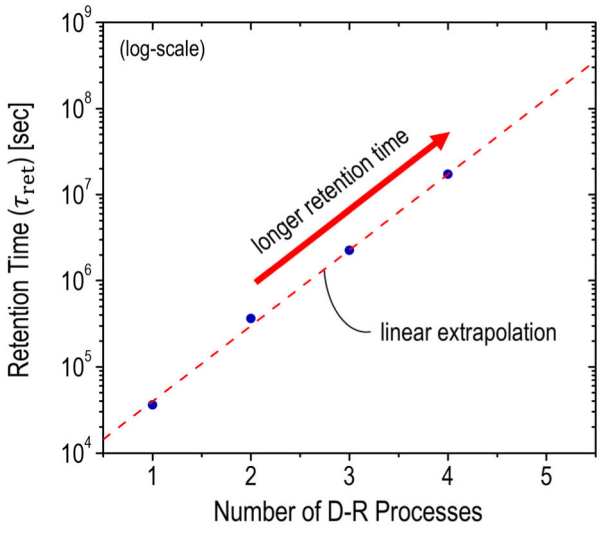

FIGURE 6. A plot of the τ_{ret} of the A/H device as a function of the number of the D and R processes on a log-scale.

IV. CONCLUSION

In this article, the experimental framework on a high-κ gate insulator stack-dependent retention properties of Syn-TFTs with a Hf-ZnO active layer has been presented. In Syn-TFTs, programming speed and retention characteristics are varied depending on the presence of the T-Ox in the gate insulator. To verify this, the static and pulsed characteristics of the fabricated Syn-TFT with the A/H/A and A/H stacks are observed, respectively. As experimental results, it has been found that the sensitivity of the Syn-TFT with the A/H stack is higher than that with the A/H/A stack whereas the extracted retention time of the A/H/A device is longer compared to the A/H device. This is because the T-Ox suppresses both the electron trapping and de-trapping for the synaptic depression and retention processes. In addition, to enhance the retention time of the A/H device, the repeated depression and retention processes can be applied to the gate terminal. It has also been observed that the extracted retention time is exponentially increased depending on the number of repeated processes. This is due to more trapped electrons into deep states as repeating processes. From these results, the T-Ox can lead to the improvement of the synaptic characteristics (e.g., the retention characteristics and robustness) of Syn-TFTs whereas it also results in the reduced programming speed for the synaptic process. This superior retention characteristics and robustness of the A/H/A Syn-TFT lead to a high memory capability and stability, thus improving the system's emulation of biological neural networks. In contrast, the programming speed of Syn-TFTs with the A/H stack is high for the synaptic process. Based on a high sensitivity, Syn-TFTs with the A/H stack are suitable as devices in neuromorphic systems that require fast processing speeds. Furthermore, the retention characteristics of the A/H device can be improved by repeating the depression and retention processes. Therefore, it is important to choose the appropriate gate insulator stack depending on the application because Syn-TFTs without or with the T-Ox can be used for excellent programming speed or long-term memory capabilities in neuromorphic system.

AUTHOR CONTRIBUTION

Gyoungyeop Do performed the fabrication process with Kunhee Tae, Nayeoung Lee, and Seokhyun Byun. Gyoungyeop Do performed the measurement and characterization of the fabricated devices with Danyoung Cha, Kunhee Tae, and Jeongseok Pi. Gyoungyeop Do did the synaptic analysis with Danyoung Cha and Jeongseok Pi. Gyoungyeop Do drew all figures. All the authors discussed together and contributed to writing the manuscript.

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(Gyoungyeop Do and Danyoung Cha contributed equally to this work.)

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