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RESEARCH ARTICLE

An Isolated DC–DC Converter for 800 V Electric Vehicle With Wide Soft-Switching Range and Low Voltage Stress on Power Switches

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ABSTRACT This paper proposes an isolated DC–DC converter to cope with 800 V input voltage and 48 V output voltage conditions of the auxiliary power module in the next generation 800 V electric vehicles. On the primary side, a split-capacitor structure and a series capacitor are utilized while on the secondary side, a current doubler rectifier is designed, which repeats a part of the primary structure. Compared with existing isolated converters, the proposed converter has attractive characteristics: 1) a double step-down ratio; 2) the voltage stress on all primary switches and primary transformer are reduced to half of the input voltage; 3) the power switches have soft-switching capability by ZVS characteristic in the primary side, ZV-ZCS in secondary side; 4) the soft-switching range is wide, which maintained even at light-load conditions. 5) allow reuse conventional devices of 400 V system in the updated 800 V system. These characteristics are achieved with a simple control strategy by the pulse width modulation method for switches on the primary side and only repeating primary gating signals for switches on the secondary side. In this paper, the operation and performance of the proposed converter are presented. Besides, an experiment at 800 V input, 48 V–1.2 kW output is also completed to validate the operation and effectiveness of the proposed converter.

INDEX TERMS Current doubler rectifier, high step-down, isolated dc–dc converter, phase-shift full-bridge, soft-switching.

I. INTRODUCTION

For electric vehicle (EV) applications, many studies have pointed out that the 800 V DC bus has some advantages compared to the conventional 400 V DC bus such as faster charging time, smaller motor and wiring sizes, and lower losses [1], [2], [3]. Therefore, recently there have been some vehicles designed with 800 V DC bus and that trend is considered as a promising evolvement direction [3], [4]. However, high DC bus voltage also creates new challenges to design and optimize the power converters, including DC-DC converters [2], [5], [6].

This paper considers the situation of the auxiliary power module in EV, which is an isolated high step-down (IHSTD) DC-DC converter. The function of this module is to connect the high voltage (HV) traction battery, which is toward 800 V [1], [2], [3], [4] with low voltage (LV) DC auxiliary load, and low voltage battery, which is toward 48 V [7], [8], [9]. Due to the safety requirement, the LV side should be isolated from the HV side to prevent leakage current and shock, as the LV battery is grounded to the chassis [2]. Normally, the Phase-Shift Full-Bridge (PSFB) converter

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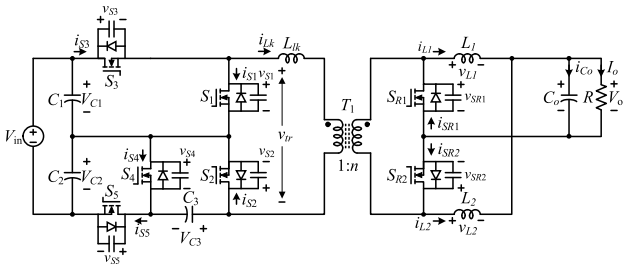

FIGURE 1. Schematic of the proposed converter.

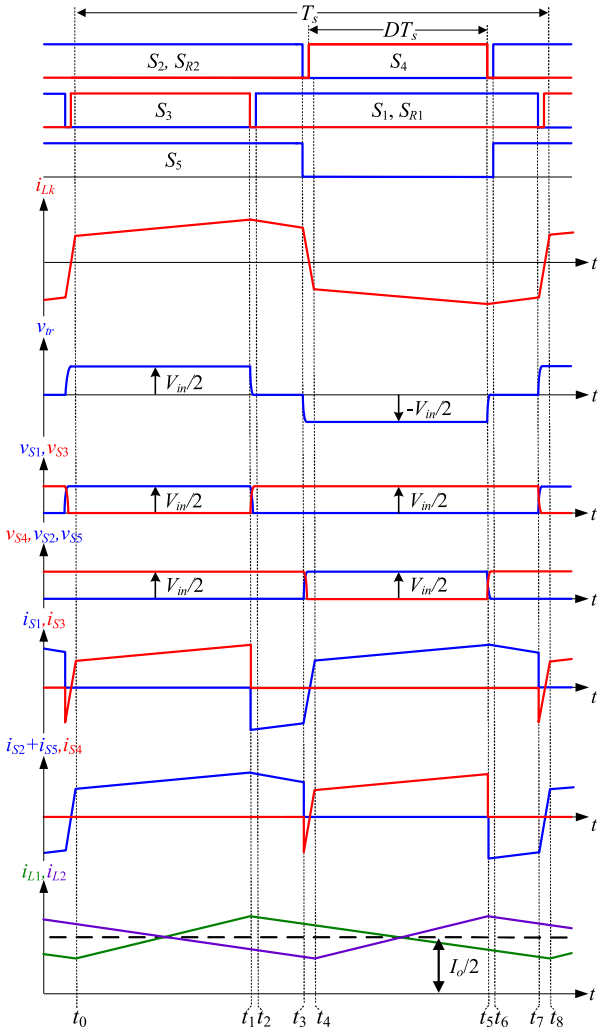

FIGURE 2. Operation waveforms of the proposed converter.

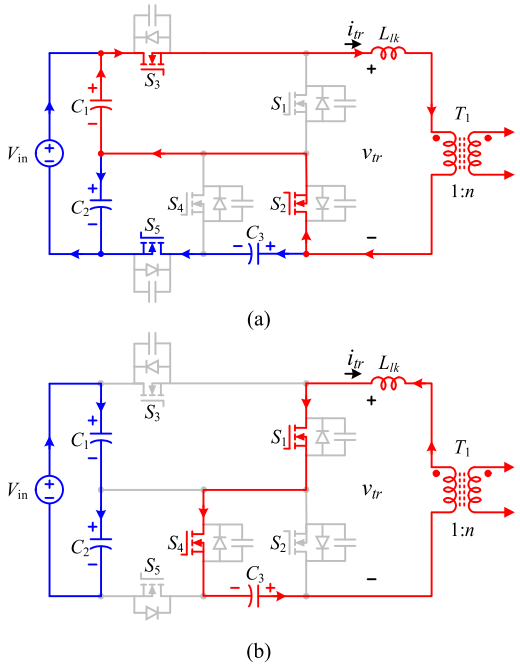

FIGURE 3. Operation of the primary capacitors in the proposed converter: (a) operation in the interval $[t_0 - t_1]$, (b) operation in the interval $[t_4 - t_5]$.

[10], [11], the Dual Active Bridge (DAB) converter [12], [13], and the LLC resonant converter [14], [15], are the conventional selections of this IHSTD converter. However, when considering 800 V input voltage, many problems need to be overcome. Indeed, with conventional IHSTD converters, under 800 V DC bus, the 1200 V switches are required, which is less competitive compared to the general 650 V rated switches in the conventional 400 V DC bus. It increases the cost, and the on-resistance, while reducing the system reliability. On the other hand, a high turn ratio transformer is inevitable because the conventional IHSTD converters achieve high buck gain only by adjusting the transformer turn ratio and the primary transformer voltage is high, which is equal to the input voltage. Therefore, when transferring to 800 V EV, it is necessary to invest in new primary switches and re-design the transformer structure [2], [3], [4].

Besides, each conventional IHSTD converter has original limitations, which should also be considered. The DAB converter is capable of bidirectional power transmission, but it brings concerns about high power loss and the high cost of four secondary switches. With the APM module, the bidirectional function is not mandatory, therefore, the PSFB converter is a better solution with a lower cost. However, with both the PSFB and DAB converters, the narrow soft-switching range is a practical problem because these converters will lose the ZVS characteristic at low load currents or when the voltage of the transformer mismatches substantially from the nominal transformer ratio [16], [17], [18]. The ZVS characteristic is an important criterion with converters in EV, which is not only related to the efficiency of converter but also influences the electromagnetic interference (EMI) level and electromagnetic compatibility (EMC) of converter with other parts in the system. The ZVS for the conventional PSFB and DAB converters is more difficult in the context of 800 V EV, which requires a double voltage transition from 400 V to 800 V in the turn-on and turn-off switching points with only half leakage inductor current compared to the conventional 400 V EV. Therefore, the ZVS range of 800 V-based PSFB and DAB converters is narrower

than 400 V-based PSFB and DAB converters. To ensure a normal ZVS range, the leakage inductor must be designed with a high value, which increases the circulating current, and output voltage ringing level, and limits the power transfer, and duty cycle range of these converters. On the other hand, the LLC converter exhibits difficulty in system optimization as the switching frequency is the control signal variable of the system but also determines the size of magnetic elements, and losses of the system. To cope with the variation in the state of batteries, the frequency variation range needs wide, but a high switching frequency leads to increasing the switching loss, and core loss while a low switching frequency results in a big size of magnetic elements, high current stress, and high conduction losses [19], [20]. Therefore, under high buck gain and high input voltage requirements, the conventional PSFB, and DAB converter have disadvantages including a low step-down ratio, high primary switches voltage stress, high primary transformer voltage rating, and narrow ZVS range. While, with LLC resonant converter, the aspects of frequency modulation control, and optimization for magnetic elements make it difficult both for hardware and software development.

To solve the above issues, some recent researchers have approached these issues from a new perspective, which uses capacitors as the switching energy elements to achieve prominent characteristics [17], [18], [21], [22], [23], [24], [25], [26], [27], [28], [29]. In [17], [18], [21] the capacitors are arranged in parallel with half-bridges in the stacked structure to achieve a high to very high step-down ratio but the number of switches is large [17], [18] or only operating hard-switching [21]. In [22], [23], and [24], the split-capacitor structure is fully utilized to improve the step-down ratio while keeping ZVS characteristics. However, there is a switch of these converters working with a high-stress voltage of V_{in}, which becomes very serious when considering the 800 V input situation and makes an asymmetric between the selected devices. In [25] and [26], the flying-capacitors-based three-level converters are presented, which creates a double step-down ratio with soft-switching characteristics, but the diodes on the primary side are forwarded in free-wheeling modes cause potential issues of high conduction loss. In [27], [28], and [29], the series capacitor is introduced on the primary side, which decreases the stress of some primary switches. However, the converter in [27] only operates hard-switching and has a nonlinear voltage gain. The converters in [28] and [29] can achieve soft-switching, but same as [22], there are primary switches that tolerates a V_{in} voltage stress. Moreover, the diode bridge rectifier topology of the converter in [28] has the disadvantage of high losses.

Given this context, there is a realistic demand to derive a converter with low voltage stress on all switching devices, keep a low transformer turn ratio, a wide soft-switching range, and try to keep as many conventional devices in the conventional 400 V system as possible. This paper proposes a new capacitor-based IHSTD converter, which meets the above criteria. The remaining content of this manuscript is organized as follows: Section II presents the main structure and principle operation of the proposed converter. Section III analyzes the characteristics of the proposed converter. Section IV provides some design considerations and compares the proposed converter with the conventional IHSTD converters and other capacitor-based IHSTD converters. Finally, Sections V and VI give the experimental and simulation results before the conclusion.

II. THE PROPOSED TOPOLOGY DESCRIPTION AND PRINCIPLE OPERATION OF THE PROPOSED CONVERTER

As shown in Fig. 1, the proposed converter consists of five switches and three capacitors on the primary side and a current doubler rectifier structure including two switches and two inductors on the secondary side. The switching network on the primary side is designed to have a double step-down property through a split-capacitor structure C_1-C_2, which is near the source, and a series capacitor C_3 operations as a voltage source, which series with the primary winding. Therefore, about the topology, the proposed converter is derived based on both concepts of split-capacitor structure as in [22], [23], and [24] and series capacitor structure as in [27], [28], and [29].

The operation waveforms of the proposed converter in a switching period are presented in Fig. 2, where a switching period T_s is divided into eight modes. The key idea here is to apply the charging and discharging process of primary capacitors to obtain the step-down feature naturally. To explain this idea, Fig. 3 gives the equivalent circuits in interval [t_0-t_1] and [t_4-t_5], where capacitor energy is transferred to the load. As can be seen from Fig. 3(a), in the positive half-period of the primary transformer current, capacitor C_1 discharges the energy to the load, and its voltage is reduced to $V_{in}/2$ through the split-capacitor structure C_1-C_2. While in the remaining negative half-period of primary current, as Fig. 3(b), capacitor C_3 with a nominal voltage of $V_{in}/2$ discharges energy to the load. Therefore, the converter is supplied by a source voltage rating of $V_{in}/2$ rather than V_{in} as the conventional IHSTD converters. By that, the proposed converter can achieve comparative advantages compared to the existing IHSTD converters, which will be analyzed in detail in Section III.

In terms of control modulation method, the proposed converter uses the pulse width modulation based on the duty cycle of switches S_3 and S_4. The control signal of switch S_4 is shifted 180° compared to the control signal of switch S_3. While, the control signals of switches S_1 and S_2 are complemented with that of switches S_3 and S_4, and the control signals of switches S_{R1}, and S_{R2}, S_5 simply repeat the control signals of switches S_1 and S_2.

Before analyzing the operation of the proposed converter in detail, without losing the generality, some assumptions are given below:

1) All of the switches are MOSFET switches, which are modeled by both the switching elements and parasitic

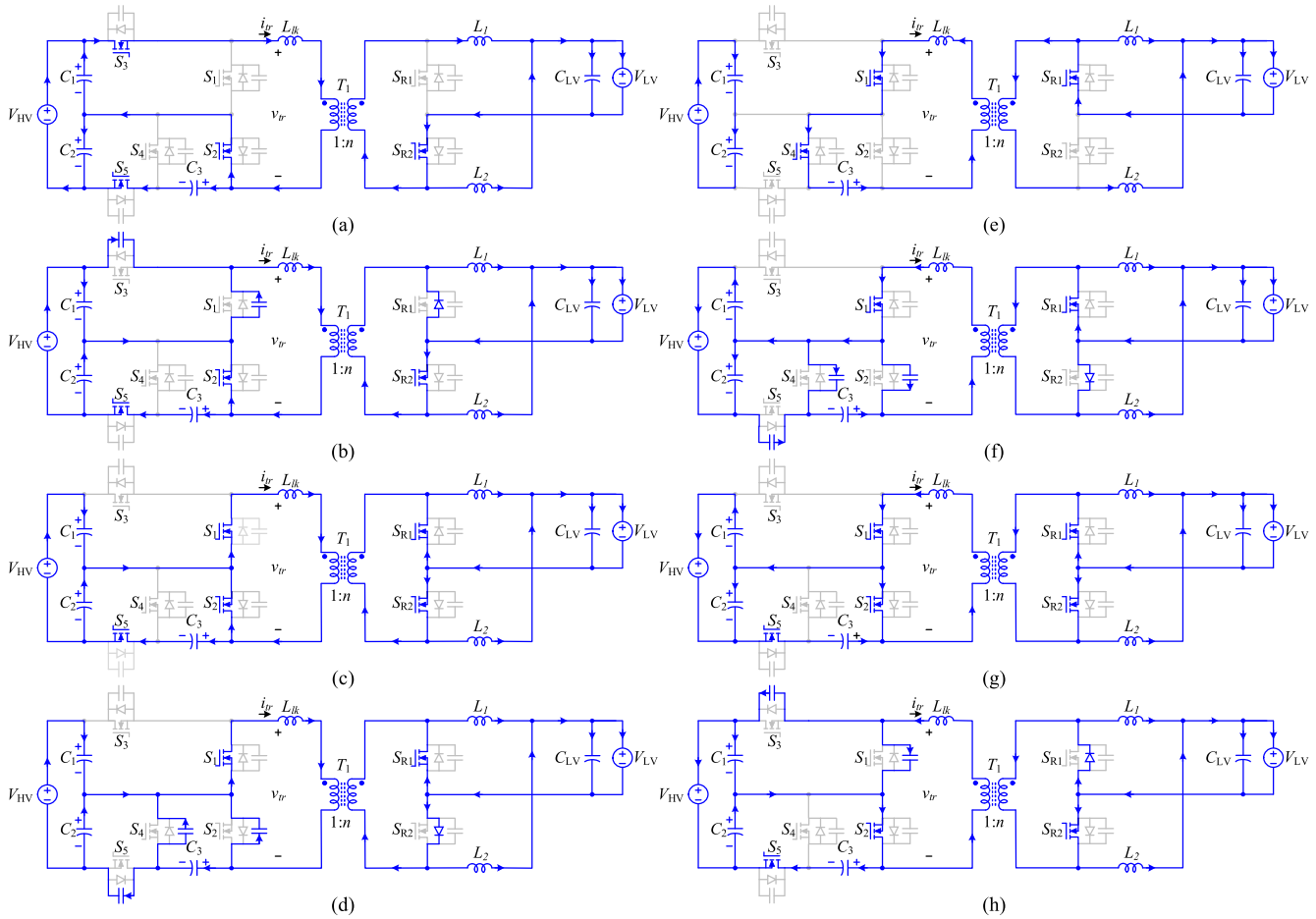

FIGURE 4. Sub-mode equivalent circuits of the proposed converter. (a) Mode 1 [$t_0 - t_1$], (b) Mode 2 [$t_1 - t_2$], (c) Mode 3 [$t_2 - t_3$], (d) Mode 4 [$t_3 - t_4$], (e) Mode 5 [$t_4 - t_5$], (f) Mode 6 [$t_5 - t_6$], (g) Mode 7 [$t_6 - t_7$], (h) Mode 8 [$t_7 - t_8$].

elements including body diode and output capacitors. The output capacitors of primary MOSFET switches are the same with a value of C_{oss}.

2) The capacitors C_1, C_2, and C_3 are large enough so that their voltages are stable under high-frequency conditions. Therefore, these capacitors work as voltage sources.
3) The deadtime intervals introduced in gating signals of switches are large enough to complete the switching transition of switches, but still very small compared to the duration of a switching period.

With the above assumptions, the operation modes of the proposed converter in modes can be briefly described below with the corresponding equivalent circuit in each mode drawn in Fig. 4:

Mode 1 [$t_0 - t_1$] – Fig. 4(a) – *Power mode*: In this mode, the energy in the input side is transferred to the load through the discharging energy of capacitor C_1. The primary voltage of the transformer is equal to the voltage of capacitor C_1, which is half of the input voltage. Simultaneously, capacitors C_2 and C_3 are charged by the input energy. The current flow in this mode is depicted in Fig. 4(a). On the secondary side, inductor L_1 stores energy from primary side while inductor L_2 transfers energy to the load. There is no current passing through switch S_{R1}, and its drain-source voltage is equal to 0 because the current only flows through the low-impedance paths. Besides, from the figure, the voltage of the primary transformer, capacitors, and voltage stress on off-switches S_1 and S_4 are as follows:

$$v_{tr} = V_{C1} = \frac{V_{in}}{2} \tag{1}$$

$$v_{S1} = V_{C1} = \frac{V_{in}}{2} \tag{2}$$

$$v_{S4} = V_{C2} = V_{C3} = \frac{V_{in}}{2} \tag{3}$$

Mode 2 [$t_1 - t_2$] – Fig. 4(b) – *Deadtime mode*: In this mode, on the primary side, only switches S_2 and S_5 are active so that the source energy does not provide energy to the load. Instead of source V_{in}, the leakage energy on L_{lk} circulates the energy with output capacitors of switches S_1 and S_3, which is an oscillation process. As a result of this osscilation process, the voltage of switches S_1 and S_3 are decreased to 0 and increased to $V_{in}/2$, respectively, as expressed in (4)-(5). Therefore, at the end of this mode, switch S_1 turns on ZVS, while switch S_3

turns off completely. On the secondary side, both inductors L_1 and L_2 transfer the energy to the load.

$$v_{S_3}(t) = \frac{1}{2C_{oss}} \int_{t_1}^{t} i_{Lk}(\tau) d\tau \approx \frac{i_{Lk}(t_1)}{2C_{oss}}(t - t_1) \quad (4)$$

$$v_{S1}(t) = v_{C1} - v_{S3}(t) = \frac{V_{in}}{2} - \frac{i_{Lk}(t_1)}{2C_{oss}}(t - t_1) \quad (5)$$

Mode 3 [t_2 – t_3] – Fig. 4(c) – *Freewheeling mode*: In this mode, the leakage inductor current continues to circulate around the primary side of the transformer. While in the secondary side, inductors L_1 and L_2 transfer energy to the load to keep the current continuous. Because of the voltage state from mode 2, switch S_{R1} is turned on under the ZVS condition. Switches S_3 and S_4 are off in this mode. Similar to mode 1, the voltage stress on switches S_3 and S_4 are rated at $V_{in}/2$:

$$v_{S3} = v_{S4} = \frac{V_{in}}{2} \quad (6)$$

Mode 4 [t_3 – t_4] – Fig. 4(d) – *Deadtime mode*: In this mode, switch S_4 turns on, switches S_2 and S_5 turn off while switch S_3 is off. The primary current is down to 0 before changing the direction to prepare for the next half-cycle. Compared to other modes, the primary current in this mode is lowest and the number of oscillation capacitors is three rather than two as in modes 2 and 8. Therefore, this mode is the critical point to determine the ZVS range of the proposed converter, and the turn-on process of switch S_4 is an important checking point to determine the soft-switching range of the proposed converter. In this mode, the switches S_3 keep the off state as mode 3 and there is no change in its voltage stress. Similar to the mode 2, the voltage of switching switches are expressed as below:

$$v_{S2}(t) = v_{S5}(t) = \frac{1}{3C_{oss}} \int_{t_3}^{t} i_{Lk}(\tau) d\tau \approx \frac{i_{Lk}(t_3)}{3C_{oss}}(t - t_3) \quad (7)$$

$$v_{S4}(t) = \frac{V_{in}}{2} - \frac{i_{Lk}(t_3)}{3C_{oss}}(t - t_3) \quad (8)$$

Mode 5 [t_4 – t_5] – Fig. 4(e) – *Power mode*: This mode is a power mode, which is the same as mode 1. However, the primary transformer voltage is provided by capacitor C_3 in an opposite current direction with mode 1. The voltage of capacitor C_3 is $V_{in}/2$, which is charged in before modes. On the secondary side, inductor L_2 stores energy from primary side while inductor L_1 transfers energy to the load. The voltage of the primary transformer, and voltage stress of off-state switches S_2, S_3, and S_5 are as follows:

$$v_{tr} = -V_{C3} = -\frac{V_{in}}{2} \quad (9)$$

$$v_{S2} = v_{S3} = v_{S5} = \frac{V_{in}}{2} \quad (10)$$

Mode 6 [t_5 – t_6] – Fig. 4(f) – *Deadtime mode*: In this mode, on the primary side, switches S_2 and S_5 turn on, switch S_4 turns off while switch S_1 keeps the on-state. On the secondary side, the voltage of switch S_{R2} is dropped down to 0, and both inductors L_1 and L_2 transfer the energy to the load. This mode is the same as mode 4 by the number of oscillation capacitors, which is larger by one compared to modes 2, and/or 8. However, in this mode, the primary transformer current is at the highest value point. Therefore, the ZVS energy is large and switches S_2 and S_5 make it easy to achieve ZVS characteristics. In this mode, the voltage stress of off switch S_3 keeps at $V_{in}/2$. Similar to the mode 2, the voltage of switching switches are expressed as below:

$$v_{S4}(t) = \frac{1}{3C_{oss}} \int_{t_5}^{t} i_{Lk}(\tau) d\tau \approx \frac{i_{Lk}(t_5)}{3C_{oss}}(t - t_5) \quad (11)$$

$$v_{S2}(t) = v_{S5}(t) = \frac{V_{in}}{2} - \frac{i_{Lk}(t_5)}{3C_{oss}}(t - t_5) \quad (12)$$

Mode 7 [t_6 – t_7] – Fig. 4(g) – *Freewheeling mode*: In this mode, both primary side and secondary side occur the freewheeling process when inductors L_{lk}, L_1, and L_2 discharge the energy. The voltage stress of switches S_3 and S_4 is kept at $V_{in}/2$.

Mode 8 [t_7 – t_8] – Fig. 4(h) – *Deadtime mode*: In this mode, switch S_3 turns on, and switch S_1 turns off. Switches S_2 and S_5 are on-state while switch S_4 is off-state. Stress volage of switch S_4 is $V_{in}/2$. On the secondary side, both inductors L_1 and L_2 transfer energy to the load. Similar to the mode 2, the voltage of switching switches are expressed as below:

$$v_{S1}(t) = \frac{1}{2C_{oss}} \int_{t_7}^{t} i_{Lk}(\tau) d\tau \approx \frac{i_{Lk}(t_7)}{2C_{oss}}(t - t_7) \quad (13)$$

$$v_{S3}(t) = \frac{V_{in}}{2} - \frac{i_{Lk}(t_7)}{2C_{oss}}(t - t_7) \quad (14)$$

III. CHARACTERISTICS OF THE PROPOSED CONVERTER

A. VOLTAGE GAIN

With the above analysis, it can be explained that the step-down feature of the proposed converter is obtained by the charge-in-series-discharge-in-parallel principle of capacitors C_1 and C_3. Indeed, capacitor C_1 is charged in a series circuit with capacitor C_3 in modes 2-4, and with capacitor C_2 in mode 5, before discharging in a parallel circuit with the primary transformer in mode 1 of the next switching period, which down the primary voltage to its rating voltage of $V_{in}/2$ level. Similarly, capacitor C_3 is discharged in a parallel circuit with the primary transformer in mode 5 with a voltage of $V_{in}/2$, which is the result of the charging process in the series circuit with capacitor C_1 in modes 1-4 before.

From the above analysis, the following equation can be expressed:

$$|v_{tr}| = V_{C1} = V_{C2} = V_{C3} = \frac{V_{in}}{2} \quad (15)$$

On the other hand, as shown in Fig. 2, inductor L_1 stores energy from the primary side in mode 1 when capacitor C_1 discharges energy, while in other modes L_1 transfers energy

to the load. Similarly, inductor L_2 stores energy in mode 5, and transfers energy to the load in other modes. Apply for the voltage-second balance principle on L_1 and L_2, and using equation (15), the voltage gain of the proposed converter can be obtained:

$$M = \frac{V_o}{V_{in}} = \frac{nD}{2} \tag{16}$$

Therefore, the buck gain of the proposed converter is better than the conventional IHSTD converters [10], [11], [12], [13], [14], [15] by $D/2$ times.

B. VOLTAGE STRESS ON POWER SWITCHES AND PRIMARY TRANSFORMER

From (2), (3), (6), and (10), the voltage stress for primary switches can be summarized as follows:

$$V_{S1} = V_{S3} = V_{C1} = \frac{V_{in}}{2} \tag{17}$$

$$V_{S2} = V_{S4} = V_{C3} = \frac{V_{in}}{2} \tag{18}$$

$$V_{S5} = V_{C2} = \frac{V_{in}}{2} \tag{19}$$

From (17)-(19), all primary switches of the proposed converter have voltage stress of half input voltage. Hence, 650 V rating semiconductor devices can be adopted in 800 V systems rather than 1200 V rating devices as with the conventional IHSTD converters. Generally, IGBTs and SiC MOSFETs are the dominant selection for voltage ratings at or above 1200 V. However, IGBTs are not suitable for high switching frequency converters while the price of SiC MOSFETs is still expensive. The lower rating voltage devices bring many benefits including higher reliability, better performance of lower drain-to-source resistance, and switching characteristics, lower price, and more popularity in the market. With current technology, GaN devices are very suitable devices for 650 V rating semiconductor, which has a better switching characteristics compared to SiC MOSFET. Therefore, this device can switch at much higher frequencies with the advantages of higher power density, and higher efficiency [30], [31]. The silicon super-junction (SJ) MOSFETs with a better price, and low output capacitance can also be a suitable solution when a 650 V rating stress voltage is available [32]. Some recent research has compared devices in around 650 V rating conditions, which has recognized the advantages of using GaN and SJ MOSFET devices in topologies having low stress voltage on power switches [32], [33].

Besides the low rating voltage of power switches, in the proposed converter, the primary voltage of the transformer is also decreased to $V_{in}/2$. This point is meaningful, especially with new technology transformers such as planar transformers. This is because, with a lower primary voltage, a lower transformer turn ratio can be obtained, thereby minimizing the length of the printed circuit board (PCB) traces, and decreasing the number of PCB layers, cost, and size [16], [17]. This is a practical benefit, because the transformer is a big problem with high conversion ratio converters [16], [17], [23].

C. SOFT-SWITCHING CHARACTERISTICS OF THE PRIMARY SWITCHES WITH A WIDE ZVS RANGE

As mentioned in Section I, the practical issue of the conventional PSFB converter is the ZVS range. This issue becomes more challenging in the context of 800 V EV. Indeed, when updating the battery system from 400 V to 800 V, the switching characteristics of primary switches in the conventional PSFB and DAB converters will be changed accordingly. The transition voltage of primary switches in switching points is increased by double from 400 V to 800 V. While, the switching current is decreased by half due to the primary transformer current being decreased to half also to balance the power level when double the input voltage. Considering the PSFB converter, the required ZVS energy $E_{required}$ will be increased by 4 times, while the leakage energy E_{Lk} will be decreased by 4 times as calculated in (20), (21). As a result, the ZVS range of 800 V-based PSFB converter is narrower 16 times compared to the conventional 400 V-based PSFB converter.

$$\frac{E_{PSFB\_required}(800V)}{E_{PSFB\_required}(400V)} = \frac{\frac{1}{2}(2C_{oss})800^2}{\frac{1}{2}(2C_{oss})400^2} = 4 \tag{20}$$

$$\frac{E_{Lk\_PSFB}(800V)}{E_{Lk\_PSFB}(400V)} = \frac{\frac{1}{2}L_{lk}(0.5I_{Lk\_PSFB})^2}{\frac{1}{2}L_{lk}I_{Lk\_PSFB}^2} = \frac{1}{4} \tag{21}$$

With the proposed converter, as mentioned in Section II, all of the primary switches can operate under ZVS conditions. Moreover, the ZVS range of these switches is extended compared to the conventional PSFB and DAB converters. These properties are obtained because of a beneficial voltage-current relation on the primary side. To explain this relation, Fig. 5 compares the operation waveforms of the proposed converter and the conventional PSFB converter. It can be seen that the primary transformer current of the proposed converter is double compared to the PSFB converter because of a $V_{in}/2$ primary transformer voltage rather than V_{in}, which enhances the leakage energy E_{Lk} by 4 times as explained by the following equations.

$$I_{Lk\_proposed} = 2I_{Lk\_PSFB} \tag{22}$$

$$E_{Lk\_proposed} = \frac{1}{2}L_{lk}(2I_{Lk\_PSFB})^2 = 4(\frac{1}{2}L_{lk}I_{Lk\_PSFB}^2) = 4E_{Lk\_PSFB} \tag{23}$$

While the switching transition voltage of all primary switches in the proposed converter is $V_{in}/2$, which is half compared to the PSFB converter. Therefore, the required ZVS energy $E_{required}$ for these switches will be decreased by 2,67 times according to the calculation below.

$$E_{PSFB\_required} = \frac{1}{2}(2C_{oss})V_{in}^2 = C_{oss}V_{in}^2 \tag{24}$$

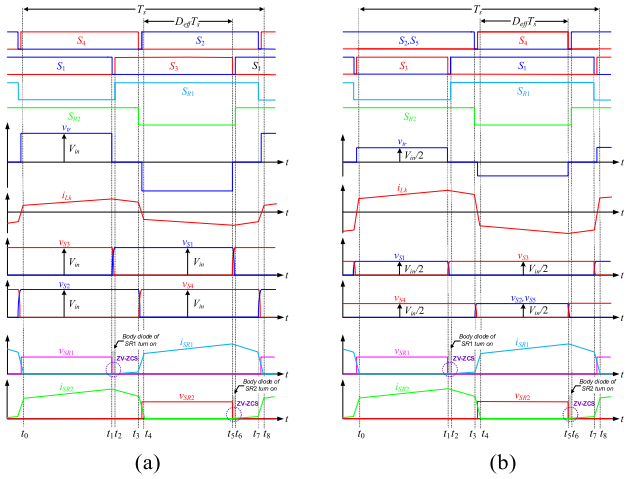

FIGURE 5. Compare operation waveforms of (a) the PSFB converter, and (b) the proposed converter.

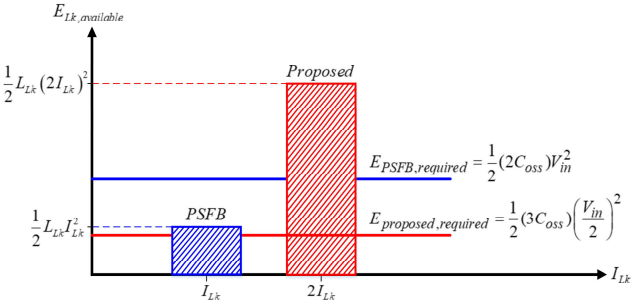

FIGURE 6. The ZVS energy comparison between the PSFB converter and the proposed converter.

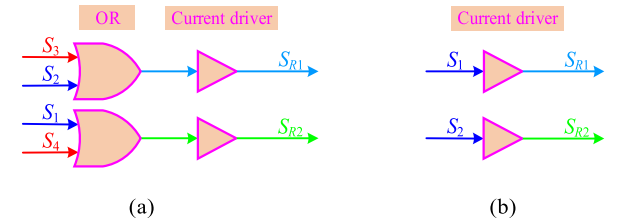

FIGURE 7. Synthesize control signals for (a) the PSFB converter, and (b) the proposed converter.

$$E_{proposed\_required} = \frac{1}{2}(3C_{oss})(\frac{V_{in}}{2})^2 = \frac{3}{8}C_{oss}V_{in}^2 = \frac{3}{8}E_{PSFB\_required} \quad (25)$$

To illustrate the benefits of the above relations, Fig. 6 considers the light load case. With the same load current and the same leakage inductance L_{lk}, the conventional PSFB converter loses the ZVS characteristic since the available leakage energy E_{Lk} is lower than the required ZVS energy $E_{required}$, while the proposed converter still ensures ZVS with a wide redundancy. That means the proposed converter solves the narrow ZVS range issue of the conventional PSFB converter by extending the ZVS range to the light load section. This characteristic is especially meaningful in the context of 800 V EV.

D. SOFT-SWITCHING CHARACTERISTICS OF THE SECONDARY SWITCHES WITH A SIMPLE DRIVER CIRCUIT

Figs. 5 and 7 show that the secondary switches of the proposed converter can achieve ZV-ZCS turning on, which is similar to the conventional PSFB converter but with a simpler driver circuit. As presented in Section II, the ZV-ZCS operation of switches S_{R1}, S_{R2} results from the operation of inductors L_1 and L_2 and the existence of body diodes, which is the same as the conventional PSFB converter. However, the conventional PSFB converter requires a more complex logic driver circuit to ensure that S_{R1} and S_{R2} are controlled to turn on in the negative half-cycle, and positive half-cycle of the transformer voltage waveform, respectively, which is proven to help optimize the conduction interval and avoid short circuit between secondary switches [34], [35]. Therefore, the PSFB converter needs a logic circuit to synthesize the control signal for S_{R1}, and S_{R2} from the original phase-shifted control signals as shown in Fig. 7(a).

With the proposed converter, the synthesizing circuit can be removed because the secondary switches S_{R1} and S_{R2} are simply repeated both in hardware and control signals of primary switches S_1 and S_2, respectively. As a result, the control signals for switches S_{R1} and S_{R2} can be directly taken from the control signals of switches S_1 and S_2 without a logic buffer circuit as shown in Fig. 7(b). This advantage helps reduce costs and complexity in the design process.

IV. DESIGN CONSIDERATION AND DISCUSSION

A. DESIGN CONSIDERATION

In this section, the design equations of the proposed converter will be considered with a focus on the primary side devices. With the secondary side devices including synchronous switches, output inductors, and output capaitors, the design methd is the same as that of the conventional PSFB converter, which can be referred to [10] and [11].

1) DESIGN EQUATION RELATED WITH SWITCHES

To begin with, the current and voltage rating of primary and secondary switches are determined. The RMS current of primary switches is obtained by the simplified current waveforms of switches in Fig. 2. According to that, the RMS value of the current through these switches can be expressed as:

$$i_{S1\_RMS} = \sqrt{D\left[\left(\frac{nI_o}{2}\right)^2 + \frac{1}{3}I_{Lm\_p}^2\right] + 2I_{Lk\_p}^2(0.5 - D)} \quad (26)$$

$$i_{S2\_RMS} = i_{S5\_RMS} = \frac{1}{2}\sqrt{D\left[\left(\frac{nI_o}{2}\right)^2 + \frac{1}{3}I_{Lm\_p}^2\right] + 2I_{Lk\_p}^2(0.5 - D)} \quad (27)$$

$$i_{S3\_RMS} = i_{S4\_RMS} = \frac{nI_o}{2}\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{I_{Lm\_p}}{nI_o/2}\right)^2} \tag{28}$$

where I_{Lm_p} and I_{Lk_p} are the maximum values of magnetizing inductor and leakage inductor, respectively.

The voltage stress of primary switches is equal to half of the input voltage, as a characteristic of the proposed converter.

$$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = \frac{V_{in}}{2} \tag{29}$$

2) DESIGN EQUATION RELATED WITH TRANSFORMER

One of the main parameters of the transformer is the turn-ratio, which can be determined with equation (30).

$$n = \frac{2V_o}{V_{in\_\min}D_{\max}} \tag{30}$$

The maximum duty cycle D_{max} selected is 0.4 since the deadtime intervals and duty cycle loss have been considered. With a desired $V_{in\_\min}$ equal to 460 V, the turn ratio of $n = 0.5$ is designed.

Other parameters of the transformer are affected by the equation (31), which is derived from Faraday's law equation [2].

$$V_m = \frac{4}{D}N_{pri}B_mA_cf_s \tag{31}$$

where $f_s = 1/T_s$ is the switching frequency, A_c is the cross-sectional area of the transformer's magnetic core, D is the duty cycle of the square waveform, N_{pri} is the number of primary winding turns, B_m is the maximum flux density of the core, and V_m is the peak amplitude of the winding voltage, which is equal to half of the input voltage. B_m is a constant number that depends on the core material.

3) DESIGN EQUATION RELATED WITH CAPACITORS

In the proposed converter, there are three capacitors on the primary side, which include input capacitors C_1, C_2, and the series capacitor C_3. The voltage rating of these capacitors is equal to $V_{in}/2$. The capacitance of C_1, C_2 can be calculated through allowable voltage ripple across them [2].

$$C_1 = C_2 \geq \frac{I_{Lk\_p}}{4f_sV_{in}\Delta V_{in\%}} \tag{32}$$

where $\Delta V_{in\%}$ is the maximum allowable voltage ripple percentage across each input capacitor.

The capacitance of C_3 is designed so that the voltage ripple is less enough to ensure that this capacitor works as an ideal voltage source [28].

$$C_3 \geq \frac{nDT_sI_o}{kV_{in}} \tag{33}$$

where k is the ripple factor of the capacitor voltage.

4) DESIGN EQUATION RELATED WITH DEADTIME INTERVAL

Deadtime T_D is a crucial parameter for achieving ZVS and high efficiency. With a small deadtime, the ZVS may not be achieved or only partly ZVS can be achieved. However, with a large deadtime, the power transfer will be limited. Therefore, the resonant between leakage inductor and output capacitors of primary switches should finished before the deadtime duration, which is expressed in (34) with the resonant frequency given in (35).

$$T_D \geq \frac{T_r}{4} \tag{34}$$

$$f_r = \frac{1}{2\pi\sqrt{L_{lk}(3C_{oss}+C_{tr})}} \tag{35}$$

with $3C_{oss}$ represent for the maximum of three output capacitors in the oscillation process as shown in Fig. 4(d). C_{tr} is the transformer parasitic capacitance which could be neglected since quite small.

B. SELECTING DEVICES DISCUSSION

Table 1 shows the comparison in terms of devices used in the proposed converter with the conventional PSFB converter. The devices and parameters are chosen according to the above analyses, and a detailed analysis in [2]. The converters are designed with the same output power, hence, the main difference appears on the primary side. According to [2], by changing the input voltage from 400 V to 800 V, the primary current can be reduced to half compared to the conventional 400 V input voltage, which can decrease the conduction loss as well as the current stress of primary switches, but as mentioned, the decreased primary current will reduce the leakage energy, mixing with a high switching voltage of 800 V, ZVS range of 800 V PSFB converter will be extremely narrow. This is the reason why a large external inductor is needed for the PSFB converter when working at 800 V input voltage conditions. Table 1 also shows the selected MOSFET switches that suitable for converters. Although the selected SiC C3M0075120K MOSFET of 800 V PSFB converter has been taken advantage of the low output capacitance, the required leakage inductance still very large, which can create a large duty cycle loss, high circulating current, high output voltage ringing, and limit the power transfer. Moreover, the updated system also requires new primary switches with 1200 V voltage stress, and a new design for transformer with a double turn ratio compared to the conventional transformer. All of these aspects increase the cost of the updated system. With the proposed converter, a double primary current compared to 800 V PSFB can bring concern of high conduction loss, but low on-resistance of low voltage switches can balance this loss while keeping a wide soft-switching range without a large leakage inductor. There are three solutions for low voltage stress of the proposed converter as shown in Table 1. All of these switches have lower on-resistance compared to the required 1200 V switches of the conventional PSFB converter. In the laboratory, the SJ

TABLE 1. Comparison proposed converter with the conventional PSFB converter in 400 V and 800 V input voltage conditions.

Output condition: 1.2 kW, 48 V		Conventional PSFB converter (Input voltage: 400 V)	800 V PSFB converter (Input voltage: 800 V)	800 V Proposed converter (Input voltage: 800 V)
Primary side	Capacitor	1EA x 470 uF, 400 V	*2EA x 60 uF, 800 V	2EA x 220 uF, 450 V 1EA x 7.5 uF, 450 V
	Switches	4EA x IPW65R029CFD7 (V_{DS} = 650 V, I_{DS} = 45 A, $R_{ds(on)}$= 29 mΩ, V_F = 1 V, C_{oss} = 120 pF)	4EA x C3M0075120K (V_{DS} = 1200 V, I_{DS} = 30 A, $R_{ds(on)}$ = 90 mΩ, V_F = 3.2 V, C_{oss} = 58 pF)	**Solution 1: SiC MOSFET**: 5EA x NTBG023N065M3S (V_{DS} = 650 V, I_{DS} = 70 A, $R_{ds(on)}$ = 23 mΩ, V_F = 4.5 V, C_{oss} = 152 pF) **Solution 2: GaN MOSFET**: 5EA x TP65H050G4QS (V_{DS} = 650 V, I_{DS} = 34 A, $R_{ds(on)}$ = 60 mΩ, V_F = 2.2 V, C_{oss} = 110 pF) **Solution 3: SJ MOSFET**: 5EA x IPW65R029CFD7 (V_{DS} = 650 V, I_{DS} = 45 A, $R_{ds(on)}$ = 29 mΩ, V_F = 1 V, C_{oss} = 106 pF)
	Control	Phase shift	Phase shift	PWM
Transformer	Core	PQ 4040	PQ 4040	PQ 4040
	Leakage inductance	12 uH	35uH	12 uH
	Turn ratio	2:1	4:1	2:1
Secondary side	Switches	IPW60R045CPA (V_{DS} = 600 V, I_{DS} = 38 A, $R_{ds(on)}$ = 45 mΩ, V_F = 0.9 V, C_{oss} = 120 pF)		
	Output inductor	$L_1 = L_2$ = 150 uH		
	Output capacitor	C_o = 220 uF, 50 V		
	Control	Complex	Complex	Simple

** Two 60 uF, 800 V capacitors are connected parallel to ensure the required capacitance of 120 uF, at 800 V DC rating.*

TABLE 2. Cost for primary side components of the prototypes.

Items		Conventional PSFB converter (Input voltage: 400 V)	800 V PSFB converter (Input voltage: 800 V)	800 V Proposed converter (Input voltage: 800 V)		
Primary side	Capacitors	EKHS451VSN471MQ50S x 1EA : $8.98 (= $8.98 x 1)	495-B32778Z8606K000 x 2EA : $17.42 (= $8.71 x 2)	450MXT220MEFCSN25X30 x 2EA B32674D4755K000 x 1EA : $21.43 (= $8.31 x 2 + $4.81 x 1)		
	Switches	IPW65R029CFD7 x 4EA : $37.8 (= $9.45 x 4)	C3M0075120K x 4EA : $80.04 (= $20.01 x 4)	IPW65R029CFD7 x 5EA: $47.25 (= $9.45 x 5)	NTBG023N065M3S x 5EA: $57.5 (= $11.5 x 5)	TP65H050G4QS x 5EA: $59.35 (= $11.87 x 5)
	Drivers	1ED020I12-F2 x 4EA : $12.48 (= $3.12 x 4)	1ED020I12-F2 x 4EA : $12.48 (= $3.12 x 4)	1ED020I12-F2 x 5EA : $15.6 (= $3.12 x 5)		
Cost		$59.26	$109.94	$84.28	$94.53	$96.38

The price is referred from www.digikey.com with USD unit prices at the time of submission.

MOSFET IPW65R029CFD7 has been selected for the prototype, which is the same as the switches used in the 400 V system. This SJ MOSFET has low on-resistance and low output capacitance. The cost of this MOSFET is also lower than other solutions, as will be shown in Table 2. Therefore, the proposed converter allows reuse switches, and transformer of the conventional 400 V PSFB converter, with low on-resistance, and low dropped voltage of body diodes for MOSFETs, and keeps the same transformer design with no modifications in turn-ratio, leakage inductor, current, and voltage rating. Also, the proposed converter has a simple control method for both the primary and secondary synchronous MOSFETs.

Table 2 compares the cost for the primary side of the conventional PSFB converter in the condition of 400 V and 800 V input voltage with the cost of the proposed converter in the condition of 800 V input voltage. Because the main change between the proposed converter and the conventional PSFB converter lies on the primary side, only the primary side cost is considered. The transformer dimension, which is the main part that determines the cost of the transformer, is shown to remain unchanged when updating voltage from 400 to 800 V according to [2], it is not included in this table. As shown, when increasing input voltage, the cost of the conventional PSFB converter increases significantly due to the cost of high voltage switches. The proposed converter has

TABLE 3. Comparison of the proposed converter with other IHSTD converters.

	Split-capacitor based PSFB converter in [23]	HBTL converter in [26]	Integrated Buck+Push-Pull converter in [27]	TS-DEACF+AHB converter in [29]	Conventional PSFB converter	Proposed converter
Device count (Sw./Di./Cap./Trans.)	6 / 4 / 5 / 1	4 / 4 / 4 / 1	3 / 3 / 4 / 1	4 / 2 / 3 / 1	6 / 0 / 2 / 1	7 / 0 / 4 / 1
Voltage gain	$nD/4$	$nD/2$	nD^2	$2nD(1\text{-}D)$	nD	$nD/2$
Transformer voltage	$V_{in}/4$	$V_{in}/2$	$DV_{in}/2$	$V_{in}/2$	V_{in}	$V_{in}/2$
Required ZVS (leakage) energy	$\frac{CV_{in}^2}{32}$	$\frac{CV_{in}^2}{4}$	-	CV_{in}^2	CV_{in}^2	$\frac{3CV_{in}^2}{8}$
Available ZVS (leakage) energy	$8L_{lk}I_{lk}^2$	$2L_{lk}I_{lk}^2$	-	$\frac{1}{2}L_{lk}I_{lk}^2$	$\frac{1}{2}L_{lk}I_{lk}^2$	$2L_{lk}I_{lk}^2$
ZVS range	Wide	Wide	Hard switching	Wide	Narrow	Wide
Voltage stress	$V_{in}/2$ for three switches $V_{in}/4$ for three switches	$V_{in}/2$ for all switches	$(1+D)V_{in}$ for S1 DV_{in} for S2, S3 V_{in} for D1	V_{in} for two switches DV_{in} for two switches	V_{in} for all switches	$V_{in}/2$ for all switches
Switching frequency	100 kHz	100 kHz	50 kHz	70 kHz	100 kHz	100 kHz
Presented peak efficiency	95.4%	95.7%	84.45%	92.7%	94.8%	96.3%

the disadvantages of increasing one primary switch and one driver circuit compared to the conventional PSFB converter, in which four out of five primary switches require high-side drivers, and more primary capacitors are needed but overall, the cost of the primary side is still lower than the conventional PSFB converter when considering 800 V input voltage.

C. COMPARISON WITH OTHER IHSTD CONVERTERS

Table 3 shows a comparative table of some existing capacitor-based IHSTD converters, which have characteristics suitable for APM module in 800 V EVs. Converters are compared in terms of voltage gain, device count, transformer primary voltage, ZVS range and parameters, voltage stress on primary switches and primary transformer, switching frequency, and peak efficiency. Regarding the voltage gain, converter in [27] has the highest step-down gain. However, the voltage gain of this converter is expressed by a nonlinear characteristic, which makes it difficult for the control system. The conventional PSFB converter, the proposed converter, and converters in [23] and [26] own a linear voltage gain characteristic, in which the converter in [23] has a better step-down voltage gain. However, converter in [23] requires a larger number of devices than other IHSTD converters. While the voltage gain of the proposed converter and the half-bridge three-level (HBTL) converter in [26] is the same, which is better than the conventional PSFB converter. The proposed converter requires a larger number of switches than other IHSTD converters mostly due to using a synchronous rectifier structure. The HBTL converter has a lower number of active switches, but this converter requires four diodes including two primary diodes and two rectifier diodes on the secondary side, therefore, the total device count of the HBTL converter is larger than the proposed converter. Regarding the ZVS characteristic, converter in [27] only works with hard-switching operation, converters [23], [26], [29], and the proposed converter achieve soft-switching operation with a wide ZVS range, in which the proposed converter and the HBTL converter has a large enough ZVS energy, and low required ZVS energy. While the ZVS range of the conventional PSFB is narrower than converters in [23], [26], and [29], and the proposed converter. Regarding the voltage stress on primary switches, the proposed converter, and the HBTL converter have a half input voltage stress for all primary switches, which is lower than the conventional PSFB converter and converters in [27] and [29]. The proposed converter and converters in [23], [26], and [29] and the conventional PSFB converter allow a high switching frequency thanks to soft-switching capability. The presented peak efficiency of the proposed converter and other converters is also pointed out in Table 3. Overall, the proposed converter has the benefits of a wide ZVS range, low voltage stress on primary switches, and high efficiency. The characteristics of the proposed converter are the same as the HBTL converter in [26], but the proposed converter does not need the diodes on the primary side, which can significantly reduce conduction losses. The structure of the proposed converter is more complex than the conventional PSFB converter, which brings concerns of long-term reliability, but this structure is needed to improve the soft-switching range and voltage stress of switches, which also contributes to improving the reliability with each switch of the converter.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

To verify the operation and characteristics of the proposed converter and compare the performance with the conventional PSFB converter, a simulation and an experimental prototype are implemented with $V_o = 48$ V, $P_o = 1.2$ kW, V_{in} in the range of 460 – 800 V; switching frequency $f_s = 100$ kHz.

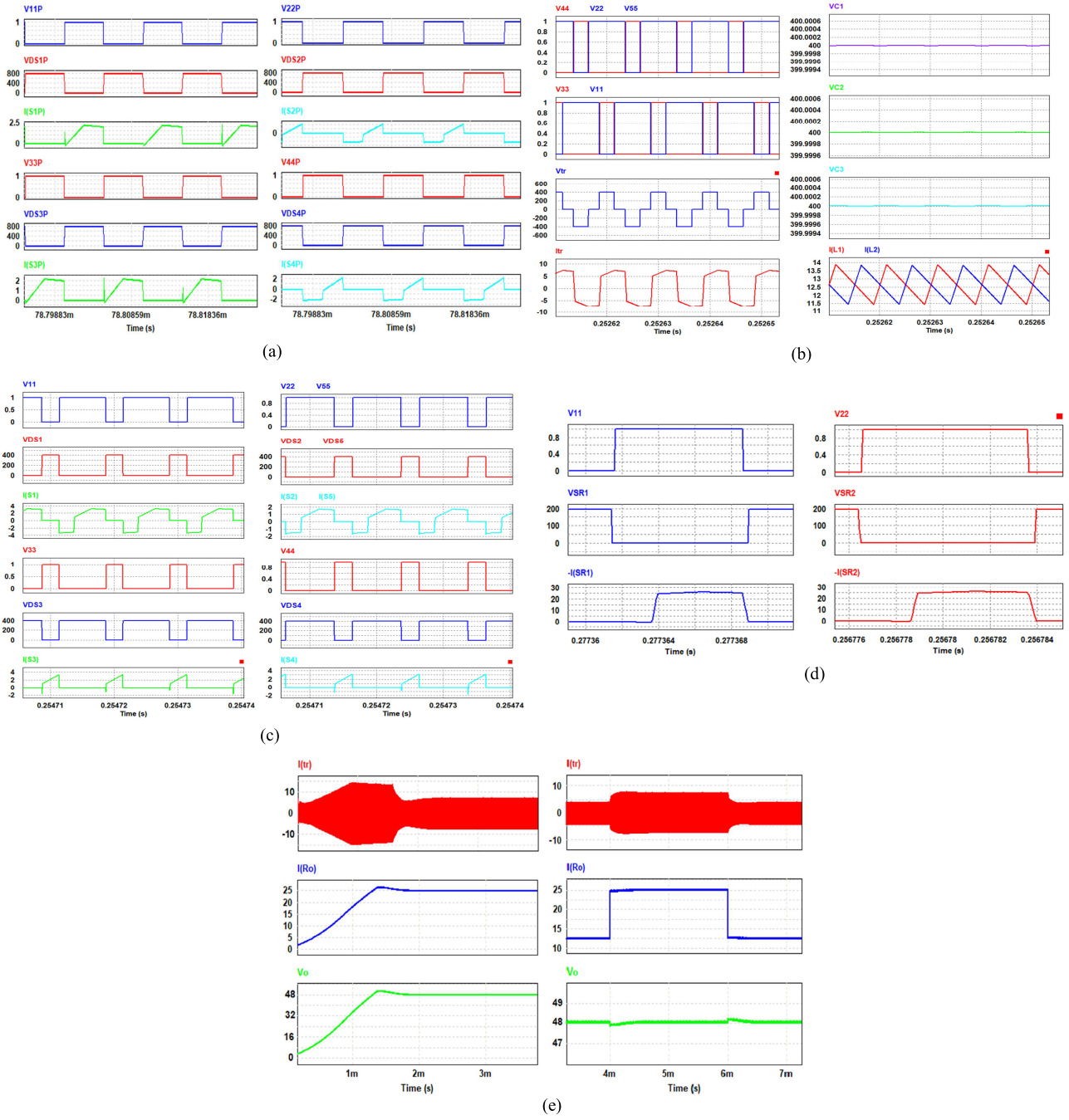

FIGURE 8. Simulated waveforms of the conventional PSFB converter and the proposed converter with 800 V input – 48 V output condition. (a) the control signals, the drain-to-source voltage, and current through primary switches of the conventional PSFB converter at 30% load. (b) the key operation waveforms of the proposed converter. (c) the control signals, the drain-to-source voltage, and current through primary switches of the proposed converter at 30% load. (d) switching characteristics with the secondary switches of the proposed converter. (e) the start-up process and changing current load waveforms of the proposed converter.

The devices, and specification parameters of converters are given in Table 1.

Fig. 8 shows the simulation results, which verify the feasibility and characteristics of the proposed converter and compare it with the conventional PSFB converter. Fig. 8(a) shows the control signals, the voltage, and the current of the primary switches in the conventional PSFB converter at 30% load, which is to check the voltage stress, and soft-switching capability of the conventional PSFB converter at light load conditions. As shown, the lagging leg switches of the conventional PSFB converter can not achieve ZVS at 30% load condition, and primary switches must withstand a large stress voltage of 800 V. Fig. 8(b) verifies the operation and feasibility of the proposed converter. As shown, under the control

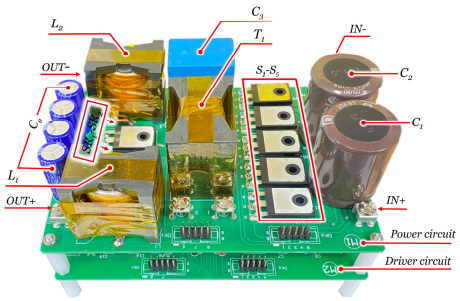

FIGURE 9. Photograph of 1.2 kW prototype of the proposed converter.

signals, the current transformer waveform has a trapezoidal shape, while the voltage waveform has a quasi-square shape with a positive pulse width equal to the duty cycle width. Besides, the voltage of capacitors C_1, C_2, C_3, and inductor currents are explored. All waveforms are matched with the theoretical analysis and the proposed converter works exactly as analyzed before. Fig. 8(c) checks the soft-switching capability at light load conditions and voltage stress of primary switches with the proposed converter. As expected, all primary switches achieve ZVS operations at 30% load, and voltage stress at 400 V. Fig. 8(c) also shows that, the current rating of primary switches is different, in which the current waveforms of switches S_3 and S_4 is the same. The current waveforms of switches S_2, and S_5 is also the same, which is equal half of current through S_1. Fig. 8(d) validates the soft-switching capability of secondary switches, which shows that all these switches are obtained ZV-ZCS turning on. Fig. 8(e) shows the dynamic operation of the proposed converter in the start-up duration and under changing load from 50% rated current to 100% rated current with a closed loop control system. As shown, the proposed converter moves toward a steady state after 1.5 ms with a stable output voltage. However, a relatively large start-up primary current appeared due to the charging process of primary capacitors, which can be solved by the method of pre-charging capacitors before the start-up process. While, under load current changing conditions, the proposed converter can return to equilibrium quickly with a small voltage fluctuation of about 0.2 V.

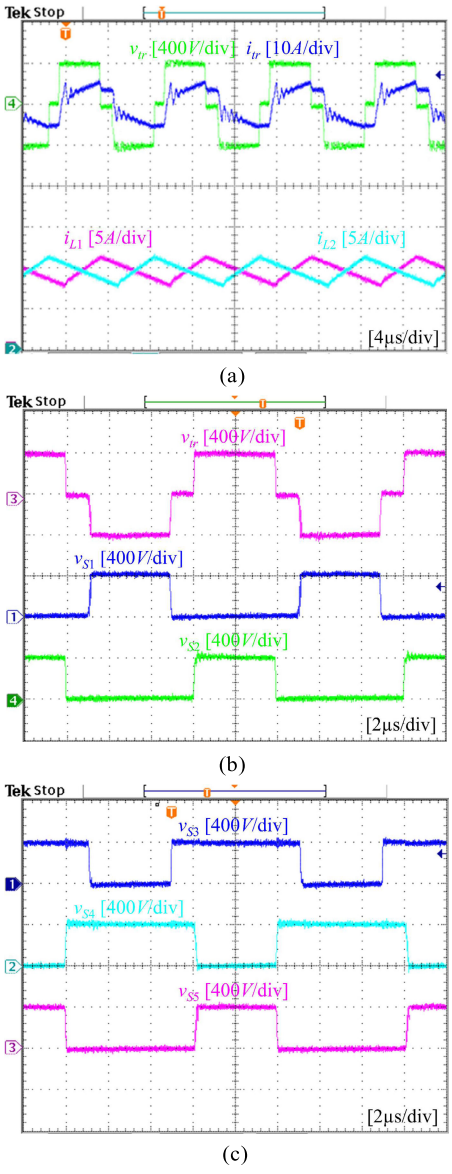

FIGURE 10. The experimental results of the proposed converter at V_{in} = 800 V, V_o = 48 V, P_o = 1.2 kW. (a) The transformer voltage, current, and output inductors current. (b) the voltage stress of the primary transformer, and switches S_1, $S2$. (c) the voltage stress of switches S_3, S_4, and S_5.

B. EXPERIMENTAL RESULTS

An experimental prototype is also carried out to verify the mentioned analyzed and simulation results. A photograph of the prototype for the proposed converter is given in Fig. 9, which is designed at 1.2 kW.

Fig. 10 shows the experimental waveforms of the proposed converter prototype to confirm the simulation results. As shown, the waveforms are the same as those analyzed in Section II and simulated waveforms. Notably, the voltage stress of both the primary transformer and primary switches are verified with a $V_{in}/2$ level.

Fig. 11 gives the measured switching waveforms of primary and secondary switches. In order to verify the wide soft-switching range of the proposed converter, Fig. 11 (a) and (b) are checked in a condition of light load at 30% rated power. As shown, switch S_1 in Fig. 11(a) can achieve ZVS easily, with the switching point at the peak of the primary transformer current while the switch S_4 can also switch softly under a ZVS condition, as can be seen in Fig. 11(b). As analyzed in Section II, if switch S_4 achieves ZVS, all other primary switches also achieve ZVS. This means that other primary power switches also achieve a ZVS characteristic.

Besides, the operation waveform of the secondary switch SR_1 is given in Fig. 11(c). As can be observed, this switch obtained soft-switching operation in full-load condition with a ZVZCS characteristic. There is a ringing phenomenon on the drain-to-source V_{SR1}, which is a consequence of the oscillation between L_{lk} of the transformer and C_{oss} of SR_1.

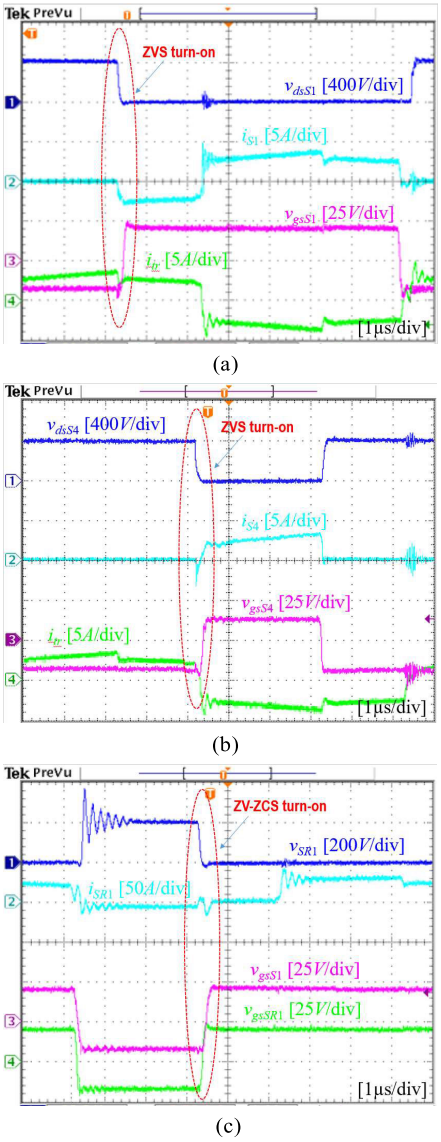

FIGURE 11. The switching waveforms of primary and secondary switches of the proposed converter with 800 V input voltage, 48 V output voltage: (a) S_1 at 30% load. (b) S_4 at 30% load. (c) S_{R1} at 100% load.

Fig. 12 shows the voltage of capacitors C_1, C_2, C_3, these voltage is balanced and is rated at half of the input voltage.

Finally, Fig. 13 gives the efficiency characteristic of the proposed converter, which shows an improved performance in the light load range when compared to the conventional PSFB converter. The performance tests are implemented at 800 V input, 48 V output voltage, with a wide load current range and the same leakage inductor of both the proposed converter and the conventional PSFB converter. The highest efficiencies of the conventional PSFB and the proposed converter are obtained at 960-W load and 480-W load with 94.8% and 96.3%, respectively.

Thus, the experimental results accurately reflect the simulation results. As the results shown, the basic characteristics of the proposed converter are to achieve soft-switching over

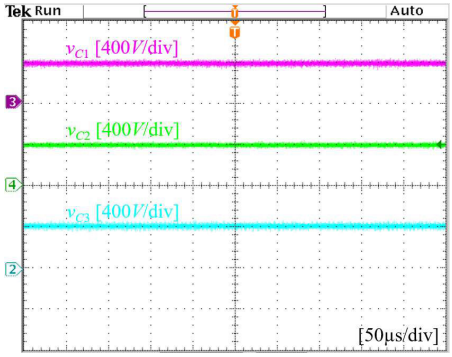

FIGURE 12. The experimental waveforms of secondary switches S_{R1}, S_{R2} of the proposed converter at V_{in} = 800 V, V_o = 48 V, P_o = 1.2 kW.

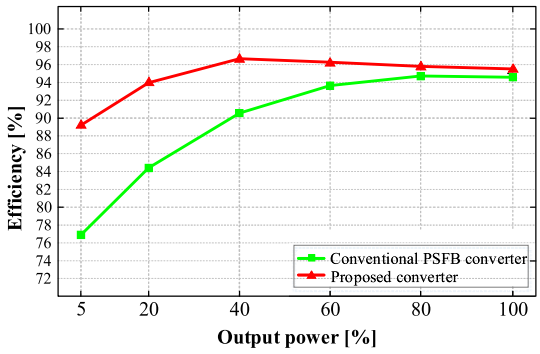

FIGURE 13. The performance curves of the conventional PSFB converter and the proposed converter.

a wide load range, and maintain the stress voltage on the primary switches at half the input voltage.

VI. CONCLUSION

This paper proposes an isolated DC–DC converter for the APM module in the 800 V EV. By placing capacitors on the primary side, the stress and switching voltage of all primary switches is kept around 400 V. By that 650 V switches can be reused rather than 1200 V switches with worst performances. Moreover, the primary transformer voltage is also reduced to 400 V, which helps overcome the challenges of high transformer turn ratio, and low step-down ratio of the conventional IHSTD converters. A lower switching transition voltage and higher primary transformer current also give meaningful relations to having a wider soft-switching range compared to the conventional IHSTD converters, especially in the context of 800 V EV. In order to achieve the above characteristic, the proposed converter requires a switched capacitor network on the primary side with three capacitors and five switches, which increases the number of driver circuits and structural complexity. The current stress and RMS current value of primary switches are also different. However, the overall cost of the proposed converter is still lower than the conventional PSFB converter with 800 V input voltage. In this paper, the operation of the proposed converter is explained, the characteristics of the proposed converter are presented in detail, and

a comparison with conventional PSFB converters has been completed. Besides, a simulation and an experiment are also implemented to validate the feasibility and properties of the proposed converter.

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