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RESEARCH ARTICLE

Comprehensive Hammering and Parasitic BJT Effects in Vertically Stacked DRAM

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ABSTRACT This study investigates the row hammer tolerance and potential degradation by capacitive crosstalk (CC) and parasitic bipolar junction transistor (BJT) effect in vertically stacked dynamic random-access memory (VS-DRAM) using technology computer-aided design (TCAD) simulations. The close arrangement of word lines in VS-DRAM results in a subthreshold leakage by the CC effect. Furthermore, as VS-DRAM has a floating body, hole accumulation in the body occurs via gate-induced drain leakage (GIDL) at the storage node in the cell that stores '1'. This can be accelerated by activating the bit-line (BL). The accumulated holes cause leakage current (I_{BJT}) by the parasitic BJT when the BL state becomes low and it is found that I_{BJT} can be enhanced by the CC effect in this study. The row hammer effect and I_{BJT} by the CC and parasitic BJT effects can be mitigated by reducing Si width.

INDEX TERMS VS-DRAM, capacitive crosstalk, parasitic bipolar junction transistor, floating body, TCAD.

I. INTRODUCTION

Saddle fin-based DRAMs have reached their size reduction limits as the size reduces down to 10 nm class, due to the limitations of minimum line resistance and capacitance values [1]. Vertically stacked DRAMs (VS-DRAMs) are expected to be the next-generation of DRAMs and can minimize the row hammer effect, considered as a major reliability concern for saddle fin-based DRAMs [2], [3]. However, VS-DRAM has the disadvantage of the floating body effect because the body is left floating for vertical stacking [4], [5]. The leakage current (I_{BJT}) due to the parasitic bipolar junction transistor (BJT) effects caused by hole accumulation can be mitigated in fully depleted structures compared with partially depleted structures. However, it can still occur as there is a strong electric field (E-field) and sufficient hole accumulation time [6]. In the case of 1T–1C DRAM, the capacitor is charged to preserve a data value of '1', and thus, a high potential is applied to the storage node (SN). This increases the E-field at the junction, resulting in enhanced gate-induced drain leakage (GIDL). In addition, bit-line (BL) activation can accelerate hole accumulation in the body. This is because of the unique structural characteristics of DRAM. As DRAM contains multiple cells connected to a single BL, when a write operation is performed by accessing a specific cell, the BL state of the connected cell toggles from the pre-charge state to V_{DD} [7], [8]. The connected cell experiences enhanced GIDL due to the high E-field on the SN and BL. When sufficient holes accumulate in the body, the body potential increases, and the conduction band energy (CBE) significantly decreases. As the BL is toggled to 0 V, I_{BJT} is caused by parasitic BJT effects [6]. For cells that were in a

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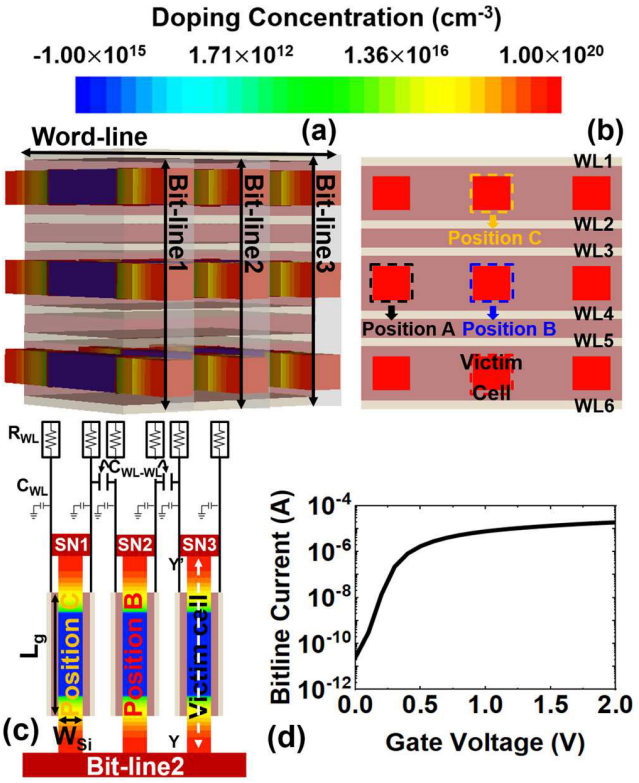

FIGURE 1. (a) 3D VS-DRAM schematic, (b) the victim and aggressive cells (Position A: adjacent cell located different column, position B: adjacent cell located same column, position C: nonadjacent cell located same column), (c) simulation resistor, and capacitors set up for CC effects and (d) I_d-V_g transfer curve.

long pre-charge state of more than 1 ms, when connected BL is toggled to 0 V for writing operation to the other cells, the retention time will be degraded by the I_{BJT} [1].

In the case of the saddle fin-based DRAM, the row hammer effect is caused by a gate that shares the same BL and a passing gate, placed near the body region of the cells. As a result, the data can be flipped '1' to '0' when the intracell aggressor is accessed continuously [9], or '0' to '1' as the intercell aggressor is accessed repeatedly [3]. The VS-DRAM structure does not include those gates, and the row hammer effect seemed eliminated. However, to increase cell integration in a VS-DRAM, the distance between cells should be minimized, causing the word lines (WLs) of each cell to be closely placed. As a result, the repeatedly accessing the cell at a certain address can degrade the retention time because the capacitive crosstalk (CC) effect is considered for the cells that have the WLs, placed closely each other [10]. Since one BL of VS-DRAM is connected with many cells [1], the potential at SN can be increased or decreased depending on the SN and BL states when neighboring cells are repeatedly accessed. Furthermore, when the writing operation is performed at the neighboring cell which shares the same BL, the subthreshold leakage can be enhanced. Also, accessing a cell, placed neighboring and shares the same BL with the victim cell after

TABLE 1. Actual device parameters for the simulations.

V_{PP}	V_{DD}	V_{off}	C_{SN}	C_{WL}	$C_{WL\text{-}WL}$
2.5 V	1.0 V	-0.2 V	6 fF	736 fF	234 fF
Gate Work Function	Interface Trap	Gate Length (L_g)	S/D Length	Si Width (W_{Si})	Gate Oxide Thickness
4.9 eV	5×10^2 cm^{-2}	100 nm	35 nm	20, 5 nm	6 nm

TABLE 2. Cases for simulation of CC effects.

	Accessing Position	BL2 State	SN3 State
Case1 / 2	A	Pre-charge	V_{DD} / 0
Case3 / 4	B	Write '0' / Write '1'	V_{DD} / 0

TABLE 3. Cases for the capacitive crosstalk and parasitic BJT Effects simulation.

	Accessing Position	SN3 / BL2 state
Case5	C	V_{DD} / Write '0' after 1ms pre-charge
Case6	B	V_{DD} / Write '0' after 1ms pre-charge

1 ms of BL pre-charge state, the CC and parasitic BJT effect are combined and this causes enhanced I_{BJT} in this study.

Herein, the row hammer effect due to CC effects, when data '1' and '0' are stored in SN, have been studied. Moreover, when the data '1' is stored, the degradation of potential at SN by parasitic BJT and CC effects has also been investigated.

II. DEVICE STRUCTURE AND SIMULATION METHOD

To investigate the CC and parasitic BJT effects, VS-DRAM with dual gate was adopted as shown in Fig. 1(a) [1]. The subthreshold slope of 96 mV/dec in I_d-V_g transfer curve was calibrated against the experimental data [1] using device parameters in Table 1. 5×10^2 cm^{-2} of the interface trap density is considered [9]. The device geometry and operation conditions are shown in Fig. 1 and Table 1. The bias values at WLs (V_{off}) and BL (1/2 V_{DD}) were set to -0.2 and 0.5 V, respectively. A bias of 2.5 V (V_{PP}) was applied at the WLs to access the cell. The line resistance (R_{WL}) and capacitance (C_{WL}) of WLs were set to 1 kΩ and 736 fF, respectively. The capacitance between WLs (C_{WL-WL}) was set to 234 fF [11], [12], [13]. The SN capacitance (C_{SN}) was set to 6 fF. When accessing the cell at position A (Fig. 1(c)), BL2 was maintained in a pre-charge state, while WL3 and WL4 were turned on and off for 12.5 and 24 ns, respectively. During the operations of writing '0' and '1' on the cell in position B (Fig. 1(c)), the on and off times of WL3 and WL4 were set to 12.5 and 24 ns, respectively. The on and off time for BL2 was set to 20 and 16.5 ns, respectively. When the parasitic BJT effect was investigated, BL2 was maintained in a pre-charge state over 1 ms. Then, repetitive accessing for the operation of writing '0' was performed on the cell in Position B (Fig. 1(c)) and the nonadjacent cell in Position C. Simulations for CC and parasitic BJT effects on VS-DRAM were performed at 300 K. The gate-induced drain leakage (GIDL) was considered using the Hurkx band-to-band tunneling (BTBT). Additionally, the inversion-accumulation layer mobility model, high-

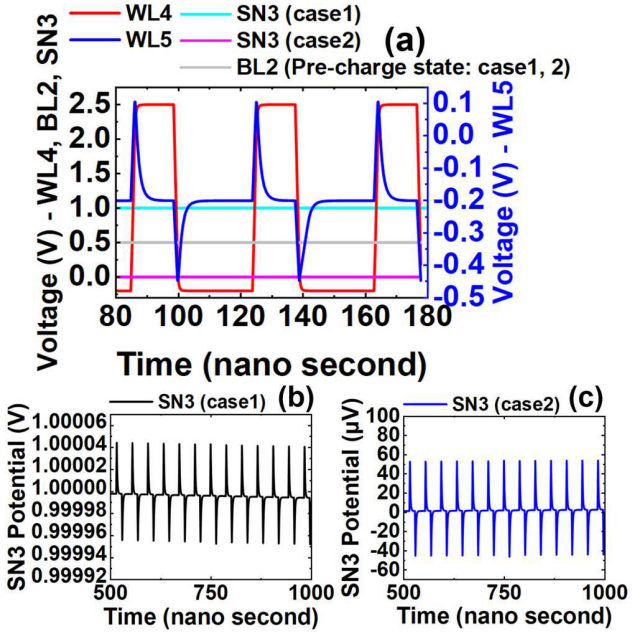

FIGURE 2. (a) Voltage waveforms at WL4, WL5, BL2 and SN3 for case1 and 2 simulations. SN3 potential (b) decrease in case1 simulation, and (c) increase in case2 simulation.

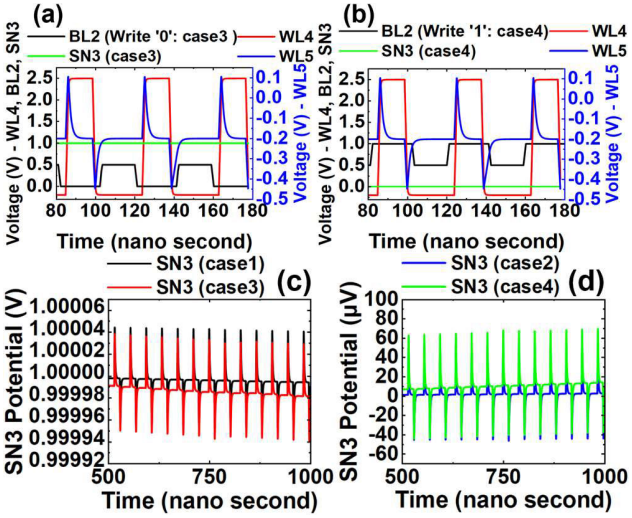

FIGURE 3. Voltage waveforms at WL4, WL5, BL2 and SN3 for (a) case3 and (b) case4 simulations. SN3 potential (c) decrease in case1 and case3 simulations, and (d) increase in case2 and case4 simulations.

field saturation, bandgap narrowing, avalanche generation-recombination model, and Shockley–Read–Hall recombination (doping- and temperature-dependent) were used. The modified local-density approximation (MLDA), quantum-mechanical model, is used for considering the confined carrier distribution.

III. RESULT AND DISCUSSION

A. POTENTIAL DEGRADATION BY CAPACITIVE CROSSTALK EFFECTS

Four simulations (cases1–4) were performed, under different conditions as shown in Table 2, to measure the leakage current caused by CC effects. Fig. 2(a) shows the pulses at WL4, WL5, BL2 and SN3 for investigating the CC effect on VS-DRAM. When a pulse was applied at WL3 and WL4 to access the cell in position A, the bias at WL5 reached a positive peak value of 0.1 V, when the bias at WL4 was approximately V_{PP}. After the pre-charge command was issued, the bias values at WL3 and WL4 returned to V_{off}, whereas the bias at WL5 reached a negative peak value of −0.45 V. As the bias at WL5 fluctuated, SN3 also experienced a transient increase or decrease in potential. As WL5 had a positive peak value, the potential barrier between the body and SN was reduced due to the temporarily increased bias at WL5. Consequently, the potential at SN3 increased due to the movement of electrons from the N^+ region, as shown in Fig. 2(b). The subthreshold leakage caused by the temporarily increased potential at WL5 degraded the potential at SN3. In the case1, the '1' data was written in SN3. As the cell in position A was repetitively accessed, the degradation of potential at SN3 was enhanced by the subthreshold leakage current. In the case2, the '0' data was written in SN3. Since the potential at BL2 was greater than the potential at SN3, the current flowed from BL2 to SN3 and the potential at SN3 gradually increased, as shown in Fig. 2(c). The potential degradation and increase at SN3 can be enhanced when writing '0' or '1' are performed at the cell in position B. Figs. 3(a) and (b) show the voltage waveforms for case3 and case4 simulations. In the case3, the data '1' at SN3 was written and the writing '0' operation is performed at the cell in position B. When an operation '0' was performed on a cell in position B that shares the same BL with the victim cell (SN3), the potential difference between SN3 and BL2 was greater than when BL was in a pre-charge state; this happened because the potential of BL was lowered to 0 V. Therefore, the subthreshold leakage was greater than when BL was in the pre-charge state and the potential degradation in the case3 was greater than in the case1. For the same reason, the potential increase at SN3 in the case4 was greater than in the case2. For investigating the row hammer tolerance (N_{RH}), the N_{RH} is defined as $0.1 \times V_{DD}/\Delta V_{SN}$ during 64 ms refresh period, where ΔV_{SN} is defined as the potential drop caused by a row hammer cycle [11], [14]. In general, the retention time should have a minimum value of 64 ms in the normal temperature range (273 K to 358 K) [15]. Since the potential fluctuation is gradually reduced as the potential difference between the SN3 and BL2 becomes smaller, ΔV_{SN} is extracted at 0.9 and 0.1 V of SN3. As a result, we found that N_{RH} has values of 367.9 and 457.8 k for case1 and case2, respectively and 117 and 167 k for case3 and case4. The results imply that the bit-flip can occur within the refresh period.

B. RETENTION DEGRADATION BY PARASITIC BIPOLAR JUNCTION TRANSISTOR AND CAPACITIVE CROSSTALK EFFECTS

The potential degradation by the parasitic BJT effect due to the floating body effect is investigated in Fig. 4 and 5.

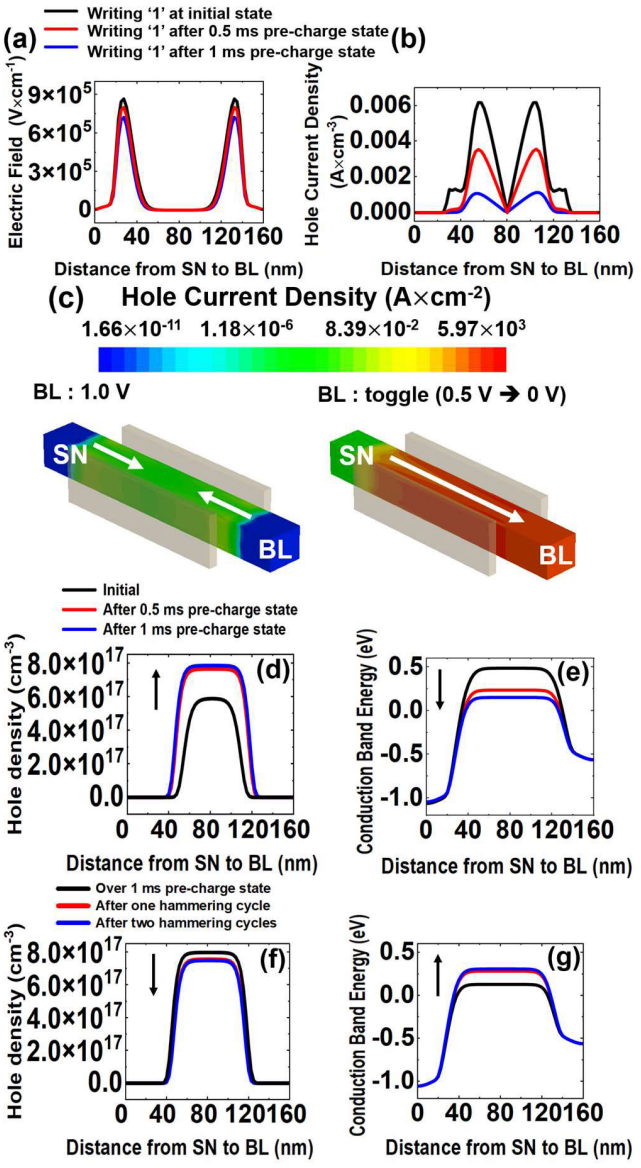

FIGURE 4. (a) E-field and (b) hole current density plots along the Y-Y′ arrow as a writing '1' operation is performed at a cell in position C after initial, 0.5 and 1 ms pre-charge state. (c) Hole current density when BL state is high and toggled to low. (d) Hole density and (e) CBE plots along the Y-Y′ arrow at initial, 0.5, and 1 ms pre-charge state. (f) Hole density and (g) CBE plots along the Y-Y′ arrow as BL is repeatedly toggled to low state.

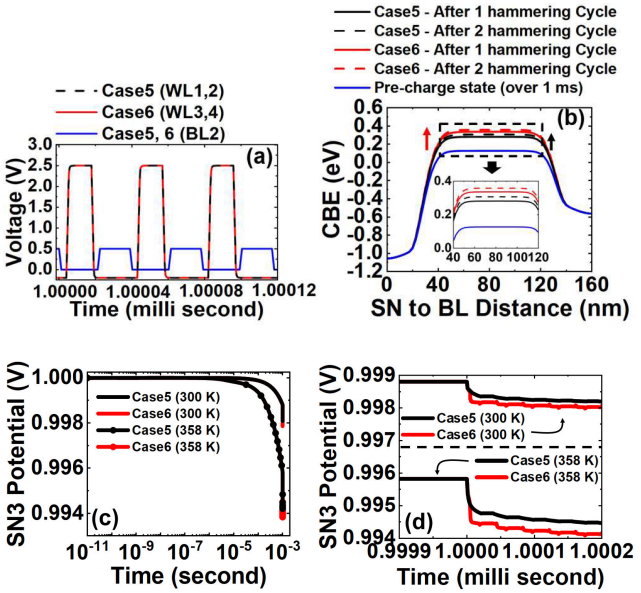

FIGURE 5. (a) Waveforms (BL and WL) for observing parasitic BJT and CC effects in case5 and case6. (b) CBE plot along the Y-Y′ arrow for case5 and 6 after hammering cycles at 300 K. Voltage degradation at SN3 (c) over time and (d) due to accessing at a cell in position C and B after 1 ms DRAM pre-charge state in the case5 and 6 at 300 and 358 K.

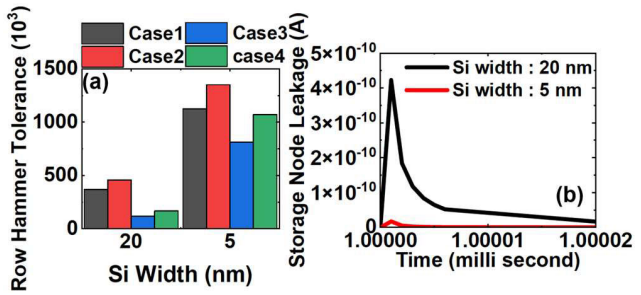

FIGURE 6. (a) Row hammer tolerance for case1, 2, 3, and 4 with the 20 and 5 nm of Si width. (b) Storage node leakage as I_{BJT} occurs for the 20 and 5 nm of Si width.

Fig. 4(a) and (b) show the E-field and hole current density as a writing '1' is performed at a cell in position C after the initial, 0.5 and 1 ms pre-charge state of BL2. The body of VS-DRAM is left floating for vertical stacking. When a data value of '1' is stored in the SN3, the capacitor is charged, and a large potential is applied to the SN3. This creates a strong E-field around the SN junction, which enhances the GIDL. In addition, when a write '1' operation is performed on a cell that shares the same BL2 with the victim cell, the BL2 rises from the pre-charge state to V_{DD}. Other cells connected by the same BL during that period are subjected to the high voltage of the BL, and a large E-field is generated around the BL junction. If the writing '1' operation is repetitively performed on the cell in position C, the victim cell suffers from the enhanced E-field near the BL (Fig. 4(a)). This enhances GIDL at the SN and BL and holes created via GIDL move toward the body owing to the strong positive potentials of the SN and BL, as shown in Fig. 4(b). As the number of writing operation cycles increases or the BL state is pre-charge state over 1 ms, the intensity of the E-field gradually decreases, resulting in a decrease in the GIDL effect and the hole density current. This is because the body potential is continuously increased by the holes accumulated on the side of the body owing to a long pre-charge state or repeated writing '1' operation. As a result, the potential difference between the body and the source/drain decreases. Thus, after 1 ms pre-charge state, as the writing '1' operation is performed on the cell in position C, the E-field near the SN3 and BL2 junctions decreases to 85.2% compared with the maximum E-field at the initial state as shown in Fig.4(a). Therefore,

holes accumulate more slowly as the E-field is decreased. Figs. 4(c), (d), (e), (f) and (g) illustrate the mechanism of the I_{BJT} that occurs when the BL2 is toggled to 0 V after 1 ms pre-charge state. When BL2 is in the pre-charge state over 1 ms, the CBE in the body is decreased to 0.127 eV by the potential increase due to hole accumulation as shown in Figs. 4(d) and (e). When the BL is toggled from 0.5 V to 0 V for writing '0' operation at the cell in position C, the difference between the CBE of the body in the victim cell and BL sharply decreases. Then, the holes accumulated in the body move to the BL (Fig. 4(c)) and the CBE is increased (Fig. 4(g)). After one hammering, remaining holes in the body can be drained to the BL by continuous hammering (Fig. 4(f)). As a result, the electrons in the BL move toward the SN, and SN leakage current occurs (Fig. 5(c) and (d)).

The pulses shown in Fig. 5(a) were applied at WL1, WL2, WL3, WL4 and BL2 to investigate I_{BJT} due to parasitic BJT and CC effects. In both simulations, the data '1' was written at SN3 and BL2 maintained in a pre-charge state for 1 ms. In the case5, after maintaining the pre-charge state for 1 ms, the writing '0' operation is performed at the cell in the position C. In the case6, the writing '0' operation is performed at the cell in position B. As shown in Figs. 5(c) and 5(d), the potential at SN3 degraded up to 1.39 mV after one writing operation was performed in case5 and 6. Since the enhanced GIDL due to the high temperature (358 K) caused greater hole accumulation than room temperature (300 K), the SN potential degradation became severe as I_{BJT} occurred. In the case6, it is found that the I_{BJT} was enhanced by the CC effect as shown in Fig. 5(d). When an operation of writing '0' was performed on the cell in position B, the accumulated holes reduced rapidly due to the temporary lowered CBE by the CC effect. Therefore, the CBE in case6 increased more rapidly than the CBE in case5, as shown in Fig. 5(b), and it caused the enhanced I_{BJT}. The leakage current caused by the parasitic BJT and CC effects could occur approximately 64 times during the refresh period. The enhanced I_{BJT} by the CC effect can cause tens of millivolts drop during the refresh period. The leakage current by the parasitic BJT and CC effects can be mitigated as the Si width is reduced. N_{RH} is increased to 1125.3, 1350.4, 812, and 1071.9 k (case1∼case4) as Si width decreases to 5 nm in Fig. 6(a). The peak I_{BJT} in 5 nm of Si width is decreased to 24.2 times compared with 20 nm of Si width in Fig. 6(b). This is due to decreased leakage current per a row hammering and hole accumulation by reduced Si width. Although the I_{BJT} can be significantly suppressed due to the reduction of the Si width, the N_{RH} of case 1, 3 and 4 in the VS-DRAM with 5 nm of Si width implies that the CC effect causes more severe reliability problem in the VS-DRAM.

IV. CONCLUSION

Comprehensive row hammer and parasitic BJT effects in VS-DRAM were studied using TCAD simulations. In VS-DRAM with a Si width of 20 nm, when '1' was written in SN3 during the case3 simulation, successive operations of writing '0' were performed on the cell in position B that shared the same BL2 with the victim cell. When '0' was written in SN3 during the case4 simulation, successive operations of writing '1' were performed on the cell in position B. In the case3 and 4 simulations, N_{RH} was 117 and 167 k. Furthermore, it was observed that the combination of parasitic BJT and CC effects could cause enhanced I_{BJT} and the potential can be more degraded during the refresh period. The reduced Si width can be adopted for mitigating the CC and parasitic BJT effects.

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