IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 4 September 2024, accepted 18 September 2024, date of publication 23 September 2024,
date of current version 18 December 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3465490

RESEARCH ARTICLE

Design of a 0.1–16GHz Reconfigurable Ultra-Wideband MMIC Power Amplifier

HEYANG SUN[1], JINGCHANG NAN[1], JIADONG YU[1], AND RUFEI WANG[2]
[1]College of Telecommunications, Liaoning Technical University, Huludao 125105, China
[2]College of Business Administration, Liaoning Technical University, Huludao 125105, China

Corresponding author: Heyang Sun (shy010504@163.com)

This work was supported in part by the National Natural Science Foundation under Project 61971210.

ABSTRACT This paper proposes a reconfigurable ultra-wideband power amplifier based on reconfigurable technology. The power amplifier consists of a gain module and reconfigurable bias circuits. The gain module is based on the structure of distributed amplifiers and innovates with peaking inductance and cascode structure to increase the output power and gain of the power amplifier. In addition, unlike the off-chip bias used in most distributed amplifiers, we have designed on-chip bias circuits through reconfigurable technology, which effectively improves the efficiency of the power amplifier and reduces the size of the chip. The power amplifier is designed to operate in the 0.1 to 16GHz, and it is capable of providing over 30dBm of output power in the operating band, with a stable gain of around 16dB and Power-Added-Efficiency (PAE) of 21%∼32%.

INDEX TERMS Reconfigurable, ultra-wideband, cascode, bias, MMIC.

I. INTRODUCTION

With the development of system generalization and multi-system integration of composite communication systems, the ultra-wideband (UWB) power amplifier (PA) has become an inevitable trend of development [1]. With the development of Monolithic Microwave Integrated Circuit (MMIC), GaAs HEMT, which has the advantages of high electron mobility, and high cut-off frequency [2], [3], [4], has become an effective way to research UWB PAs [5].

The techniques to realize UWB PA usually include negative feedback, continuous impedance matching, balanced structure and distributed amplifier (DA). DA is a special type of PA. In reference [6], negative feedback technology is used to expand the bandwidth of the power amplifier at the expense of low-frequency gain. Due to the frequency roll-off characteristics of the gain, this method is not suitable for the millimeter wave frequency range. The design process for continuous impedance matching is shown in reference [7] which achieves a bandwidth of 4 octaves. As the bandwidth requirement increases, the difficulty of this method will increase dramatically, and the circuit volume will become larger. The bandwidth of a balanced power amplifier is limited by both the amplifier and the coupler, as described in reference [8]. The reference [9] has cascaded the classical distributed structure with 3-stage, which achieves a bandwidth of 2.3∼21GHz, but the efficiency is low (PAE<20%). Utilizing a three-stack FET structure as a power-controllable gain unit, and employing a dual-gate bias control scheme on the bottom and middle FETs to reconfigure the output power, is the approach mentioned in reference [10], which does not yield high output power. In reference [11], optimizing the cutoff frequency of the drain line to reduce its losses for increased gain is discussed. However, this method is not suitable for wider bandwidth applications.

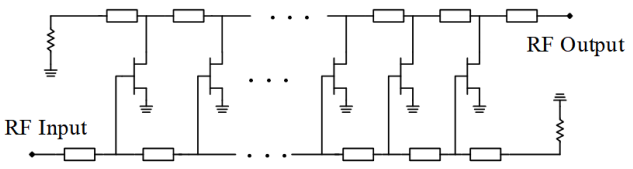


FIGURE 1. The topology of classic DA.

Fig.1 shows the topology of classic DA [12]. Because the parasitic capacitance and inductance of the transistors are

The associate editor coordinating the review of this manuscript and approving it for publication was Sungyong Jung.

absorbed by artificial transmission lines (ATL), DA can get rid of the gain-bandwidth-product limitation of traditional PAs and achieve a large bandwidth easily [13], [14], [15]. The output power and efficiency of the DA are low due to a large number of signal components absorbed by the terminal resistors [15], [16], [17]. Meanwhile, the bias of DA is usually off-chip, which increases its size and limits the development of DA [18].

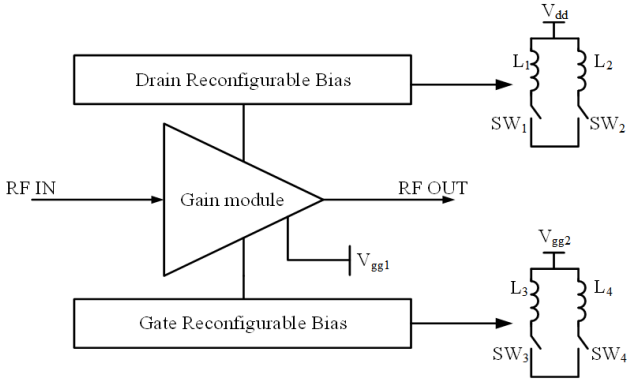


FIGURE 2. Structure of reconfigurable UWB PA.

Fig.2 shows the proposed reconfigurable UWB PA in this paper consists of a gain module based on DA structure and bias circuits based on reconfigurable technology.

In summary, this design has made a breakthrough in the efficiency, output power, gain, integration and other aspects of PA, which has a strong practical value.

II. THEORY AND DESIGN OF THE GAIN MODULE

In the classic DA topology shown in Fig.1, the common-source transistor output capability is weak. If the size of a single transistor is increased, although the output capacity is improved, the parasitic capacitance and resistance of the transistor will be increased at the same time, so that the bandwidth of PA will get narrower [19], [20]. In contrast, the advantages of stack technology are more obvious.

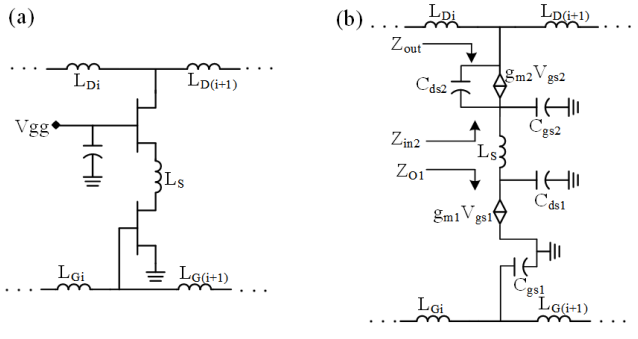


FIGURE 3. Cascode cell structure. (a) cascode cell circuits. (b) Equivalent model of the cascode cell.

As shown in Fig.3(a), the cascode cell is a typical structure of the stack technology. For one thing, it can connect two transistors in series to increase the output power by increasing the drain voltage; for another, the common-gate transistor can shield the influence of the voltage change of the output point on the performance of the cascode cell, which is conducive to the construction of the drain ATL. Moreover, to improve the high-frequency gain, a peaking inductance L_S is added to the cascode cell [21].

Fig.3(b) shows the equivalent model of cascode cell. Z_{O1}, Z_{in2}, and Z_{out} represent the equivalent intrinsic impedance of the common-source transistor, the input equivalent impedance of the common-gate transistor, and the equivalent intrinsic impedance of the cascode cell, respectively [22] and [23]. The analysis of the model shows that:

$$Z_{o1} = \frac{1}{j\omega C_{ds1}} \tag{1}$$

$$Z_{in2} = \frac{1}{j\omega C_{gs2} + g_{m2}} \tag{2}$$

$$Z_{out} = g_{m2}\frac{1 - \omega^2 L_s C_{ds1}}{\omega^2\left[\omega^2 L_s C_{ds1} C_{gs2} C_{ds2} - \left(C_{ds1} + C_{gs2}\right) C_{ds2}\right]} \tag{3}$$

The voltage gain A_V of the cascode cell can be expressed as:

$$A_V = g_{m1} g_{m2}\frac{Z_{o1} Z_{out}}{Z_{o1} + Z_{in2} + j\omega L_s} \tag{4}$$

It follows from Eq. (4) that A_V is a function of Z_{O1}, Z_{in2}, and Z_{out}, while Z_{O1} and Z_{in2} present capacitive impedances. Therefore, A_V is a frequency-sensitive variable that has an impact on the bandwidth and gain. In the structure proposed in Fig. 3, the inductive impedance of the peaked inductance L_S cancels out the capacitive impedance, thus improving the high-frequency gain of the cascode cell.

This design is based on a 0.15um GaAs process. The size of the two transistors in the cascode cell are 6*45um and 4*45um respectively. According to the above, the proposed gain module requires very high accuracy of the intrinsic parameters of the cascode cell, so the intrinsic parameters need to be extracted in the ADS with the help of Y-parameters. The intrinsic parameters can be extracted by the following equations:

$$C_{gd} = -\frac{im\left(Y_{12}\right)}{\omega} \tag{5}$$

$$C_{gs} = \frac{im\left(Y_{11}\right) - \omega C_{gd}}{\omega}\left[1 + \frac{\left(re\left(Y_{11}\right)\right)^2}{im\left(Y_{11}\right) - \omega C_{gd}}\right] \tag{6}$$

$$R_{gs} = \frac{re\left(Y_{11}\right)}{\left[im\left(Y_{11}\right) - \omega C_{gd}\right]^2 + \left[re\left(Y_{11}\right)\right]^2} \tag{7}$$

$$C_{ds} = \frac{im\left(Y_{22}\right) - \omega C_{gd} d}{\omega} \tag{8}$$

$$R_{ds} = \frac{1}{re\left(Y_{22}\right)} \tag{9}$$

When building two ATLs with a characteristic impedance of 50Ω, the intrinsic parameters of the cascode cell are

first characterised using the ideal capacitance model. The relationship between the characteristic impedance and cut-off frequency, of the ATL is shown in Eq. (10) and Eq. (11):

$$Z_0 = \sqrt{\frac{L}{C}} \tag{10}$$

$$f_C = \frac{1}{\pi\sqrt{LC}} \tag{11}$$

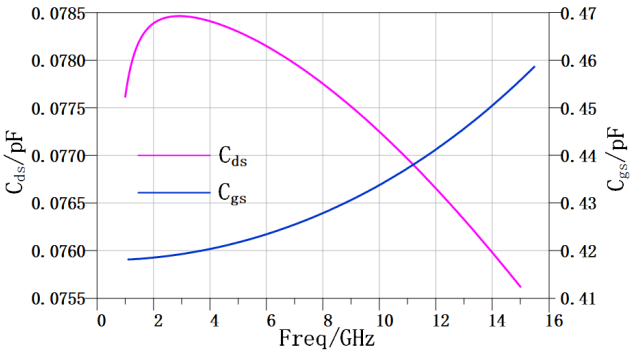


FIGURE 4. Results of intrinsic parameters extraction.

Fig. 4 shows that C_{gs} is much larger than C_{ds}, so the cut-off frequency of the gate ATL is much lower than that of the drain ATL, making the gate ATL become the main factor limiting the bandwidth of the PA. Therefore, ATLs should be modified. We make C_{gx} in series with C_{gs} to reduce the equivalent drain capacitance and C_{dx} in parallel with C_{ds} to increase the equivalent gate capacitance, thus achieving the same cut-off frequency for both ATLs [24]. The relationship between the two is shown in Eq. (12) and Eq. (13):

$$f_C = \frac{1}{\pi\sqrt{L_g C_{ge}}} = \frac{1}{\pi\sqrt{L_d C_{de}}} \tag{12}$$

$$Z_0 = \sqrt{\frac{L_g}{C_{ge}}} = \sqrt{\frac{L_d}{C_{de}}} \tag{13}$$

In the above equations, L_d and L_g denote the drain inductance and gate inductance respectively; C_{de} and C_{ge} denote the modified drain equivalent capacitance and gate equivalent capacitance respectively. C_{dx} and C_{gx} can be solved, according to Eq. (14) and Eq. (15).

$$C_{ge} = \frac{C_{gs}C_{gx}}{C_{gs}+C_{gx}} \tag{14}$$

$$C_{de} = C_{ds} + C_{dx} \tag{15}$$

The modified ATLs (at 6-stage, for example) are shown in Fig.5.

A comparison of the S-parameter simulation results for the modified ATLs and the typical ATLs is shown in Fig.6.

The simulation results show that the typical drain ATL cut-off frequency is much higher than 30GHz, while the typical gate ATL cut-off frequency only reaches 13GHz. If typical ATLs are used for the design of the proposed gain module, the bandwidth of it will drop below 13GHz.

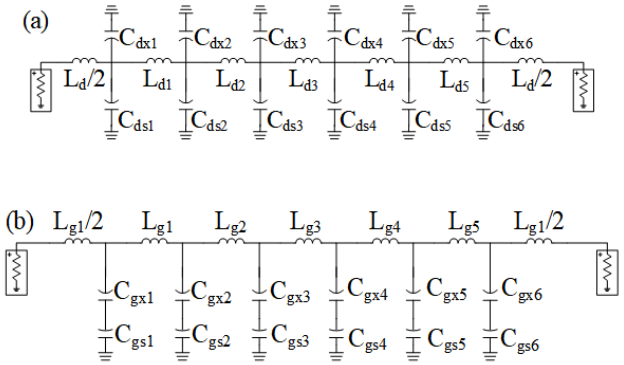


FIGURE 5. The circuit of ATLs. (a)Gate ATL. (b)Drain ATL.

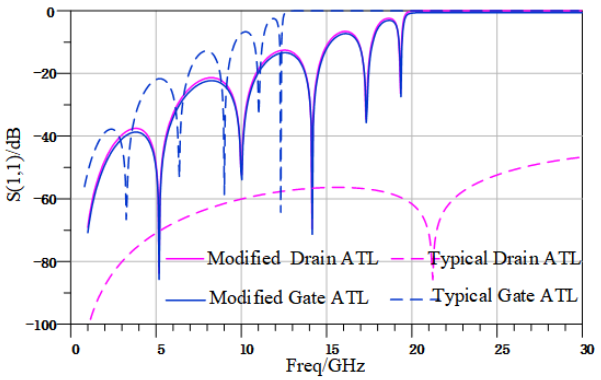


FIGURE 6. ATLs performance comparison.

The ATLs have been modified to have the same cut-off frequency and keep the signals in the same phase, giving full play to the gain module's output capability.

The design of the gain module part is completed by replacing C_{ds} and C_{gs} with cascode cells [25]. The circuit of the gain module is obtained by combining and adjusting the individual cells.

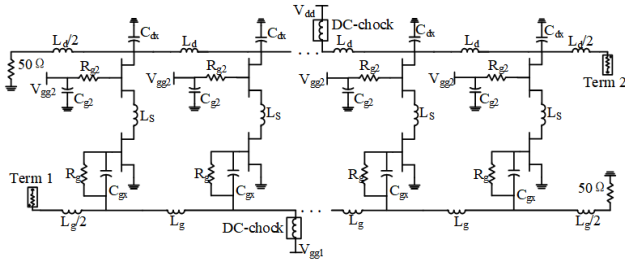


FIGURE 7. The circuit of gain module.

The gain module proposed in this paper is implemented using 6-stage cascode cells, with the duplicate cascode cells omitted in fig.7. R_g provides a DC path to the gate and together with C_{gx} forms a stable network; the C_{g2} provides the AC ground and in conjunction with the R_{g2}, the two ensure the absolute stability of transistors. Here, an ideal

DC-chock is used in the bias circuit. The handbook shows that the maximum withstand drain voltage for a single transistor is +6 V, so in this design V_{dd} is set to +10 V, V_{ggl} is set to −0.8 V and V_{gg2} is set to +3.7 V.

In fig8,small-signal simulation shows that S_{ll} is less than −10 dB in the DC ∼ 16GHz, proving that the gain module is well matched and can achieve broadband; the gain flatness is only ±0.8 dB and the gain is stable in this frequency range; S_{22} is less than 14 dB in this frequency range and the gain module is in an absolutely stable state.

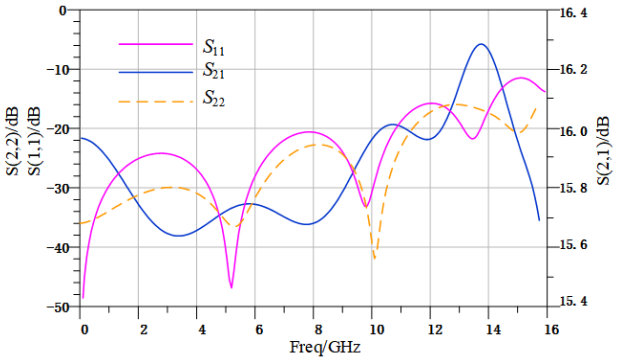


FIGURE 8. Small-signal simulation of gain module.

III. REALIZATION AND ANALYSIS OF RECONFIGURABLE BIAS

The ideal DC-chock used for powering the gain module cannot be applied in practice. At present, there is no better solution to the volume problem of off-chip bias and the performance problem of on-chip bias. In this section, the impact of bias on the performance of UWB PA will be analyzed and an effective solution will be proposed.

A. THE RECONFIGURABLE SCHEME OF BIAS

In the narration above, the gain module is not reconfigurable, gate and drain bias circuits are reconfigurable and can power the gain module. Under ideal conditions, looking outwards from the gain module, the impedance of the bias is infinite [26], but in fact, this condition is impossible to achieve. And the upper limit f_h and lower limit f_l of the operating bandwidth are influenced by the ratio of bias impedance Z_B to the load impedance Z_l, as follows:

$$\frac{f_h}{f_l} = \frac{\pi - \tan^{-1}(Z_B/Z_l)}{\tan^{-1}(Z_B/Z_l)} \tag{16}$$

From Eq. (16), it can be seen that to achieve a relatively large f_h/f_l when the load impedance is 50Ω, the bias requires a larger impedance. However, a fixed inductance cannot provide sufficient impedance for bias at UWB conditions. This is why the bias limits the bandwidth of the gain module.

Fig. 9 shows the equivalent model of an on-chip spiral inductance, then C_p and R_p represent the parasitic capacitance and parasitic resistance, respectively. L affects low-frequency performance and C_P affects high-frequency performance.

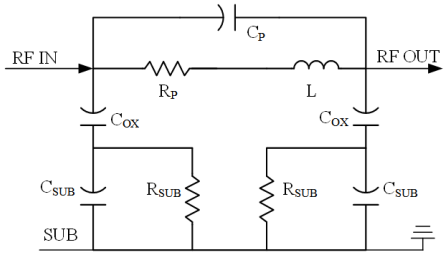


FIGURE 9. The spiral inductance equivalence model.

When using a spiral inductance as a choke, it is necessary to keep L as large as possible and C_P as small as possible. However, L and C_P are mutually restricted and cannot be achieved simultaneously. This is why the industry generally uses off-chip bias circuits, resulting in particularly large sizes.

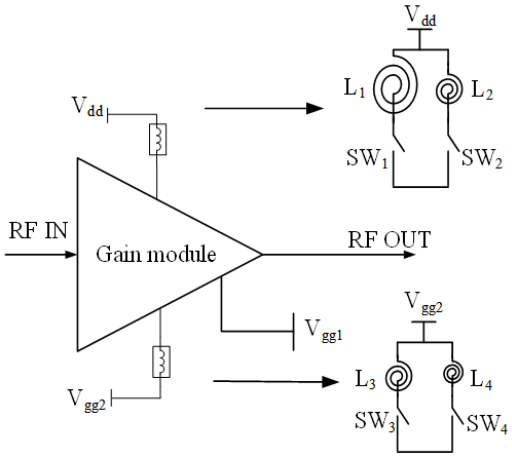


FIGURE 10. Reconfigurable scheme structure diagram.

The proposed reconfigurable scheme can perfectly break through these limitations and achieve on-chip bias. As shown in Fig.10, the design of switches 1-4 employs highly reliable MOSFET switches and utilizes a voltage-controlled switch device to connect the switches to L1-L4 respectively. Finally, protective circuits are designed to ensure that no damage to the power amplifier chip or signal distortion occurs during the switching process. By closing SW_1 and SW_3, large inductances are connected to the circuit to ensure the low-frequency performance of the gain module; by closing SW_2 and SW_4, small inductances are connected to the circuit to ensure the high-frequency performance of the gain module and overcome the influence of parasitic parameters.

B. SIMULATION OF RECONFIGURABLE BIAS

The lower the impedance of the bias, the better it is for UWB realization, but it can also cause signal leakage and reduce the efficiency of the DA. In order to achieve the best performance, the gate low-frequency mode requires higher maximum bias impedance at certain frequencies. The circuit was optimized according to the requirements

TABLE 1. PA operating mode control methods.

Mode	SW_1	SW_2	SW_3	SW_4	Band
Low	ON	OFF	ON	OFF	$0.1 \sim 6.5$GHz
High	OFF	ON	OFF	ON	$6.5 \sim 16$GHz

at different frequency ranges, and ultimately different bias impedances for the gate low-frequency mode were found to achieve optimal performance at different frequencies. The reconfigurable bias described in 3.1 was simulated and the results are shown in Fig.11.

The drain bias and gate bias provide high impedance to inhibit signal leakage from 0.1 to 20GHz. Two inductances for the low-frequency mode have self-resonance points greater than 10GHz, while two inductances for the high-frequency mode have the self-resonance points greater than 20GHz, avoiding the negative effects of self-resonant points on performance of gain module.

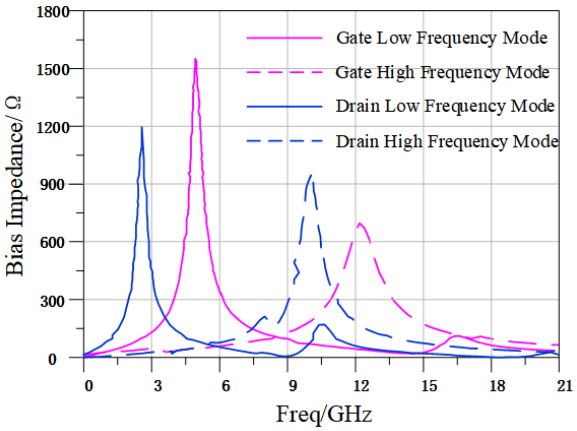


FIGURE 11. Simulation results of reconfigurable bias impedance.

IV. MEASUREMENT OF RECONFIGURABLE UWB PA

The inductances on the ATLs are replaced by microstrip lines, thus reducing the size of the chip. The overall circuit layout of reconfigurable UWB PA is shown in Fig.12.

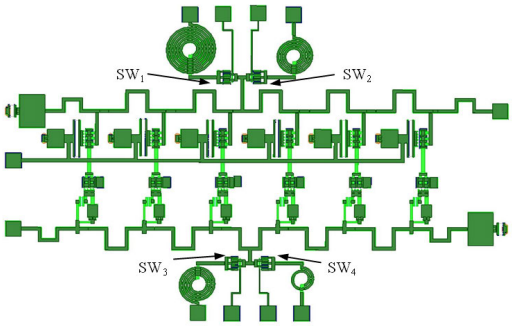


FIGURE 12. The overall circuit layout.

Fig 13 shows the chip photograph of the fabricated UWB power amplifier. After tape-out, the size of the chip is 5.88 mm^2 (3.03 × 1.94 mm). Fig 14 presents the

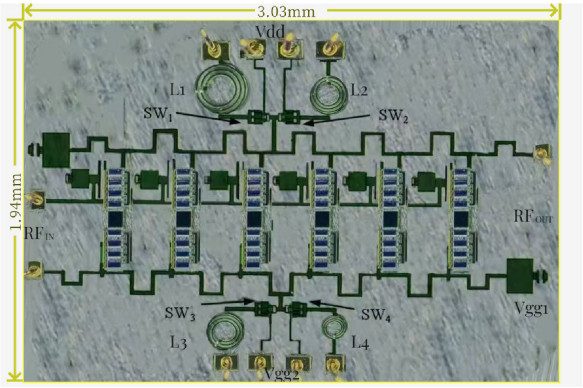


FIGURE 13. Chip photo of the fabricated UWB PA.

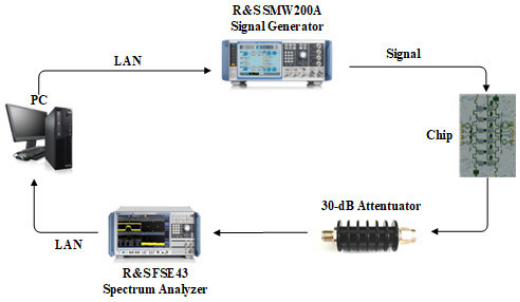


FIGURE 14. Large-signal measurement results.

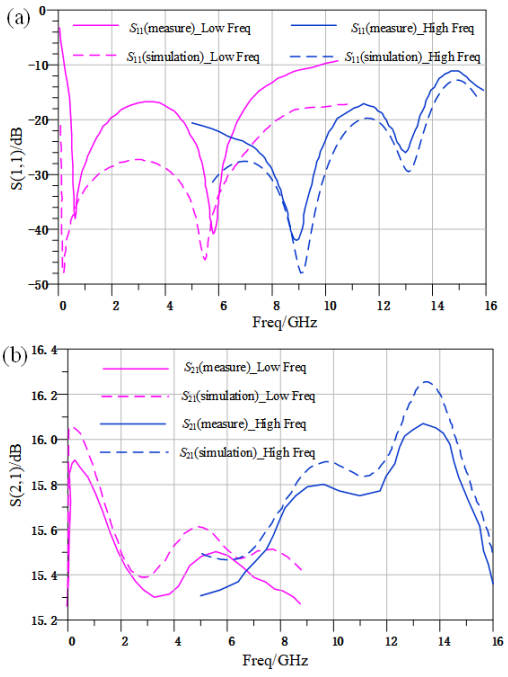


FIGURE 15. Comparison diagram of small signal test and simulation. (a) S_{11} curves. (b) S_{21} curves.

measurement setup for both large-signal and modulated signals, along with the flowchart of the entire testing procedure. We have divided the PA into two operating modes, high frequency and low-frequency, and the control method is shown in Tab.1.

Firstly,small-signal measurement and analysis of the PA show that it has typical frequency reconfiguration characteristics. PA can perform frequency-reconfiguration at 6.5GHz. As shown in Fig 15, S_{11} is less than -10 dB for two operating modes; S_{21} stays near 16 dB, and the gain flatness is maintained at ± 0.4 dB.

Next, we performed a large-signal measurement on this PA using continuous waves. The results are shown in Fig.16. The results show that the gain flatness is less than ± 1 dB and the gain is maintained at a stable level. The PAE reaches around $21\% \sim 32\%$, significantly higher than classic PA.

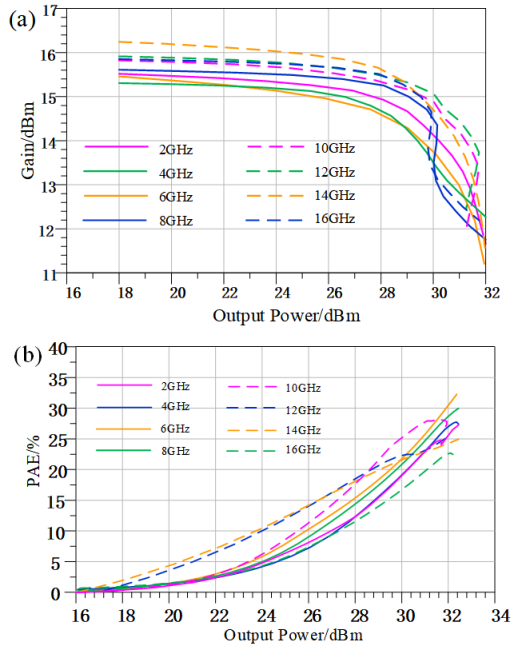


FIGURE 16. Large-signal measurement results.

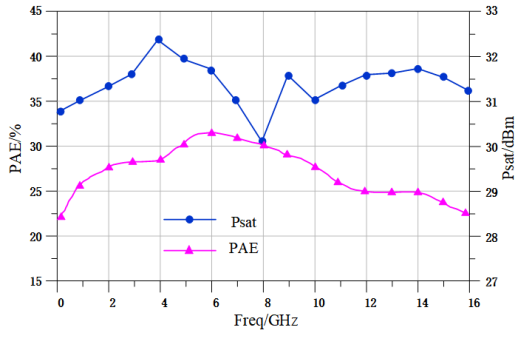


FIGURE 17. Frequency-domain measurement results.

Finally, the measurement results of PA in the frequency domain are shown in Fig.17. The proposed PA is capable of maintaining a saturation output power of more than 30dB at 0.1 to 16GHz. Compared to traditional DAs (PAE is generally less than 20%), the PA proposed in this paper always maintains the adaptation of the bias and gain module, reducing the leakage of RF signals and increasing the PAE to 21%∼32%.

The analysis above shows that there is a degree of deterioration in PA performance at f_h and f_l. This is due to the fact that in this paper the analysis is mainly carried out with 2 -stage of reconfigurable inductance, with relatively low fitness at f_h and f_1. In practice, more inductances can be used to achieve finer band divisions and increase the fitness of the bias for the entire operating band. The scheme in this paper is therefore high expansibility.

TABLE 2. Performances compared with PA proposed in other articles.

Ref	Bandwidth/GHz	Gain/dB	Psat/dBm	PAE/%	Size/mm^2	Bias
[27]	7	23.2	> 40	> 28.8	11.55	Off-chip
[28]	6.5	14	30	$18 \sim 24$	7.5	Off-chip
[29]	12	15.3	40.3	$16 \sim 27$	13.8	Off-chip
This work	15.9	16	> 30	$21 \sim 32$	5.88	On-chip

V. CONCLUSION

In this paper, a reconfigurable UWB PA is proposed based on reconfigurable technology. We have increased the output power of the PA through cascode cells and modified ATLs. In addition, by using reconfigurable technology, this paper breaks through the limitations of off-chip bias and on-chip spiral inductances on the UWB PA and achieves integration. Based on the above scheme, we have designed a reconfigurable UWB PA operating from 0.1 to 16 GHz using a 0.15um GaAs process. It is capable of providing over 30dBm of output power in the operating band, with a stable gain of around 16dB and PAE of 21%∼32%. This paper provides a new scheme for UWB PA research by achieving a breakthrough in gain, bandwidth, and efficiency through an innovative structure.

REFERENCES

[1] K. Y. Yap, H. H. Chin, and J. J. Klemeš, "Future outlook on 6G technology for renewable energy sources (RES)," *Renew. Sustain. Energy Rev.*, vol. 167, Oct. 2022, Art. no. 112722, doi: 10.1016/j.rser.2022.112722.

[2] M. Chegini, J. Yavandhasani, and M. Kamarei, "A new design for mode transfer-based harmonic tuned power amplifier (MHPA)," *AEU Int. J. Electron. Commun.*, vol. 155, Oct. 2022, Art. no. 154335, doi: 10.1016/j.aeue.2022.154335.

[3] Y. Lu, X. Xu, H. Han, B. Zhao, H. Zhang, Z. Zhao, C. Yi, Y. Wang, L. Guo, and X. Ma, "A UHF-band 100 W broadband hybrid GaN power amplifier based on the regional modulation of impedance distribution method," *AEU Int. J. Electron. Commun.*, vol. 141, Nov. 2021, Art. no. 153959, doi: 10.1016/j.aeue.2021.153959.

[4] N. V. Dien, N. V. Tuan, L. T. P. Mai, N. V. Hieu, V. Q. Phuoc, N. Q. N. Quynh, and N. T. Hung, "Tolerance of SCM Nyquist and OFDM signals for heterogeneous fiber-optic and millimeter-wave mobile backhaul links under the effect of power amplifier saturation induced clipping," *Comput. Netw.*, vol. 204, Feb. 2022, Art. no. 108697, doi: 10.1016/j.comnet.2021.108697.

[5] S. Hao, Y.-W. Tang, X. Ding, L. Du, Y. Du, A. Tang, Q. J. Gu, and M. F. Chang, "An 8.3% efficiency 96–134 GHz CMOS frequency doubler using distributed amplifier and nonlinear transmission line," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2020, pp. 1–2, doi: 10.1109/A-SSCC48613.2020.9336113.

[6] L. Y. Shen and D. B. Yang, "Broadband linear power amplifier based on GaN HEMT," *Semicond. Technol.*, vol. 45, no. 3, pp. 195–199, 2020, doi: 10.13290/j.cnki.bdtjs.2020.03.004.

[7] J. C. Nan, Z. Li, and X. Y. Nan, "Reconfigurable continuous class F ultra wideband power amplifier," *J. Electron. Meas. Instrum.*, vol. 36, no. 5, pp. 67–77, 2022, doi: 10.13382/j.jemi.B2104882.

[8] Z. Yin and H. Q. Tao, "X-band 20W high efficiency load modulation balanced amplifier MMIC," *Prog. Solid State Electron.*, vol. 42, no. 1, pp. 5–9, 2022.

[9] E. B. Moustapha, E. Hanae, A. T. Naima, and E. Taj-Eddin, "2.3–21 GHz broadband and high linearity distributed low noise amplifier," *Integration*, vol. 76, pp. 61–68, Jan. 2021, doi: 10.1016/j.vlsi.2020.09.005.

[10] J. Kim, Y. Kim, S. Lee, J. Jeong, and Y. Kwon, "A broadband power-reconfigurable distributed amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2012, pp. 1–3, doi: 10.1109/MWSYM.2012.6259761.

[11] Z. Lin, J. Li, Y. Chen, Y. Guo, R. Xu, B. Yan, L. Luo, Q. Wang, K. Kang, and Y. Xu, "A millimeter-wave ultra-wideband non-uniform distributed power amplifier with improved efficiency," in *Proc. 13th U.K.-Eur.-China Workshop Millimetre-Waves THz Technol. (UCMMT)*, Aug. 2020, pp. 1–3, doi: 10.1109/UCMMT49983.2020.9295977.

[12] L. Diego, B. Haentjens, C. A. Mjema, I. Barrutia, A. Herrera, and Y. Haentjens, "A DC to 40 GHz, high linearity monolithic GaAs distributed amplifier with low DC power consumption as a high bit-rate pre-driver," in *Proc. 15th Eur. Radar Conf. (EuRAD)*, Sep. 2018, pp. 497–500, doi: 10.23919/EuRAD.2018.8546599.

[13] P. V. Testa, C. Carta, U. Jörges, and F. Ellinger, "Analysis and design of a 30- to 220-GHz balanced cascaded single-stage distributed amplifier in 130-nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1457–1467, May 2018, doi: 10.1109/JSSC.2018.2797240.

[14] C.-H. Han and H.-Q. Tao, "A 18-40 GHz 10W GaN power amplifier MMIC utilizing combination of the distributed and reactive matching topology," in *Proc. 14th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2019, pp. 228–231, doi: 10.23919/EuMIC.2019.8909556.

[15] T. Jyo, M. Nagatani, M. Ida, M. Mutoh, H. Wakita, N. Terao, and H. Nosaka, "A 241-GHz-bandwidth distributed amplifier with 10-dBm P1dB in 0.25-μm InP DHBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1430–1433, doi: 10.1109/MWSYM.2019.8700975.

[16] U. Çelik and P. Reynaert, "Robust, efficient distributed power amplifier achieving 96 Gbit/s with 10 dBm average output power and 3.7% PAE in 22-nm FD-SOI," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 382–391, Feb. 2021, doi: 10.1109/JSSC.2020.3020229.

[17] T. Shivan, E. Kaule, M. Hossain, R. Doerner, T. Johansen, D. Stoppel, S. Boppel, W. Heinrich, V. Krozer, and M. Rudolph, "Design and modeling of an ultra-wideband low-noise distributed amplifier in InP DHBT technology," *Int. J. Microw. Wireless Technol.*, vol. 11, no. 7, pp. 635–644, Sep. 2019, doi: 10.1017/s1759078719000515.

[18] C. V. Vangerow, D. Stracke, D. Kissinger, and T. Zwick, "Variable gain distributed amplifier with capacitive division," in *Proc. 13th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2018, pp. 281–284, doi: 10.23919/EuMIC.2018.8539959.

[19] O. El-Aassar and G. M. Rebeiz, "A cascaded multi-drive stacked-SOI distributed power amplifier with 23.5 dBm peak output power and over 4.5-THz GBW," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 3111–3119, Jul. 2020, doi: 10.1109/TMTT.2020.2984226.

[20] P. V. Testa, B. Klein, R. Hahnel, C. Carta, D. Plettemeier, and F. Ellinger, "140–220-GHz distributed antenna and amplifier co-integrated in SiGe BiCMOS process for UWB receivers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2018, pp. 1515–1518, doi: 10.1109/MWSYM.2018.8439496.

[21] G. Du, Q. Li, and S. Zhang, "Design of a 0.1–40 GHz distributed broadband power amplifier," in *Proc. Int. Conf. Microw. Millim. Wave Technol. (ICMMT)*, Sep. 2020, pp. 1–3, doi: 10.1109/ICMMT49418.2020.9386581.

[22] S. Lee, I. Ju, Y. Gong, A. S. Cardoso, J. D. Connor, M.-K. Cho, and J. D. Cressler, "Design of an 18–50 GHz SiGe HBT cascode non-uniform distributed power amplifier," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2020, pp. 1–4, doi: 10.1109/BCICTS48439.2020.9392963.

[23] S. A. Zavyalov, K. V. Murasov, R. R. Fakhrutdinov, A. N. Liashyk, V. Y. Shein, and V. V. Erokhin, "Broadband low noise distributed-gain amplifier designed in 130 nm process," in *Proc. 20th Int. Conf. Young Spec. Micro/Nanotechnologies Electron Devices (EDM)*, Jun. 2019, pp. 119–123, doi: 10.1109/EDM.2019.8823198.

[24] O. El-Aassar and G. M. Rebeiz, "A DC-to-108-GHz CMOS SOI distributed power amplifier and modulator driver leveraging multi-drive complementary stacked cells," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3437–3451, Dec. 2019, doi: 10.1109/JSSC.2019.2941013.

[25] J.-S. Moon, J. Kang, D. Brown, R. Grabar, D. Wong, H. Fung, P. Chan, D. Le, and C. McGuire, "Wideband linear distributed GaN HEMT MMIC power amplifier with a record OIP3/Pdc," in *Proc. IEEE Topical Conf. Power Modeling Wireless Radio Appl. (PAWR)*, Jan. 2016, pp. 5–7, doi: 10.1109/PAWR.2016.7440127.

[26] M. Zhu and C. M. Wu, "Reconfigurable series feed network for squint-free antenna beamforming using distributed amplifier-based negative group delay circuit," in *Proc. 49th Eur. Microw. Conf. (EuMC)*, Oct. 2019, pp. 256–259, doi: 10.23919/EuMC.2019.8910773.

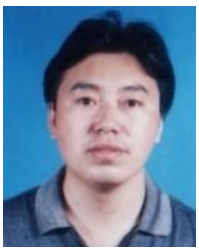
[27] L.-L. Hu, D.-H. Hu, H.-F. Wu, Q. Lin, Y.-N. Hua, S.-W. Chen, and X.-M. Zhang, "An ultra-wideband GaAs pHEMT distributed power amplifier," in *Proc. IEEE 4th Adv. Inf. Technol., Electron. Autom. Control Conf. (IAEAC)*, vol. 1, Dec. 2019, pp. 2144–2147, doi: 10.1109/IAEAC47372.2019.8997602.

[28] H. Park, H. Nam, K. Choi, J. Kim, and Y. Kwon, "A 6–18-GHz GaN reactively matched distributed power amplifier using simplified bias network and reduced thermal coupling," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 6, pp. 2638–2648, Jun. 2018, doi: 10.1109/TMTT.2018.2817521.

[29] C. H. Han and H. Q. Tao, "1 ∼ 8 GHz GaN 10 W balun distributed power amplifier," *Prog. Solid State Electron.*, vol. 39, no. 3, pp. 159–162, 2019, doi: 10.19623/j.cnki.rpsse.2019.03.002.

HEYANG SUN received the B.S. degree in electronic science and technology from Liaoning Technical University, Huludao, China, in 2023, where he is currently pursuing the master's degree.

He is with the School of Electronic and Information Engineering, Liaoning Technical University. His current research interests include RF circuits and monolithic microwave integrated circuits (MMICs).



JINGCHANG NAN received the Ph.D. degree in electromagnetic field and microwave technology from Beijing University of Posts and Telecommunications, Beijing, China, in 2007.

He was a Senior Visiting Scholar with the University Michigan, in 2012, ICNC-FSDK2013, and CISP-BMEI2014; the Chairman of the CISP-BMEI2015 Organizing Committee; and the Leader of the First-Level Discipline of Information and Communication Engineering, Liaoning Technical University. He is currently the Dean, a Professor, and a Doctoral Supervisor with the School of Electronics and Information Engineering, Liaoning Technical University, and a Distinguished Professor of Liaoning Province. His current research interests include RF circuits and systems, electromagnetic field and microwave technology, and communication signal processing and information processing.

JIADONG YU was born in 2000. He received the B.S. degree in electronic information engineering from Dalian Jiaotong University, Dalian, China, in 2022. He is currently pursuing the M.E. degree with Liaoning Technical University, Huludao, China.

His research interests include broadband power amplifier design, highly efficient power amplifiers, and monolithic microwave integrated circuits (MMICs).

RUFEI WANG received the bachelor's degree in international trade from Liaoning Technical University, Huludao, China, in 2023, where she is currently pursuing the master's degree.

She is with the School of Business Administration, Liaoning Technical University. Her current research interests include supply chain management and business administration.