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RESEARCH ARTICLE

A New Single Stage Common Ground Five-Switch Boosting Transformerless Inverter

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ABSTRACT Transformerless inverters (TIs) are widely employed in photovoltaic (PV) applications due to their cost-effectiveness, compact size, low weight, and high efficiency. However, the absence of electrical isolation can result in ground leakage current due to the parasitic behavior of PV systems, resulting in safety concerns and compromised power quality. Conventional five-level common-ground inverters can eliminate ground leakage current through the common-ground technique and achieve double voltage boosting capability. However, this topology necessitates a considerable amount of capacitance to efficiently minimize voltage ripple due to the extended discharge time during the negative half-cycle. Moreover, the high capacitance raises concerns regarding the potential for high current stress on switches during charging modes. In this article, a new single-stage common-ground boosting transformerless inverter is introduced. The proposed topology has fewer components, a lower number of conducting devices, and reduced capacitance requirements. The proposed topology can also be extended to three-phase applications using a single power source. The article includes explanations of the proposed topology, the control method, the component design process, and the power loss calculations. In addition, a comparison with similar topologies is conducted to highlight the advantages and disadvantages of the proposed topology. Simulation results are included to confirm the functionality and practicality of the proposed topology. Finally, experimental results for a 500-W prototype operating in a closed-loop system under different loads and load changes are presented. The converter demonstrates its capability in both buck and boost modes, achieving a high efficiency of over 95%.

INDEX TERMS Buck-boost inverter, common-ground inverter, leakage current elimination, single stage inverter.

I. INTRODUCTION

Worldwide endeavors to secure sustainable energy supplies have driven the advancement of grid-connected photovoltaic (PV) and fuel cell systems, signifying a noteworthy transition towards the production of renewable energy [1], [2]. Inverters are key in integrating these sources into existing infrastructure, particularly grid-tied inverters for PV systems, which are gaining popularity due to falling panel costs. However, challenges like common mode (CM) currents threaten system efficiency and safety [3]. Traditional transformers made from iron and copper are commonly used in PV systems to prevent leakage current. However, they come with drawbacks, increasing the size and cost of inverter systems while reducing efficiency and power density [4].

In response to these challenges, researchers and engineers have developed transformerless inverter solutions to enhance efficiency and reduce the footprint and cost. The absence of transformers in these configurations removes the weight and size limitations associated with traditional setups, rendering them more agile and adaptable to diverse applications. However, this transition has necessitated more attention to safety standards, particularly in terms of mitigating potential hazards, including ground fault and leakage currents due to

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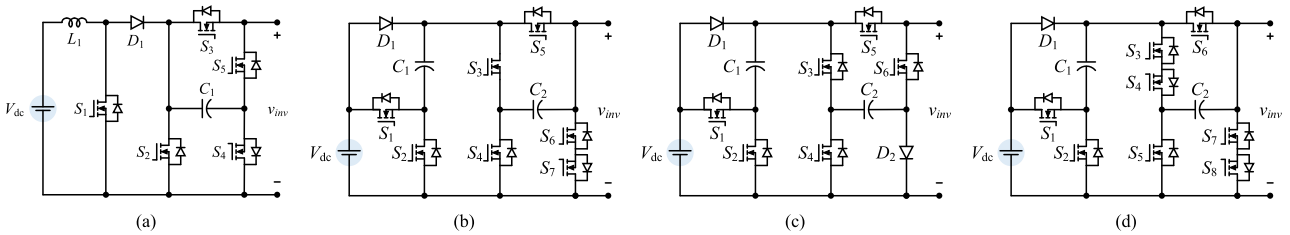

FIGURE 1. Existing transformerless inverter topologies. (a) [20], (b) [26], (c) [29], and (d) [30].

the parasitic capacitance between the PV panels or fuel cell systems and ground [5].

The single-phase transformerless H-bridge inverter is known for its efficient utilization of DC input voltage and ability to generate a three-level output voltage with a high-quality AC output voltage. However, traditional H-bridge inverters can only adjust the output voltage within the range of the supplied input voltage, essentially functioning as a buck converter. In low-voltage PV systems, the inverter needs to increase the output voltage to meet the grid voltage level. The simplest method to achieve this is to use multiple DC sources to increase the DC voltage on the H-bridge's input side [6]. However, increasing the number of DC sources also increases the number of switches and independent DC voltage sources, resulting in higher voltage stresses on the H-bridge. This can result in voltage source imbalance issues, adding complexity and cost to the system.

An intriguing solution to these issues is to combine a DC-DC boost converter with an H-bridge inverter to perform boost functionality. This allows for adjustment of the output voltage to create a stable voltage transformation, regardless of grid conditions. However, the presence of the H-bridge inverter in the power conversion interface eliminates the possibility of having a common ground (CG). Consequently, this results in the emergence of common-mode voltage (CMV) and leakage current, even when utilizing a DC-DC converter with a shared ground connection with the input source [7]. Reduced efficiency is another disadvantage of the two-stage power conversion structure, which primarily originates from significant losses across the boost converter. These issues can potentially affect the system's performance and must be carefully addressed during the design process [8].

In an effort to address the disadvantages associated with the H-bridge, researchers have explored advanced H-bridge designs [9], [10], [11], [12]. Fundamentally, the aim of these derived H-bridge structures is to reduce leakage current. They can be broadly classified into two primary categories: DC and AC decoupling. The developed DC decoupling techniques include H5 [9], oH5 [10], and H6 [11]. H5 improves the conventional H-bridge design by adding a switch on the positive DC rail, while oH5 and H6 enhance the design further by incorporating two switches and a split capacitor on the DC side. The AC decoupling technique has also gained widespread recognition and is notably represented by HERIC [12], which incorporates two extra switches coupled at the output of the H-bridge to achieve AC side decoupling. However, the problem of leakage current remains a challenge in these inverter structures. Furthermore, conduction losses and the inability to boost voltage during inverter operation are significant limitations associated with these interconnected inverter structures.

Common ground inverter topologies have been extensively investigated as a viable approach for mitigating leakage current [13]. Here, the common-mode voltage is effectively regulated to zero by establishing a direct connection between the neutral line of the grid and the negative of the PV panels. This approach is exemplified by the virtual DC-bus inverter presented in [14], which comprises five switches and a single capacitor, designated as a virtual capacitor. This is charged in the positive half-cycle and discharged in the negative half-cycle. However, a key drawback of this design is the absence of a pathway to charge the capacitor during the negative cycle, resulting in the output having high levels of total harmonic distortion (THD). Several other similar structures based on the virtual DC-bus concept have been introduced [15], [16], [17], [18], [19]. However, these structures usually only provide the buck feature and require a front-end DC–DC converter for the boost feature. In [20], a fundamental boost circuit was integrated into the virtual DC-bus inverter to provide a boosting capability, as displayed in Fig. 1(a). This structure employs five power switches, which incur significant switching losses due to high-frequency operation during the entire output cycle. Furthermore, it only delivers a two-level output voltage and requires a large output filter. The switched-boost CG inverter in [21] uses seven switches and provides a five-level output voltage, resulting in reduced output filter size and enhanced power quality. However, the voltage stress on the switches is high and requires a large capacitance, which is achieved through virtual capacitors. The single-stage CG five-level inverter in [22] offers boosting functionality, although it requires a higher number of switches. In a different approach, a single-stage CG inverter was detailed in [23] that employs a quasi-Z-source network to achieve the boost feature. In [24], a similar voltage-boosting solution employing two inductors is used within the boosting network. However, these topologies incorporate bulky inductance components that increase the overall size of the system.

Another solution to achieve voltage-boosting functionality involves employing a structure based on the switched capacitor (SC) unit [25]. This method requires a converter

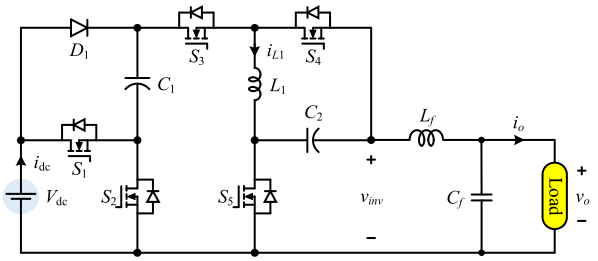

FIGURE 2. Proposed CG-5S-BTI.

TABLE 1. Switching states of the proposed CG-5S-BTI.

AC output	Switches states						Mode
	S_1	S_2	S_3	S_4	S_5	D_1	
Positive half cycle	1	0	1	1	0	0	I
	0	1	1	1	0	1	II
	0	1	0	1	1	1	III
Negative half cycle	0	1	1	0	1	1	IV
	0	1	0	1	1	1	V

comprising two switches, one capacitor, and one diode. SC-based topologies for voltage boosting and achieving enhanced efficiency were investigated in [26], [27], [28], [29], and [30]. In [26], as depicted in Fig. 1(b), and [27], these topologies required the use of seven and six switches, respectively, to achieve a three-level output voltage and doubled boost capacity. In [28], research on three-level inverters achieved a triple-boost voltage, although it required the use of nine switches. Generally, these three-level designs have resulted in higher device stresses. To mitigate voltage stresses on the components, conventional five-level common-ground inverters have been introduced [29], [30], as displayed in Fig. 1(c) and 1(d), respectively. These highlight the advantage of achieving double voltage boosting while generating a five-level output voltage. However, all these topologies depended on a large capacitor to produce a negative output voltage, raising concerns about high current stress of switches when the large capacitors are charging, potentially affecting inverter lifespan.

In this article, a new single-stage common ground five-switch boosting transformerless inverter (CG-5S-BTI) is introduced. This structure is capable of eliminating leakage current by providing a common ground between input and output terminals. Additionally, it achieves a buck-boost operation with a voltage boost factor of two, eliminating the need for virtual DC-link capacitors and reducing peak current stress on the switches. The proposed inverter operates within a single stage, reducing the number of switches and minimizing the number of switches operating at high switching frequency in each cycle, which lowers switching losses during power conversion, enhancing efficiency and reliability. A control strategy for the switches is implemented, ensuring synchronous operation between the positive and negative half-cycles of the output voltage. Moreover, by combining three CG-5S-BTI modules without requiring any redesign, it is possible to create a new three-phase inverter system that maintains a single power source and common ground characteristics.

The remaining sections of this article are organized as follows: Section II presents a full description of the proposed topology, control method, and three-phase expansion structure. Section III focuses on the design criteria, encompassing the evaluation of current and the size of passive components. Section IV provides the loss calculation for the proposed inverter, while Section V presents a comparative analysis of the various topologies. Section VI includes the outcomes of the simulations and experimental investigations, and Section VII presents the conclusions.

II. PROPOSED CG-5S-BTI

Fig. 2 depicts the design of the proposed CG-5S-BTI, which is configured to achieve a voltage output of twice the input voltage by combining a CG-5S-BTI with one boost SC converter and one buck-boost converter. The inverter consists of five power switches (S_1, S_2, S_3, S_4, and S_5), two capacitors (C_1 and C_2), one inductor (L_1), one diode (D_1), and an LC filter (L_f, C_f) located at the output of the inverter. The boost SC converter comprises components S_1, S_2, D_1 and C_1, while the buck-boost converter is composed of L_1, S_3, S_4, S_5, and C_2.

Among the five switches (S_1–S_5), S_1 and S_2 always operate at a high frequency when the output voltage is higher than the input voltage. Conversely, when the output voltage is lower than the input voltage, S_1 turns off, S_2 remains on, and S_3 operates at a high frequency during the output cycle. S_4 and S_5 only operate at a high frequency during the negative and positive half-cycles, respectively.

By connecting the negative terminal of the output inverter in Fig. 2 to the negative terminal of the input DC source, all leakage currents are eliminated. This characteristic obviates the need for a common-mode filter and enhances overall system efficiency.

A. OPERATION MODES

This section of the paper provides a comprehensive overview of the operational modes of the proposed CG-5S-BTI, covering both the positive and negative half-cycles of the output voltage waveform.

There are five operating modes of the proposed CG-5S-BTI, with three modes (I - III) operating during the positive half-cycle and two modes (IV and V) operating during the negative half-cycle. Table 1 presents the various possible states of the switches in the proposed CG-5S-BTI.

The equivalent electrical circuit for the inverter's operational modes during the positive half-cycle is depicted in Fig. 3(a)–(c). Additionally, Fig. 4(a) and (b) illustrate the equivalent electrical circuit for the operational modes during the negative half-cycle. In these figures, the blue dashed line depicts the path of the current through capacitor C_1, while the green and orange dashed lines depict the paths of the currents through inductors L_f and L_1, respectively.

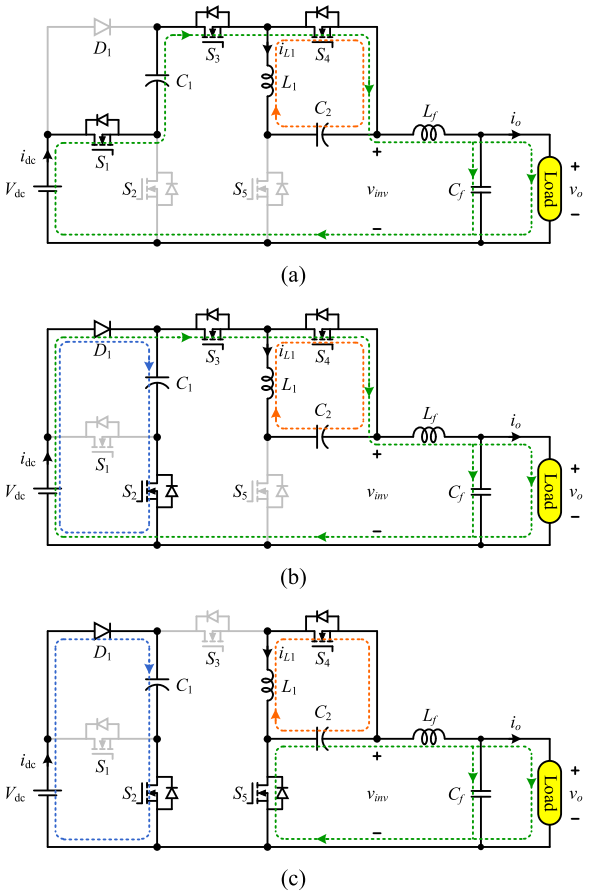

FIGURE 3. Operating modes of the proposed CG-5S-BTI under positive-half cycle (a) Mode I, (b) Mode II, (c) Mode III.

The operational modes of the CG-5S-BTI throughout both the positive and negative half-cycles of the output voltage are described as follows:

Mode-I: In the first operating mode, as depicted in Fig. 3(a), switches S_1, S_3, and S_4 are in the on-state, and diode D_1 is reverse biased. The capacitor C_1 is connected in series with the input voltage source (V_{dc}), and the inverter's output is connected in series with V_{dc} and capacitor C_1. As a result, the peak value of the output voltage reaches $2V_{dc}$. Capacitor C_2 and inductor L_1 are connected in parallel by turning on switch S_4. During the positive-half cycle, there is no charging process for inductor L_1. The average voltage of the voltages across inductor L_1 and capacitor C_2 is zero. The differential equations are obtained as

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = -v_{C2} \\ v_{Lf} = L_f \dfrac{di_{Lf}}{dt} = V_{dc} + V_{C1} - v_o \end{cases} \tag{1}$$

$$\begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = -i_{Lf} \\ i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = i_{L1} \end{cases} \tag{2}$$

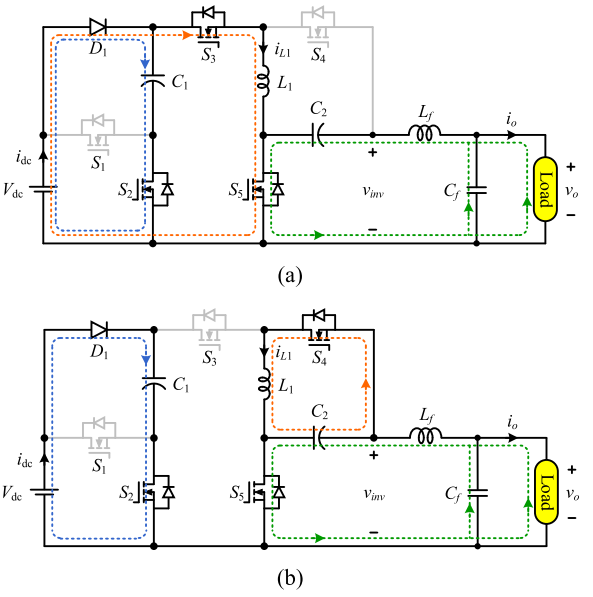

FIGURE 4. Operating modes of the proposed CG-5S-BTI under negative-half cycle (a) Mode IV, (b) Mode V.

Mode-II: Fig. 3(b) depicts the second operation mode, in which the output voltage is positive. Here, switches S_2, S_3, and S_4 are in the on-state. Capacitor C_1 is connected in parallel with V_{dc} due to the forward biased of diode D_1 and on-state of switch S_2. Capacitor C_1 is charged to V_{dc}. Inductor L_1 and capacitor C_2 keep the same connection as in the first operation mode, the average voltage of capacitor C_2 is zero. The output voltage is maintained by the V_{dc} through switches S_3 and S_4. The mathematical expressions for Mode II can be deduced as follows:

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = -v_{C2} \\ v_{Lf} = L_f \dfrac{di_{Lf}}{dt} = V_{dc} - v_o \end{cases} \tag{3}$$

$$\begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = i_{dc} - i_{Lf} \\ i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = i_{L1} \end{cases} \tag{4}$$

Mode-III: During this mode, the equivalent circuit is displayed in Fig. 3(c). Here, diode D_1 is forward biassed, and switch S_2 is turned on, ensuring that the voltage of capacitor C_1 is equal to V_{dc}. Switch S_3 is turned off, meaning no energy is transferred to L_1 in this mode. Inductor L_1 and capacitor C_2 are connected in parallel through switch S_4. The average voltage of both inductor L_1 and capacitor C_2 is zero. The switch S_5 is turned on, which helps connect capacitor C_2 in parallel to the output side. The inverter output voltage is zero in this mode. The differential equations are obtained as

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = -v_{C2} \\ v_{Lf} = L_f \dfrac{di_{Lf}}{dt} = -v_{C2} - v_o \end{cases} \tag{5}$$

$$\begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = i_{dc} \\ i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = i_{L1} + i_{Lf} \end{cases} \tag{6}$$

Mode-IV: Fig. 4(a) presents the corresponding circuit representation of the proposed inverter in this mode, in which diode D_1 is in forward-biased condition. Here, the voltage across capacitor C_1 is maintained in balance with V_{dc} by turning on switch S_2. The switches S_3 and S_5 are in on-state, meaning inductor L_1 is charged from V_{dc}. The current in inductor L_1 increases linearly. Furthermore, capacitor C_2 is connected to the output side through switch S_5. The energy on the capacitor C_2 is transferred to the output load. The differential equations are derived as

$$\begin{cases} v_{L1} = L_1 \dfrac{di_{L1}}{dt} = V_{dc} \\ v_{Lf} = L_f \dfrac{di_{Lf}}{dt} = -v_{C2} - v_o \end{cases} \tag{7}$$

$$\begin{cases} i_{C1} = C_1 \dfrac{dv_{C1}}{dt} = i_{dc} - i_{L1} \\ i_{C2} = C_2 \dfrac{dv_{C2}}{dt} = i_{Lf} \end{cases} \tag{8}$$

Mode-V: Fig. 4(b) presents the corresponding circuit representation of the proposed inverter. In this mode, switch S_4 is turned on and switch S_3 is turned off, and inductor L_1 is connected in parallel with capacitor C_2. The energy from L_1 is discharged through capacitor C_2, and the current in inductor L_1 decreases linearly. Moreover, capacitor C_2 is connected in parallel with the load side, helping to maintain the output voltage as a sine wave. The mathematical equations in this mode are similar to those in Mode III.

B. MODULATION STRATEGY

The analyses presented in this section are examined for an ideal case, where the internal resistance of components is eliminated, the circuit operates under unity power factor conditions, and the output voltage is symmetrical.

The output voltage of the proposed inverter is given by:

$$v_o = V_{o.\max} \sin\theta \tag{9}$$

where $V_{o.max}$ represents the maximum output voltage.

The voltage gain (G) of the proposed CG-5S-BTI is given by:

$$G = \frac{V_{o.\max}}{V_{dc}} \tag{10}$$

The equations of transition angles θ_1 and θ_2 can be obtained as

$$\begin{cases} \theta_1 = \sin^{-1}\left(\frac{1}{G}\right) \\ \theta_2 = \pi - \sin^{-1}\left(\frac{1}{G}\right) \end{cases} \tag{11}$$

When the voltage gain G of the proposed inverter ranges from 1 to 2, the transition angles θ_1 and θ_2 are defined as follows

$$\begin{cases} \dfrac{\pi}{6} \le \theta_1 \le \dfrac{\pi}{2} \\ \dfrac{\pi}{2} \le \theta_2 \le \dfrac{5\pi}{6} \end{cases} \tag{12}$$

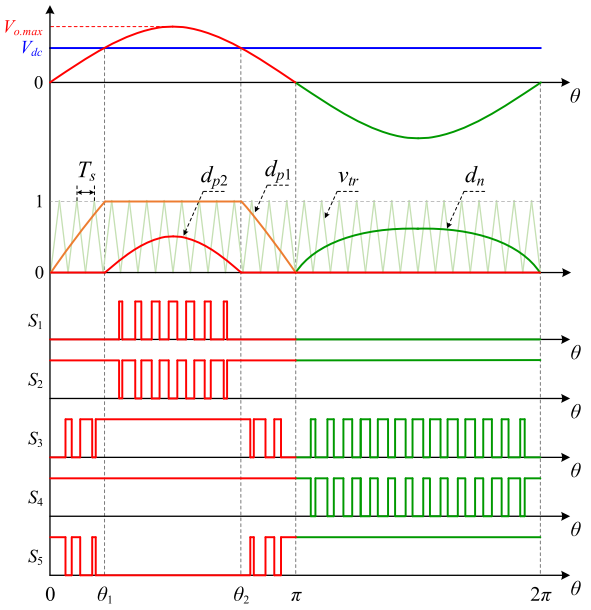

FIGURE 5. Gate signals of all switches for the proposed inverter.

Considering (1) and (3), the duty ratio of S_1 can be expressed as follows:

$$d_{p2} = \begin{cases} 0, & 0 < \theta \le \theta_1 \\ \dfrac{v_o}{V_{dc}} - 1, & \theta_1 < \theta \le \theta_2 \\ 0, & \theta_2 < \theta \le \pi \end{cases} \tag{13}$$

where d_{p2} is the duty ratio of the switch S_1.

The duty ratio of switch S_3 is defined based on (3) and (5), as follows:

$$d_{p1} = \begin{cases} \dfrac{v_o}{V_{dc}}, & 0 < \theta \le \theta_1 \\ 1, & \theta_1 < \theta \le \theta_2 \\ \dfrac{v_o}{V_{dc}}, & \theta_2 < \theta \le \pi \end{cases} \tag{14}$$

where d_{p1} is the duty ratio of the switch S_3 during the positive half-cycle.

Referencing (5) and (7), the duty ratio of S_3 can be represented as follows:

$$d_n = \frac{v_o}{v_o - V_{dc}}, \quad \pi < \theta \le 2\pi \tag{15}$$

where d_n is the duty ratio of the switch S_3 during the negative half-cycle.

The PWM control method for the switches of the proposed CG-5S-BTI is displayed in Fig. 5. In the figure, three control waveforms (d_{p1}, d_{p2}, and d_n) are used and compared to a high-frequency triangle waveform (v_{tr}). During the positive half-cycle (0–π), control waveforms d_{p1} and d_{p2} exhibit

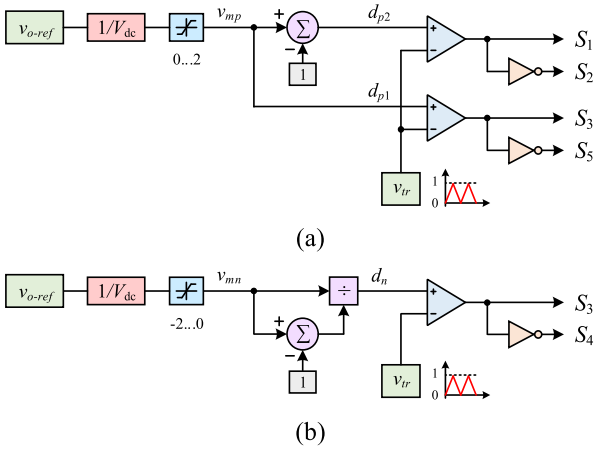

FIGURE 6. Logic gates used for the PWM generation for the proposed inverter: (a) for Modes I, II, and III and (b) for Modes IV and V.

TABLE 2. Switching conditions at various time intervals.

Intervals	(θ_1-θ_2)	(0-θ_1) or (θ_2-π)	(π – 2π)
Conditions	$v_o > V_{dc}$	$V_{dc} > v_o > 0$	$v_o < 0$
S_1	H	0	0
S_2	H	1	1
S_3	1	H	H
S_4	1	1	H
S_5	0	H	1

*H: Operating at high frequency

variation. Specifically, d_{p2} varies within the time interval (θ_1–θ_2), whereas d_{p1} varies within the time intervals (0-θ_1) and (θ_2–π). Conversely, during the negative half-cycle (π–2π), the control waveform d_n displays variation.

When the output voltage is greater than the input voltage, which occurs between time points θ_1 and θ_2. Gate signals for switch S_1 are generated by comparing the control waveform d_{p2} to the triangle waveform v_{tr}. The gate signal for switch S_2 is inverted from the gate signal for switch S_1.

When the output voltage is lower than the input voltage, gate signal for switch S_5 within the time intervals (0–θ_1) and (θ_2–π) are generated by comparing the control waveform d_{p1} to the triangle waveform v_{tr}. The gate signal for switch S_3 is inverted from the gate signal for switch S_5 in the positive half-cycle.

In both cases of output voltage versus input voltage, gate signal for switch S_4 is generated by comparing the control waveform d_n to the triangle waveform v_{tr}. The gate signal for switch S_3 is inverted from the gate signal for switch S_4 in the negative half-cycle.

Table 2 lists the switching states under various input voltage conditions at different time intervals.

According to Table 2, only two of the five switches operate at high frequency throughout each time interval, helping to reduce switching losses in the proposed inverter. As displayed in Fig. 6, the gate signals of the switches are represented

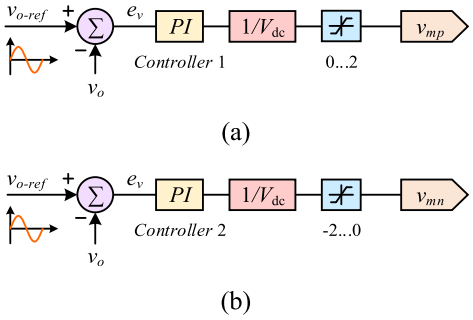

FIGURE 7. Closed-loop control diagram of the proposed inverter: (a) control for Modes I, II, and III, and (b) control for Modes IV and V.

as follows:

$$S_1 = \begin{cases} 0, & d_{p2} < v_{tr} \\ 1, & d_{p2} \geq v_{tr} \end{cases} \tag{16}$$

$$S_2 = \overline{S_1} \tag{17}$$

$$S_5 = \begin{cases} 0, & d_{p1} \geq v_{tr} \\ 1, & d_{p1} < v_{tr} \end{cases} \tag{18}$$

$$S_4 = \begin{cases} 0, & d_n \geq v_{tr} \\ 1, & d_n < v_{tr} \end{cases} \tag{19}$$

$$S_3 = \overline{S_4} + \overline{S_5} \tag{20}$$

C. DESIGN OF THE VOLTAGE CONTROLLER

The operating modes during the negative and positive half-cycles of the proposed inverter are different, resulting in asymmetrical output voltage characteristics. The output voltage in the positive and negative half-cycles of the inverter is expressed as follows:

$$v_o = \begin{cases} V_{p.\max} \sin\theta, & \text{for } v_o > 0 \\ V_{n.\max} \sin\theta, & \text{for } v_o < 0 \end{cases} \tag{21}$$

where $V_{p.max}$ and $V_{\text{n.max}}$ respectively represent the peaks of the output voltage in the positive half-cycle and the negative half-cycle.

A symmetric output voltage occurs when the peaks of the voltage in the positive and negative half-cycles are equal:

$$V_{p.\max} = V_{n.\max} = V_{o.\max} \tag{22}$$

To address the asymmetry issue of the output voltage, the proposed inverter implements two controllers, employing an adaptive method. This method uses a PI controller to fine-tune the balance of the output voltage in each half-cycle. Fig. 7 illustrates the control block diagram of the proposed inverter. Here, the output voltage (v_o) is compared with the reference voltage (v_{o-ref}), generating the error signal (e_v). The voltage error passes through the PI controller, resulting in the output of the control signal.

The control process of the output voltage in the positive half-cycle is based on the analysis derived from (13) and (14). Consequently, d_{p2} and d_{p1} are designed as follows:

$$d_{p2} = v_{mp} - 1 \tag{23}$$

$$d_{p1} = v_{mp} \tag{24}$$

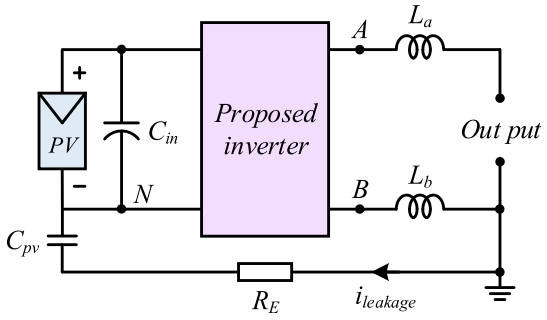

FIGURE 8. Schematic diagram of the proposed inverter with leakage current.

The control process of the output voltage in the negative half-cycle is based on the analysis derived from (15). Accordingly, the design of d_n is as follows:

$$d_n = \frac{v_{mn}}{v_{mn} - 1} \tag{25}$$

where the control signals v_{mp} for the positive half-cycle and v_{mn} for the negative half-cycle are determined as follows:

$$v_{mp} = \frac{1}{V_{dc}}\left[k_{p1}e_v + k_{i1}\int e_v\, dt\right] \tag{26}$$

$$v_{mn} = \frac{1}{V_{dc}}\left[k_{p2}e_v + k_{i2}\int e_v\, dt\right] \tag{27}$$

where k_{p1} and k_{i1} are the proportional and integral gain of PI controller 1, respectively, and k_{p2} and k_{i2} are the proportional and integral gain of PI controller 2, respectively.

From (23) and (25), the maximum values of the duty ratios d_{p2} and d_n are given by:

$$d_{p2.\max} = V_{mp.\max} - 1 \tag{28}$$

$$d_{n.\max} = \frac{V_{mn.\max}}{V_{mn.max} + 1} \tag{29}$$

where $V_{mp.max}$ and $V_{mn.max}$ represent the maximum values of v_{mp} and v_{mn}, respectively.

D. LEAKAGE CURRENT ANALYSIS

Fig. 8 illustrates the proposed simplified model of a transformerless inverter with parasitic capacitance. The absence of galvanic isolation may result in a direct ground-current path between the PV panel and the grid. Moreover, the substantial stray capacitance (C_{pv}) between the PV and grid grounds introduces a variable voltage, which is commonly known as the common-mode voltage. This excites the resonant circuit formed by the parasitic capacitor and the inverter filter inductor, which produces a high common-mode ground current (leakage current) [15], [16]. To mitigate this leakage current ($i_{leakage}$) and ensure stability, it is imperative to maintain a constant common voltage (V_{cm}) throughout all operating periods. In Fig. 8, V_{cm} and the differential-mode voltage (V_{dm}) are defined as follows:

$$V_{cm} = \frac{V_{AN} + V_{BN}}{2} \tag{30}$$

$$V_{dm} = V_{AN} - V_{BN} \tag{31}$$

where V_{AN} represents the voltage between terminals A and N, and V_{BN} is the voltage between terminals B and N.

As documented in [29], it was established that V_{dm} also influences the leakage current. Consequently, the total common-mode voltage (V_{tcm}) can be expressed as follows:

$$V_{tcm} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2}\frac{L_b - L_a}{L_b + L_a} \tag{32}$$

In the proposed inverter, $L_b = 0$, and $V_{BN} = 0$. Consequently, (32) can be simplified to:

$$V_{tcm} = V_{BN} \tag{33}$$

Due to the common-ground structure in the proposed inverter, where both the end of B and N are shorted, (33) ensures the absence of any switching-frequency common-mode voltage.

E. THREE-PHASE EXTENSION OF THE PROPOSED CG-5S-BTI

Three-phase inverters play a critical role in various industries and commonly consist of three traditional half-bridge inverters, which produce a two-level voltage in each phase. While this configuration is widely used, there have been continuous efforts to improve the voltage quality and develop more advanced three-level phase voltage solutions. To address this demand, innovative inverter topologies have been introduced, such as neutral point clamped (NPC) [31], T-type [32], and flying-capacitor [33] inverters. However, although these advanced topologies can generate a three-level voltage, they only operate in the buck mode. Accordingly, the three-phase extension of CG-5S-BTI offers a compelling alternative. Owing to its common-ground structure, this innovative inverter design avoids neutral-point voltage imbalance issues.

The three-phase extension of CG-5S-BTI is illustrated in Fig. 9. This structure has the advantage of generating higher output voltages compared to the input voltages. In this topology, a total of 15 power switches are required, contributing to the common ground of every phase. In applications where the inverter is required to in buck feature, only nine switches are active at high frequencies.

Significantly, the capacitors employed in this design are characterized by their low values. Among these capacitors, three are tailored to match the input voltage, while the remaining three are designed to match the output voltage. This helps to reduce losses from the capacitors while optimizing the utilization of the input DC source.

III. COMPONENT SELECTION

This section provides a comprehensive explanation of the component design for the proposed CG-5S-BTI. For simplicity in the component selection calculations, the inverter is analyzed under ideal conditions. This means that the internal resistances of the components are neglected, the circuit operates under unity power factor conditions, and the output voltage is symmetrical.

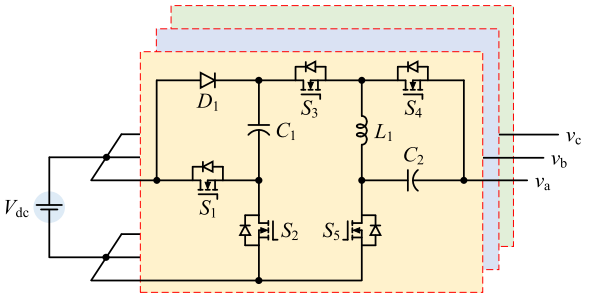

FIGURE 9. Three-phase extension of the proposed CG-5S-BTI.

A. INDUCTANCE AND CAPACITANCE SELECTIONS

Inductor L_1 is charged when switches S_3 and S_5 are turned on and the energy stored in inductor L_1 is controlled by the duty ratio d_n. From (2), (4), (6), (8). The current in inductor L_1 is given by

$$i_{L1} = \begin{cases} i_o\left(d_{p1} - 1\right), & 0 < \theta \le \theta_1 \ \ or \ \ \theta_2 < \theta \le \pi \\ 0, & \theta_1 < \theta \le \theta_2 \\ i_o/\left(d_n - 1\right), & \pi < \theta \le 2\pi \end{cases} \tag{34}$$

The calculation of the current ripple for inductors L_1 and L_f is based on equation $v_L = Ldi/dt$. The current ripple of inductors L_1 and L_f can be determined as follows:

$$\Delta i_{L1} = \frac{V_{dc} d_n}{L_1 f_s} \tag{35}$$

$$\Delta i_{Lf} = \frac{\left(2V_{dc} - v_o\right) d_{p2}}{L_f f_s} \tag{36}$$

where f_s represents the switching frequency.

The maximum current in inductor L_1 is obtained from

$$I_{L1.\max} = (G+1)\, I_{o.\max} + \left(\frac{1}{G+1}\right) \frac{V_{o.\max}}{2L_1 f_s} \tag{37}$$

The maximum value of Δi_{L1} occurs when d_n reaches its maximum value. By referring to (10), (15), (35) and (36), the size of L_1 and L_f are obtained as follows:

$$L_1 = \left(\frac{1}{G+1}\right) \frac{V_{o.\max}}{\Delta i_{L1.\max} f_s} \tag{38}$$

$$L_f = \left(\frac{3G - G^2 - 2}{G}\right) \frac{V_{o.\max}}{\Delta i_{Lf.\max} f_s} \tag{39}$$

From (1), (3), (5), and (7). The voltages of capacitors C_1, C_2 are given by

$$v_{C1} = V_{dc} \tag{40}$$

$$v_{C2} = \begin{cases} 0, & 0 < \theta \le \pi \\ -v_o, & \pi < \theta \le 2\pi \end{cases} \tag{41}$$

In the first operation mode, as displayed in Fig. 3(a), the current through the C_1 (i_{C1}) is equal to the output current (i_o). The voltage ripple of the capacitor C_1 can be written as follows:

$$\Delta v_{C1} = \frac{1}{C_1}\left(i_{C1}.d_{p2}.T_s\right) = \frac{i_o}{C_1}.\left(G\sin\theta - 1\right).T_s \tag{42}$$

The maximum values of Δv_{C1} are obtained when d_{p2} reaches its maximum value. From (42), the values of capacitors C_1 can be determined as follows:

$$C_1 = (G-1)\frac{I_{o.\max}}{\Delta v_{C1.\max} f_s} \tag{43}$$

Similarly, the ripple voltage of the capacitor C_2 can be written as follows:

$$\Delta v_{C2} = \frac{1}{C_2}\left(i_{C2}.d_n.T_s\right) = \frac{i_o}{C_2}.\left(\frac{G\sin\theta}{G\sin\theta - 1}\right).T_s \tag{44}$$

The values of capacitors C_2 can be determined as follows:

$$C_2 = \left(\frac{G}{G+1}\right)\frac{I_{o.\max}}{\Delta v_{C2.\max} f_s} \tag{45}$$

B. SEMICONDUCTOR DEVICES SELECTION

By referring to the operational modes of the proposed CG-5S-BTI, as described in Section II, the voltage stresses on the switches are as follows:

$$\begin{cases} V_{S1} = V_{S2} = V_{dc} \\ V_{S3} = V_{S4} = V_{dc} + V_{o.\max} \\ V_{S5} = V_{o.\max} \end{cases} \tag{46}$$

The peak currents of S_3, S_4, S_5 are linked to $i_{L1.max}$ in (37). When disregarding the current ripple, the switch current stresses are given by

$$\begin{cases} I_{S1} = I_{o.\max} \\ I_{S2} = I_{C1.ch} \\ I_{S3} = I_{S4} = (G+1)\, I_{o.\max} \\ I_{S5} = (G+2)\, I_{o.\max} \end{cases} \tag{47}$$

The peak charging current of capacitor C_1 can be written as follows:

$$I_{C1.ch} = \frac{\Delta V_{C1}}{R_{eq1}} \tag{48}$$

where R_{eq1} is the equivalent resistance in the charging path of C_1 and can be calculated as follows:

$$R_{eq1} = r_{DS1} + r_{D1} + r_{C1} \tag{49}$$

where r_{DS1}, r_{D1}, and r_{C1} are the on-resistance of the switch S_1, diode D_1, and equivalent series resistance (ESR) of capacitor C_1, respectively.

IV. LOSS ANALYSIS

The main sources of power losses in the proposed CG-5S-BTI design originate from the capacitors, inductors, diodes, and MOSFETs. The power loss in the capacitor is primarily

TABLE 3. Comparison of the proposed inverter and existing inverters.

Topology	Active elements		Passive elements			No. of on state switches	Gain	TSV (p.u.)	Leakage current	Capacitance	Reported experimental efficiency
	S	D	C	L	L_f						
[9]	5	0	1	0	2	3	1	5	Non Zero	-	98.5%@0.5 kW
[10]	6	0	2	0	2	3	1	5	Non Zero	2×470 µF/400 V	97.2%@1 kW
[11]	6	2	2	0	2	3	1	5	Non Zero	Not Reported	97.4%@1 kW
[12]	6	2	1	0	2	2	1	5	Non Zero	-	97%@1 kW
[14]	5	0	1	0	1	2	1	5	Zero	940 µF/450 V	95.5%@0.5 kW
[15]	4	2	3	0	2	2	1	8	Zero	220 µF/400 V 330 µF/400 V	97.4%@0.5 kW
[16]	4	1	2	0	1	2	1	5	Zero	470 µF/400 V	99.1%@0.8 kW
[17]	8	0	3	0	2	4	1	7	Zero	3×1000 µF/200 V	97.1@NA
[18]	6	1	2	0	1	3	1	5	Zero	500 µF/200 V 2000 µF/400 V	96.5%@0.4 kW
[20]	5	1	2	1	2	3	4.4	6	Zero	220 µF/400 V	96%@0.2 kW
[21]	7	2	2	1	1	3	2	8	Zero	470 µF/200 V 1000 µF/400 V	97%@0.75 kW
[22]	10	0	2	1	1	6	4	5	Zero	2×1200 µF/100 V	97.1%@0.6 kW
[23]	4	3	4	2	1	3	3	9	Zero	2×470 µF/450 V 2×560 µF/450 V	95.4%@0.7 kW
[24]	6	2	3	2	1	3	3.1	6.3	Zero	2×47 µF/150 V 180 µF/400 V	96.4%@.03 kW
[26]	7	2	2	0	1	4	2	8	Zero	3×10 µF/200 V 3×10 µF/400 V	98.1%@0.51 kW
[27]	6	3	3	0	1	3	2	9	Zero	120 µF/250 V 2×470 µF/450 V	97.9%@0.5 kW
[28]	9	3	3	0	1	5	3	8	Zero	3×680 µF/450 V	97.7%@0.5 kW
[29]	6	2	2	0	1	3	2	6.5	Zero	6×20 µF/220 V 680 µF/400 V	98.1%@0.51 kW
[30]	8	1	2	0	1	5	2	8.5	Zero	2200 µF/100 V 2200 µF/200 V	97.7%@0.55 kW
[35]	7	2	2	0	2	4	2	6	Non Zero	2×1000 µF/250 V	96%@0.66 kW
[36]	4	2	1	1	2	2	1	8.5	Zero	1 µF/250 V	98.6%@0.35 kW
[37]	4	0	2	2	1	2	2.6	5.7	Zero	3 µF/450 V 6 µF/400 V	95.7%@0.3 kW
[38]	9	0	2	0	1	6	2	6.5	Zero	1640 µF/450V	98.5%@1 kW
[39]	9	1	3	0	1	5	2	8	Zero	2×470 µF/250V 1000 µF/450V	96.5@0.6 kW
Proposed Inverter	5	1	2	1	1	3	2	5.1	Zero	220 µF/250 V 5 µF (Film cap.)	96.6%@0.3 kW

due to its *ESR* and the root mean square (rms) of the current. This relationship is described as follows.

$$P_C = \sum_{i=1}^{2} r_{Ci} I_{Ci.rms}^2 \tag{50}$$

where $I_{Ci\cdot rms}$ and r_{Ci} represent the rms current flowing through the capacitors and their *ESR* values, respectively.

The temperature increase in L_1 is a result of the copper losses (P_{cu}) and core losses (P_{Fe}). The total power losses (P_{L1}) of inductor L_1 can be calculated as follows:

$$P_{L1} = P_{cu} + P_{Fe} \tag{51}$$

$$\begin{cases} P_{cu} = I_{L1.rms}^2 . r_{L1} \\ P_{Fe} = a.f^b.B^c.A_e.l_e \end{cases} \tag{52}$$

where $I_{L1.rms}$ and r_{L1} represent the rms current and *ESR* of inductor L_1. Additionally, A_e is the cross-sectional area of the inductor's core, l_e refers to the length of the magnetic path, B represents half of the alternating current flux swing, and a, b, and c are empirical parameters adjusted based on the core's datasheets.

The power losses in a diode consist of two main factors: conduction loss ($P_{D\cdot c}$) and reverse recovery loss ($P_{D\cdot sw}$). These combined power losses of a diode (P_D) can be represented as follows:

$$P_D = P_{D.c} + P_{D.sw} \tag{53}$$

$$\begin{cases} P_{D.c} = \dfrac{1}{T_s}\displaystyle\int_0^{T_s} \left(V_{FD1} i_{D1} + r_{D1} i_{D1}^2 \right) dt \\ \qquad = V_{FD1} I_{D1.avg} + r_{D1} I_{D1.rms}^2 \\ P_{D.sw} = \dfrac{1}{T_s}\displaystyle\int_0^{t_{rrD1}} p_{D1} dt = \dfrac{1}{6} f_s V_{D1} I_{rrD1} t_{rrD1} \end{cases} \tag{54}$$

where $I_{D1.avg}$, $I_{D1.rms}$, r_{D1}, V_{FD1}, I_{rrD1} and t_{rrD1} are the average current, rms current, on-resistance, forward voltage drop, reverse recovery current and reverse recovery time of diode D_1.

Switch losses include both conduction losses ($P_{S\cdot c}$) and switching losses ($P_{S\cdot sw}$) [34]. As a result, the overall power

TABLE 4. Voltage stress comparison of selected topologies.

	Ref. [20] Fig. 1(a)	Ref. [26] Fig. 1(b)	Ref. [29] Fig. 1(c)	Ref. [30] Fig. 1(d)	Prop.
D_1	$3.2V_{dc}$	V_{dc}	V_{dc}	V_{dc}	V_{dc}
D_2	-	-	$2V_{dc}$	-	-
S_1	$3.2V_{dc}$	V_{dc}	V_{dc}	V_{dc}	V_{dc}
S_2	$3.2V_{dc}$	V_{dc}	V_{dc}	V_{dc}	V_{dc}
S_3	$3.2V_{dc}$	$2V_{dc}$	V_{dc}	V_{dc}	$2.56V_{dc}$
S_4	$3.2V_{dc}$	$4V_{dc}$	$2V_{dc}$	$2V_{dc}$	$2.56V_{dc}$
S_5	$3.2V_{dc}$	$3V_{dc}$	$3V_{dc}$	$4V_{dc}$	$2V_{dc}$
S_6	-	$2V_{dc}$	$2V_{dc}$	$3V_{dc}$	-
S_7	-	$2V_{dc}$	-	$2V_{dc}$	-
S_8	-	-	-	$2V_{dc}$	-
C_1	$3.2V_{dc}$	V_{dc}	V_{dc}	V_{dc}	V_{dc}
C_2	-	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	$1.56V_{dc}$
TSV (p.u.)	6	8	6.5	8.5	5.1

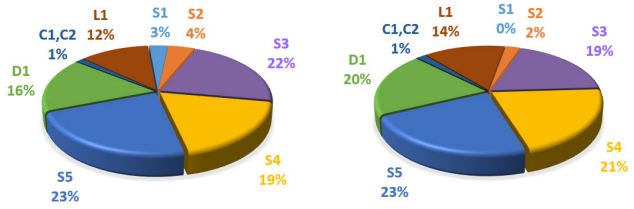

FIGURE 10. Power loss distribution of proposed CG-5S-BTI under 500W: (a) Boost mode. (b) Buck mode.

loss in the power switch can be formulated as follows:

$$P_S = \sum_{i=1}^{5} (P_{Si.c} + P_{Si.sw}) = \sum_{i=1}^{5} \left[P_{Si.c} + \left(\sum_{j=1}^{N_{on,i}} P_{Si.sw(on),j} + \sum_{j=1}^{N_{off,i}} P_{Si.sw(off),j} \right) \right] \tag{55}$$

$$\begin{cases} P_{Si.c} = \dfrac{1}{T_s} \displaystyle\int_0^{T_s} r_{Si} i_{Si}^2 dt = r_{Si} I_{Si.rms}^2 \\ P_{Si.sw(on)} = \displaystyle\int_0^{t_{on}} V_{Si} i_{Si} dt = \frac{1}{6} V_{Si} I_{Si.on} t_{on} \\ P_{Si.sw(off)} = \displaystyle\int_0^{t_{off}} V_{Si} i_{Si} dt = \frac{1}{6} V_{Si} I_{Si.off} t_{off} \end{cases} \tag{56}$$

where $P_{Si.sw(on)}$ and $P_{Si.sw(off)}$ are turn-on and turn-off loss of the switches. $I_{Si.rms}$, $I_{Si.avg}$, and r_{Si} are the rms current, average current, and on-resistance of the switches. N_{on} and N_{off} are the number of turn-on and turn-off during one cycle, t_{on} is rising time, t_{off} is the falling time, V_{Si} is the voltage stress of the switches, $I_{Si.on}$, $I_{Si.off}$ are the current stresses of on-state and off-state.

The efficiency of the proposed CG-5S-BTI can be defined as follows:

$$\eta = \frac{P_o}{P_o + P_{Loss}} \tag{57}$$

TABLE 5. Simulated parameters for comparison.

Parameters		Values
Input voltage (V_{dc})		100 V
Output voltage (v_o)		110 V_{rms}
Output voltage (P_o)		500 W
Line frequency (f_o)		50 Hz
Switching frequency (f_s)		30 kHz
On-resistance of the power diode (r_D)		0.05 Ω
Forward voltage drop of diode (V_F)		1 V
On-resistance of the power switch (r_S)		0.05 Ω
Capacitor	in inverters [20], [29], [30]	2200 µF (0.12 Ω)
	in inverter [26]	50 µF (0.004 Ω)
	in proposed inverter	220 µF (0.05 Ω) 5 µF (0.025 Ω)
Inductor	in inverter [20]	1.5 mH (0.1 Ω)
	in proposed inverter	0.4 mH (0.04 Ω)

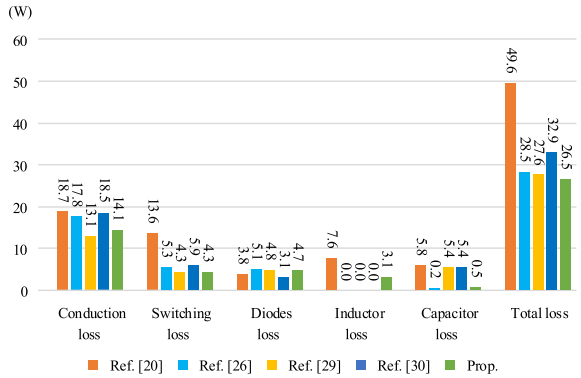

FIGURE 11. Component loss distribution of inverters under 500 W.

where

$$P_{Loss} = P_C + P_L + P_D + P_S \tag{58}$$

Fig. 10 illustrates the detailed distribution of power losses among individual components, with the parameters of the components presented in Table 8 in Section VI. Notably, the losses in switches S_3, S_4, and S_5 dominate the overall power losses in the inverter. This result is due to S_3, S_4, and S_5 experiencing higher voltage stress and current levels compared to S_1 and S_2.

V. COMPARISON

To assess the advantages and drawbacks of the proposed CG-5S-BTI, two comparisons have been conducted. One comparison is made between the proposed inverter and recently common transformerless. Another comparison is drawn between the proposed inverter and the selected inverters shown in Fig. 1.

A. COMPARISON WITH EXISTING TI TOPOLOGIES

Table 3 provides a comprehensive comparison between the proposed CG-5S-BTI topology and prior-art topologies. This evaluation aims to highlight the potential advantages of the proposed inverter topology by examining several key aspects:

TABLE 6. Comparison of power quality at output of proposed inverter under open-loop and closed-loop conditions.

P_o	Parameter	V_{dc} = 100V		V_{dc} = 200V	
		open-loop	closed-loop	open-loop	closed-loop
200W	$V_{o,avg}$ (V)	8.59×10^{-1}	3.75×10^{-4}	5.47×10^{-1}	6.70×10^{-5}
	$I_{o,avg}$ (A)	1.42×10^{-2}	4.98×10^{-5}	9.05×10^{-3}	2.73×10^{-6}
	$THD.I_o$ (%)	1.13	0.702	0.782	0.551
300W	$V_{o,avg}$ (V)	1.14	1.24×10^{-6}	6.72×10^{-1}	6.43×10^{-5}
	$I_{o,avg}$ (A)	2.83×10^{-2}	2.52×10^{-6}	1.67×10^{-2}	1.57×10^{-6}
	$THD.I_o$ (%)	1.54	0.874	0.915	0.528
400W	$V_{o,avg}$ (V)	1.41	1.47×10^{-5}	7.94×10^{-1}	7.32×10^{-5}
	$I_{o,avg}$ (A)	4.68×10^{-2}	6.01×10^{-6}	2.62×10^{-2}	2.39×10^{-6}
	$THD.I_o$ (%)	1.96	1.07	1.08	0.511
500W	$V_{o,avg}$ (V)	1.58	7.35×10^{-5}	9.14×10^{-1}	6.70×10^{-5}
	$I_{o,avg}$ (A)	6.9×10^{-2}	2.75×10^{-5}	3.78×10^{-2}	2.74×10^{-6}
	$THD.I_o$ (%)	2.28	1.28	1.25	0.511

the number of active and passive components, the count of switches in the on-state, total standing voltage (TSV), voltage gain, leakage current, capacitance, and peak measured efficiency. It should be noted that in the topologies presented in [17], [21], [26], [28], [38], and [39], bidirectional switches are counted as two individual switches. Additionally, input and filter capacitors are not listed in the table.

As shown in Table 3, the proposed topology uses five switches, which is fewer than the topologies in [21], [26], [30], [38], and [39] when considering the same voltage gain of 2. Topologies [23], [24], and [28] achieve a higher voltage gain of 3 but require additional diodes and an increased number of switches.

Regarding the count of switches in the on-state, the proposed topology uses three, which is lower than in topologies [26], [28], [35], [38], and [39]. This reduction in switch count is beneficial for decreasing switching losses and improving efficiency.

In terms of TSV, the proposed topology has a TSV of 5.1, which is lower than those in [27], [30], and [36], where the TSV exceeds 8. A low TSV indicates reduced semiconductor usage, leading to lower system costs. Topologies [9], [10], [11], [12], [13], [14], [16], and [18] have the lowest TSV. However, these topologies have voltage gains lower than 1. Topology [22] achieves both low TSV and a high voltage gain, but the trade-off is an increased number of components and switches in the on-state.

Topologies [20], [22], [23], [24], [28], and [37] have higher voltage gains than the proposed topology, with [20] achieving the highest at 4.4. This topology uses a number of semiconductor components equal to the proposed topology. However, it outputs two voltage levels, causing high voltage stress on the components. Topology [23] has a voltage gain of 3 with four switches used but requires additional passive components and high voltage stress on the components.

Leakage current elimination is an outstanding property of the CG-based structure. The proposed inverter is also designed based on this structure, effectively reducing leakage current, which improves safety and operational efficiency. However, unlike the proposed topology, topologies [9], [10], [11], [12] and [35] have variable CM voltage. Consequently, their leakage current is not zero, which poses potential risks.

Regarding required capacitance, topologies based on the virtual DC-bus concept [14], including [16], [17], [18], [21], [29], [30], [38], and [39], require larger capacitance values to facilitate long discharge times, leading to high current stress on the switches. As shown in Table 3, topologies [17], [18], and [21] require capacitors exceeding 1000 μF for power levels below 1 kW. To reduce the required capacitance value, topologies based on the charge pump circuit concept [15], including [23], [24], [26], [27], and [28], perform capacitor voltage equalization during each switching cycle, thereby reducing the capacitance demand. However, topologies in this group generally still have high TSV values. In contrast, the proposed inverter uses two capacitors with smaller values and lower TSV to achieve the same voltage gain as topologies [21], [26], [27], [29], [30], [38], and [39]. This characteristic can also enhance the overall efficiency of the proposed topology compared to other topologies.

B. COMPARISON WITH SELECTED TOPOLOGIES

For a more comprehensive evaluation of the proposed CG-5S-BTI, the proposed inverter is compared with a boost two-level inverter from [20], a three-level inverter from [26], and two five-level inverters from [29] and [30]. All these selected inverters share the common features of voltage boosting and common-ground structure.

Table 4 presents a comparison of the voltage stresses across the components in these inverters when V_{dc} = 100 V and $V_{o.rms}$ = 110 V. The table indicates that the inverters in [20], [29], and [30] each have five switches experiencing high voltage stress ($2V_{dc}$ or higher). Notably, the proposed CG-5S-BTI and inverter in [29] stand out due to only three switches experiencing high voltage stress. Additionally, the table demonstrates that the proposed inverter has the lowest TSV among all the considered topologies.

The selected inverters are simulated in PSIM at a power of 500 W with an input voltage of 100 V. Table 5 describes the physical model of the interconnected simulation structures. The on-state resistance of the switches (r_S) is 0.05Ω, and the forward voltage (V_F) and internal resistance in the diodes are 1 V and 0.05 Ω, respectively. Based on Table 5, the loss distribution of the proposed inverter and the selected inverters is illustrated in Fig. 11.

VI. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS OF THE PROPOSED INVERTER IN STAND-ALONE OPERATION

In this section, simulation studies were undertaken in the PSIM software to validate the theoretical operational principles of the proposed CG-5S-BTI. In this simulation model, the parameters are as shown in Table 8. The input DC source was set to 100 V and 200 V for boost mode and buck mode, respectively, with a voltage gain of 1.55 and 0.78. The output voltage is 110 V with a frequency of 50 Hz, and it is symmetrical by applying the control strategy introduced in Fig. 7.

Fig. 12 presents the voltage and current waveforms for the proposed CG-5S-BTI during transient response as the output load power changes from 250 W to 500 W in both boost and buck modes. Despite the variation in output power, the peak output voltage remains stable at 155.6 V. The peak output current changes from 3.22 A to 6.39 A.

When considering the output power of 500 W, in boost mode, $V_{mp.max}$ and $V_{mn.max}$ are 1.571 and 1.645, respectively, as shown in Fig. 12(a). In buck mode, $V_{mp.max}$ and $V_{mn.max}$ are 0.784 and 0.80, respectively, as shown in Fig. 12(b). The difference in the peak values of V_{mp} and V_{mn} indicates that the closed-loop control process has been implemented to maintain a symmetrical output voltage.

Table 6 provides insights into the average output voltage ($V_{o.avg}$), average output current ($I_{o.avg}$), and THD of the output current (THD.I_o) in both open-loop and closed-loop operation modes of the CG-5S-BTI inverter. An analysis of Table 6 reveals that when CG-5S-BTI operated in open-loop mode (Fig. 6), $V_{o.avg}$ increased corresponding to the increase in load power. Consequently, this variation influenced THD.I_o, resulting in an increase in THD.I_o. For closed-loop operation (Fig. 7), $V_{o.avg}$ approached zero and THD of the output current in the proposed inverter is lower under closed-loop control compared to open-loop control. This outcome demonstrated the improvement in power quality at the inverter's output during closed-loop operation.

B. SIMULATION RESULTS OF THE PROPOSED INVERTER USED FOR PV SYSTEMS

This section presents the simulation results of the proposed inverter for photovoltaic (PV) systems, focusing on its performance under varying environmental conditions and its ability to efficiently track the maximum power point (MPP) and synchronize with the grid. The system parameters used in the simulation are detailed in Table 7. The PV array consists of 11 series-connected modules with 36 cells per module, designed to deliver a maximum power of 0.88 kW at the MPP, corresponding to a voltage of 196.8 V and a current of 4.47 A. The inverter is connected to the grid with a voltage of 220 V (rms) and a frequency of 50 Hz. As depicted in Fig. 13, the simulation was conducted using a detailed model of the proposed inverter, incorporating the MPPT algorithm, phase-locked loop (PLL), and PI control strategies. The MPPT algorithm [26], [29] used to extract the maximum power from the PV panel (P_{max}). The reference current (i_{ref}) was accurately computed based on active and reactive power (Q_{ref}), and the actual current (i_g) followed i_{ref} closely, demonstrating the PI controller's precision in current regulation.

Fig. 14 illustrates the response of the grid-connected inverter system under variations in irradiance and temperature, as well as the operation of the maximum power point tracking (MPPT) algorithm. The monitored parameters include solar irradiance, temperature, PV voltage (V_{PV}), PV current (I_{PV}), PV power (P_{PV}), and grid power (P_g) as shown in Fig. 14(a). Two cases are considered: changes in temperature (from the 1st second to the 2nd second) and changes in irradiance (from the 3rd second to the 4th second). Initially, the irradiance is kept constant at 1000 W/m^2, and the temperature decreases from 50°C to 25°C from the 1st second to the 2nd second, with the voltage changing from 183 V to 200 V and the current varying slightly from 4.21 A to 4.38 A. This indicates that temperature changes also affect the

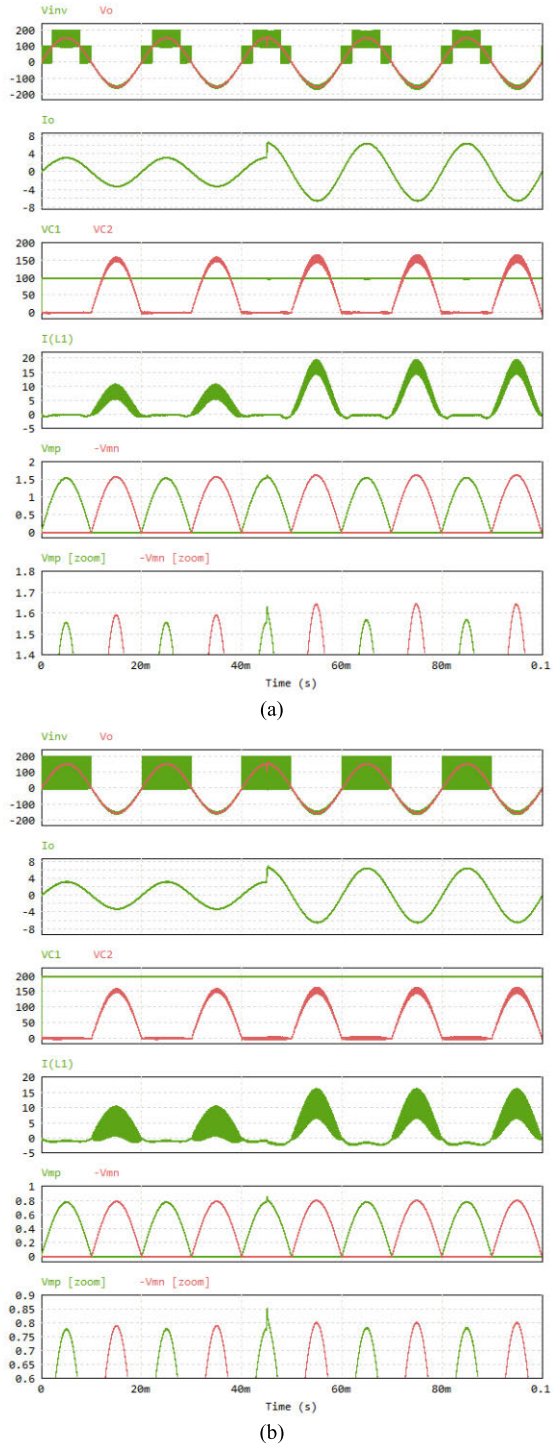

FIGURE 12. Simulation results during transient response from $P_o = 250$W to $P_o = 500$W in (a) Boost mode and (b) Buck mode.

TABLE 7. Parameters of PV inverter system.

Element	Value
PV Power at MPP (P_{mpp})	0.88 kW
Cells per module (N_{cell})	36
Parallel strings	1
Series-connected modules per string	11
Standard light intensity	1000 W/m²
Reference temperature	25°C
PV Voltage at MPP (V_{mpp})	196.8 V
PV Current at MPP (I_{mpp})	4.47 A
Open-circuit voltage (V_{oc})	235 V
Short-circuit current (I_{sc})	4.75 A
Inductors (L_1, L_g)	0.3 mH, 6 mH
Inverter Capacitor (C_1, C_2)	220 µF, 5 µF
Switching frequency (f_s)	30 kHz
PI controller parameters	$K_P = 0.02$, $K_I = 4.2\times10^{-7}$
PV-side capacitance (C_{pv})	2.2 mF
Grid voltage ($V_{g,rms}$)	220 V
Grid frequency (f_g)	50 Hz

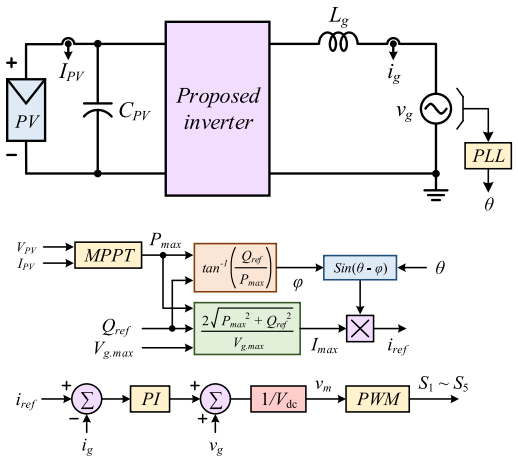

FIGURE 13. Block Diagram of Inverter Control System for Optimal PV Integration.

power output of the solar panel (from 772 W to 876 W) [40]. Subsequently, the temperature is held constant at 25°C, and the irradiance decreases from 1000 W/m^2 to 500 W/m^2 from the 3rd second to the 4th second. The PV voltage remains almost unchanged throughout this period, maintaining stability around 200 V, while the current decreases from 4.38 A to 2.05 A. Consequently, the PV output power also decreases correspondingly (from 876 W to 410 W). This characteristic aligns with the actual operating characteristics of the PV module [40]. Fig. 14(b) displays the output voltage waveform of the inverter, the grid voltage, and the grid current when the proposed inverter is used in a PV power generation system under changing irradiance and temperature conditions. As the irradiance and temperature vary, the PV output power and the current at the output of the proposed inverter change accordingly.

These results demonstrate the effectiveness of the inverter in maintaining operational performance and optimizing power output under varying environmental conditions.

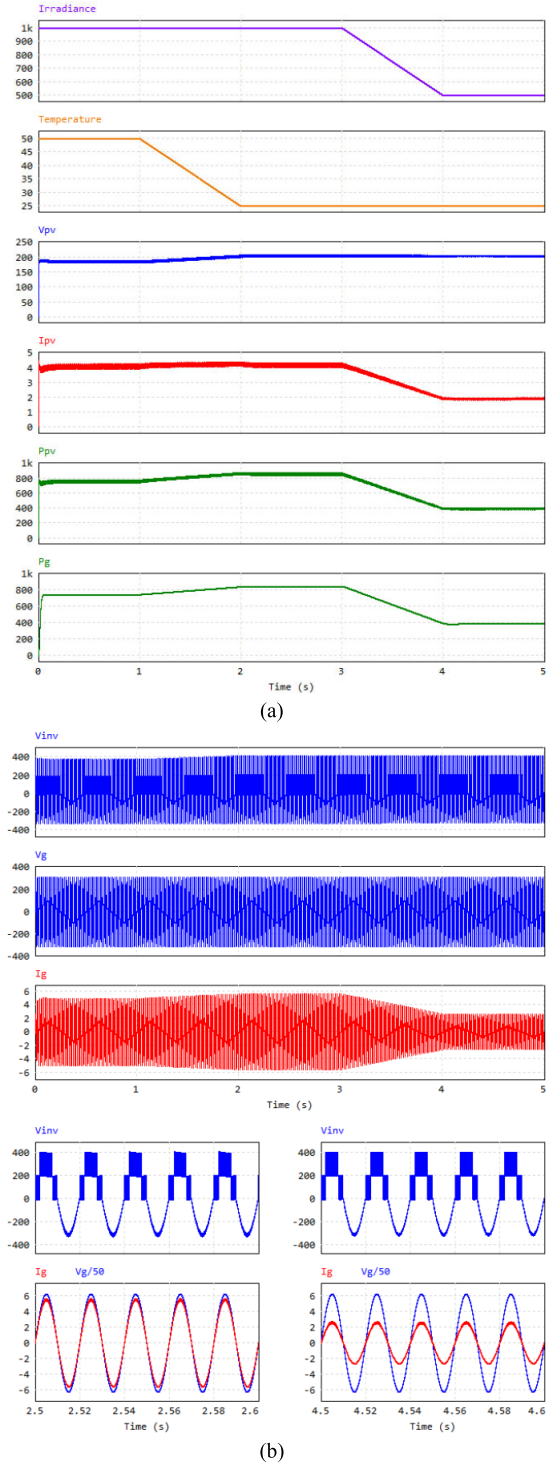

FIGURE 14. Simulation results grid-connected inverter dynamics with changing Solar Irradiance and Temperature. (a) V_{pv}, I_{pv}, P_{pv}, P_g. (b) V_{inv}, V_g, I_g.

C. EXPERIMENTAL RESULTS

A laboratory prototype was constructed and tested based on the parameters presented in Table 8 to verify the performance of the proposed CG-5S-BTI. A visual representation of the experimental setup is depicted in Fig. 15. Specifically, key

TABLE 8. Laboratory prototype specifications.

Element	Type	Description
Diode D_1	STPS60SM200C	200V/60A
Switches S_1, S_2	IRFP4868PBF	300V/70A/25.5mΩ
Switches S_3, S_4, S_5	C3M0045065D	650V/49A/45mΩ
Capacitor C_1	B43504A2227M000	220 µF
Capacitor C_2	B32674D6505K	5 µF
Filter capacitor C_f	B32654A4225J000	2.2 µF
Inductor L_1	Ferrite Core	0.4 mH
Filter Inductor L_f	Iron Core	1 mH
Gate Driver	TLP-250	-
Voltage Sensor	LEM LV 25-P	-
DSP controller	TMS320F280049C	-
Input voltage V_{dc}	-	100 V – 200 V
Output voltage v_o	-	155 V_{peak}
Output Power P_o	-	500 W
Line frequency f_o	-	50 Hz
Switching frequency f_s	-	30 kHz

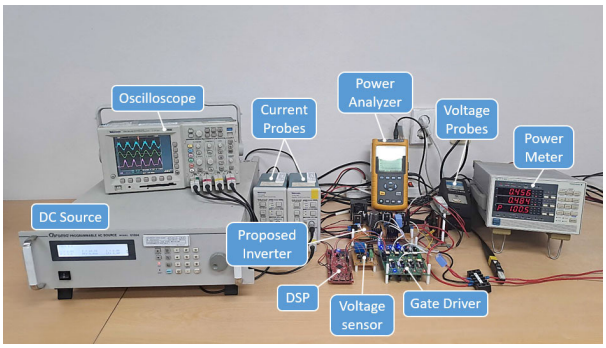

FIGURE 15. Experimental setup of the proposed CG-5S-BTI.

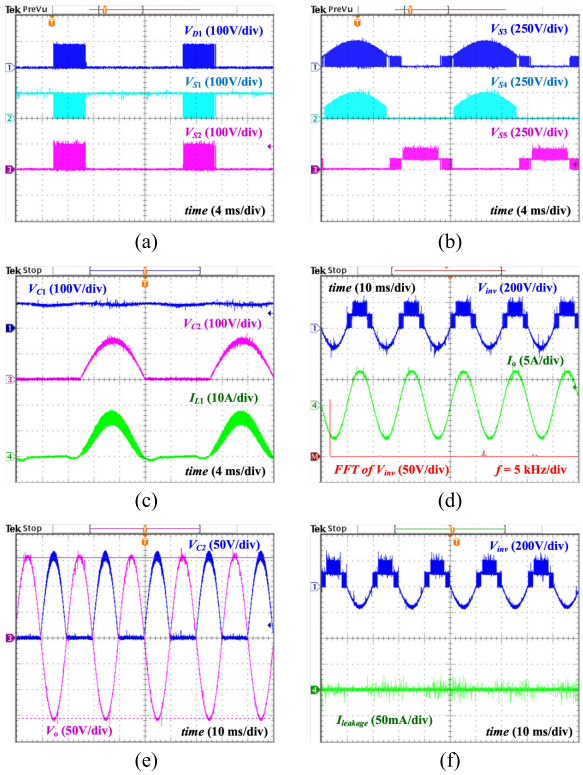

FIGURE 16. Experimental results. (a) VD_1, VS_1 and VS_2. (b) VS_3, VS_4 and VS_5. (c) VC_1, VC_2 and IL_1. (d) V_{inv}, I_o and FFT of V_{inv}. (e) V_o and VC_2. (f) V_{inv} and $I_{leakage}$.

components included the following: IRFP4868PBF MOSFETs are used for S_1 and S_2, C3M0045065D MOSFETs are used for S_3, S_4, and S_5, while D_1 is represented by the STPS60SM200C. Electrolytic capacitor C_1 is a 220 μF, film capacitor C_2 is a 5 μF, and inductor L_1 is a 0.4 mH. The main control board employed a TMS320F280049C DSP processor, and gate signals are transmitted from the DSP board to the MOSFETs through TLP 250 optocouplers. These optocouplers ensured electrical isolation between the low-voltage DSP logic circuit and the high-voltage gate-side circuit of the MOSFETs. The experimental data are captured using a 4-channel TDS 3014B oscilloscope (Tektronix). A Chroma 61604 DC power supply provided the DC input voltage. The performance of the CG-5S-BTI was evaluated for two cases: one with an input voltage of 100 V for the boost mode, and the other with 200 V for the buck mode. In both cases, the output voltage and load power are set to 110 Vrms and 500 W, respectively.

Fig. 16 displays the experimental results for a 100 V input voltage with a voltage gain of 1.55. In Figs. 16(a) and 16(b) depict the voltage stresses on the switches and diodes, with diode D_1 and switches S_1 and S_2 maintaining approximately 100 V. Switches S_3 and S_4 exhibited voltages of approximately 250 V, while the voltage on switch S_5 is 200 V. This is because, $v_{S4} = v_{C2} + v_{L1}$ in Mode IV, $v_{S3} = v_{C1}$ - v_{L1} in Mode V, and $v_{S5} = V_{dc} + v_{C1}$ in Mode I, as displayed in the Figs. 4(a), 4(b) and 3(a), respectively.

Fig. 16(c) displays voltage waveforms across capacitors C_1 and C_2, and the current of inductor L_1. The voltage on capacitor C_1 is maintained at 100 V, while the voltage across capacitor C_2 varied. In the positive half-cycle, the voltage across capacitor C_2 is zero, and in the negative half-cycle, the voltage across capacitor C_2 is -v_o. Inductor L_1 operated in the positive half-cycle, and in the negative half-cycle, it transferred energy from the DC source to the load.

The average current and ripple magnitude of inductor L_1 are 4.37 A and 5.8 A, respectively. As demonstrated in Fig. 16(d), the peak values of the inverter output voltage are approximately 200 V for the positive half-cycle and 155 V for the negative half-cycle. The peak output current is 6.22 A, and the total harmonic distortion (THD) of the output load current is 1.72%. An FFT analysis of the proposed CG-5S-BTI is illustrated in Fig. 16(d).

Fig. 16(e) displays symmetric output voltage waveforms, where the voltage across capacitor C_2 is equal to the output voltage in the negative half-cycle. It is evident that the output voltage in the positive and negative half-cycles was symmetrical.

To assess the inverter's leakage current, capacitor C_{pv} (100 nF) and a resistor R_E (10 Ω) were employed to emulate the PV parasitic capacitance and ground resistance, as

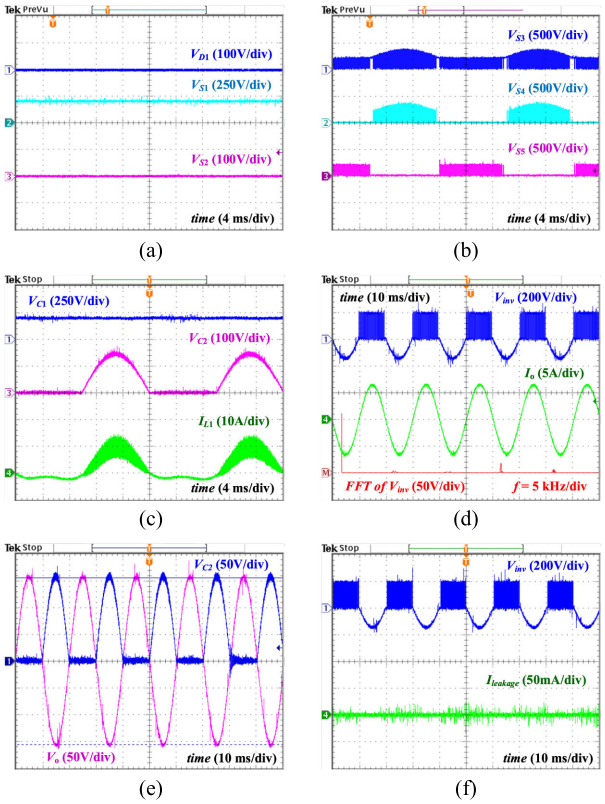

FIGURE 17. Experimental results. (a) VD_1, VS_1 and VS_2. (b) VS_3, VS_4 and VS_5. (c) VC_1, VC_2 and IL_1. (d) V_{inv}, I_o and FFT of V_{inv}. (e) V_o and VC_2. (f) V_{inv} and $I_{leakage}$.

illustrated in Fig. 8. Consequently, the leakage current could be determined by measuring the current passing through R_E. The measured rms value of the leakage current was close to zero, which was attributed to the common-ground features of the proposed inverter. The leakage current in this mode is depicted in Fig. 16(f).

Fig. 17 displays the experimental output voltage and current waveforms of the CG-5S-BTI operating in buck mode. The input voltage is set to 200 V, with a voltage gain of 0.78. Fig. 17(a) illustrates the voltage stresses on switches S_1, S_2, and diode D_1. In this mode, diode D_1 and switch S_2 are conducted, resulting in zero voltage across them. In contrast, switch S_1 maintained a voltage close to the input voltage. Fig. 17(b) displays that the voltages on switches S_3 and S_4 are approximately 352 V, and switch S_5 is about 200 V. In Fig. 17(c) displays the voltage waveforms across capacitors C_1 and C_2 and the current of inductor L_1. Here, capacitor C_1 maintained the input voltage, while the voltage across capacitor C_2 resembled the output voltage waveform with a voltage ripple (Δv_{C2}) of approximately 18V, which was consistent with the theoretical calculations. The average current flowing through inductor L_1 is measured at 4.21 A. The current through inductor L_1 in buck mode is lower compared to boost mode because d_n in buck mode is always lower, as clarified in (35). Fig. 17(d) displays the inverter output voltage and output current with a peak output current value of 6.31 A. The THD of the output load current is recorded

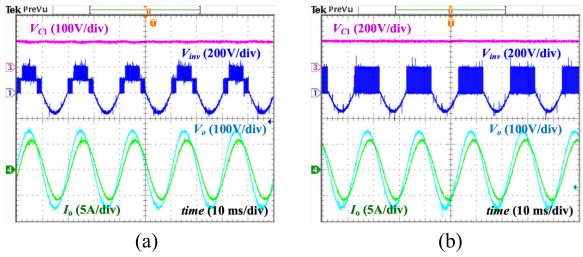

FIGURE 18. Experimental results under a series resistive–inductive RL load: (a) Boost mode. (b) Buck mode.

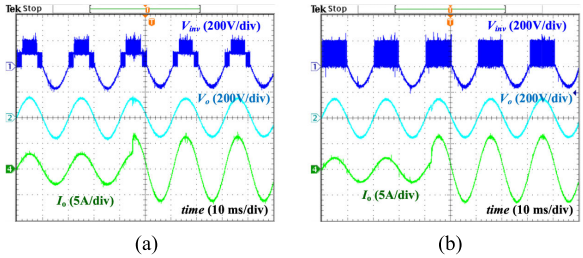

FIGURE 19. Experimental results of the proposed inverter when load is changed from 250W to 500W: (a) Boost mode. (b) Buck mode.

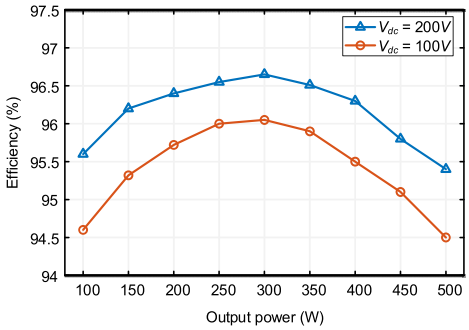

FIGURE 20. Efficiency versus output power.

at 1.05%, and the FFT analysis of the proposed CG-5S-BTI is also illustrated in this figure. Fig. 17(e) demonstrates the symmetrical output voltage at 155.5V. while Fig. 17(f) indicates that the measured leakage current is close to zero.

An RL (resistive–inductive) load is illustrated in Fig. 18, comprising resistive and inductive components of 25 Ω and 24 mH, respectively. Here, the load current exhibited sinusoidal behavior with an amplitude of approximately 6.1 A and a phase angle of 17.4° between the voltage and current. Fig. 19 depicts the dynamic response of the proposed inverter under sudden load changes based on the control strategy illustrated in Fig. 7 and verified through simulations in Fig. 12. The inverter output voltage (V_{inv}) and the voltage across the resistive load remained stable, even when the load was increased from 250 W to 500 W. These results demonstrate that the control strategy effectively stabilizes the inverter's output under varying load conditions, validating the theoretical performance of the PI controllers.

The experimental efficiency of the CG-5S-BTI is presented in Fig. 20, which was measured using a WT230 YOKOGAWA power analyzer. The highest efficiency at 300 W in

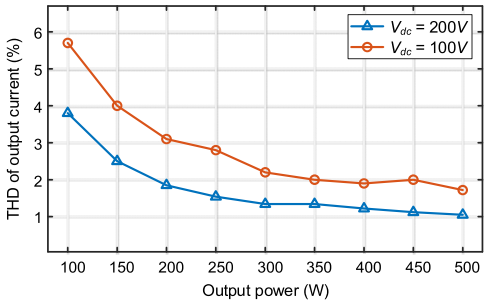

FIGURE 21. THD of the output current versus output power.

buck mode was approximately 96.65%, compared to 96.05% in boost mode.

Fig. 21 illustrates the THD of the output current (%) for various output powers. Considering input voltages of 100 and 200 V, it is evident that starting from an output power of 150 W and above, the THD remained below 5% for both cases. This demonstrates the high quality of the output current, as minimal distortion ensures high efficiency and reduced energy losses in electrical devices.

VII. CONCLUSION

This paper introduced a novel topology based on a common-ground approach for buck/boost functionality. The proposed topology employed five switches and one diode to achieve double voltage gain capability. An input-side SC unit is used to boost the voltage, where the two switches within this unit consistently operated at the input voltage limit, ensuring stable and efficient performance. In addition, a simple PWM modulation strategy was applied to seamlessly integrate this SC unit into the inverter, enabling it to operate in a single stage. Furthermore, during each half-cycle, only two switches operated at a high frequency, reducing switching losses and enhancing overall efficiency. Instead of employing a polarized capacitor (as in conventional five-level common-ground inverters), a film capacitor is used to create the negative half-cycle voltage, effectively reducing voltage ripple on the capacitor, and improving the output voltage quality and efficiency. A comparative analysis illustrated the potential advantages and feasibility of the proposed topology in comparison to recent structures. Finally, the experimental results are presented to further validate the practicality of the proposed topology.

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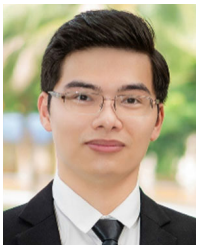

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