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RESEARCH ARTICLE

Mitigation of Single Event Upset Effects in Nanosheet FET 6T SRAM Cell

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ABSTRACT The effects of single event upset (SEU) by alpha particles and heavy ions on the data flip of a 3 nm technology node gate-all-around (GAA) nanosheet field-effect transistor (NSFET) 6T static random-access memory (SRAM) cell was studied through technology computer-aided design (TCAD) simulations. It was found that the sensitivity to radiation in the ''off'' pull-down transistor varies depending on the position of the alpha particle and heavy ions in the incident. The most significant radiation-induced increase in electron density occurs at the drain–channel junction. Heavy ion strikes lead to the lowest threshold linear energy transfer (LET_{th}) value during the hold operation compared to read and write operations. The partial bottom dielectric isolation (PDI) scheme demonstrates lower radiation sensitivity than the conventional scheme, as the PDI layer acts as a physical barrier preventing charge migration from the substrate to the drain.

INDEX TERMS Gate-all-around (GAA), nanosheet field-effect transistor (NSFET), static random-access memory (SRAM), single event upset (SEU), technology computer-aided design (TCAD) simulation.

I. INTRODUCTION

Complementary metal–oxide–semiconductor (CMOS) technology has been continuously improved to enhance performance while reducing power consumption. This is achieved by reducing feature size, node capacitance, and operating voltage. Advances in CMOS technology have led to high-density static random-access memory (SRAM) by reducing its layout area within the wafer area. Highly integrated SRAM is a component used to create the central processing unit cache memory in PCs and mobile products, enabling high-speed operation.

Vertically stacked silicon gate-all-around (GAA) nanosheet field-effect transistors (NSFETs) are increasingly favored for SRAM. That is because NSFETs offer superior electrostatic channel control in the same footprint compared to fin field-effect transistors (FinFETs), which is ideal for scaling down to sub-5nm technology nodes [1], [2].

In sub-10 nm devices, radiation-induced soft errors are still considered the bottleneck for device reliability issues [3]. The single event upset (SEU) phenomenon caused by radiation can cause transient errors in SRAM.

The primary contributors to SEU are alpha particles and neutrons from cosmic rays. Alpha particles, composed of two protons and two neutrons, are emitted when radioactive isotopes contained in package materials and solder in semiconductors decay at low energies. The resulting alpha particles have energies of 4–9 MeV and lose an average of 3.6 eV per electron-hole pair (EHP) as they pass through silicon [4]. This means that millions of EHPs are created

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within the silicon. Neutrons, secondary radiation from the collision of high-energy protons with air molecules, reach the surface [5]. At this time, fast neutrons with energies above 5 MeV can cause soft errors [6], [7].

When high-energy ionized particles strike a sensitive node in an SRAM cell (typically the drain junction of an "off" pull-down transistor), energy is transferred from the ionized particles to the silicon atoms by the Coulomb force between them. The ionized particle passes through the silicon atom along an ion track, creating EHPs. When the ionized particle reaches the depletion region of the pn junction, the generated EHPs temporarily reduce the electric field in the depletion region. The EHPs are separated by the electric field in the depletion region and drift into n- and p-type materials. An electric field is generated along the ion tracks, causing charges to move and generate current, thereby creating a funneling effect. After prompt collection by drift, the remaining carriers move owing to diffusion, which depends on the concentration gradient of the charge carriers. The transport due to diffusion is generally slower than that resulting from drift and lasts until the charge is recombined or collected at the pn junction. The drift current induces a fast initial flip of the cell, whereas the diffusion current affects the recovery process [8]. As the charge is collected, a transient current flows through the struck drain. Restoring transistors (e.g., "on" pull-up transistors) attempt to offset the generated transient current; however, their limited current carrying capacity and conductivity cause the voltage in the drain to drop. This voltage drop can cause an upset phenomenon that can change the logic state of the stuck node (e.g., from "0" to "1" or "1" to "0") [9].

Soft errors in terrestrial applications lead to transient malfunctions, such as blue screens and reboots, which are typically resolved through device replacement or repair. However, in applications used in space environments with abundant high-energy particles and radiation, immediate response to soft errors is challenging. Furthermore, trivial errors in devices used in life-critical fields, such as autonomous vehicles, can cause catastrophic consequences [5].

Transient faults in SRAM devices caused by bit flips can lead to system failures; thus, ensuring reliability against soft errors is crucial. However, research on soft errors has been limited to FinFETs and nanowire SRAM, with no studies on the SEU phenomenon in NSFET SRAM [10].

Prevention techniques are implemented during the chip design and development stages to mitigate the soft error rates of microchips [8]. Radiation-hardened process technologies are used to minimize the collected charge at sensitive nodes or maximize the critical charge [11]. Previous studies investigated heavy ion-induced SEUs in dual- and triple-well 40 nm CMOS SRAMs using additional well isolation techniques. For low linear energy transfer (LET) particles (LET = 8 MeV·cm^2/mg) by heavy ion exposure, triple-well technology is more vulnerable than dual-well. For high-LET particles (LET = 20 MeV·cm^2/mg), triple-well technology further improves the radiation immunity of SRAMs through an "SEU reversal mechanism" However, because the SEU reversal mechanism is determined by various factors, such as the depth of the p-well and doping, it has the limitation that triple-well technology cannot completely prevent the upset of memory cells [12]. Therefore, it is essential to study radiation-hardened process technologies that are not dependent on the SEU reversal mechanism. In a previous study, the sensitivity of SEU to 0.18 μm fully depleted (FD) silicon-on-insulator (SOI) and partially depleted (PD) SOI SRAMs with different SOI film thicknesses has been analyzed and compared [13]. It was found that using FD-SOI devices with a smaller SOI thickness (5 nm) at a high V_{DD} leads to SEU at a high threshold LET (LET_{th}). However, the thickness of the SOI affects the radiation immunity of FD-SOI devices. Previously studied radiation-hardened process technologies focused on devices above 40 nm; therefore, the radiation immunity at technology nodes below 5 nm cannot be guaranteed [12], [13].

As the node shrinks from 40 nm planar SRAM to 7 nm FinFET SRAM, the SER caused by radiation particles decreased, while the 5 nm FinFET SRAM has recently shown an increase in SER [3], [14], [15].

Therefore, it is important to study the radiation response and radiation immunity of 3 nm NSFETs, the state-of-the-art process.

In this study, a scheme was developed to increase the radiation immunity of NSFET 6T SRAM cells. To consider the incident randomness of alpha particles and heavy ions in Section III, the electron density variation at different ion strike positions was examined. The operation of an NSFET 6T SRAM cell, which is the most vulnerable to radiation particles at the worst strike position, was analyzed. The SEU immunity of the partial bottom dielectric isolation (PDI) scheme was compared with that of the conventional scheme through the variation of voltage as a function of time. The conclusions of the study are presented in Section IV.

II. SIMULATION MODELING METHODOLOGY

A 3 nm node NSFET 6T SRAM cell was simulated using Sentaurus technology computer-aided design (TCAD) [16]. The following device physics were applied to validate the accuracy of the simulated model. The high field saturation mobility model characterizes the mobility of carriers that depend on the electric field. The inversion and accumulation layer mobility model was used to accurately predict the change in mobility caused by the interaction of Coulomb impurity scattering, phonon scattering, and surface roughness scattering as the channel length decreases. The Philips unified mobility model describes the bulk mobility of major and minor carriers. In addition to describing the temperature dependence of mobility, the model considers electron–hole scattering, screening of ionized impurities by charge carriers, and clustering of impurities. The Shockley–Read–Hall model with doping dependence, Hurkx band-to-band tunneling model, and Auger recombination model consider

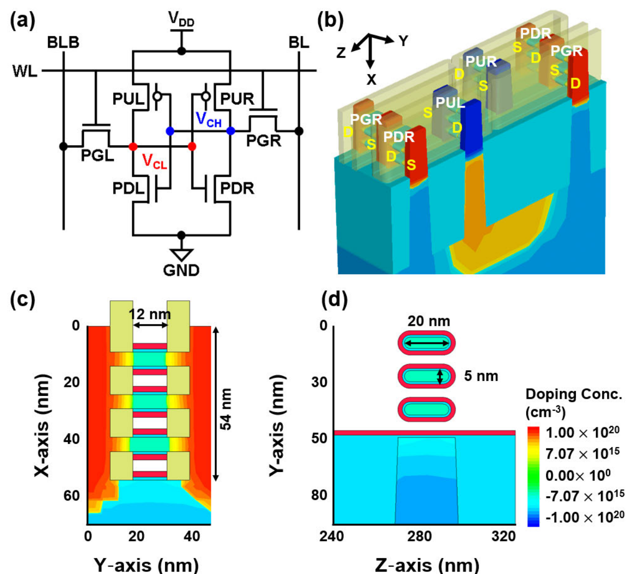


FIGURE 1. (a) The diagram and (b) structure of NSFET 6T SRAM cell. (c) 2-D cross-section view (X-Y). (d) 2-D cross-section view (Y-Z).

gate-induced drain leakage. The modified local density approximation model accounts for the quantum confinement by calculating the confined carrier distribution near the semiconductor–insulator interface. The old Slotboom bandgap narrowing model describes the doping-induced bandgap narrowing in highly doped semiconductors. The stress and strain effects are reflected in a deformation potential model. SiGe in PMOS improves hole mobility with compressive stress. Tensile stresses are considered to improve the mobility of electrons by using SiC in NMOS. The model considers the effects on bandgap, effective mass, effective density of state, carrier mobility, and band structure.

Figs. 1(a) and **(b)** are schematic diagrams of a 3 nm node NSFET 6T SRAM cell. The supply voltage (V_{DD}) provides power to the SRAM cells. The word line voltage (V_{WL}) selects a specific row in the memory array. Bit line voltage (V_{BL}) and bit line bar voltage (V_{BLB}) are the voltages applied to the cells for reading and writing data. The voltage on the CL node (V_{CL}) acts as the input voltage to the right inverter. The voltage at the CL node (V_{CL}) acts as the input voltage to the right inverter, which operates complementary to V_{CH}. The NFET/PFET threshold voltages are 0.38 V and −0.41 V, respectively. The geometric parameters were applied depending on previous studies and are listed in **Table 1** [1]. The device dimensions are shown in **Figs. 1(c)** and **(d)**.

The source and drain regions are doped with phosphorus (boron) at 1×10^{20} cm^{-3} in the NFET and PFET, respectively. The channel of the NFET and PFET is undoped, with 1×10^{15} cm^{-3}. The body doping concentration is 1×10^{18} cm^{-3}. The gate metal work functions of the NFET and PFET are 4.51 and 4.76 eV, respectively. **Fig. 2** illustrates the calibration of the I_d–V_g curve based on previous

TABLE 1. Geometrical parameters for NSFET 6T SRAM cell.

Parameter	Description	Values (nm)
FP	Fin pitch	34
CPP	Contacted poly-gate pitch	48
EOT	Equivalent oxide thickness	1.4
L_g	Gate length	12
L_{eff}	Effective gate length	12
L_{sp}	Spacer length	8
T_{sd}	Source/drain thickness	8
T_{hk}	High-k thickness	2
T_{sheet}	Sheet thickness	5
W_{sheet}	Sheet width	20

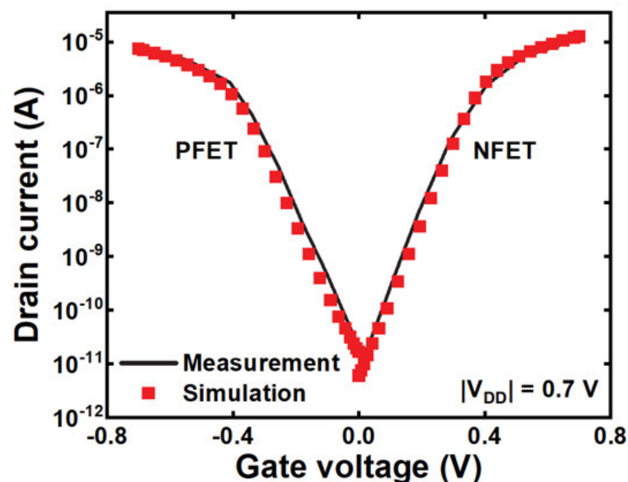


FIGURE 2. I_d-V_g curves for simulation model calibration.

measurement data from a 3nm node NSFET to ensure the accuracy of the simulated NSFET SRAM [1].

Alpha particle and heavy ion radiation models are used to describe the ion strike process. The EHP production rate in the heavy ion radiation model is calculated using LET [17].

The LET measures the energy delivered to the device per unit traverse length, expressed in pC/μm or MeV·cm^2/mg. A charge deposition of 1 pC/μm in silicon equates to 97 MeV·cm^2/mg [18]. Alpha particles are typically expressed in MeV, a unit that represents the kinetic energy of a particle and is considered to have an energy of 1–4 MeV [19]. In contrast, the LET of the heavy ions used in this study ranges from 5–10 MeV·cm^2/mg. The LET above 5 MeV·cm^2/mg assumes cosmic heavy ion strikes [20], [21]. A 10 nm track radius of the Gaussian charge distribution is employed. The particle direction adopts the fin height direction (90°), which was identified as the most severe incident angle in a previous study [22].

III. RESULT AND DISCUSSION

The sensitivities of SEU in the "off" state right pull-down transistor (PDR) of a NSFET 6T SRAM cell to alpha particles with energies = 1 MeV, 3 MeV and heavy ions with LET = 5 MeV·cm^2/mg, 7 MeV·cm^2/mg were investigated;

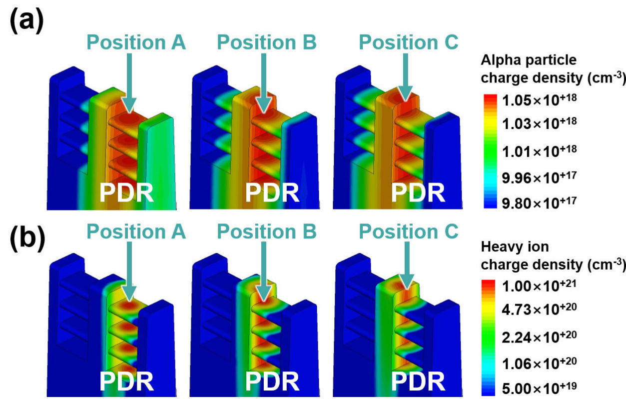


FIGURE 3. Ionized charge distribution during hold operation due to strikes from (a) alpha particles with energy = 1 MeV and (b) heavy ions with LET = 5 MeV·cm^2/mg at Position A (drain–channel junction region), Position B (drain extension region), and Position C (drain region).

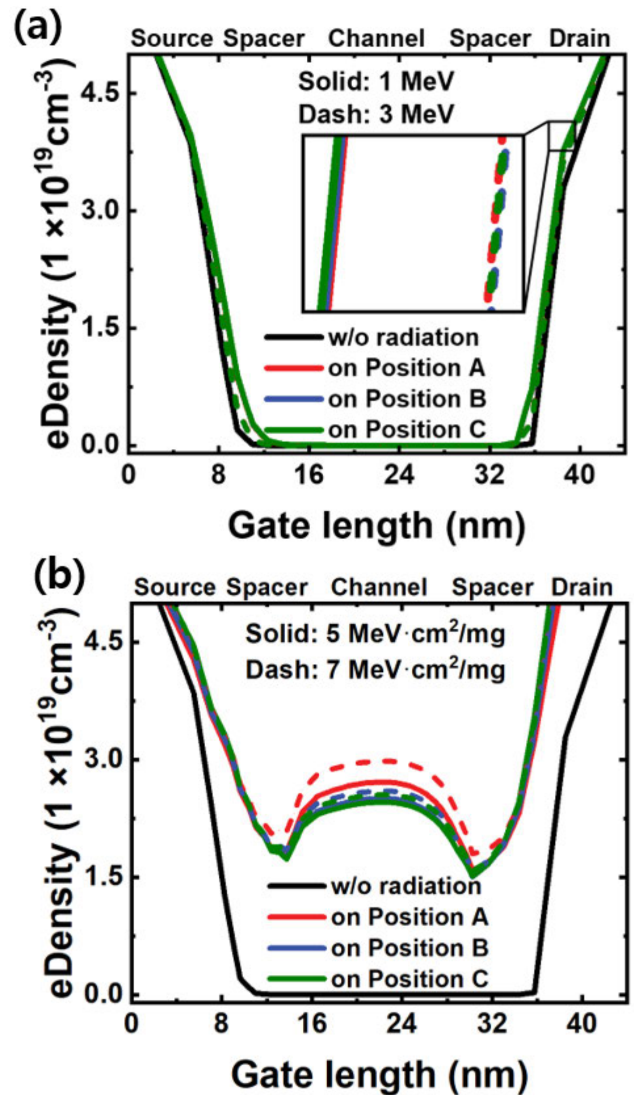


FIGURE 4. Comparison of electron densities at Positions A, B, and C caused by strikes from (a) alpha particles with energies = 1 MeV, 3 MeV and (b) heavy ions with LET = 5 MeV·cm^2/mg, 7 MeV·cm^2/mg at time = 230 ps (w/o radiation) and time = 270 ps (after 20 ps) during hold operation.

the sensitivities were found to depend on the position of the strike. **Figs.** 3(a) and (b) show the strikes at Positions A (drain–channel junction region), B (drain extension region), and C (drain region) during the hold operation at 250 ps. The electron density was extracted from the channel region of the top sheet (height = 15.5 nm) of the "off" PDR of the NSFET.

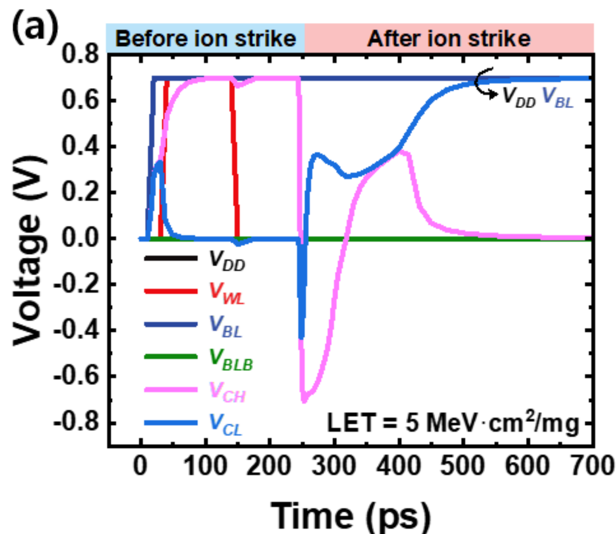
The curve labeled "w/o radiation" refers to the state before the ion is struck. **Fig.** 4(a) compares the electron density before and after an alpha particle with different energies strikes Positions A, B, and C.

When alpha particle with an energy of 3 MeV strikes at position A, the electron density is 1.24 and 1.14 times higher than at Positions B and C, respectively. In contrast, when an alpha particle with an energy of 1 MeV strikes at position A, the electron density increases by 40.70 times compared to 3 MeV. This is due to the lower kinetic energy of the radiation generally resulting in a higher LET, which results in more EHP generation. However, from **Fig.** 4(a), we observe that the effect of the assumed energy of the alpha particles struck at Positions A, B, and C on the variation in electron density is negligible.

In **Fig.** 4(b), when a heavy ion with LET = 7 MeV·cm^2/mg strikes at Positions A, B, and C, the electron density increases by 1.22, 1.24, and 1.23 times compared to LET = 5 MeV·cm^2/mg. At Position A, the electron density increases to 2.56 × 10^{19} cm^{-3} by LET = 5 MeV·cm^2/mg. For positions B and C, it increases to 2.35 × 10^{19} cm^{-3} and 2.32 ×10^{19} cm^{-3}, respectively. This is because Position A is affected by a strong electric field caused by the reverse-biased junction, which reduces the SRH recombination rate. However, the relatively weak electric field at Positions B and C increases the SRH recombination rate, resulting in a lower electron density than at A. Therefore, as the strike position moves from C to A, a channel can be formed for the "off" PDR to switch to "on", improving SEU sensitivity.

The purpose of this study is to observe the mitigation effect on radiation response in the worst-case scenario. While experiments were conducted with alpha particles and heavy ions, the subsequent study focused on the radiation response caused by heavy ions.

Figs. 5(a) and (b) depict the penetration of heavy ions with LET = 5 MeV·cm^2/mg, 7 MeV·cm^2/mg into Position A of the "off" state PDR during hold operation at 250 ps. Ion-induced ionization generates EHPs along the ion track. The electric field separates the generated EHPs within the depletion region of the drain–substrate junction. Electrons are rapidly collected by the drain, generating a transient current pulse. This transient current pulse temporarily reduces the threshold voltage of the "off" PDR, forming an inversion layer and a conductive channel between the source and drain. The formation of the conductive channel results in a high drain-to-source current (I_{ds}). As a result, the drain of the



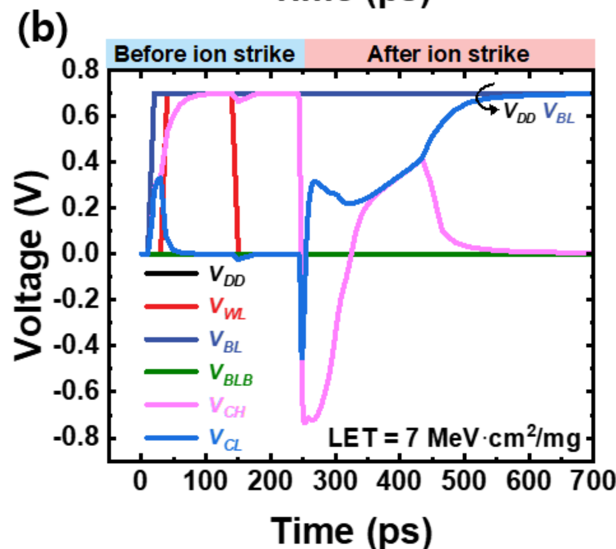
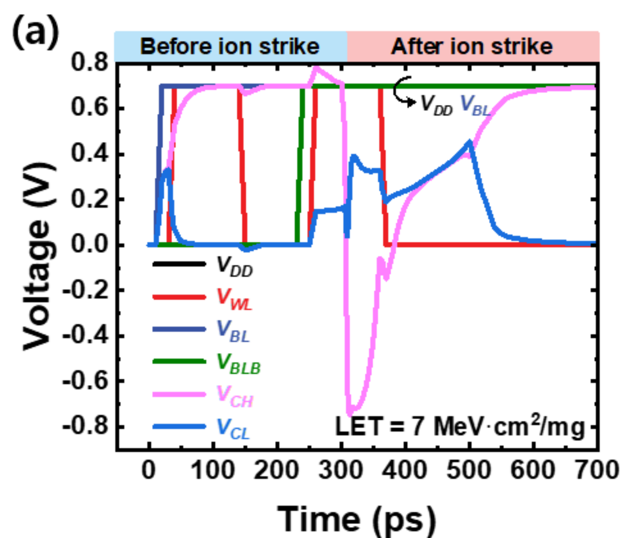


FIGURE 5. SEUs at Position A are caused by heavy ion strikes with (a) LET = 5 MeV·cm^2/mg and (b) LET = 7 MeV·cm^2/mg in the PDR of the NSFET 6T SRAM cell during hold operation. The heavy ion strikes occur at 250 ps, and V_{DD} is kept at 0.7 V after 10 ps.



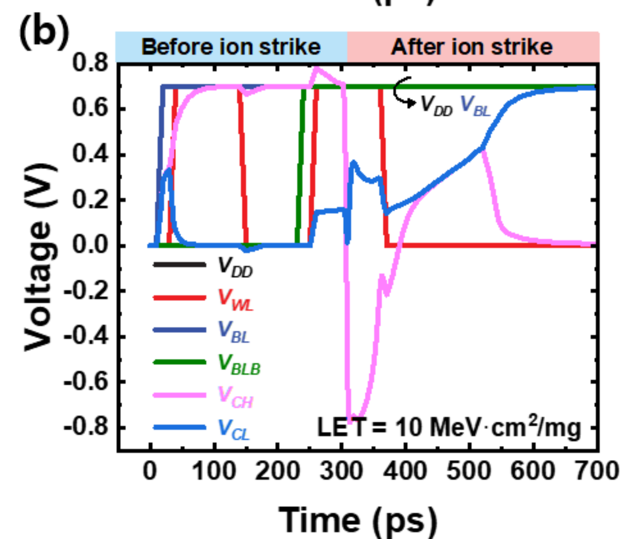


FIGURE 6. During the read operation, (a) no SEU occurs at Position A due to heavy ion strikes with LET = 7 MeV·cm^2/mg, and (b) SEU occurs due to heavy ion strikes with LET = 10 MeV·cm^2/mg in the PDR of the NSFET 6T SRAM cell. The heavy ion strikes occur at 310 ps, and V_{DD} remains at 0.7 V after 10 ps.

PDR discharges, causing the V_{CH} to drop to -0.70 V and -0.76 V when heavy ions with LET = 5 MeV·cm^2/mg and 7 MeV·cm^2/mg strike, respectively. This explains the discharge of logic 1 (= 0.7 V) toward the ground (GND) potential. The voltage drop in V_{CH} supplies the gate of the left pull-up (PUL) through the feedback mechanism of the cross-coupled inverter. As the gate–source voltage (V_{gs}) of the PUL increases, the source–drain current (I_{sd}) increases, as does the V_{CL}. As V_{CL} increases, the V_{gs} of the PDL decreases below the threshold, turning off simultaneously as the PUL turns on. As V_{CL} sufficiently rises to pass through the switching threshold voltage of the left inverter, the logic state flips from logic 0 (= 0 V) to 0.7 V.

Fig. 6(a) illustrates the impact of heavy ion strike with LET = 7 MeV·cm^2/mg at 310 ps on an NSFET 6T SRAM cell during a read operation. The initial state of the read operation was as follows. V_{BL} and V_{BLB} were precharged to 0.7 V. V_{WL} rose to 0.7 V, turning on the right pass gate (PGR) and the left pass gate (PGL). The PDR was off, and the right pull-up transistor (PUR) was on, maintaining the V_{CH} at 0 V. Conversely, the left pull-down transistor (PDL) was on, and PUL was on, keeping the V_{CL} at 0.7 V, representing the state of the cross-coupled inverter pair. As depicted in **Fig. 6(a)**, the V_{CH} temporarily dropped to -0.74 V because of the heavy ion strike. However, after 600 ps, V_{CH}, and V_{CL} recovered to their original logic values. **Fig. 6(b)** shows the occurrence of SEU at 310 ps resulting from the heavy ion strike with LET = 10 MeV·cm^2/mg. The ion strike caused the drain to collect the ion-induced current, thereby turning the PDR into a conductive channel. This resulted in the discharge of electrons from the BL through the PDR to the GND, causing a voltage drop in the V_{CH}. When the V_{CH} dropped to

−0.78 V, the source-to-drain potential of the PUR decreased. The decrease in the V_{gs} of the PUL and PDL caused the V_{CL} to increase above the threshold voltage of the left inverter, turning off the PDL. Electrons generated in the substrate by heavy ions with a value of LET = 10 MeV·cm^2/mg do not recombine sufficiently for the V_{CH} to recover. Therefore, LET_{th} in read operation is 10 MeV·cm^2/mg.

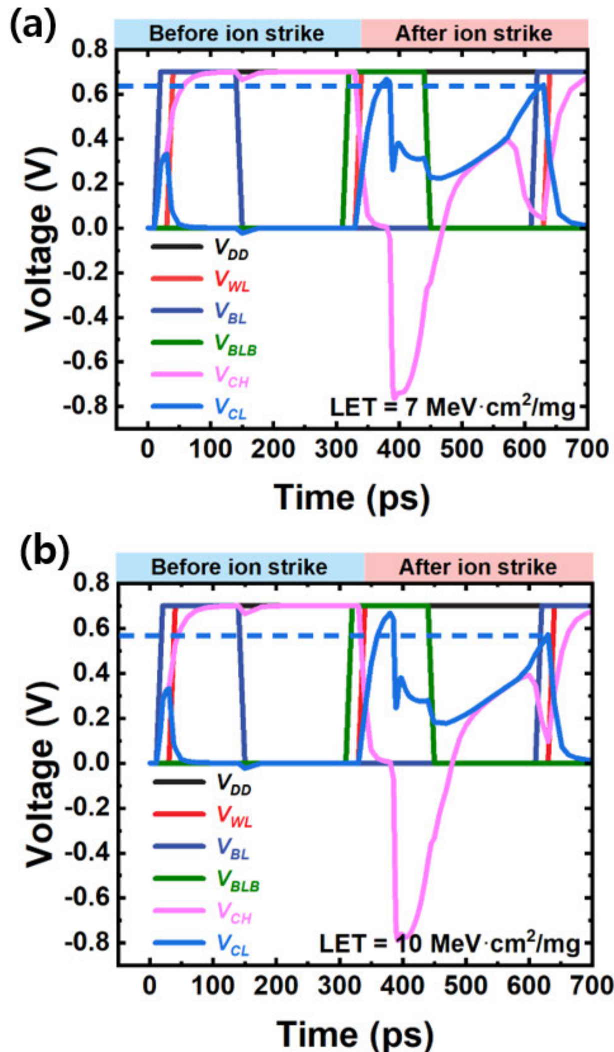


FIGURE 7. During the write operation, no SEU occurs at Position A due to heavy ion strikes with (a) LET = 7 MeV·cm^2/mg and (b) LET = 10 MeV·cm^2/mg in the off-state PDL of the NSFET 6T SRAM cell. The heavy ion strikes occur at 390 ps, and V_{DD} maintains a voltage of 0.7 V following 10 ps.

Figs. 7(a) and (b) demonstrate the occurrence of bit flips during the write operation due to radiation strikes. Initially, V_{CH} and V_{CL} are set to 0.7 V and 0 V, respectively, which is indicated by BLB at 0.7 V and BL at 0 V.

Heavy ions strike the drain–channel junction, position A of the "off" PDL, at 390 ps. When enough charge is collected to form a channel, the PDL turns on, temporarily decreasing the V_{CL}, but V_{CL} is gradually pulled up by V_{BLB}. When V_{CL} drops below the threshold, the channel forms on PUR, causing V_{CH} to temporarily increase.

However, V_{CH} and V_{CL} are switched back to their original logic states of 0 and 1 due to V_{BL}.

From **Figs. 5, 6**, and **7**, it can be observed that the worst-case scenario is the hold operation. This is because the LET_{th} of the hold operation is 5 MeV·cm^2/mg, which is lower than that of the read and write operations, making it more susceptible to bit flips.

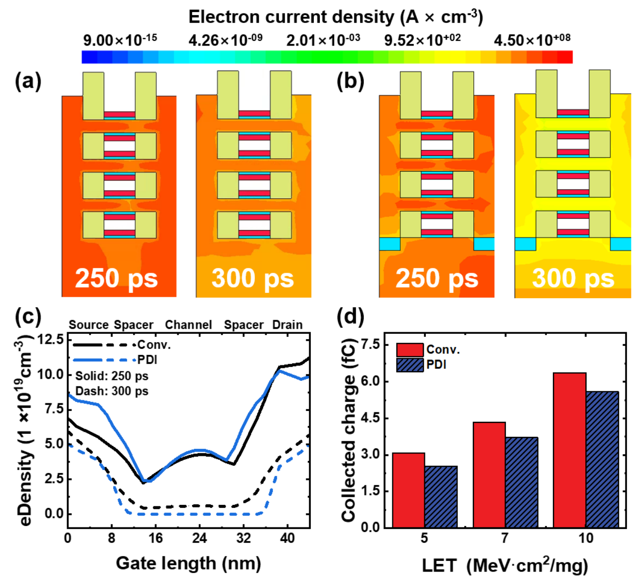


FIGURE 8. The variations in electron current density at (a) conventional (Conv.) scheme NSFET 6T SRAM cells and (b) PDI scheme NSFET 6T SRAM cells are shown at 250 ps, which is the time of heavy ion strike during hold operation, and 50 ps after the strike. (c) The electron density is extracted from the channel of the top sheet (height = 15.5 nm), and (d) the collected charge is observed in both the conventional scheme and PDI scheme when LET = 5 MeV·cm^2/mg, 7 MeV·cm^2/mg, and 10 MeV·cm^2/mg.

Figs. 8(a) and (b) show a comparison of the electron current density of the 6T SRAM cell under the conventional scheme and PDI scheme with suppressed sub-sheet leakage [1], [23], [24]. The PDI scheme adopts an oxide thickness of 5 nm [25]. In the PDI scheme, after heavy ion with LET = 5 MeV·cm^2/mg impinged on Position A, the electron current density decreased compared with the conventional scheme. As shown in **Fig.** 8(c), the peak electron density in the channel of the PDI scheme was 5.77 × 10^{17} cm^{-3}, which was lower than the 3.00 × 10^{19} cm^{-3} observed in the conventional scheme. This decrease is attributed to the PDI scheme, which restricted the electrons generated in the substrate region by preventing the heavy ions from collecting into the drain through drift and diffusion.

Fig. 8(d) shows the collected charge in the drain by the heavy ions with values of LET = 5 MeV·cm^2/mg, 7 MeV·cm^2/mg, and 10 MeV·cm^2/mg for the conventional and PDI schemes. The collected charge was calculated from the electron current densities between 250 ps and 300 ps.

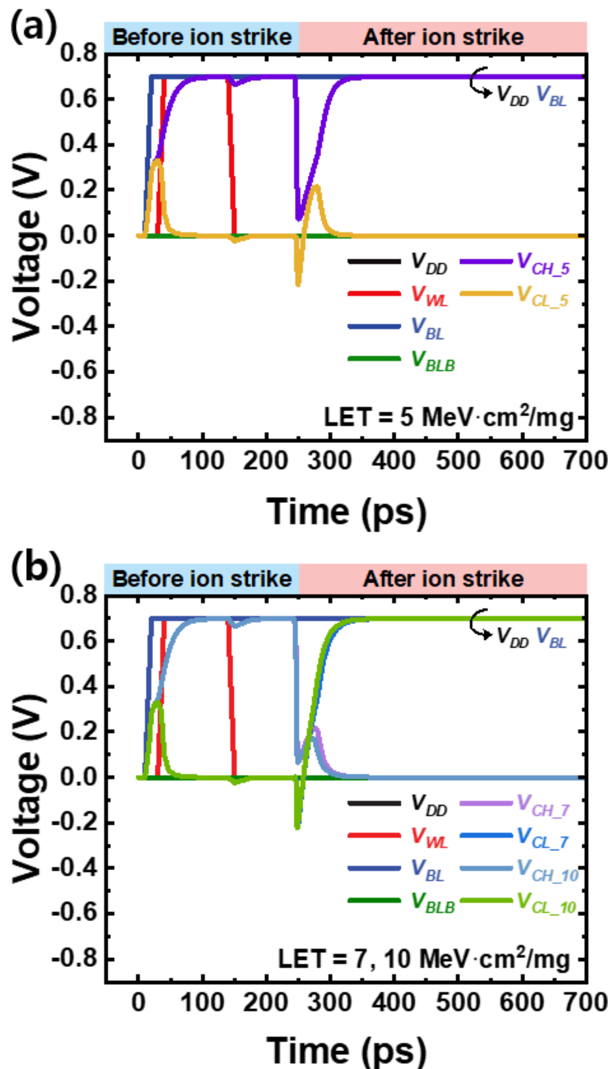


FIGURE 9. The voltage drop induced by heavy ions with (a) LET = 5 MeV·cm^2/mg, (b) LET = 7 MeV·cm^2/mg, and (c) LET = 10 MeV·cm^2/mg in a PDI scheme NSFET 6T SRAM cell, where V_{DD} is maintained at 0.7 V after 10 ps, is examined. Here, V_{CH_5} denotes the scenario where heavy ion with LET = 5 MeV·cm^2/mg impacts the cell. Similarly, V_{CH_7} represents the scenario with heavy ion impact of LET = 7 MeV·cm^2/mg, and V_{CH_10} corresponds to the case of heavy ion impact with LET = 10 MeV·cm^2/mg.

For the conventional scheme, the collected charges were 3.07 fC, 4.35 fC, and 6.37 fC for LET = 5 MeV·cm^2/mg, 7 MeV·cm^2/mg, and 10 MeV·cm^2/mg, respectively. The PDI scheme had lower collected charges compared with the conventional scheme: 2.54 fC, 3.71 fC, and 5.60 fC for all struck LET values of 5 MeV·cm^2/mg, 7 MeV·cm^2/mg, and 10 MeV·cm^2/mg, respectively. The PDI scheme physically isolated the bottom of the drain from the substrate, minimizing the collected charge.

Figs. 9(a) and **(b)** show the voltage transient response of the PDI scheme SRAM cell for different LET values. For the conventional scheme, the conductive channel is maintained by the collected carriers for a sufficiently long time so that the logic of the V_{CH} needs time to change from 0.7 V to 0 V. **Fig. 9(a)** shows that when the LET of heavy ions is 5 MeV·cm^2/mg, the voltage drop of the V_{CH} is −0.21 V, which is lower than the conventional scheme. This is because the PDI layer limits the diffusion and induces localized charge collection, as shown in **Fig. 8(d)**. The localized charge collection is mitigated by the restoring transistor, PUR, which quickly recovers to the initial logic state after a radiation strike.

Fig. 9(b) shows the flipped SRAM cell when heavy ions are struck with LET = 7 MeV·cm^2/mg, 10 MeV·cm^2/mg. The PDI scheme reduced the collected charge of the generated, decreased the voltage drop, and simultaneously reduced the persistence of the conductive channel, which means that the logic of the V_{CH} changed from 0.7 V to 0 V faster. Despite the lower voltage drop, the collected charge exceeds the critical charge, preventing the restoring transistor from performing its feedback mechanism. In conclusion, the PDI scheme reduces the amount of collected charge due to its limited sensitive volume but is limited in increasing SEU immunity at high values of LET, so it is essential to understand the mechanism in that range.

IV. CONCLUSION

We investigated the radiation response of the NSFET 6T SRAM cell using TCAD simulation. The study found that the radiation response induced by alpha particles is significantly lower than that of heavy ions. The worst strike location was identified as the drain–channel junction, and the hold operation exhibited the highest radiation sensitivity with the lowest LET_{th} compared to read and write operations. The adoption of the PDI scheme for radiation response mitigation showed that the effect is limited to LET values up to 7 MeV·cm^2/mg.

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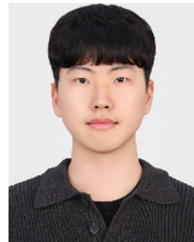

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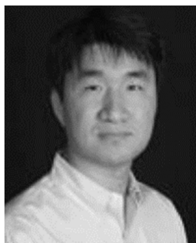

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