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RESEARCH ARTICLE

TPCSA-MRAM: Ternary Precharge Sense Amplifier-Based MRAM

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ABSTRACT The emerging multi-value logic technology in memory systems has increased data storage capacity and power efficiency. In this paper, to address the power consumption challenge of ternary memory, a ternary precharge sense amplifier (TPCSA)-based magnetic random-access memory (MRAM) is designed and simulated for the first time. The proposed TPCSA-MRAM leverages both low power consumption and high performance of TPCSA-based memory and nonvolatility of the magnetic tunnel junction (MTJ). The proposed TPCSA-MRAM also offers high resilience against process variation, which is critical in the ternary circuits. This process variation resilience is validated through Monte Carlo and process corners simulations. A ternary memory array architecture is also designed and simulated based on the proposed design to show the scalability of the proposed TPCSA-MRAM. Detailed post-layout simulations using the 7nm FinFET technology as an industrially available technology for digital circuit fabrication indicate that the proposed design's read and write energy is up to 80% and 37% lower than the existing nonvolatile ternary memories.

INDEX TERMS MRAM architecture, nonvolatility, spintronics, ternary logic.

I. INTRODUCTION

The use of binary logic in digital circuits has been widespread in recent decades [1], [2], [3]. By increasing the complexity of integrated circuits and the number of transistors per unit area, interconnects and pin count density increased significantly [4], [5]. These issues drew scientists' attention to the multi-valued logic (MVL) [6], [7], [8]. MVL is a non-classical logic that extends the principles of classical (binary) logic by allowing more than two truth values [9]. Three-valued logic (ternary logic) is one of the most popular MVL systems due to its ease of circuit-level realization [10], [11]. By utilizing an additional state, ternary systems can represent information more compactly, potentially reducing power consumption and increasing computing speeds compared to traditional binary systems [7].

Hardware implementation of MVL requires multi-threshold transistors [10], [11], [12]. These two features are hardly available in conventional CMOS transistors [13]. FinFET or field-effect transistors have emerged to offer these and other fascinating advantages, such as excellent gate control, higher carrier mobility, smaller drain-induced barrier lowering (DIBL) effect, and high subthreshold swing [14], [15], [16]. Thanks to these features, FinFETs ease the way of the MVL circuit implementation, and recently, scientists and researchers have used FinFET and designed many MVL circuits such as adders, multipliers, memories, and registers [17].

Nonvolatility, high density, and compatibility with other devices cause spintronics-based devices to find an important place in digital circuits [18], [19]. The most important and widely used magnetic-based device is magnetic tunnel junctions (MTJ), made of two ferromagnetic layers separated by a dielectric tunneling barrier [20], [21]. Recently, spintronic technology has also made its way to MVL circuits. The proof of this claim is the design of the different MVL circuits, especially the MVL memories, by many researchers [5], [6], [22].

MVL spintronic memories have been designed [5], [6], [22], [23], [24]. All these memories are based on voltage division. Voltage division is the most straightforward way to read an MTJ state, but this method suffers from high static

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FIGURE 1. Simplified structure of MTJ.

power consumption, large area overhead, and read disturbance [22].

Among these challenges, high static power is important in battery-based devices with limited energy. Read disturbance is also troublesome because it can change the stored data [25]. This paper proposes a layout-level design of magnetic random-access memory (MRAM) based on a ternary precharge sense amplifier (TPCSA), which has low static power and low area overhead, for the first time. Because there are no MTJs in the active path between supply and ground during the read phase, the read disturbance problem is effectively eliminated. Also, due to the symmetric design of the proposed TPCSA, the proposed TPCSA-MRAM is resilient against the fabrication process variations.

The rest of the paper is organized as follows: Section II overviews FinFET, MTJ, and ternary logic. Also, the previous MTJ-based ternary memories are investigated at the end of Section II. Section III explains the design and functionality of the proposed TPCSA-MRAM. Section IV provides the functional simulation, comparative analyses, memory array implementation results, and Monte Carlo simulation results. Finally, Section V concludes the paper.

II. BACKGROUND

A. FinFET

FinFET is a three-dimensional transistor with a Fin-like channel that protrudes from the substrate and is surrounded by a gate on three sides. The structure of a FinFET allows for better control of the current flow, which leads to improved switching speed and reduced leakage current compared to traditional planar transistors [26]. The threshold voltage of a FinFET is the voltage at which the transistor switches from the off state to the on state. In a FinFET, the threshold voltage is affected by several factors, including the width and height of the fin, the gate length, and the doping concentration in the channel [26]. The drain current of a FinFET can be expressed as Eq. 1 [27].

$$I_D = \beta N_{Fin} \frac{2H_{Fin} + T_{Si}}{L} (V_{GS} - V_{th})^{\alpha} \tag{1}$$

where H_{Fin} denotes the height of the fins, NFin is the number of transistor fins, L is the gate length, and T_{si} denotes the fins' thickness. H_{Fin}, T_{si}, and L are usually fixed and are fabrication-related parameters. In Eq. 1, α and β are experimental fitting constants [27], [28]. Based on Eq. 1, by controlling the number of fins (N_{Fin}), the current driving capability of a FinFET can be adjusted. One of the advantages of FinFET is access to different threshold voltages (V_{th}) in these transistors. In general, there are four types of FinFET with different terminal voltages:

- HVT (SRAM) type with high threshold voltage
- RVT type with regular threshold voltage
- LVT type with low threshold voltage
- SLVT type with super-low threshold voltage

Access to different threshold voltages and the commercial availability of FinFETs make these transistors a suitable option for the hardware implementation of MVL systems [27].

B. SPINTRONIC

MTJ is the main element of MTJ/CMOS hybrid circuits [20]. As shown in Fig. 1, an MTJ consists of two ferromagnetic (FM) layers on top of a heavy metal strip separated by a thin oxide barrier [25]. MTJ can exhibit two modes depending on the orientation of the magnetization vector of the FM layers. One of the modes is the parallel mode (P), which occurs when the magnetization vectors of both FM layers are in the same direction [25], [29]. The second mode is the antiparallel mode (AP), which occurs when the magnetization vectors of both FM layers are in opposite directions [6], [30]. The resistance of an MTJ in the antiparallel mode (R_{AP}) is larger than that of an MTJ in the parallel mode (R_P). The ratio of these to resistance is known as the tunnel magnetoresistance (TMR) ratio and is given by Eq. 2 [31].

$$TMR = \frac{R_{AP} - R_P}{R_P} \tag{2}$$

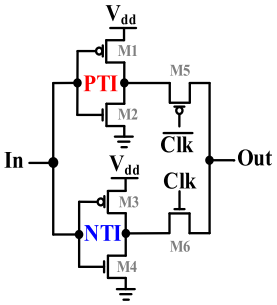
A higher TMR ratio provides higher readability and stability [25], [32], [33]. Notably, a TMR ratio of 604% for in-plane MTJs [34] and a TMR ratio of 249% for perpendicular MTJs [35] were reported in the literature.

C. TERNARY LOGIC

Ternary logic is a logical system that uses three ('0', '1', and '2') [28], [36], [37]. Ternary logic can be used to represent more information than binary logic, and it can be used to create more efficient and powerful circuits [38]. Ternary logic has several advantages over binary logic [10]. For example, as mentioned, ternary logic can represent more information, leading to more efficient and powerful circuits [39]. This feature also reduces the volume of interconnects and pins, easing the circuit design and routing [24], [36].

Ternary systems also find applications in signal processing, where the additional state can be used to model and process complex signals more accurately [9]. In telecommunications, ternary signaling techniques can enhance data transmission rates and improve noise immunity, which is critical for reliable communication over various channels.

Ternary logic can lead to simpler and more efficient circuit configurations in digital circuit design. Some research suggests that ternary logic gates could be more effective than their binary counterparts in certain types of computations, offering the potential for innovation in integrated circuit design [8]. Moreover, in the emerging field of quantum



(a)

Transistors	Type of FinFet	Number of fins
M6	RVT	1
M1, 2, 4, 5	HVT	1
M3	SLVT	2

(b)

In	STI(In)	NTI(x)	PTI(In)
'0'	'2'	'2'	'2'
'1'	'1'	'0'	'2'
'2'	'0'	'0'	'0'

(c)

FIGURE 2. Clocked STI a) circuits structure b) fin counts and transistor types c) truth table of the ternary inverter.

computing, ternary systems are being explored as a possible basis for quantum bits, which could significantly surpass the capabilities of traditional binary computing systems [40].

The common implementation of ternary logic is based on multi-V_{th} transistors at the inputs to detect logic levels and voltage division at the output to generate different output levels [36], [37]. When FinFETs are used for hardware implementation of ternary circuits, the HVT and SLVT FinFET types, mentioned in section II-A, are usually employed [6].

The standard ternary inverter (STI) is the building block of the ternary circuits [10]. The output of an STI gate is '2' if the input is '0', '1' if the input is '1', and '0' if the input is '2.' As shown in Fig. 2, the output of an STI is derived by two inverters, namely PTI and NTI, through M5 and M6. If the input is '0' ('2'), PTI and NTI become '2' ('0') and the output becomes '2' ('0'), and if the input is '1', NTI becomes '0' and PTI becomes '2' resulting in a voltage division and '1' output.

D. PREVIOUS WORK

Generally, a ternary latch requires three stable states and circuitry to transition between them in response to inputs. A conventional ternary latch is composed of two back-to-back STIs. Although the conventional ternary latch has a simple design and low area overhead, it suffers from volatility.

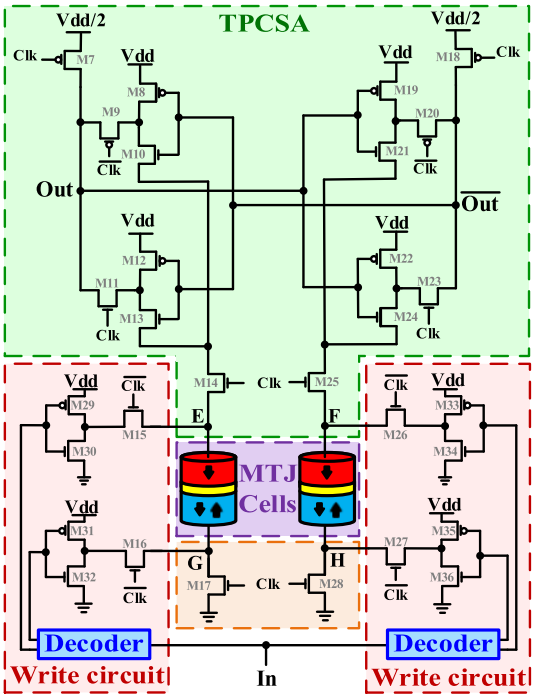
In [6], a ternary MRAM was designed using carbon nanotube FETs (CNTFET). The proposed ternary MRAM in [6] used spin Hall-assisted spin-transfer torque (SHE-STT) MTJ to reduce the write energy. While SHE-STT lowers the writing energy, it requires complex signaling. The read circuitry of the proposed ternary MRAM in [6] does not require a sense amplifier or bistable feedback and is based on voltage division. This feature makes the ternary MRAM proposed in [6] immune to radiation effects. The disadvantage of voltage division is that because this method includes an active path between Vdd and ground, it consumes high static power. However, passing a constant current through the MTJ during the read phase creates a probability of read disturbance.

A spintronic ternary Flip-Flop was also proposed in [22]. This design used master-slave-shadow architecture. In this architecture, a master-slave latch forms a Flip-Flop, and a nonvolatile shadow latch is used for the backup operation. Using a shadow latch ensures that the writing delay of the magnetic tunnel junctions (MTJs) does not affect system performance because the MTJs are not placed on the main data path. The design proposed in [22] is based on voltage division and suffers from high static power consumption and read disturbance problems, similar to the design presented in [6].

III. PROPOSED DESIGN

A. TPCSA-MRAM CIRCUIT

The block diagram of the proposed ternary precharge sense amplifier-based MRAM is shown in Fig. 3. This circuit



(a)

Transistors	Number of Fins
M12-M22	2
M7, 8, 9, 10, 11, 13, 14, 17, 18, 19, 20, 21, 23, 24, 25, 28	1
M15, 16, 26, 27, 29, 30, 31, 32, 33, 34, 35, 36	8

(b)

Transistors	Types of FinFet
M11, 23, 29, 31, 33, 35	RVT
M7, 8, 10, 13, 18, 19, 21, 24	HVT
M9, 12, 14, 15, 16, 17, 20, 22, 25, 26, 27, 28, 30, 32,34, 36	SLVT

(c)

FIGURE 3. Proposed TPCSA-MRAM a) circuits structure b) fin counts c) transistor types.

TABLE 1. The output of the input decoder.

In	In1	In1not	In2	In2not	MTJ1	MTJ2
'0'	'0'	'2'	'2'	'0'	AP	P
'1'	'2'	'0'	'2'	'0'	P	P
'2'	'2'	'0'	'0'	'2'	P	AP

comprises three main parts. The TPCSA contributes to sensing the state of the MTJs and generating outputs.

The MTJ cells are the nonvolatile memory elements of the proposed circuit, and circuits are written to reconfigure the MTJ cells. Based on the clock signal (Clk), the operational phase of the proposed TPCSA-MRAM can be divided into two following phases:

1) PRECHARGE PHASES

In the Precharge phase, Clk is '0', and accordingly, M7 and M18 turn on and Out and $\overline{\text{Out}}$ are precharged to Vdd/2. At the same time, data is written to the MTJ through the write circuit. The write circuit comprises two pass transistors connecting the MTJs to the write circuit, two inverters, and an input decoder [6]. The input decoder converts the ternary input data into four binary signals (In1, In1not, In2, and In2 not). The structure of the input decoder is illustrated in Fig. 4. This circuit comprises four FinFET-based inverters, an NTI, a PTI, and two binary inverters.

The NTI and PTI circuits are low-skew and high-skew binary inverters, respectively. Table 1 also shows the truth table of the input decoder and MTJs states based on the ternary input value.

2) EVALUATION

During the reading mode, the Clk is '2,' and transistors M7 and M18 are turned off, allowing the discharge of Out and $\overline{\text{Out}}$ through the MTJ cells and M14, M17, M25, and M28. Based on Table 1, MTJs can have three distinct states. Given that Out and $\overline{\text{Out}}$ were initially precharged to Vdd/2, and considering the resistance of the MTJ cell in the AP/P (P/AP) configuration, a difference in the discharging current arises due to the resistance difference. The side with lower resistance discharges faster, resulting in a '0' on the side and a '2' on the other side. In the case of both MTJs being in P state, the current becomes equal on both sides, thereby causing Out and $\overline{\text{Out}}$ retain their initial value of Vdd/2, equal to '1.' In the case of both MTJs being in P state, since both Out and $\overline{\text{Out}}$ in Clk='0' being Vdd/2 provided in Clk='2' and there is no race between two MTJs. In a binary cross-coupled inverter pair, positive feedback ensures that the system remains in one of its stable states (usually Vdd or '0'). However, in ternary one, at Vdd/2, both inverters are equally influencing each other, creating a metastable point. Near the Vdd/2 point, the cross-coupled transistors exhibit a kind of pseudo-negative feedback. If the voltage on one side increases slightly above Vdd/2, the opposite transistor will conduct more, pulling the voltage back down. Conversely, if the voltage drops below Vdd/2, the opposite side will pull it back up. Therefore, both inverters connected to the Out nodes guarantee that these nodes are tied to Vdd/2. This scenario is the same for $\overline{\text{Out}}$. In other words, when both MTJs are parallel, we can consider that two resistors are added to the outputs, causing the same current to be drawn from both outputs, so the voltage of the output node does not change.

It is also notable that fabrication process variations can cause resistance differences between the MTJs. However, due to the threshold adjustment of STI, this difference is not significant enough to cause incorrect readings. But if one MTJ is parallel and the other is antiparallel, these two MTJs create sufficiently different currents to cause a voltage difference. This difference is then amplified through positive feedback of two cross-coupled STIs, causing a flip in the outputs.

Figure 5 also shows the layout of the proposed TPCSA-MRAM designed in the Cadence Virtuoso environment using the 7nm FinFET technology kit [26].

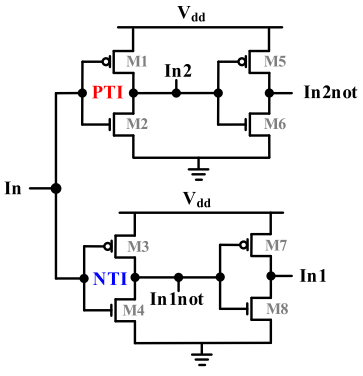
B. ARRAY STRUCTURE

The proposed TPCSA-MRAM can also be employed to implement a memory array. An example of such a design is illustrated in Fig. 6. This arrangement is a 2m word × n trit configuration. Each TPCSA is connected to 2m trits in this configuration and with a shared write circuit and decoder.

IV. SIMULATION RESULTS AND COMPARISON

A. FUNCTIONAL SIMULATIONS

The Cadence Virtuoso and HSPICE tools have been utilized to simulate the proposed TPCSA MRAM circuit at the post-layout level. The 7nm FinFET technology kit [26] and the experimentally validated MTJ model [41] were employed for these simulations. Table 2 details the key parameters of the MTJ cells and FinFETs.



(a)

Transistors	Types of FinFet
M2, 3, 5, 6, 7, 8	HVT
M1, 4	SLVT

(b)

FIGURE 4. a) Decoder structure (all transistors are single-fin) b) transistor types.

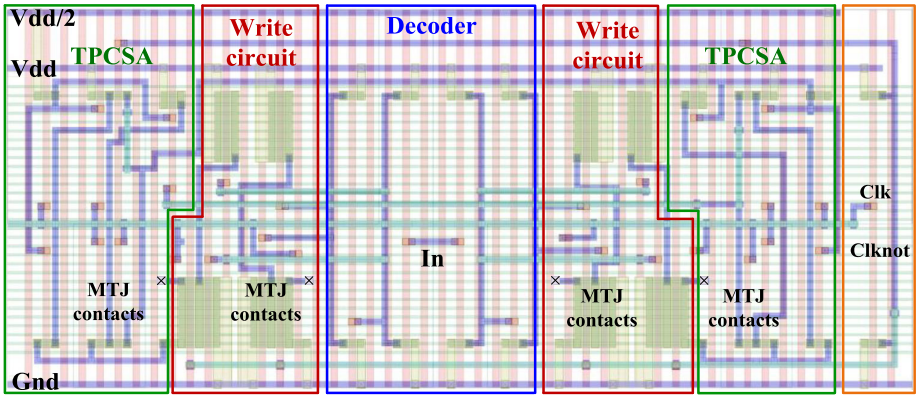


FIGURE 5. The layout of the proposed FinFET-based TPCSA-MRAM.

TABLE 2. The critical MTJ and FinFET parameters considered in the simulations.

Description	Value
MTJ	
Shape	Round
Oxide barrier thickness	1 nm
TMR ratio under zero bias voltage	300%
TMR ratio under operational bias voltage	270%
Free layer thickness	0.85 nm
Surface diameter	40 nm
Resistance-area product	10 pΩ/m2
Resistance	5 kΩ-15 kΩ
FinFET	
Fin thickness (TFin)	6.5 nm
Fin height (HFin)	32 nm
Gate length (Lg)	2.1 nm
Oxide thickness (Tox)	2.1 nm

The waveforms of the proposed TPCSA-MRAM are shown in Figure. 7. This waveform indicates the correct operation of the proposed TPCSA-MRAM. As seen from the waveform of Figure. 7, at the low level of the Clk signal, the write circuits configure MTJs based on the In signal.

As Figure. 7 shows that when Clk is low and In is '0' ('2'), write circuits and configure MTJ1 to parallel (antiparallel) and MTJ2 to antiparallel (parallel) state. Upon the consecutive high level of the Clk, the Out will be '0' ('2') and $\overline{\text{Out}}$ will be '2' ('0'). On the contrary, when Clk is low and In is '1,' the write circuit configures both MTJs to parallel state, and upon the consecutive high level of Clk, the Out and $\overline{\text{Out}}$ will be '1.'

B. COMPARISON

The proposed TPCSA-MRAM is compared to the previous ternary spintronic memories and conventional ternary latch. The results of these comparisons are provided in Table 3. As this table indicates, the proposed TPCSA-MRAM consumes up to 87%, 88%, 12%, and 90% lower average, static, write power, and read power, respectively. This power efficiency is because all previous ternary nonvolatile memories of [6] and [22] are based on the voltage division, which creates an active path between the supply voltage and ground, causing high power consumption. This active path causes a constant current passing through the MTJ, which can cause read disturbance and reduce MTJ endurance.

Compared to the design presented in [6], the proposed TPCSA-MRAM has an 8.8% lower write delay, and compared to the design presented in [22], the proposed TPCSA-MRAM offers the same write delay. Regarding area, the proposed TPCSA-MRAM occupies at least 44% smaller area than the design proposed in [22]. Only the FinFETs are considered in area comparison because MTJs are fabricated in a separate layer above the transistors. This means they don't take up any extra space except for the connections that connect the MTJs to the transistors.

C. PROCESS, VOLTAGE, AND TEMPERATURE VARIATIONS

To evaluate the performance and functionality of the proposed TPCSA-MRAM in the presence of the process, voltage, and temperature (PVT) variations, 1000 runs of Monte Carlo simulations were conducted considering the variations in critical parameters of the MTJ and FinFET devices. These variations are considered to follow a Gaussian distribution at the $\pm 3\sigma$ level. Specifically, the 3σ variations for key parameters of FinFETs, including fin height (H_{Fin}), fin thickness (T_{Fin}), gate length (L_g), and oxide thickness (T_{ox}) are assumed to be 10%. Additionally, we consider variations in other parameters such as tunneling magnetoresistance (TMR), oxide barrier thickness (t_b), resistance-area product, and surface diameter. These variations are set at 10%, 5%, 15%, and 7%, respectively [33]. Figure 8 shows the transient waveform of the proposed TPCSA-MRAM when subjected to fabrication process variations. Figure 9 also illustrates the effect of fabrication process variations on the performance of the proposed TPCSA-MRAM. As these figures indicate, the proposed TPCSA-MRAM has robust functionality even when subjected to fabrication process variations.

Additionally, corner simulations were conducted to verify the functionality of the proposed TPCSA-MRAM under worst-case fabrication conditions, with the corner values

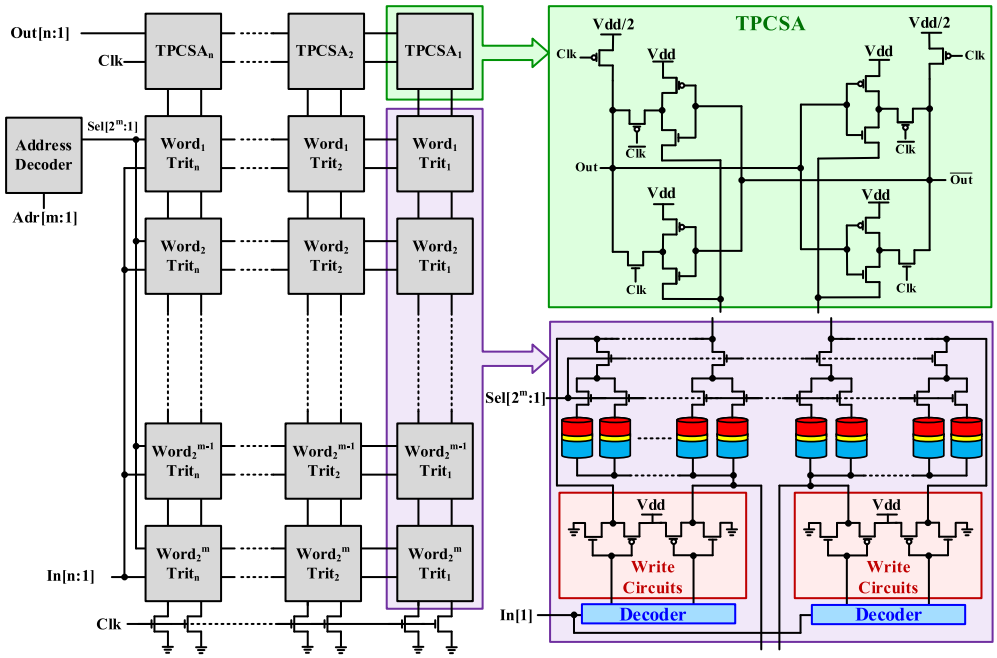


FIGURE 6. The 2^m word × n trit memory array structure based on the proposed TPCSA-MRAM.

TABLE 3. Simulation results.

Design	Average power (uW)	Static power (uW)	Write power (uW)	Read power (uW)	Read delay (ps)	Write delay (ns)	Area (μm2)	Nonvolatility
Conventional TSRAM	3.3	2.1	NA	1.9	6	NA	0.015	No
[6]	69.3	37.1	14.0	63.4	46	4.5	0.820	Yes
[22]	21.2	12.1	19.7	11.3	76	4.11	0.098	Yes
Proposed TPCSA-MRAM	8.4	4.3	12.3	5.9	97	4.1	0.054	Yes

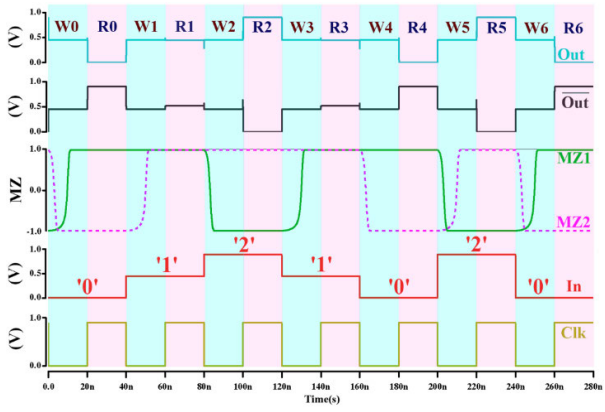


FIGURE 7. Transient response of the proposed circuit.

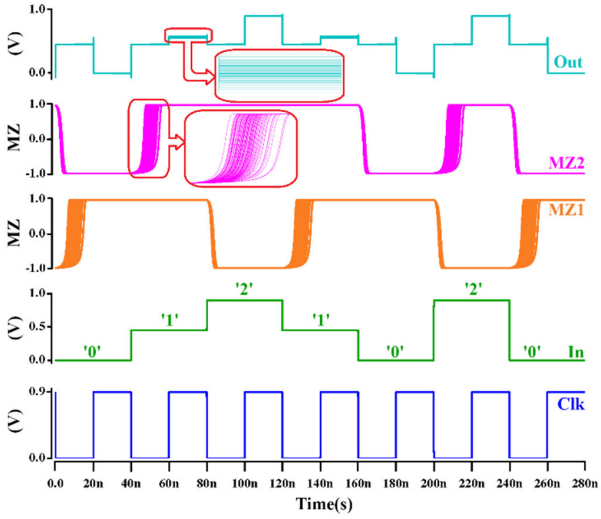


FIGURE 8. Transient waveform of the proposed TPCSA-MRAM when subjected to fabrication process variations.

taken from [26] and [33]. This approach evaluated eight process corners, FFF, FFS, FSF, FSS, SFF, SFS, SSF (nine Fins), and SSS (nine Fins). The results of these simulations are shown in Table 4.

D. ARRAY SIMULATION

To assess the performance of the TPCSA-MRAM in memory array implementation, a 512 × 16 block was evaluated based on the proposed array architecture shown in Fig. 6. The simulation includes all possible read and write operations. The results presented in Table 5 demonstrate that the proposed TPCSA-MRAM operates flawlessly in array

TABLE 4. The results of the process corners simulation.

Corners			Average power (uW)	Static power (uW)	Write power (uW)	Read power (uW)	Read delay (ps)	Write delay (ns)
MTJ	n-Type	p-Type						
F	F	F	11.7	5.8	17.3	8.0	98.8	3.3
F	F	S	10.9	5.0	16.6	7.8	86.8	3.3
F	S	F	11.1	4.4	17.4	8.2	72.5	3.6
F	S	S	10.3	3.6	16.7	8.1	93.1	3.6
S	F	F	7.5	5.1	9.6	4.6	99.5	4.8
S	F	S	6.7	4.3	8.8	4.4	101.4	4.8
S	S	F	6.7	4.0	9.0	4.6	103.6	5.7
S	S	S	6.5	3.6	8.6	4.6	105.0	5.5

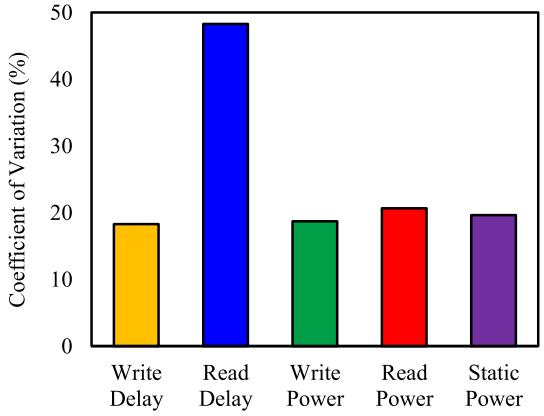


FIGURE 9. Effects of the fabrication process variations on the performance of the proposed TPCSA-MRAM.

TABLE 5. Simulation results of the memory array based on the proposed TPCSA-MRAM.

Parameter	Value
Write power (uW)	173.6
Read power (uW)	131.5
Read delay (ns)	276
Write delay (ns)	17.6

architecture and can be used to implement large-density memories.

V. CONCLUSION

This paper proposes a power and area-efficient ternary precharge sense amplifier-based MRAM for the first time. The proposed TPCSA-MRAM cell utilizes MTJs as its nonvolatile memory elements. Unlike previous nonvolatile ternary memories, the proposed TPCSA-MRAM MTJs do not place an active path between supply voltage and ground, significantly reducing power consumption, eliminating the risk of read disturbance, and increasing the MTJ's endurance. Post-layout simulation results using 7nm FinFET technology show up to 87%, 88%, and 90% lower average, static, and read power consumption and 93% lower area compared to the state-of-the-art nonvolatile ternary memories. Monte Carlo and process corners simulations also show the resilience of the proposed TPCSA-MRAM against fabrication process variation. Our proposed ternary design based on well-established and experimentally validated technologies is a cornerstone for the industrial class of ternary nonvolatile memories in the near future.

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