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RESEARCH ARTICLE

# A Differential PD/TIA Interface for Enhanced SNR and Baseline Wander Reduction in High-Speed CMOS Optical Receivers

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**ABSTRACT** In this paper, a photodiode (PD)/transimpedance (TIA) interface is presented. The cathode terminal of the PD is AC-coupled to one of the inputs of a pseudo-differential TIA while the anode terminal is DC-coupled to the other input of the TIA. The DC-coupled input provides a path for the low-frequency component of the input signal to reach the output. This component is extracted by a baseline wander compensation scheme (BWCS) and fed to the input to eliminate signal drift after long data runs. Compared with the conventional pseudo-differential receiver, the proposed interface improves the gain, the gain-bandwidth product (GBW), and the signal-to-noise ratio (SNR) by 5dB, 1.37× and 4.5dB, respectively, while maintaining 209× smaller low cutoff frequency than the AC coupled receiver. The proposed interface is compatible with any TIA topology. Post-layout simulations and analytical models validate the feasibility of the proposed technique.

**INDEX TERMS** Transimpedance amplifier, optical receiver, signal-to-noise ratio, gain-bandwidth product, baseline wander.

## I. INTRODUCTION

Differentia signal processing provides better immunity against common-mode disturbances than its single-ended (SE) counterpart [1]. However, differential circuit implementations usually trade off with performance metrics. For example, in the pseudo-differential (Ps-Diff) optical receiver in Fig. 1 (a), a replica transimpedance amplifier (TIA) connected to a dummy photodiode is employed to feed the common-mode signal to the second input of main amplifier (MA). This replica TIA does not contribute to signal amplification but increases power dissipation and doubles the input-referred noise power [2]. Therefore, the Ps-Diff structure achieves a 3dB worse signal-to-noise ratio (SNR) compared to its SE counterpart. A differential TIA can be employed to sense the current from both terminals of the PD as shown in Fig. 1 (b). In principle, this differential interface doubles both the gain and output noise power compared to the SE structure, resulting in 3dB and 6dB improvements in the SNR compared to the SE and Ps-Diff structures, respectively.

However, differential sensing increases the effective input capacitance which reduces the bandwidth and degrades noise performance. Furthermore, biasing requirements of the PD prevent direct DC coupling. In [3], [4], and [5], AC coupling was inserted, as shown in Fig. 1(c), to isolate distinct DC voltage levels. The values of $C_C$ and $R_{bias}$ cannot be made arbitrarily large for bandwidth and PD biasing considerations [3], [6]. Therefore, AC coupling introduces a significantly large lower cutoff frequency $f_L$ which causes a severe baseline wander in the output signal when the input data include a long run of consecutive identical digits (CIDs) [Fig. 1(d)].

This work leverages the gain and noise advantages of the differential interface and addresses the limitations of AC coupling by proposing 1) a novel PD/TIA interface,

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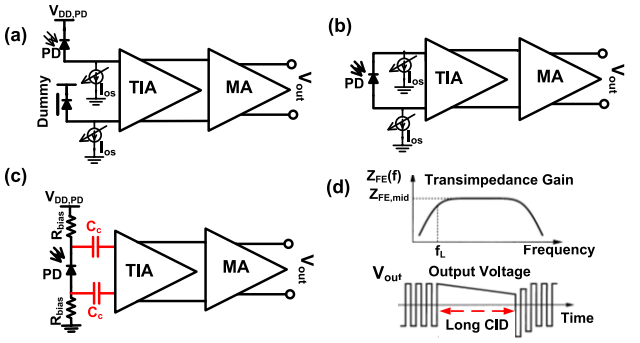



**FIGURE 1.** Various PD/TIA interfaces (a) Pseudo-differential, (b) DC coupled differential, (c) AC coupled differential, and (d) effect of AC coupling in frequency and time domains. Ios removes the average value of the input current.

2) a novel baseline wander compensation scheme (BWCS), and 3) a cross-coupling technique for bandwidth extension. These modifications significantly improve the performance compared with the conventional structures with no power or silicon area overhead.

## II. THE PROPOSED PD/TIA INTERFACE WITH BASELINE WANDER COMPENSATION

Fig. 2 shows a block diagram of the proposed photocurrent sensing technique. The cathode and anode terminals of the PD are AC- and DC-coupled to the inputs of the TIA, respectively. Therefore, the low-frequency component of the input current finds a path to the output through the DC-coupled input. A baseline wander compensation scheme (BWCS) extracts the low-frequency component of each output using a low-pass filter $C_{LPF}$ and $R_{LPF}$, creating $V_{LPF1,2}$ which are converted to currents $I_{BWC1,2}$by a transconductance of $g_{m,BWC}$. The missing low-frequency information can be restored by adding $I_{BWC1,2} = g_{m,BWC}V_{LPF1,2}$ to the input. At the PD's cathode node, the current is divided between the PD's bias resistor $R_{bias}$ and the TIA's input impedance $R_{in}$. Therefore, the voltages at the receiver outputs are calculated as

$$V_2 = Z_{TIA}(s)\,A_{MA}(s)\left(I_{PD} - g_{m,BWC}V_{LPF1}\right) \tag{1.a}$$

$$V_1 = -\alpha Z_{TIA}(s)\,A_{MA}(s)\left[\frac{I_{PD}s}{(\omega_{ac}+s)} + g_{m,BWC}V_{LPF2}\right] \tag{1.b}$$

where, $\alpha = R_{bias}/(R_{bias}+Z_{in})$, $\omega_{ac}= 1/R_{bias}C_{ac}$ is the pole frequency associated with the AC coupling, and $Z_{TIA}(s)$ and $A_{MA}(s)$ represent the transfer functions of the TIA and the MA, respectively. Recognizing that $V_{LPF1} = -V_{LPF2}$ and $V_{LPF2}$ is low pass filtered version of $V_2$, the differential output is

$$V_1 - V_2 = -Z_{TIA}(s)\,A_{MA}(s)\,I_{PD} \cdot\left[1 + \frac{\alpha s}{(\omega_{ac}+s)} + \frac{Z_0A_0(1+\alpha)\,g_{m,BWC}}{\left(1+s/\omega_{LPF}\right)}\right] \tag{2}$$

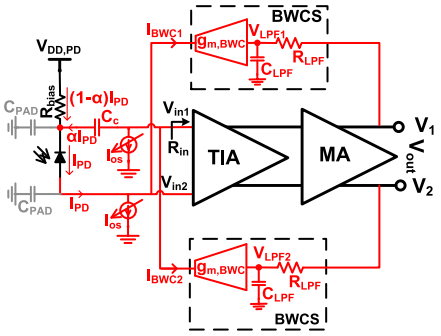



**FIGURE 2.** Block diagram of the proposed PD/TIA interface with BWCS.

where, $Z_0$, and $A_0$ are the midband gains of the TIA and the MA, respectively, and $\omega_{LPF} = 1/R_{LPF}C_{LPF}$ is the cutoff frequency of the LPF in the BWCS. The baseline wander is eliminated when the square brackets in (2) shrink to $(1+\alpha)$, leading to

$$g_{m,BWC} = \frac{\alpha}{(1+\alpha)\,Z_0A_0} \tag{3.a}$$

$$\omega_{LPF} = \omega_{ac} \tag{3.b}$$

More specifically, (3.a) and (3.b) express the *required conditions* for the proposed BWCS to function properly (see Appendix A for detailed proof).

In the proposed frontend, the current sources $I_{os}$ sink the average value of $I_{PD}$ to achieve a differential operation. $I_{os}$ is implemented by an offset compensation loop (OCL) that employs a Mega-Ω resistor and a Millar-boosted capacitance [7]. Therefore, the OCL can achieve a significantly smaller lower cut-off frequency $\omega_{ocl}$ compared with that associated with the AC coupling and hence maintaining a negligible baseline wander.

In addition to signal amplification, the MA is required in this work so that the condition in (3.a) is satisfied with a reasonable value of the transconductance $g_{m,BWC}$. The overall transfer function $Z_{FE}(s) = (V_1 - V_2)/I_{PD}$ of the proposed receiver is

$$Z_{FE}(s) = (1+\alpha)\,\frac{s}{(s+\omega_{ocl})}Z_{TIA}(s)\,A_{MA}(s) \tag{4}$$

The lower cutoff frequency is determined by the OCL rather than being determined by the AC coupling. The gain improves by a factor of $(1+\alpha)$ compared to the PS-Diff structure in Fig. 1 (a) while avoiding the baseline wonder associated with the AC coupling in Fig. 1 (c). The factor $(1+\alpha)$ reaches 2 as $\alpha$ approaches unity (*i.e.*, $R_{in} \ll R_{bias}$).

The MA is usually designed with a sufficiently wide bandwidth so that the TIA sets the overall bandwidth Considering a typical case where the TIA's input pole $\omega_{in}$ dominates its output pole, the 3dB bandwidth of the overall front-end in Fig. 2 is set by $\omega_{in}$

$$\omega_{3dB} = \omega_{in} = \frac{1}{R_{in}(2C_D + C_{PAD} + C_{in})} \tag{5}$$

**TABLE 1. Performance comparison with other PD/TIA interfaces.**

| | Single-ended (Reference Design) | Pseudo-differential | Ac-coupled differential | This work | |
|---|---|---|---|---|---|
| | | | | Asymmetrical differential W/O BWCS | Asymmetrical differential with BWCS |
| [1]Gain | $Z_0A_0$ | $Z_0A_0$ | $\mathbf{2}\boldsymbol{\alpha}Z_0A_0$ | $(\mathbf{1}+\boldsymbol{\alpha})Z_0A_0$ | |
| [2]BW | $\frac{1}{(C_D+C_{PAD}+C_{in})R_{in}}$ | $\frac{1}{(C_D+C_{PAD}+C_{in})R_{in}}$ | $\frac{1}{(\mathbf{2}\boldsymbol{C_D}+C_{PAD}+C_{in})R_{in}}$ | $\frac{1}{(\mathbf{2}\boldsymbol{C_D}+C_{PAD}+C_{in})R_{in}}$ | |
| [3]GBW change | 1 Reference design | 1 No change | $\mathbf{2}\boldsymbol{\alpha}\frac{(C_D+C_{PAD}+C_{in})}{(\mathbf{2}\boldsymbol{C_D}+C_{PAD}+C_{in})}$ $>\mathbf{1}$ | $\frac{(\mathbf{1}+\boldsymbol{\alpha})(C_D+C_{PAD}+C_{in})}{(\mathbf{2}\boldsymbol{C_D}+C_{PAD}+C_{in})}$ $>\mathbf{1}$ | |
| Integrated output Noise power | $V_n^2$ | $2V_n^2$ | $2V_n^2$ | $2V_n^2$ | |
| [4]SNR change | 0dB Reference design | −3dB | +3dB | +3dB | |
| $\mathbf{2}\boldsymbol{\pi f_L}$ | $\omega_{OCL}$ | $\omega_{OCL}$ | $\omega_{ac}$ | $\sim\omega_{ac}/2$ | $\omega_{OCL}$ |

[1] The factor $\alpha$ results from the leakage of the input current in the PD' bias resistor. Therefore, $\alpha$ approaches unity for $R_{in} \ll R_{bias}$.
[2] All differential structures double the PD capacitance seen from each input to ground
[3] The GBW of each structure is divided by that of the reference single-ended design
[4] $Output\ SNR = 10\log\frac{(i_{in}gain)^2}{output\ noise\ power}$

where, $C_D$, $C_{PAD}$, and $C_{in}$ are PD's capacitance, pad capacitance, and TIA's input capacitance, respectively. The bandwidth of the Ps-Diff receiver Fig. 1 (a) is given by the same expression as in (5) without the factor two in the denominator. Therefore, differential sensing reduces the bandwidth by a factor of $1 < BW_{\downarrow} = \frac{(2C_D+C_{in}+C_{PAD})}{(C_D+C_{in}+C_{PAD})} < 2$. A negligible bandwidth reduction (i.e., $BW_{\downarrow} = 1$) is obtained if $2C_D \ll (C_{in}+C_{PAD})$. Considering the gain improvement, a net improvement in the GBW is obtained as long as $BW_{\downarrow} < (1+\alpha)$.

The noise power spectral densities (PSDs) $V_{n,1}^2$ and $V_{n,2}^2$ at the frontend outputs are derived as

$$V_{n,1(or\ 2)}^2 = \left(I_{n,os}^2 + I_{n,BWC}^2 + \frac{V_{n,in1(2)}^2}{R_{in}^2} + \frac{g_{m,BWC}^2 V_{n,2(1)}^2}{\left|1+s/\omega_{LPF}\right|^2}\right) |Z_{TIA}(s)\, A_{MA}(s)|^2 \quad (6)$$

where $I_{n,os}^2$ and $I_{n,BWC}^2$ represent the thermal noise PSDs of the transistors used to realize $I_{os}$ and $g_{m,BWC}$, respectively, and $V_{n,in}^2/R_{in}^2$ includes the noise contribution from the TIA's core circuitry. The last term in (6) indicates that the proposed BWCS boosts the low-frequency noise. Since $\omega_{LPF} \ll \omega_{3dB}$, this boost can be ignored (this assumption is verified by simulation in Section IV-B). Therefore, the differential input-referred noise PSD $I_{n,in}^2 = \left(V_{n,1}^2 + V_{n,2}^2\right) / |Z_{FE}(s)|^2$ is calculated as

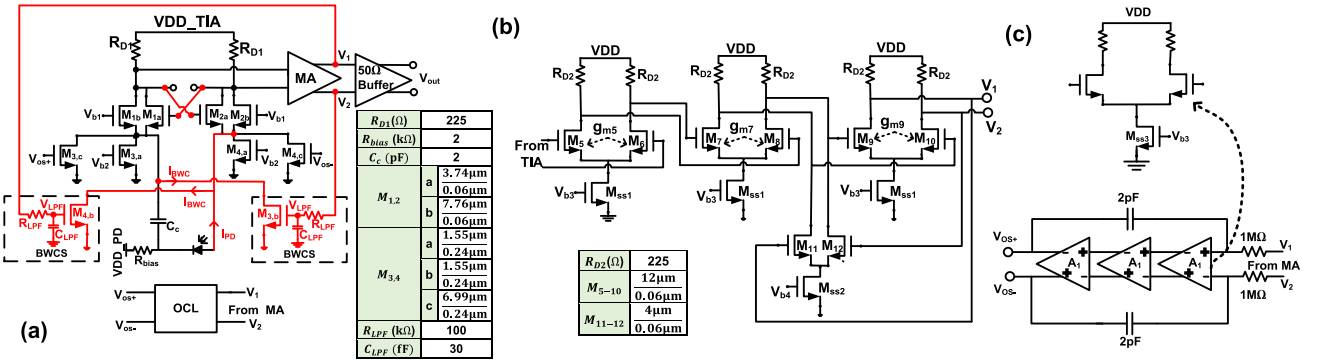
$$I_{n,in}^2 = \frac{2}{(1+\alpha)^2}\left|\frac{s+\omega_{ocl}}{s}\right|^2 \left(I_{n,os}^2 + I_{n,BWC}^2 + \frac{V_{n,in}^2}{R_{in}^2}\right) \quad (7)$$

The input-referred noise PSD of the proposed receiver is reduced by a factor of $(1+\alpha)^2$ compared to that of the Ps-Diff structure in Fig. 1 (a). As $\alpha$ approaches unity, this factor approaches four. This translates to a $10\log 4 = 6$dB enhancement in the SNR for the same input current.

Table 1 summarizes the performance of the proposed receiver in comparison to other well-known PD/TIA interfaces. Compared to the single-ended and the pseudo-differential receiver, differential current sensing improves the gain by $2\alpha$ and $(1+\alpha)$ in the AC-coupled receiver and the proposed receiver, respectively. The factor $\alpha$ results from the leakage of the input current in the PD bias resistor. Therefore, $\alpha$ approaches unity for $R_{in} \ll R_{bias}$, achieving a gain improvement of $2\times$. The bandwidth, on the other hand, is reduced by a factor of $1 < BW_{\downarrow} = \frac{(2C_D+C_{in}+C_{PAD})}{(C_D+C_{in}+C_{PAD})} < 2$. This factor shrinks to 1 (*i.e.,* no bandwidth reduction) for $2C_D \ll C_{in} + C_{PAD}$, making this technique more suitable for silicon photonic applications where the PD capacitance can be reduced to 30fF [8], [9]. Even with traditional technologies, net gain-bandwidth product improvement is achieved as long as $BW_{\downarrow} < (1+\alpha)$.

Differential interfaces also double the output noise power. Considering the gain improvement, the proposed receiver improves the output SNR by $10\log\frac{(1+\alpha)^2}{2}$, achieving a maximum improvement of 3dB and 6dB compared to the single-ended and pseudo-differential structures, respectively.

The AC-coupled differential receiver suffers from a high lower cutoff frequency $\omega_{ac}$ associated with the AC coupling. The elimination of the coupling capacitor at the PD anode terminal and before the incorporation of the proposed BWCS reduces the lower cutoff frequency to approximate $\omega_{ac}/2$. The incorporation of the proposed BWCS significantly reduces the lower cutoff frequency to be determined by the OCL as in the single-ended structure instead of being determined by the AC coupling. The OCL usually employs Mega-Ω resistors and Millar-boosted capacitances. Therefore, the OCL can achieve a significantly smaller lower cut-off frequency $\omega_{ocl}$ compared to that associated with AC coupling $\omega_{ac}$.




| | | |
|---|---|---|
| $R_{D1}(\Omega)$ | | 225 |
| $R_{bias}$ (kΩ) | | 2 |
| $C_c$ (pF) | | 2 |
| $M_{1,2}$ | a | 3.74µm / 0.06µm |
| | b | 7.76µm / 0.06µm |
| $M_{3,4}$ | a | 1.55µm / 0.24µm |
| | b | 1.55µm / 0.24µm |
| | c | 6.99µm / 0.24µm |
| $R_{LPF}$ (kΩ) | | 100 |
| $C_{LPF}$ (fF) | | 30 |

| | |
|---|---|
| $R_{D2}(\Omega)$ | 225 |
| $M_{5-10}$ | 12µm / 0.06µm |
| $M_{11-12}$ | 4µm / 0.06µm |

**FIGURE 3.** Circuit level implementations of the (a) TIA, (b) MA, and (c) OCL and transistor-level realization of the gain stage A1.

## III. CIRCUIT-LEVEL IMPLEMENTATION OF THE PROPOSED RECEIVER

In principle, the proposed sensing technique works with any TIA topology. However, with the common-gate (CG) TIA, the proposed technique has an additional advantage of improving the GBW without being limited by the voltage headroom ([1], Section IV-B). In the proposed TIA in Fig. 3 (a), the cathode and anode terminals of the PD are AC and DC coupled to two single-ended CG-TIAs, respectively. The low-frequency component of an amplified version of the TIA's output is extracted using the low-pass filter $C_{LPF}$ and $R_{LPF}$, creating $V_{LPF1,2}$. The tail transistor $M_3$ is split into three parts: $M_{3,a}$, $M_{3,b}$, and $M_{3,c}$ with gate terminals connected to a biasing voltage $V_{b2}$ to provide a fixed biasing current, $V_{LPF}$ to produce the current required for baseline wander compensation, and a voltage $V_{os}$ produced by the OCL for offset cancellation, respectively. The input transistors $M_1$ and $M_2$ are split into two pairs: a cross-coupled pair $M_{1,a}$, $M_{2,a}$ and another pair $M_{1,b}$, $M_{2,b}$ with the gate connected to a bias voltage $V_{b1}$. The input resistance of the TIA in Fig. 3 (a) is calculated from the small-signal model as

$$R_{in} = \frac{1 + (g_{ds1a} + g_{ds1b} - g_{m1a})\, R_{D1}}{g_{m1b} + g_{m1a} + g_{ds1a} + g_{ds1b}} \tag{8}$$

Therefore, an appropriately sized cross-coupled pair reduces the rate at which $R_{in}$ increases with $R_{D1}$ in the presence of the MOSFET short-channel effect [1]. The reduced $R_{in}$ improves the bandwidth at no power overhead since no auxiliary amplifier is employed as in the RGC-TIA [10].

Fig. 3 (b) shows the transistor-level realization of the MA. Active feedback ($M_{11}$ and $M_{12}$) is employed for wideband performance. The midband gain of the MA is calculated as [11]

$$A_0 = g_{m5} R_{D2} \frac{g_{m7} g_{m9} R_{D2} R_{D2}}{1 + g_{m9} g_{m11} R_{D2} R_{D2}} \tag{9}$$

where, $g_{mx}$ is the transconductance of transistor $M_x$.

The MA is usually designed with a bandwidth equal to the targeted data rate. Therefore, the TIA sets the receiver's overall bandwidth.

The OCL in Fig. 3 (c) senses the difference between the DC levels at the MA outputs and returns a feedback voltage $V_{os}$ which is then converted into current $I_{os}$ by the transconductance of $M_{3,c}$. The average value of the input current is removed by subtracting $I_{os}$ at the input node, as shown in Fig. 3 (a). The OCL employs a Miller-boosted 2pF capacitor and a 1MΩ polysilicon resistor. An $f_L < 0.15$MHz is achieved as a tradeoff between the on-chip area and a tolerable baseline wander.

The output buffer in Fig. 3 (a) is a simple differential pair with a load resistor of 75Ω, chosen as a trade-off between signal attenuation and matching with 50Ω measurement equipment.

## IV. PERFORMANCE VALIDATION AND COMPARISON

### A. DESIGN CONSIDERATIONS

The resistor $R_{LPF}$ in the BWCS in Fig. 3 (a) must be sufficiently large to prevent $C_{LPF}$ from loading the output of the MA. Once $R_{LPF}$ is set, $C_{LPF}$ is calculated as $C_{LPF} = C_c R_{bias}/R_{LPF}$ to satisfy the condition in (3.b). The transconductance in the BWCS given by (3.a) is implemented by $M_{3,b}$ and $M_{4,b}$ and is calculated in term of circuit parameters as

$$g_{m,BWC} = \frac{\alpha \left(1 + g_{m9} g_{m11} R_{D2} R_{D2}\right)}{(1+\alpha)\, g_{m5} g_{m7} g_{m9} R_{D1} R_{D2} R_{D2} R_{D2}} \tag{10}$$

Following (7), the input-referred noise PSD is calculated in terms of circuit parameters as

$$I_{n,in}^2 = \frac{2 \times 4kT}{(1+\alpha)^2} \left| \frac{s + \omega_{ocl}}{s} \right|^2 \left( \gamma\, g_{m,M3} + \frac{1}{R_{D1}} \right) \tag{11}$$

where $\gamma$ is the excess noise factor and $g_{m,M3} = g_{m,M3,a} + g_{m,M3,b} + g_{m,M3,c}$. The obtained noise performance is similar to that of the CG-TIA [1] but reduced by a factor $(1+\alpha)^2$. The noise of $R_{D1}$ and $M_{3a-c}$ directly refers to the input. Therefore, for a given bias current, $M_{3a-c}$ are realized by long-channel transistors (to reduce $\gamma$) and their overdrive voltages are maximized to improve the noise performance.

The TIA's input impedance calculated from the circuit parameters using (8) is approximately 60Ω. Therefore,

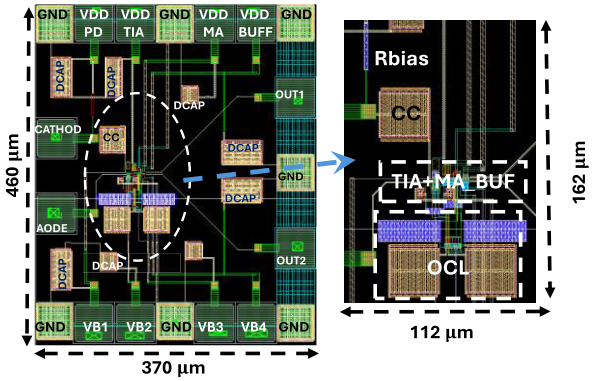



**FIGURE 4.** Layout of the proposed receiver.

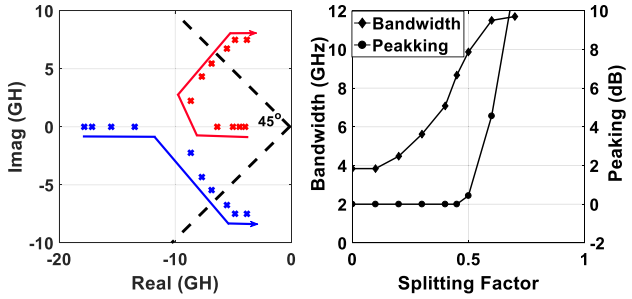



**FIGURE 5.** Impact of sizing the cross-coupled pair on (a) pole locations (b) bandwidth and peaking. The dash lines in Fig. 5 (a) make +45° and −45° with the horizontal axis. Therefore, the intersection of these lines with the root locus identifies the location of the Butterworth poles.

$R_{bias}$ needs to be much greater than this value to achieve $\alpha = 1$ and hence maximum performance improvement. The maximum value of $R_{bias}$, on the other hand, is limited by the PD biasing. The PD and the TIA are power by $V_{DD,PD}$ and $V_{DD,TIA}$, respectively (see the layout in Fig. 4). The latter is set by the CMOS technology node used in this work to 1V. Therefore, the anode terminal of the PD is DC-biased at approximately 0.3V (the required drain-to-source voltage of the tail current source). Therefore, a proper reverse bias of the PD can be maintained by setting $V_{DD,PD}$, for example, to 2.5V. Therefore, setting re $R_{bias}$ to 2kΩ is sufficiently low to avoid significant DC voltage drop and maintain a proper biasing for the PD up to an input current of $500\mu A_{pp}$ [3]. The selected value of $R_{bias}$ along with the simulated input impedance leads to a calculated $\alpha$ of 0.97.

### B. POST-LAYOUT SIMULATION RESULTS

Fig. 4 shows the layout of the proposed receiver in TSMC 65 nm CMOS technology. Post-layout simulations are performed with voltage supply and PD capacitance of 1 V and 200 fF, respectively. Pads contribute a 40 fF capacitance from each input node to the ground. Bonding wires are modeled by 0.5nH inductance. The TIA, the MA, and the OCL dissipate DC powers of 2.02mW, 6.04mW, and 3.05mW, respectively.

The effect of cross-coupling on the TIA's bandwidth is investigated in Fig. 5. A splitting factor is defined as

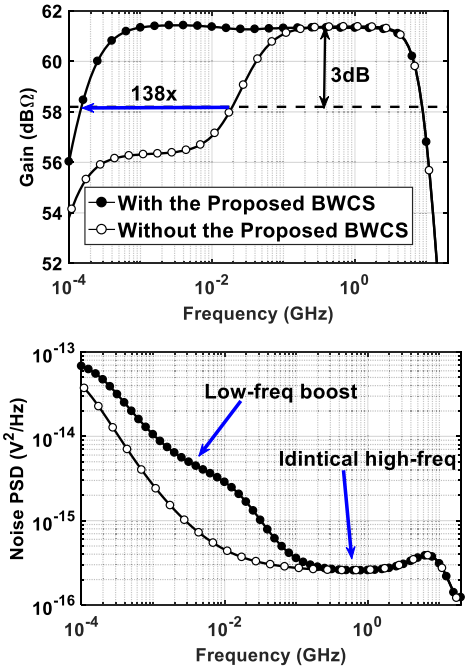



**FIGURE 6.** Post layout simulated (a) amplitude responses and (b) output noise PSD. Simulations are performed with and without the proposed BWCS under fixed power dissipation constraint.

$X_f = W_{M1a}/(W_{M1a} + W_{M1b})$. Fig. 5 (a) shows that at $X_f = 0$, the TIA acts as a conventional CG-TIA with two real distinct poles. As $X_f$ increases, the two poles move toward each other and become identical at $X_f = 0.28$. As $X_f$ continues to increase, the two poles become complex and may travel to the right-hand side at a very high $X_f$. A splitting factor of $X_f = 0.41$ is chosen for a Butterworth response. At this value of $X_f$, Fig. 5 (a) shows that the TIA achieves a bandwidth of 8.6 GHz, achieving a bandwidth extension of 2.4× compared with the case of $X_f = 0$. Fig. 5 (b) also shows that the proposed TIA exhibits a negligible peaking in the amplitude response up to $X_f = 0.5$, then the peaking starts to rapidly accumulates.

To investigate the impact of the proposed BWCS on the performance, the proposed receiver is simulated with and without the proposed BWCS. When the proposed BWCS is disabled, the gate terminals of $M_{3b}$ and $M_{4b}$ in Fig. 3 (a) are connected to a proper bias voltage to attain a constant power dissipation. The simulated amplitude responses in Fig. 6 (a) demonstrate that the incorporation of the proposed BWCS significantly reduces $f_L$ from 20.4MHz to 0.151MHz. The figure also shows that the proposed receiver achieves a gain and a bandwidth of 61.3dBΩ and 8.5GHz, respectively. Fig. 6 (b) shows that the proposed BWCS boosts the output noise PSD at frequencies less than 200MHz. The integrated output rms noise voltage $V_{n,rms}$ with and without the BWCS is 2.17mV and 2.15mV, respectively. This minor increases in $V_{n,rms}$ demonstrates that the BWCS has a negligible impact on the noise performance and justifies our analysis in (6).

**TABLE 2.** Performance comparison with CMOS TIAs.

| | [15][2] | [16][2] | [17][1] | [18][1] | [19][1] | This work1 | |
|---|---|---|---|---|---|---|---|
| **CMOS tech. (nm)** | 65 | 55LP | 65 | 180 | 180 | **65** | |
| **Topology** | RGC | RGC | CC-CG | RGC | SF | **CC-CG** | |
| **Output type** | Diff | Diff | Ps-Diff | SE | Diff | **Diff** | |
| **Input coupling** | AC | DC comp. | DC | DC | DC | **AC/DC+BWCS** | |
| **$f_L$ (MHz)** | 30 | 0.3 | 0.0074 | NA | NA | **0.15** | |
| **Inductor** | Yes | No | No | No | Yes | **No** | |
| **PD Cap. (fF)** | 200 | 200 | 200 | 250 | 200 | **200** | |
| **Supply (V)** | 3 | 2-2.7 | 1.2 | 1.8 | 3.3 | **1** | |
| **Architecture** | TIA+Balun | TIA+Balun | TIA+MA | TIA only | TIA+MA | **TIA** | **TIA+MA** |
| **Gain (dBΩ)** | 62 | 69 | 73.1 | 59.5 | 68.4 | **51.98** | **61.3** |
| **BW (GHz)** | 9 | 9 | 10.2 | 3.7 | 6 | **9.19** | **8.5** |
| **Noise ($\mu A_{rms}$)** | NA | NA | NA | NA | 0.56 | **1.87** | |
| **Eq. Input noise ($pA/\sqrt{Hz}$)** | 30 | 15 | 30.5 up to 10.2GHz | NA | 7.2 | **20.11 up to 16GHz** | |
| **DC Power[3] (mW)** | 10 | 15.7 | 9.6 | 3 | 83 | **2.02** | **11.11** |
| **Active Area $mm^2$** | 0.08 | 0.07 | 0.043 | 0.004 | NA | **0.0181** | |

NA: Not Available, SE: single-ended, SF: shunt-feedback CC: cross-coupled, and DC comp.: DC compensation
[1]Post-layout simulation [2]Electrically measured S-parameter combined with a PD model. [3]excluding the output buffer

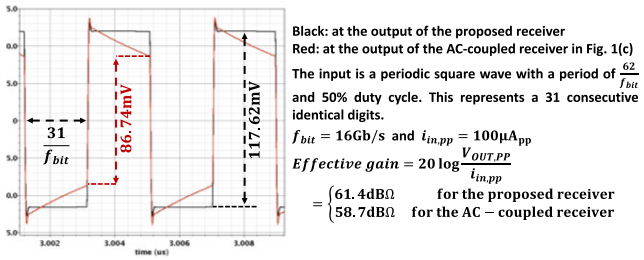



**FIGURE 7.** Post-layout simulated transient differential output voltage.

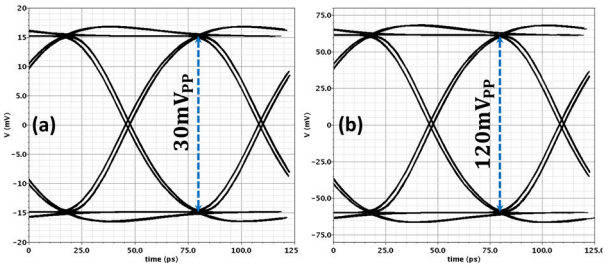



**FIGURE 8.** 16 Gb/s post-layout simulated eye diagrams at (a) at the sensitivity level ($i_{in}^{pp} = 26\mu A_{pp}$) and (b) at 4× the sensitivity level ($i_{in}^{pp} = 104\mu A_{pp}$).

The proposed PD/TIA interface is compared with other interfaces in Fig. 1. The comparison is performed under a fixed power constraint. The Ps-Diff structure in Fig. 1 (a) achieves a gain, bandwidth, and $V_{n,rms}$ of 56.33dBΩ, 12.42GHz, and 2.052mV, respectively. That is, the proposed interface improves the gain, the GBW, and the SNR by 5dB, 1.37× and 5.55dB, respectively, compared to the structure in Fig. 1 (a). The performance has significantly improved but did not reach the theoretical limit in Table 1. This is attributed to the top/bottom plate parasitic of capacitor $C_C$ that shunts the photocurrent which reduces the signal current flowing into the TIA and lowers the TIA gain at high frequencies.

The AC-coupled architecture in Fig. 1 (c) achieves an $f_L$ of 31.57MHz that is 209× higher than that of the proposed receiver. For accurate comparison with the AC-coupled receiver in Fig. 1 (c), the *effective* gain is calculated from the transient simulations in Fig. 7 [12], [13]. The proposed BWCS compensates for the signal drift after long runs of CIDs, improving the effective gain by 2.7 dB. The proposed receiver achieves an average input noise $i_{n,av}$ of 20.11pA/$\sqrt{\text{Hz}}$. Fig. 8 shows the post-layout simulated eye diagram at a data rate of 16 Gb/s various amplitudes, demonstrating the linearity of the proposed receiver at high input current amplitudes.

Fig. 9 shows the performance of the proposed receiver over process, voltage, and temperature (PVT) variations. The worst case higher cutoff frequency (6.12GHz) is sufficiently large to support the targeted 16Gb/s data rate [12], [13], [14]. The worst-case lower cutoff frequency (0.42MHz) is 71× lower than that associated with AC coupling at its typical operating conditions. The proposed receiver shows a negligible amplitude peaking over all PVT conditions.

Table 2 shows that the proposed receiver achieves differential operation with comparable power to [15] and [16] that employ active balun and DC current compensation. Unlike [15] and [16], the presented receiver operates at the technology's nominal supply voltage. More importantly, the proposed BWCS significantly reduces $f_L$ compared to the AC-coupled receiver in [15]. The proposed differential receiver achieves better noise than the Ps-Diff receiver in [17] which is implemented in the same technology

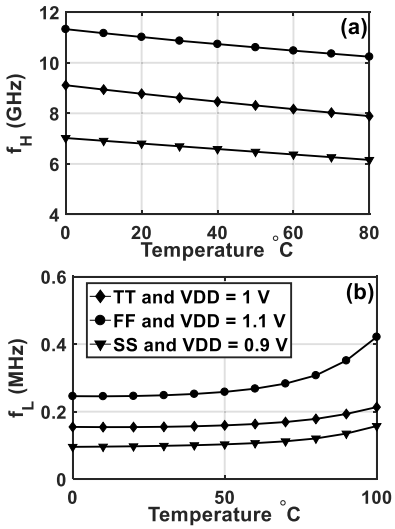



**FIGURE 9.** Performance over PVT variations (a) higher cutoff frequency and (b) lower cutoff frequency.

and employs a cross-coupled technique. Despite the differential connection that significantly increases the input capacitance, the proposed TIA alone achieves a higher GBW than the TIA in [18] that employs a modified RGC topology. The excellent noise performance of the differential receiver in [19] is achieved at the price of increased power dissipation resulting from stacking two single-ended receivers in the voltage domain while the proposed receiver achieves a good noise performance with a reasonable power dissipation.

## V. CONCLUSION

A differential PD/TIA interface with a baseline compensation scheme (BWCS) has been presented. To the best of the authors' knowledge, the BWCS is used in optical receivers for the first time in this work. The presented receiver leverages the gain and noise advantages of differential connection and improves the gain-bandwidth product while avoiding the limitations of AC coupling at no power or silicon area overhead. The presented receiver operates at the technology's nominal supply voltage and requires no special design considerations. Post-layout simulation results demonstrate the feasibility of the proposed BWCS. The proposed interface has the potential to double the gain and improve the SNR by 6dB compared to the pseudodifferential interface.

## APPENDIX A
## REQUIRED CONDITIONS FOR THE PROPOSED BWCS

This Appendix provides a detailed proof for the required conditions for the proposed BWCS to function properly. Starting from (1.a), the differential output is written as

$$V_1 - V_2 = -Z_{TIA}(s) A_{MA}(s) \left[ \frac{\alpha I_{PD} s}{(\omega_{ac} + s)} + \alpha g_{m,BWC} V_{LPF2} + I_{PD} - g_{m,BWC} V_{LPF1} \right] \quad (A.1)$$

Substituting $V_{LPF2} = \frac{Z_0 A_0 I_{PD}}{(1+s/\omega_{LPF})} = -V_{LPF1}$ results in

$$V_1 - V_2 = -Z_{TIA}(s) A_{MA}(s) I_{PD} \left[ 1 + \frac{\alpha s}{(\omega_{ac} + s)} + \frac{(1+\alpha) Z_0 A_0 g_{m,BWC}}{1 + s/\omega_{LPF}} \right] \quad (A.2)$$

To eliminate the baseline wander, the square brackets in (A.2) must equal $(1+\alpha)$. Therefore,

$$\left[ 1 + \frac{\alpha s}{(\omega_{ac} + s)} + \frac{(1+\alpha) Z_0 A_0 g_{m,BWC}}{1 + s/\omega_{LPF}} \right] = 1 + \alpha \quad (A.3)$$

Which can be reduced to

$$\frac{\alpha s^2}{\omega_{LPF}} + \left[ (1+\alpha) Z_0 A_0 g_{m,BWC} + \alpha \right] s + (1+\alpha) Z_0 A_0 g_{m,BWC} \omega_{ac} = \frac{\alpha s^2}{\omega_{LPF}} + \alpha \left( 1 + \frac{\omega_{ac}}{\omega_{LPF}} \right) s + \alpha \omega_{ac} \quad (A.4)$$

The $s^2$ terms cancel each other. Comparing the coefficients of $s^0$ directly leads to

$$g_{m,BWC} = \frac{\alpha}{(1+\alpha) Z_0 A_0} \quad (A.5)$$

The above equation represents the first condition in (3.a). Using this result to compare the coefficients of $s$ leads to

$$(1+\alpha) Z_0 A_0 g_{m,BWC} + \alpha = \alpha \left( 1 + \frac{\omega_{ac}}{\omega_{LPF}} \right)$$
$$\alpha + \alpha = \alpha \left( 1 + \frac{\omega_{ac}}{\omega_{LPF}} \right)$$

Leading to

$$\omega_{ac} = \omega_{LPF} \quad (A.6)$$

The above equation represents the second condition in (3.b).

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