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TOPICAL REVIEW

Receivers for Improving Signal Integrity and Data-Rate in Controller Area Networks

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ABSTRACT This paper presents additional circuits and characterization methodologies of novel CAN (Controller Area Networks) receivers that implement new features, aiming at improving CAN signal integrity and data-rate. The first receiver shown includes a circuit for ringing removal. The use of a Notch filter is meant to remove the ringing. The pulse-width symmetry is improved to a range just lower than −20 ns and +15 ns. As a result, during arbitration, the transmission data-rate can be increased up to 8 Mbit/s, a higher limit must be evaluated on a network system level. The second receiver shown is conceived for multi-bit communication. The possibility of parallelizing data transmission leads to an efficient use of the bandwidth available. A table compares the achieved results with the specifications of the latest available protocols. The chips of both receivers were designed and fabricated with a 0.18-μm BCD technology. After a block level description of the receivers, a Direct Power Injection (DPI) methodology is described. It is used to evaluate the receiver's immunity to conducted continuous-wave interference. Considerations regarding future technological directions for new applications are provided at the end of the paper.

INDEX TERMS CAN, IC, DPI, EMC, immunity, receiver, comparator, simulation, automotive.

I. INTRODUCTION

Several apparatuses contain a large number of components that communicate to each other exchanging data. A vehicle is an example, as it is made up of ECUs (electrical control units) that control different vehicle functions, such as sensors communication, gearbox controllers and engine controllers. The communication can occur through wires or it can be wireless. In the case of CAN a twisted pair of wires is used, as the signal is differential. Wired communication is employed in many applications.

Recent developments are focused on improving bus and network systems based on Ethernet [1], in what respect a focus is on systems with high throughput, which is strictly required for autonomous driving assistance systems.

However, there are some use cases, such as power train and chassis subsystems, it connects for example engine and brake control, or body electronics such as door and climate control [2], [3]. These applications require robust, simple and low-cost technologies like CAN.

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Support from academia for evaluating bottlenecks and areas of improvement of the network was provided [4].

As a result, efforts for improving the signal integrity and data-rate are necessary. Increasing the data-rate in CAN is challenging because bus topologies might include stubs and nodes that are not properly terminated. These networks that are not properly homogeneous suffer from signal reflections due to impedance mismatches [5], [6].

The recent development and release of CAN XL [7] is the proof that there is demand for further improvements of this technology. In order to accommodate this demand, a study was carried out regarding novel receivers that can implement improved functions.

The first receiver proposed, that is described in section II, implements an active circuit to remove the ringing affecting the CAN signal [8]. The second receiver proposed, that is described in section III, includes four more comparators to enable flash A-D conversion for multi-bit communication [9]. Section IV provides a description of an EMC characterization flow of the receivers. Section V shows the simulation and measurements results obtained from both the receivers. Finally, section VI concludes the paper.

II. RECEIVER WITH RINGING CANCELLATION

The following receiver, implements a circuit in front of the comparator based on a second-order Twin-T Notch filter, shown in Fig. 1, and performs an equalization for ringing cancellation.

The block behavior has already been described in the previous work extensively.

The other receiver's building blocks are the comparators, the glitch filters, the resistive divider and the bus bias. Because the building blocks topology is the same for the multi-bit receiver, they will be presented in the following chapter.

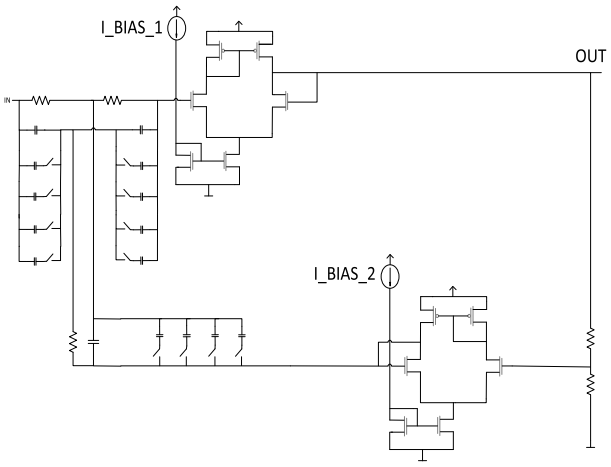

FIGURE 1. Ringing cancellation circuit.

The chip, fig. 2, was fabricated with a 0.18-μm technology.

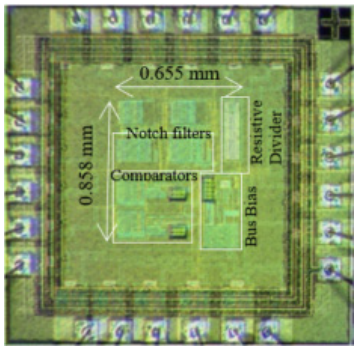

FIGURE 2. Die photo. Area without including pad-ring: 0.566 mm^2.

III. RECEIVER FOR MULTI-BIT COMMUNICATION

The following receiver allows multi-bit communication. Because of stringent latency requirements [10], implementing a sigma-delta ADC is not practical.

In addition, power consumption is not a critical constraint in CAN receiver design, due to the presence of a dedicated sleep mode, and area is also not particularly critical. Moreover, EMC issues must be taken into account [11]. As a result, a flash ADC was preferred to a SAR ADC for receiving multi-bit data, the idea is to keep one channel for the arbitration phase (Sic mode: data-rate up to 8 Mbit/s) and enable the other channels only during data transmission (Fast mode: data-rate up to 20 Mbit/s). The receiver is shown in Fig. 3.

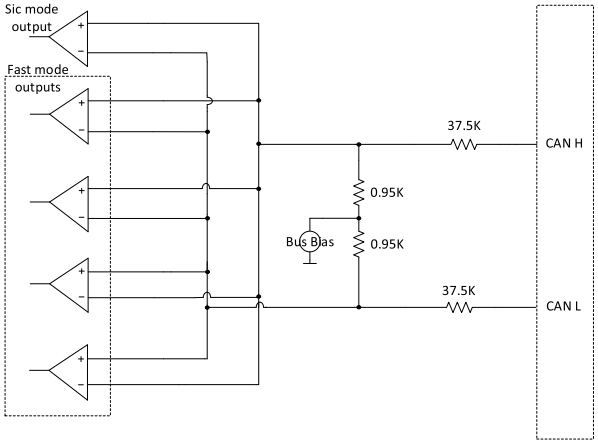

FIGURE 3. Schematic diagram of the proposed multi-bit receiver.

The total number of comparators is five: one always dedicated to arbitration (Sic mode), the other four to data transmission (Fast mode). A glitch filter is placed at the output of each comparator to avoid undesired transitions due to noise and emissions. The same topology was used for all the comparators in order to provide the same features to all the channels.

The comparator and the bus bias topologies are described respectively.

A. COMPARATOR

Speed and accuracy were the drivers for the design of the comparator. It is shown in Fig. 4. Multiple stages topology was preferred to other kinds of solutions.

There's a first gm*R gain stage where the threshold is implemented, then a source follower stage for making the signal compliant with the pmos input pair of the third stage that convert the signal from differential to single-ended is performed.

A buffer made up of two inverters is the last stage of the comparator.

Due to the shared input node among all the comparators, as depicted in Fig. 2b, using npn bipolar transistors as the input stage becomes impractical. This is because the base currents would interact with each other, resulting in highly inaccurate threshold voltages under specific process, voltage, and temperature conditions.

As a result, the npn input stage is replaced with an nMOS input stage. To establish the appropriate threshold voltage, a deliberate systematic offset is introduced by mismatching the transistors within the differential pair. Additionally, a resistor is inserted between the sources of the transistors in the input pair.

The current flowing through this resistor represents the disparity between the currents in the two input branches. The magnitude of the offset increases with the magnitude of the current passing through the resistor.

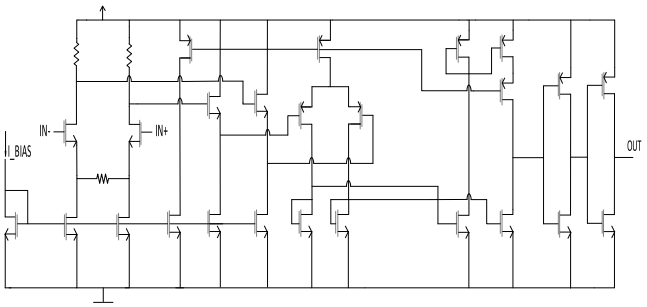

FIGURE 4. Comparator.

B. BUS BIAS

The bus bias block, illustrated in Fig. 5, serves the purpose of establishing the common-mode voltage level at 2.5 V. This voltage is generated by a bandgap reference and then supplied to an operational amplifier, operating in a closed-loop configuration.

The operational amplifier is equipped with a push-pull output stage. Additionally, a capacitor placed in the feedback path is utilized for compensation. The push-pull output stage drives a resistive load, which is essential for setting the common mode voltage in the divider.

The decision to opt for a push-pull output stage was motivated by two factors. Firstly, it was chosen to meet the high-linearity requirements at the output. Secondly, it allows the circuit to both source and sink current from the load. This capability is vital since the common mode level of the CAN bus has the potential to shift between $+12$ and -12 V.

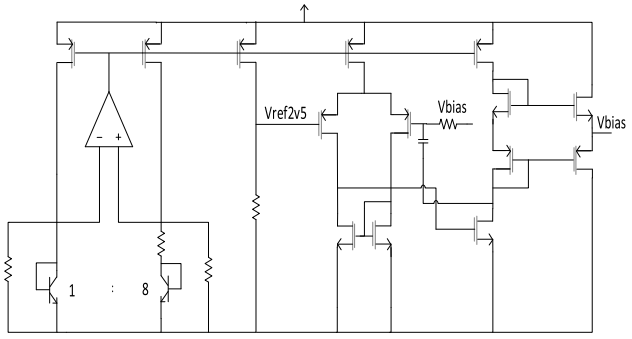

FIGURE 5. Bus bias.

The OTA used in the bandgap that generates the reference voltage is the following one shown in Fig. 6.

It's a two stages OTA with pmos input pair and Miller compensation.

The bias current is generated through the divider directly connected to the supply.

The chip of this multi-bit receiver, Fig. 7, was fabricated with a 0.18-μm BCD technology.

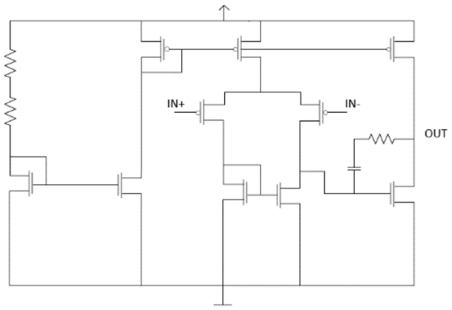

FIGURE 6. Two stages OTA.

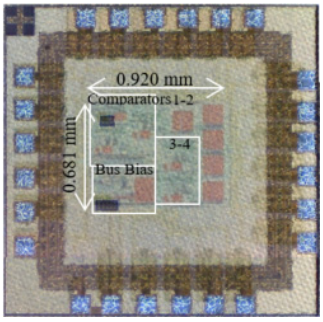

FIGURE 7. Die photo. Area without including pad-ring: 0.625 mm^2.

The results and further discussion related to this OTA are provided in chapter 5.

The following chapter provides a description of an EMC characterization flow of the receivers.

IV. DPI SIMULATION FOR EMC CHARACTERIZATION

In order to translate coupling and noise sources in a harsh environment like the automotive one, to something that can be used by the IC designer to design a robust receiver, the Direct Power Injection (DPI) test has become the standard for the robustness evaluation of a CAN receiver [12]. Common mode chokes are used in some systems to minimize the radiated emissions; therefore, they can have an impact on the test results. However, in this study, these effects are not considered. For a proper evaluation of the receiver immunity, knowing the exact power injected into the circuit is required.

The test accuracy increases by modeling each part of the setup such as the injection probe, the injection capacitor, the PCB, the directional coupler and the IC itself [13]. As a results different results can be obtained depending on the instrumentation and PCB used.

However, the purpose of this chapter is to describe the methodology used that can be then reproduced in every specific setup.

For this reason, only the models of the injection probe and decoupling capacitors are used.

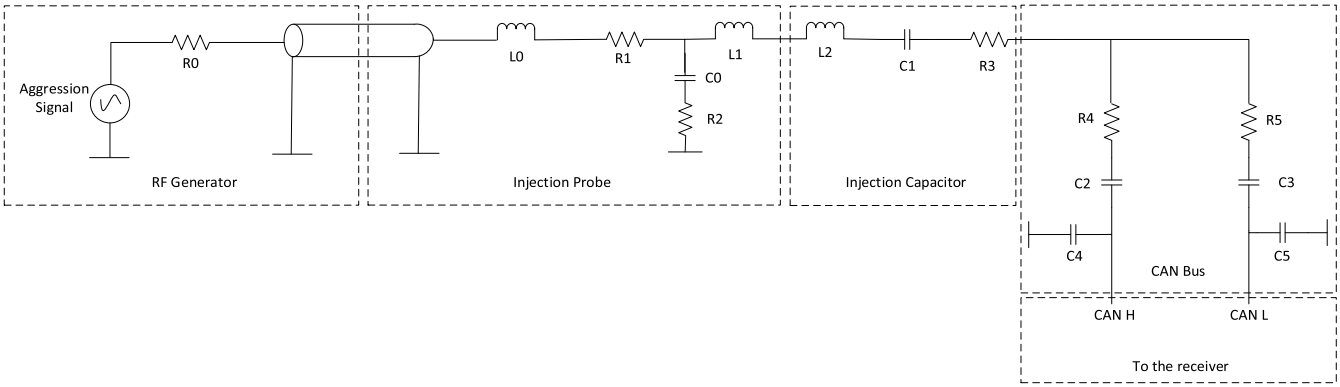

FIGURE 8. DPI Setup electrical model.

A. INJECTION PROBE

The DPI test injection probe is a coaxial cable with a core made up of copper. The injection probe model is inductive with a series resistance. The receiver is probed through the decoupling capacitor and the outer connector of the injection probe is soldered on the ground plane of the PCB.

As a result, the inner wire of the probe is connected to the ground plane via a capacitance and a resistance, which symbolize the dielectric properties of the coaxial cable. The model includes also the equivalent inductance of the small wire connecting the core of the cable with the receiver input. The electrical model of the injection probe is shown in Fig. 8.

Table 1 reports the values of its equivalent elements.

B. INJECTION AND DECOUPLING CAPACITORS

The DPI setup comprises two separate capacitors: a 1 nF injection capacitor, utilized to avoid the reinjection of the DC voltage from the board into the RF power amplifier, and a 47 nF decoupling capacitor situated on the PCB. The equivalent inductance can be computed from Eq. 1:

$$L = \frac{1}{4\pi^2 f_{res}^2 C} \tag{1}$$

The resonant frequency of the capacitor, represented by f_{res}, can be determined using the same procedure. This process can be repeated for the decoupling capacitor as well. The corresponding equivalent elements for both capacitors are listed in Table 1. The equivalent model and its parameters value are taken from [13].

The electrical model of the injection and decoupling capacitor is shown in Fig. 8, together with the injection probe and CAN bus models.

The DPI test is reported in the following chapter together with the two ICs test for verifying the ringing cancellation and the multi-bit communication.

The following table reports the values of the elements of the DPI setup electrical model.

V. RESULTS

A. ELECTROMAGNETIC IMMUNITY SIMULATIONS

The RF power amplifier injects a common-mode AC signal to the CAN bus receiver inputs during transmission and the Rx output is monitored for any jitter or glitches based on the Rx mask [12].

TABLE 1. DPI electrical model elements.

Elements	Value
R0	50 Ω
L0	2.05 nH
R1	1.06 Ω
C0	0.85 pF
R2	300 Ω
L1	3.4 nH
L2	0.8 nH
C1	1 nH
R3	0.12 Ω
R4	120 Ω
R5	120 Ω
C2	4.7 nF
C3	4.7 nF
C4	250 pF
C5	250 pF

Pulse-width distortion is carefully evaluated. These simulations were performed during arbitration phase for both the receivers developed, the one with the Notch for the ringing suppression and the other for the Multi-bit communication.

The RF signal frequency ranges from 1 MHz to 300 MHz and the amplitude ranges from +/− 28 Vpeak for a 50 Ω termination to +/− 56 Vpeak for a high impedance load.

Fig. 9. shows the aggression signal, with an amplitude of +/− 56 Vpeak and a frequency of 10 MHz, superimposed over the CAN signal and the Rx output. Fig. 10 shows the aggression signal, with an amplitude of +/− 56 Vpeak and a frequency of 50 MHz, superimposed over the CAN signal and the Rx output. Fig. 11 shows the aggression signal, with an amplitude of +/− 56 Vpeak and a frequency of 300 MHz, superimposed over the CAN signal and the Rx output.

The CAN signal pulse width distortion between input and output of the receiver was kept within the symmetry requirements given by the latest CAN versions.

B. RINGING CANCELLATION

The manufactured sample of Fig. 2 was characterized and verified in nominal conditions at room temperature. The

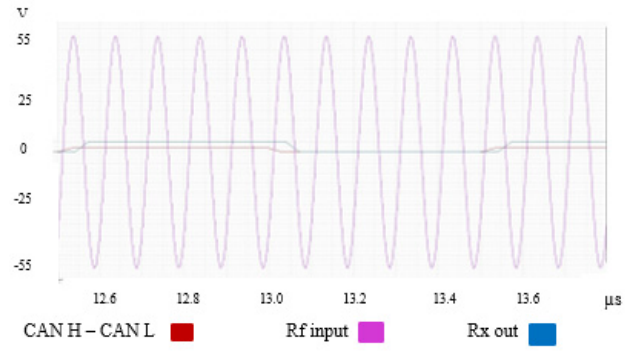

FIGURE 9. RF input at +/− 56 Vpeak and 10 MHz vs CAN H – CAN L and Rx out.

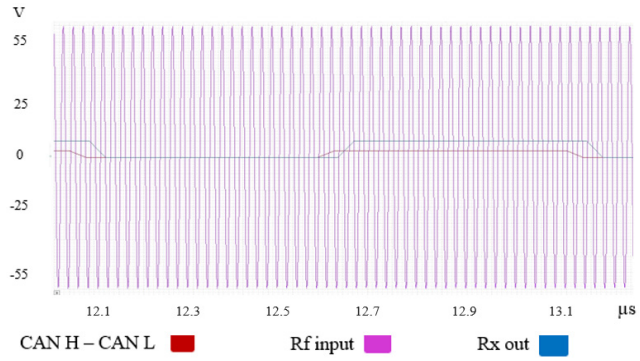

FIGURE 10. RF input at +/− 56 Vpeak and 50 MHz vs CAN H – CAN L and Rx out.

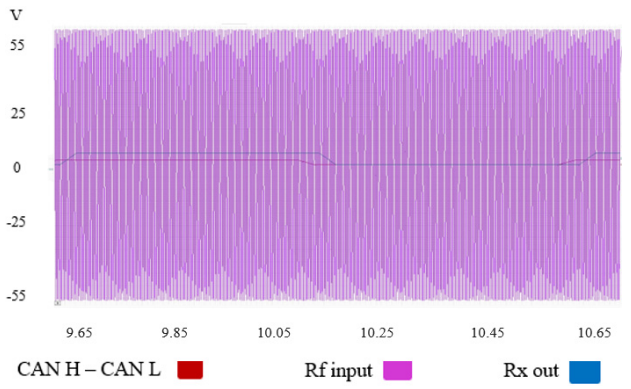

FIGURE 11. RF input at +/− 56 Vpeak and 300 MHz vs CAN H – CAN L and Rx out.

CAN signal was generated using a square wave generator connected to an LC network for ringing emulation.

The signals were read with an oscilloscope.

In Fig. 12 the top waveform represents the input signal of the equalizer, evident with the presence of ringing.

The second waveform illustrates the equalizer output, which still retains some ringing due to the notch frequency being positioned 20 MHz away from the ringing frequency.

The third waveform demonstrates the equalizer output when the notch frequency is set at a frequency offset of 1 MHz from the ringing frequency. In this scenario, the ringing is nearly entirely eliminated.

The measurement outcomes demonstrate that the implementation of the Notch is effective in considerably diminishing the ringing in the CAN signals, while still allowing the receiver to achieve a bit width symmetry within ±25 ns and maintain a propagation delay below 120 ns.

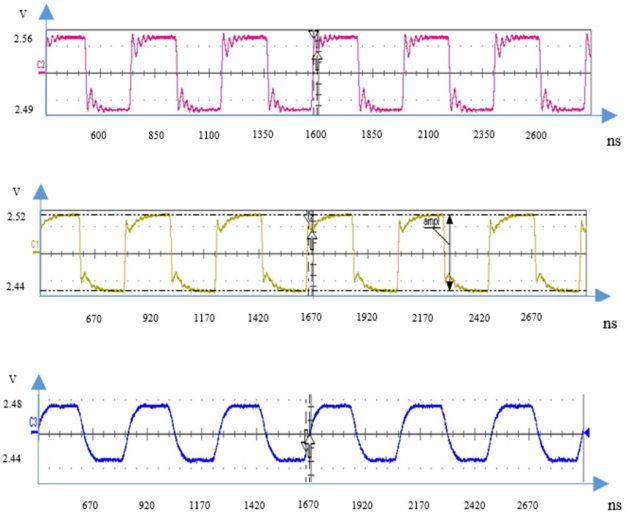

FIGURE 12. Notch input and output signals waveforms.

C. MULTI-BIT COMMUNICATION

The manufactured sample of Fig. 7 was characterized and verified in nominal conditions at room temperature.

The signals were read with an oscilloscope and the waveforms are shown in Fig. 13 and 14.

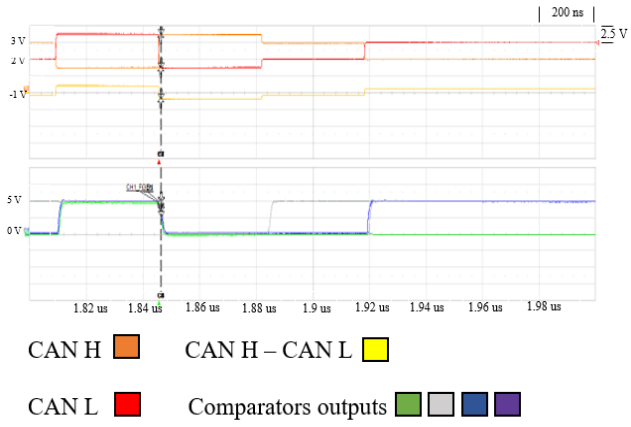

FIGURE 13. CAN high, CAN low, CAN differential signal, and Fast mode output signal waveforms.

The CAN low signal is depicted by the orange waveform, while the CAN high signal is represented by the yellow waveform. The purple waveform signifies the disparity between the CAN high and CAN low signals. Additionally, the

TABLE 2. Performance summary.

	Multi-bit receiver version Fig.2a PVT and Montecarlo 4 sigma simulations only	Multi-bit receiver version Fig.2b Measured results	CAN FD/SiC/XL [4][6]
Thresholds accuracy	Fast mode 500 mV with tolerance +/-100mV -500 mV with tolerance +/-100mV 1.3 V with tolerance +/-100mV -1.3 V with tolerance +/-100mV	Fast mode 500 mV with tolerance +/-150mV -500 mV with tolerance +/-150mV 1.3 V with tolerance -200 mV and +150 mV -1.3 V with tolerance -200 mV and +150 mV	XL 0V with tolerance +/-100mV
Input voltage range	+/- 12 V	+/- 12 V	+/- 12 V
Data-rate	Up to 8 Mbit/s in Sic mode Up to 20 Msym/s in Fast mode	Up to 8 Mbit/s in Sic mode From simulations up to 20 Msym/s in Fast mode From measurements up to 10 Msym/s in Fast mode	FD-SiC up to 5-8Mbit/s XL up to 10 Mbit/s and beyond
Pulse-width symmetry	+/- 10 ns in Fast mode	-23 ns and +29 ns in Fast mode	SiC – 20 ns and +15 ns
Propagation delay	110 ns	102 ns	XL 110 ns

remaining waveforms illustrate the pulses generated by the four comparators specifically designed for the Fast mode.

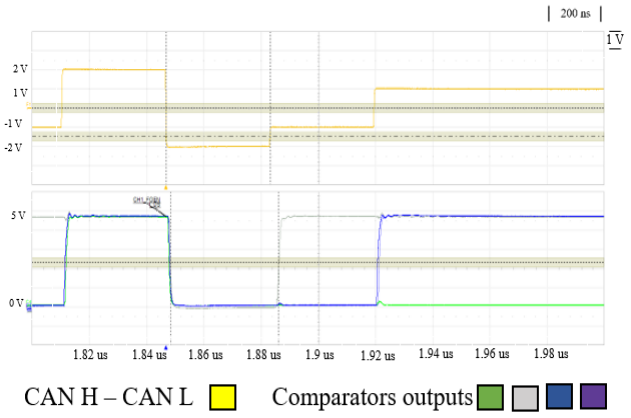

FIGURE 14. CAN differential signal and Fast mode output signal waveforms.

The multi-bit communication through the CAN differential signal employs four distinct voltage levels: ± 2 V or ± 1 V. Each comparator triggers when its respective threshold voltage is crossed. A unique configuration is generated for each CAN differential signal state, which can then be encoded into a binary representation of the multi-bit word using an encoder.

As illustrated in Fig. 13 and Fig. 14, when the differential signal reaches $+2$ V or -2 V, all outputs are either high or low, respectively. Conversely, when the differential signal is $+1$ V, one output is low and the others are high, and this pattern is reversed when the signal is -1 V.

It's imperative that each output state satisfies the timing requirements for pulse width symmetry and propagation delay on both rising and falling edges.

Table 2 summarizes the performances of the proposed multi-bit receivers and compares them to the expected parameter values of the latest CAN version.

VI. CONCLUSION

The paper showed circuits, simulations and test results related to CAN receivers that implement new features for improving CAN signal integrity and data-rate. The direct power injection method (DPI) for the EMC characterization was described. The use of a Notch filter is meant to remove the ringing. The pulse-width symmetry is improved to a range just lower than -20 ns and $+15$ ns. As a result, during arbitration, the transmission data-rate can be increased up to 8 Mbit/s. The second receiver shown is suitable for multi-bit communication. The possibility of parallelizing data transmission leads to an efficient use of the bandwidth available. More advanced CAN transceivers with increased data-rates and improved EMC performance are expected to be released in the coming years on the market. CAN, due to the characteristics of being simple and low cost, fully decentralized and extremely robust, will play a relevant role in the ongoing transition to fourth and fifth generations of E/E architectures [14] and Ethernet tunneling through CAN receivers [15].

As an example, upcoming fourth-generation systems will incorporate centralized domain controllers, while

fifth-generation systems will utilize a blend of cross-domain vehicle computers and zone controllers. Cross-domain vehicle computers will centralize functions that are currently distributed across various electronic control units (ECUs) in today's third-generation systems. Zone controllers, on the other hand, will primarily serve as gateways and consolidate input and output functions for specific areas within the vehicle. Although third-generation systems are anticipated to be the prevalent choice in the market for the next few years, fourth-generation systems are poised to swiftly become the standard option for premium OEMs.

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