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SURVEY

Oversampling ADC: A Review of Recent Design Trends

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ABSTRACT Oversampling analog-to-digital converters (ADC) serve as the backbone of high-performance, high-precision data interfaces, owing to their remarkable ability to filter out quantization noise. This attribute makes them the preferred choice for applications requiring high signal-to-noise ratio (SNR) and moderate bandwidth, with great design flexibility. This paper provides an extensive survey of the latest advancements in oversampling ADC tailored for such applications as documented in recent literature. Specifically focusing on design techniques employed within the last five years, the survey encompasses various oversampling ADC architectures, including discrete-time and continuous-time $\Delta\Sigma$, noise-shaping SAR, zoom, incremental, and time-domain modulators. A thorough performance comparison between these different topologies is presented, highlighting designs that achieve the best figures-of-merit. Furthermore, the paper explores circuit-level design trends commonly shared among these architectures, with particular attention given to amplifier designs for loop filters. Conclusions drawn highlight the limitations of much of the research works in the context of implementing ADC within complete systems, while also providing insight into the expected future trends that will shape the field moving forward.

INDEX TERMS Analog-to-digital converter (ADC), data converter, delta-sigma modulator, incremental ADC, noise-shaping, oversampling, successive-approximation ADC (SAR), system on a chip, time-domain ADC, zoom ADC.

I. INTRODUCTION

The relentless advance of semiconductor technology has brought in an era of increasingly efficient digital signal processing as CMOS technology nodes continue to shrink. This progression has led to remarkable improvements in computational power, speed, and energy efficiency, making signal processing in the digital domain the preferred approach in modern electronic systems. Nevertheless, the physical world operates in the analog domain, necessitating cutting-edge analog interfaces to fully leverage the benefits of digital signal processing. Consequently, analog-to-digital converters (ADC) can quickly become bottlenecks in the signal chain if they are not specified and designed with great care.

To meet the demands of modern electronic systems, research on improving ADC circuits in terms of resolution, power efficiency, noise reduction, speed, accuracy, and miniaturization is relentless. Among all the proposed solutions and topologies, the delta-sigma ($\Delta\Sigma$) configuration is of particular interest. By cleverly combining feedback error correction and oversampling to push quantization noise outside of the signal band, the $\Delta\Sigma$ architecture allows for very high precision using electronic blocks with looser specifications than with alternate ADC topologies.

Although the original concepts of $\Delta\Sigma$ modulation date back to the early 1960s [1], [2], [3], $\Delta\Sigma$ converters (and oversampling ADC in general) remain a primary research focus

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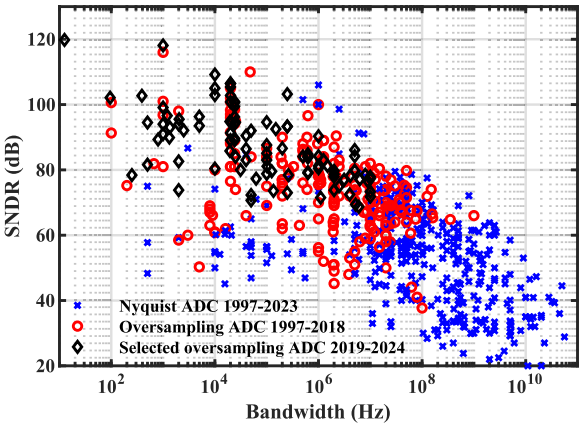

FIGURE 1. Scatter plot illustrating the relationship between SNDR and bandwidth for the selected oversampling ADC and those from Murmann's database.

for high signal-to-noise-and-distortion ratio (SNDR) applications. The prevalence of oversampling converters among designs with a SNDR above 80 dB, as illustrated in Fig. 1, underscores their critical role in achieving high precision and high performance in ADC design, especially in recent years. The ADC data points are sourced from Murmann's database [4] which comprises data from the International Solid-State Circuits Conference (ISSCC) and the IEEE VLSI Technology Symposium from 1997 to 2023. The black diamond datapoints on the figure represent the ADC designs studied in this review paper, all of them oversampling topologies gathered from various IEEE journals and conferences published in the past 5 years.

With such a clear trend, it should be no surprise that oversampling ADC stand out as the go-to in high-precision, low-bandwidth applications. For instance, high-performance $\Delta\Sigma$ ADC are often used in wireless sensor nodes, precision industrial and research process instrumentation or high-fidelity audio processing. However, such applications demand not only high SNDR, but also low power consumption (given that many of these systems are battery-powered) and cost effectiveness (to facilitate widespread adoption). Satisfying these requirements imposes strict design constraints, which have been the focus of numerous research endeavors. Hence, this review paper aims to explore recent trends in oversampling ADC where research emphasis lies not on maximizing bandwidth, but rather on enhancing SNDR at minimal cost and power overhead.

The paper is structured as follows. Firstly, section II presents the methodology. Section III then provides a concise review of $\Delta\Sigma$ modulation and an introduction to the different oversampling ADC topologies. Next, section IV offers an overview of the current state of the art, including a comparison of key figures-of-merit (FOM) and performance metrics. Subsequently, sections V and VI explore in depth system-level and circuit-level design trends, respectively. Section VII discusses system-on-chip (SoC) implementation and ADC benchmarking, shedding light on FOM limitations. Finally, section VIII summarizes the main findings and presents future perspectives.

II. METHODOLOGY

To ascertain the prevailing trends in oversampling ADC design tailored for high-precision applications, an exhaustive review was conducted throughout prominent IEEE journals and conferences spanning the past five years. Only oversampling ADC designs deemed suitable for high-precision and moderate bandwidth applications were considered, discarding those with an effective number of bits (ENOB) below 11 bits and those with a bandwidth in excess of 10 MHz. Numerous applications require ADC performance within these specifications [5], [6], [7], [8], [9]. For instance, sensor data acquisition in Internet of things (IoT), sensor nodes and industrial process instrumentation demands high precision, often well over 11 bits. Depending on the nature of the signals involved, bandwidth can vary from a few hertz for temperature or humidity detection to megahertz for ultrasound imaging. Signal processing in audio and biomedical monitoring applications is also notable for requiring high accuracy, but moderate bandwidth. Furthermore, low-bandwidth, low-power communication protocols benefit from such specifications with highly efficient oversampling ADC.

The lower cutoff ENOB limit of 11 bits is selected since simpler Nyquist ADC are able to achieve ENOB up to 10 to 12 bits with standard manufacturing process matching. Beyond this precision level, calibration or other special design techniques are required to improve accuracy, enhancing the attractiveness of the oversampling ADC alternative. This survey focuses on energy efficiency enhancement and implementation cost reduction, rather than bandwidth boosting, which is not a critical factor for the target applications considered.

The scrutinized publications include the Journal of Solid-State Circuits (JSSC), IEEE Transactions on Circuits and Systems I & II (TCAS I & II), IEEE Transactions on VLSI Systems, Solid-State Circuit Letters, as well as the International Solid-State Circuits Conference (ISSCC) and Custom Integrated Circuits Conference (CICC). Additionally, five papers sourced from Murmann's database [4] were considered, despite dating from more than five years, since their performance still rivals even the latest state-of-the-art designs. Each selected paper presents a physical tape-out implementation and corresponding measurement results.

The analysis and discussion in this survey revolve around the design techniques used in the selected works, which are grouped by topology, with the main innovations and design trends identified. All techniques discussed have been used in some of the selected state-of-the-art designs.

III. OVERVIEW OF OVERSAMPLING ADC STRATEGIES

This section will cover the basics of oversampling ADC. The principle of operation of this ADC category will be demonstrated using the quintessential oversampling topology, the

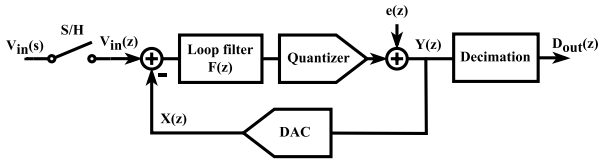

FIGURE 2. Block diagram of the DT ΔΣ ADC.

discrete-time (DT) ΔΣ ADC. Following this, we will introduce and discuss the various other oversampling ADC topologies featured in this review.

The principle of operation of oversampling ADC is to convert numerous successive low bit-count samples into a single high-resolution output, thus earning its designation as an *oversampling* ADC. By incorporating the quantizer component within an error-correcting feedback loop, precision can be significantly enhanced.

For readers new to this field, some excellent textbooks offer more in-depth insight into the inner workings of this ADC family [5], [10].

A. THE DISCRETE-TIME ΔΣ MODULATOR

Fig. 2 depicts the block schematic of the DT version of the ΔΣ ADC. The conversion process begins with the sample-and-hold (S/H) stage, which discretizes the analog input signal in time. Subsequently, the signal undergoes low-pass filtering through the loop filter F(z). This circuit block serves as the error correction element in the feedback loop and is commonly implemented using a switched-capacitor integrator circuit. Following this, the signal enters a quantizer, typically a flash ADC [11] with a low bit-count (1 to 4 bits). The feedback path features a digital-to-analog converter (DAC) allowing for the subtraction of the digital output of the quantizer Y(z) from the analog input $V_{in}(z)$. This DAC is one of the most critical blocs in the architecture as any error or distortion it introduces are not shaped by the error-correcting loop due to its placement in the feedback path. The high-frequency digitized data stream Y(z) is finally converted into a lower frequency, high bit-count output data $D_{out}(z)$ by means of a decimation filter. The ratio of decimation, equal to the sampling frequency ratio between Y(z) and $D_{out}(z)$, is known as the oversampling ratio (OSR). All things being equal, increasing OSR enhances ADC precision. However, this represents a key trade-off in ΔΣ ADC design, as higher OSR improves SNDR but reduces bandwidth for the same power consumption.

The low bit-count quantizer, due to its coarse voltage steps, introduces substantial errors termed quantization noise and denoted e(z) in Fig. 2. Classic feedback theory can be applied to derive ADC transfer functions for both input $V_{in}(z)$ and quantization noise e(z), designated respectively as signal transfer function

$$STF(z) = \frac{Y(z)}{V_{in}(z)} = \frac{F(z)}{1+F(z)} = z^{-1} \tag{1}$$

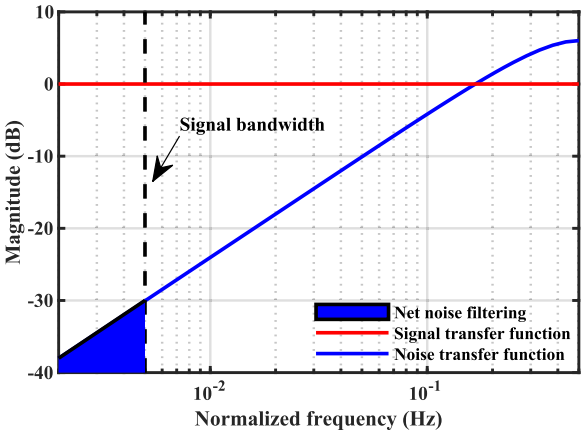

FIGURE 3. Signal and noise transfer function of a typical ΔΣ ADC. The shaded region shows the total shaping of the quantization noise from both the loop filter and the decimation filter.

and noise transfer function

$$NTF(z) = \frac{Y(z)}{e(z)} = \frac{1}{1+F(z)} = 1 - z^{-1}, \tag{2}$$

where

$$F(z) = \frac{z^{-1}}{1-z^{-1}} \tag{3}$$

is the transfer function of an ideal integrator loop filter.

With these equations plotted in Fig. 3, it becomes clear that the error signal undergoes strong filtration, while the input signal is unaffected. As highlighted with the blue shading, the remaining noise in the signal band is significantly attenuated by high-pass filtering through the feedback loop, an effect commonly referred to as noise shaping. Indeed, at the ADC output, the decimation filter acts as a sharp low-pass filter, effectively removing residual noise above the signal band. To achieve sharper noise shaping, a higher-order loop filter may be used, which can be performed simply by cascading additional switched-capacitor integrators. Higher-order noise shaping may reduce the OSR required to meet specific SNDR requirements, albeit at the cost of critical stability challenges.

Fig. 4 illustrates the transient waveforms of a 1st-order DT ΔΣ ADC. Both sampling frequency and amplitude are normalized to 1 Hz and ±1 V, respectively. Input $V_{in}(s)$ is a sinusoid with a frequency one-thousandth that of the sampling frequency. OSR is set to 32 and the quantizer has 9 levels. Modulator output Y(z), prior to decimation, presents a rapidly varying low-resolution digital stream, which, for visual convenience, is illustrated through DAC output X(z) on the figure. The error-correcting loop ensures that the mean value of X(z) closely tracks input $V_{in}(s)$. Notably, upon zooming into the rising slope of the input sinusoid, it becomes evident that bits are predominantly low at the onset and tend to shift high more often later since the amplitude of the input has risen. After decimation, output $D_{out}(z)$ yields a slower, high-resolution digital code.

One notable limitation of ΔΣ ADC, clearly depicted in the figure, is the substantial delay imposed by the decimation

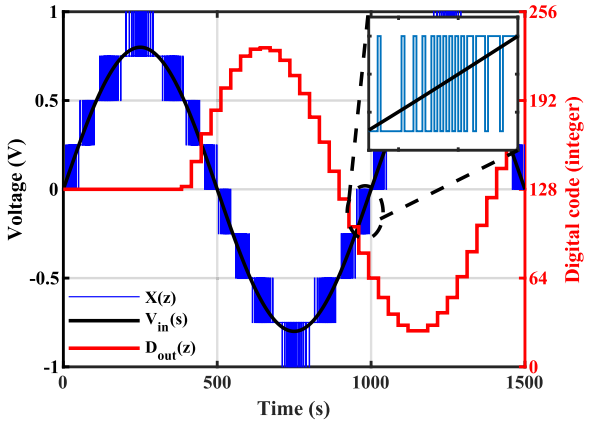

FIGURE 4. Simulated transient waveforms of a 1st-order ΔΣ ADC with 9 quantizer levels for signals labelled in Fig. 2.

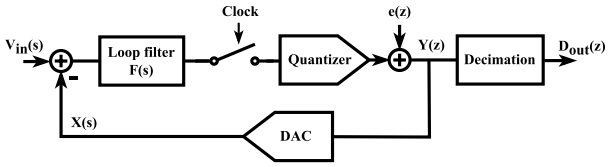

FIGURE 5. Block diagram of the CT ΔΣ ADC.

filter before the high-resolution sample is accessible at the output. A solution for this latency issue, which will be covered in detail in a subsequent section, is to use an incremental ΔΣ architecture. In such a structure, the memory elements of the integrators and of the decimation filter are reset after each conversion, eliminating the conversion latency.

B. THE CONTINUOUS-TIME ΔΣ MODULATOR

Fig. 5 illustrates the continuous time (CT) variant of the ΔΣ ADC. Unlike its DT counterpart, the input remains in the analog domain and is not sampled before entering the loop. Nevertheless, sampling still needs to take place within the quantizer, which requires clocking. In this configuration, the loop filter typically takes the form of an active RC filter. A significant advantage of this setup is its intrinsic anti-aliasing property, a consequence of the filtering operation preceding the sampling. Detailed discussions about this phenomenon and the derivation of loop filter equations can be found in [5]. The CT ΔΣ modulator is easier to drive because its input impedance is resistive, unlike the switched-capacitor input stage of the DT ΔΣ. As for noise shaping, it occurs analogously to the DT case. However, the CT architecture is not devoid of drawbacks, including sensitivity to process variations. Indeed, in the CT architecture, the integration constants depend on the RC time constant, which is more liable to be affected by fabrication variations compared to the easily matchable capacitor ratios used in the DT architecture. Additionally, the CT nature of the circuit heightens sensitivity to jitter and DAC waveform symmetry.

C. THE INCREMENTAL ΔΣ MODULATOR

The incremental ΔΣ ADC, initially proposed with a current-mode input in [12] and further refined in [13], is a variant

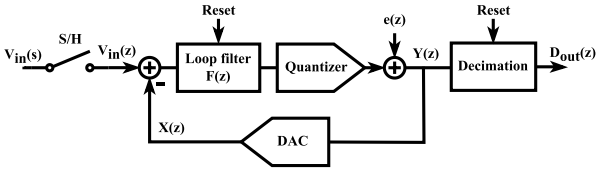

FIGURE 6. Block diagram of the incremental ΔΣ ADC.

of the conventional ΔΣ architecture. In this topology, the memory elements of the loop filter and the decimation filter are reset for each conversion as depicted in Fig. 6, resulting in a Nyquist rate ADC. This resetting of memory elements eliminates output delays, facilitates multiplexing of inputs from an array of sensors and enables implementation of sleep mode between acquisition periods. The formation of idle tones with DC input is also alleviated [5]. Moreover, the decimation filter in the incremental variant is implemented as a simple finite impulse response (FIR) filter instead of the usual infinite impulse response (IIR) filter. Optimal filtration is achieved by weighting the filter more heavily with the first samples and less with the last ones. Indeed, this weighting is optimal because the quantization noise from the last few samples is not shaped by subsequent samples which will serve for the next conversion [5]. However, it is worth noting that the reduced weighting in the incremental variant leads to inferior thermal noise performance compared to conventional ΔΣ ADC. While conventional ΔΣ ADC benefit from a thermal noise reduction by a factor of OSR, the incremental variant experiences a less pronounced reduction, especially with higher-order modulators [8]. Consequently, to meet a given SNR specification, the incremental modulator consumes more power, as higher capacitive loads are required to mitigate thermal noise. Detailed noise analysis and design considerations for incremental ΔΣ ADC are provided in [14], [15], and [16].

D. THE NOISE-SHAPING SAR TOPOLOGY

The successive approximation (SAR) ADC [11] is a Nyquist ADC which performs a binary search algorithm to discretize signals. It reutilizes the same comparator for every successive comparison, with one comparison per output bit. The SAR ADC is highly efficient, especially in its typical implementation with a capacitive DAC (CDAC). However, at higher precision, the capacitive loading and the area occupied by the CDAC increase significantly, as the capacitor size doubles with each additional bit. Additionally, maintaining low comparator noise becomes more challenging, often requiring a power-hungry preamplifier before the comparator to achieve the necessary accuracy.

An approach to improve the SAR ADC precision without excessive comparator and capacitor requirements is to use it in an oversampling topology: the noise-shaping SAR (NS-SAR). This topology is a relatively recent oversampling ADC architecture introduced in 2012 [17]. It differs from traditional ΔΣ ADC in several key ways. Its unique features include: 1) the direct sampling and quantization of the input

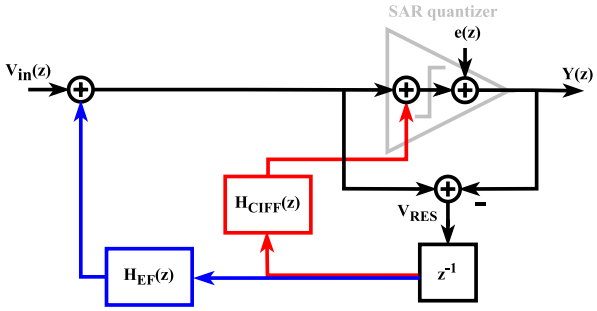

FIGURE 7. Block diagram of the NS-SAR ADC.

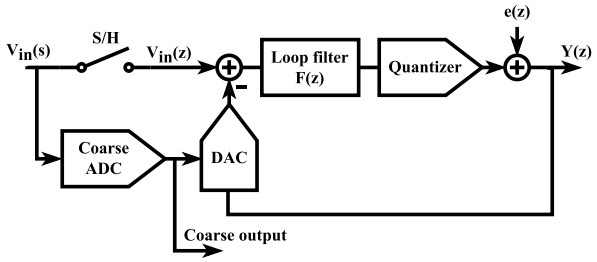

FIGURE 8. Block diagram of the zoom ADC.

signal by the SAR quantizer, which typically uses a higher bit-count than conventional $\Delta\Sigma$ designs; 2) the precise extraction of the residue error at the end of the SAR conversion, which is determined from the remaining voltage on the SAR CDAC array; and 3) the feedback mechanism that conveys only the residue error instead of the full modulator output [18]. High bit-count quantization, as well as only needing to process the residue error, allow the linear blocks of the filter to handle signals with very low swing, significantly easing design constraints.

Fig. 7 illustrates the two main NS-SAR topologies: error feedback (EF) [19] and cascaded integrator feed-forward (CIFF) [17]. The fundamental distinction between these architectures lies in the feedback return path: the EF structure feeds back into the CDAC array, while the CIFF structure feeds back into the comparator as an additional offset. This difference affects noise shaping to yield two alternate transfer functions:

$$NTF_{EF}(z) = 1 - H_{EF}(z)z^{-1}, \tag{4}$$

$$NTF_{CIFF}(z) = \frac{1}{1 + H_{CIFF}(z)z^{-1}}. \tag{5}$$

In (4), the EF case, $H_{EF}(z)$ appears in the numerator, facilitating its implementation through a straightforward FIR filter to achieve the desired noise shaping. However, $NTF_{EF}(z)$ is sensitive to gain variation, as filter coefficients may drift and degrade performance. Conversely, in (5), the CIFF case, $H_{CIFF}(z)$ resides in the denominator, necessitating the use of an integrator or IIR filter to achieve a proper high-pass filter $NTF_{CIFF}(z)$, increasing circuit complexity. However, while a sufficiently high gain is required, it need not be precisely tuned, thus relaxing matching constraints compared to the EF case [18]. Combined implementations of both EF and CIFF filter structures have been proposed [20], resulting in a total NTF derived from the multiplication of (4) and (5).

E. THE ZOOM TOPOLOGY

The zoom topology, pioneered by Souri and Makinwa in the early 2010s [21], [22], stands out as the ideal architecture for achieving high precision in low-bandwidth applications. Illustrated in Fig. 8, this architecture closely resembles the two-step ADC [11]. Initially, a Nyquist ADC performs coarse quantization, typically using a SAR ADC of 4 to 6 bits. Subsequently, a fine quantization stage employs an incremental $\Delta\Sigma$ in which the feedback DAC output range is dynamically adjusted based on the coarse quantization results. This significantly reduces the resolution requirement of the $\Delta\Sigma$ stage as the feedback DAC range narrows within a few coarse LSB of the input signal. Hence, selecting a single-bit quantizer is a common design choice due to its inherent linearity. Furthermore, the loop filter is subjected to a minimal input swing thanks to the output of the feedback DAC being zoomed in close proximity to the input level, facilitating simple and power-efficient loop filter amplifier design. A key distinction from conventional two-step ADC is the absence of explicit residue signal computation, which typically introduces offset, gain, and linearity errors through amplification and subtraction circuitry before the fine quantization stage [22].

F. THE TIME-DOMAIN $\Delta\Sigma$ MODULATOR

In the context of this survey, a *time-domain* (TD) $\Delta\Sigma$ modulator refers to a $\Delta\Sigma$ ADC where all or part of the signal processing occurs in the time domain instead of the conventional voltage amplitude domain. The time-encoded information can be represented as frequency, phase, or pulse-width modulation (PWM). The primary objective of this configuration is to achieve a digital-like design that leverages advancements in technology scaling for improved speed and power efficiency. This approach can prove particularly advantageous in deep submicron technology nodes where maintaining accuracy in voltage domain quantizers and filters becomes more challenging at low supply voltage, whereas time-domain accuracy improves due to reduced transition times. However, the typical voltage-controlled oscillators (VCO) used for processing data in the time domain are nonlinear, often requiring the use of calibration and/or linearization techniques [23].

Fig. 9 illustrates a typical configuration of TD $\Delta\Sigma$ ADC. The loop filter can be implemented either using a classical CT integrator or a VCO-based TD integrator. The quantizer is VCO-based and often also contains a digital backend, which includes a counter and additional processing. Accumulating the VCO output in a counter provides intrinsic signal integration, resulting in inherent first-order noise shaping to complement the noise shaping of the loop filter. An overview of different TD $\Delta\Sigma$ ADC architectures is presented in [24]

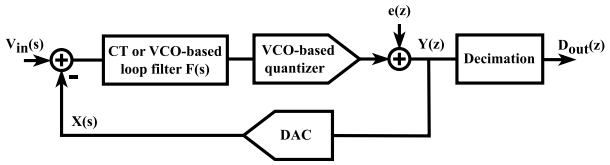

FIGURE 9. Block diagram of a typical TD $\Delta\Sigma$ ADC.

while detailed exploration of the recent state-of-the-art design trends is covered in later sections of this paper.

IV. STATUS OF THE STATE OF THE ART

A. COMPARISON WITH OLDER DESIGNS AND NYQUIST ADC

The oversampling ADC targeted in this review paper are compared with various Nyquist and older oversampling ADC designs from Murmann's database [4] in Fig. 10. The scatter plot relates energy per conversion to ENOB, visually illustrating the trade-offs between ADC resolution and conversion efficiency.

Trade-offs can also be quantified using FOM, taking into account key performance metrics such as SNDR, bandwidth, and power consumption. Among the most commonly used FOM for oversampling ADC are Schreier's [5]:

$$FOM_{Sc} = SNDR + 10\log\frac{BW}{P}, \tag{6}$$

and Walden's [25], [26]:

$$FOM_{Wa} = \frac{P}{2^{ENOB}F_s}, \tag{7}$$

where

$$ENOB = \frac{SNDR - 1.76}{6.02}, \tag{8}$$

BW is the ADC bandwidth, P is the power consumption and F_s is the Nyquist sampling frequency. Isolating the energy as P/F_s in (6) and (7) allows for the plotting of the corresponding slopes in Fig. 10. Consequently, we observe that the most optimal designs, exhibiting the highest FOM, tend to cluster towards the lower right corner of the scatter plot along the slopes of the FOM. Indeed, the state-of-the-art frontier closely follows the slope of FOM_{Sc} at high ENOB and FOM_{Wa} at lower ENOB, suggesting that these FOM effectively encapsulate relevant design trade-offs. Furthermore, the figure highlights that oversampling ADC feature superior precision due to their inherent noise-shaping capabilities. The selected designs clearly rank among the top performers.

B. SELECTED OVERSAMPLING ADC

Fig. 11 dives deeper into the selected ADC from the previous figure, specifying their topologies: DT $\Delta\Sigma$, CT $\Delta\Sigma$, NS-SAR, TD $\Delta\Sigma$ and hybrid designs incorporating both voltage-domain and time-domain stages. The five data points depicted in red, as opposed to the usual color, represent older designs sourced from Murmann's database that are still

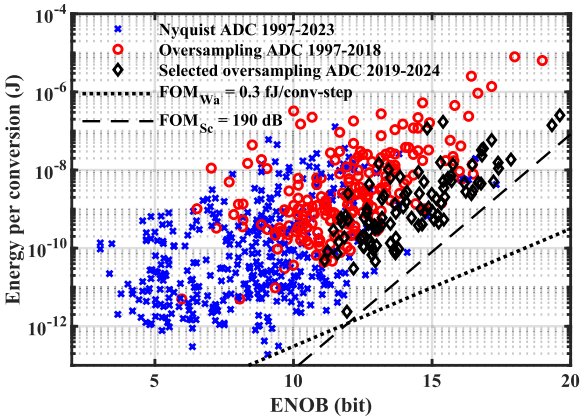

FIGURE 10. Scatter plot illustrating the trade-off between conversion efficiency and resolution for the selected oversampling ADC and those from Murmann's database.

competitive with the state of the art of the last 5 years and are thus selected for analysis in this paper. Also, gray triangles represent state-of-the-art designs identified in a previous survey from 2015 [6].

Remarkably, there has been a significant enhancement in energy efficiency over the past decade. Many recent designs consume less than a tenth of the energy per conversion while maintaining similar precision compared to state-of-the-art designs from 2015. The designs boasting the highest FOM are identified in the figure, featuring either or both of FOM_{Wa} below 6.5 fJ/conv-step [27], [28], [29], [30], [31] and FOM_{Sc} in excess of 183 dB [31], [32], [33], [34], [35], [36], [37], [38], [39], [40].

From a system-level perspective, NS-SAR designs are the top performers at low ENOB. This is demonstrated by the cluster of stars along the FOM_{Wa} slope between ENOB of 12 and 14 bits in the figure. Between ENOB of 14 and 17 bits, various topologies compete for supremacy. Interestingly, the designs by Lee and Moon [36] and Liu et al. [37] stand out as the only DT $\Delta\Sigma$ converters offering truly cutting-edge performance. For designs requiring precision beyond ENOB of 17 bits, the zoom architecture emerges as the clear leader.

TD $\Delta\Sigma$ converters exhibit comparatively mediocre power efficiency, as no design comes close to the FOM boundaries shown in the figure. Additionally, the nonlinearity issues of the VCO commonly used in this topology prevent these converters from achieving an ENOB higher than 15 bits. In contrast, every other topology features designs with resolutions exceeding this threshold. Nevertheless, the TD topology remains of interest because it holds significant potential for improvement with recent and upcoming technology nodes, given its compatibility with digital-friendly circuits. Furthermore, hybrid designs including a TD stage are already demonstrating impressive results with Hsieh's highly efficient design [31].

An important piece of information missing from Fig. 11 and the prior discussion is bandwidth performance. Focusing solely on the precision vs. energy per conversion tradeoff disregards the value of faster designs, as techniques for

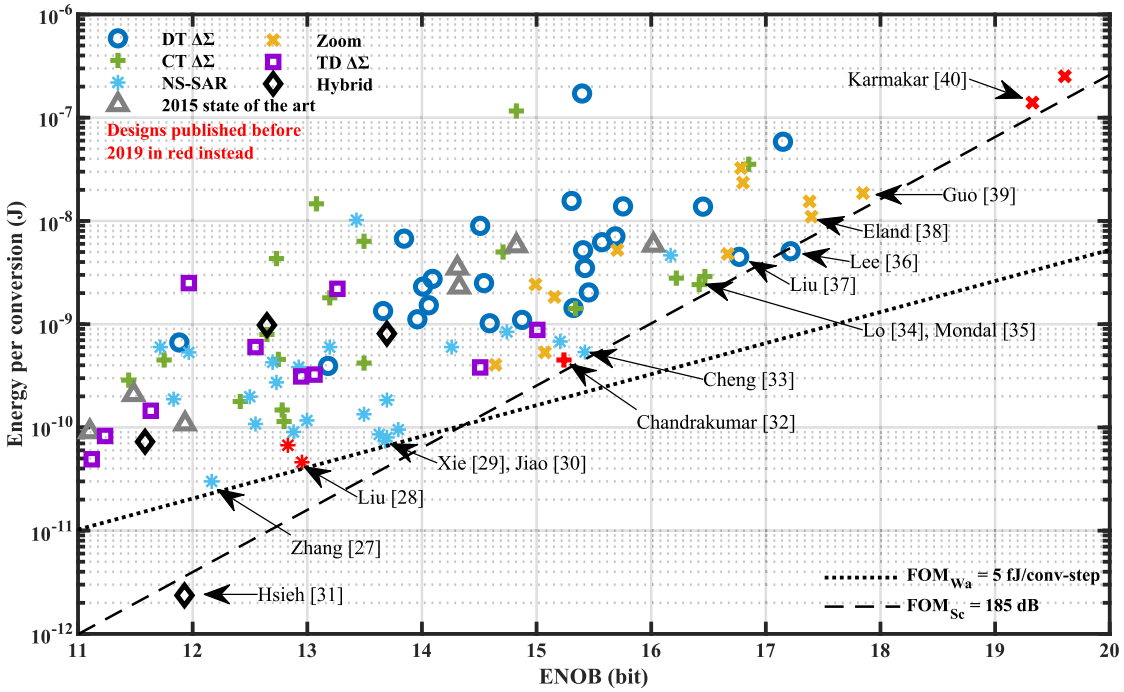

FIGURE 11. Scatter plot showcasing the energy/resolution trade-off for the selected ADC with their respective architectures highlighted. Designs with the highest figures of merit are labelled on the plot.

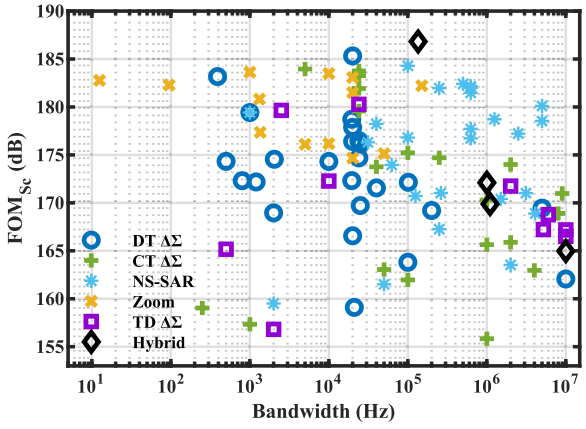

FIGURE 12. Scatter plot illustrating the FOM_{Sc} of the selected ADC in terms of bandwidth with their respective architectures highlighted.

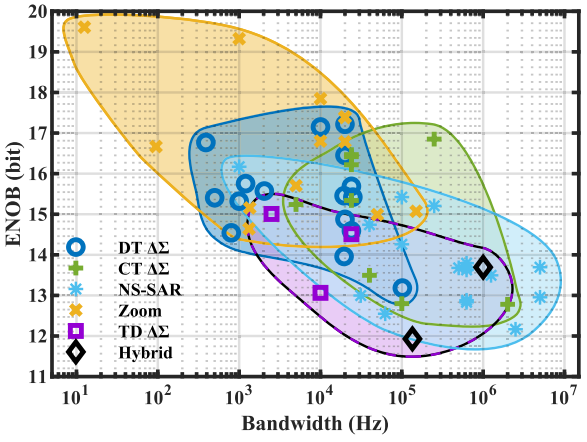

FIGURE 13. Scatter plot indicating ENOB and bandwidth for the top sixty selected ADC (FOM_{Sc} > 172 dB). The zone of optimal operation for each architecture family is highlighted.

higher-speed circuits are generally expected to be more complex, thus to consume more power and require a larger area footprint. Hence, Fig. 12 presents architecture performance relative to conversion speed, by displaying FOM_{Sc} of all the designs in Fig. 11, but according to bandwidth as the x-axis.

Similarly, Fig. 13 presents the bandwidth and ENOB specifications of the top sixty designs that surpass a FOM_{Sc} of 172 dB. The highlighted areas indicate the design space occupied by each topology, illustrating the trade-offs between bandwidth and precision for each family.

Some clear trends emerge by inspecting these three figures. For higher bandwidth, ranging from 100 kHz up to the 10 MHz limit of this survey, NS-SAR designs dominate performance, particularly at moderate ENOB. As anticipated, the fastest designs exhibit a slight reduction in peak FOM_{Sc}, with only Liu's design [28] managing to surpass 180 dB above 1 MHz. In the intermediate bandwidth range of 5 kHz to 100 kHz, top performance is shared between CT and DT $\Delta\Sigma$, as well as zoom architectures. While zoom architectures excel in achieving high ENOB, DT and CT $\Delta\Sigma$ designs lead the moderate to high ENOB space, with CT designs generally demonstrating higher bandwidth. Finally, for bandwidths below 5 kHz, zoom architectures clearly dominate, aside from the DT $\Delta\Sigma$ design by Liu et al. [37], which presents state-of-the-art performance in this range.

Once more, most TD $\Delta\Sigma$ and their hybridization with other topologies lag slightly behind in terms of performance. However, their ability to reach high bandwidth due to their TD digital-like processing circuit is clearly illustrated by the group of purple squares and black diamonds on the far right of Fig. 12. Maturation of these budding approaches can be expected to yield more competitive performance in the future.

The subsequent sections of the paper delve into the analysis of the design trends studied in the ADC implementations of Fig. 11 and Fig. 12, starting with a system-level perspective and thereafter honing in on circuit-level techniques.

V. SYSTEM-LEVEL DESIGN TRENDS

A. DESIGN TRENDS IN THE CONVENTIONAL DISCRETE-TIME AND CONTINUOUS-TIME $\Delta\Sigma$ TOPOLOGIES

1) THE MULTI-STAGE NOISE-SHAPING TECHNIQUE

The primary design considerations in a conventional $\Delta\Sigma$ architecture revolve around the power/precision trade-off for a given bandwidth constrained by OSR. To benefit from a more favorable trade-off, many designs opt to increase the modulator's noise-shaping order, allowing for a reduction in OSR while maintaining SNDR. However, at higher order, stabilizing the feedback loop becomes increasingly challenging, as the modulator may exhibit instability at high input amplitudes, limiting the practical input range [5]. Addressing this challenge, a clever technique known as multi-stage noise shaping (MASH) was introduced in [41]. This approach involves cascading multiple noise-shaping loops to achieve high-order noise shaping without encountering stability issues. In this method, the quantization error from the first stage is fed into a second noise-shaping modulator stage. The digitized error is ultimately subtracted from the output of the first stage, as depicted in Fig. 14. Additional digital filters are required before the subtraction to ensure proper quantization noise filtration. The resulting transfer function is expressed as:

$$Y_{out}(z) = H_1 Y_1 - H_2 Y_2. \tag{9}$$

Replacing Y_1 and Y_2 for the noise and signal transfer functions gives:

$$\begin{aligned} Y_{out}(z) = {} & H_1 STF_1 V_{in}(z) + H_1 NTF_1 e_1(z) \\ & - H_2 STF_2 e_1(z) - H_2 NTF_2 e_2(z). \end{aligned} \tag{10}$$

Designing digital filters H_1 and H_2 to meet the condition

$$H_1 NTF_1 = H_2 STF_2 \tag{11}$$

yields:

$$Y_{out}(z) = STF_1 STF_2 V_{in}(z) - NTF_1 NTF_2 e_2(z). \tag{12}$$

As a result, MASH effectively nullifies the error from the initial stage, e_1, leaving behind solely the error introduced by the second stage quantizer, e_2, which undergoes substantial attenuation by both NTF. Despite its inception in the 1980s,

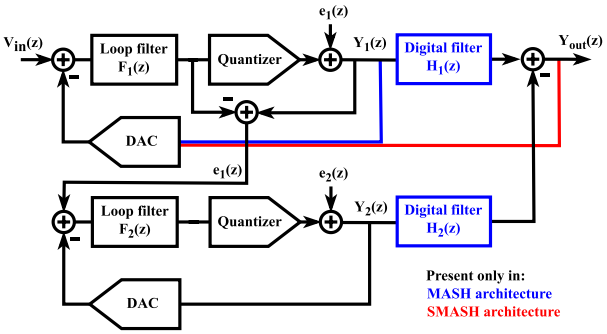

FIGURE 14. Block diagram of the multi-stage noise-shaping (MASH) and the sturdy multi-stage noise-shaping (SMASH) $\Delta\Sigma$ ADC architectures.

contemporary designs frequently adopt this strategy, amalgamating stages based on diverse architectures such as NS-SAR, TD, and conventional CT / DT $\Delta\Sigma$ modulators [30], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52]. Leveraging this approach incorporating a Nyquist converter as either the first stage (0-Xth order modulator) or the second stage (X-0th order modulator) can also be a great technique to improve performance. On one hand, the use of a 0-X MASH narrows the input range of the $\Delta\Sigma$ modulator [44], [53], relaxing design constraints in a manner similar to a zoom ADC. On the other hand, the X-0 MASH enhances SNDR in a power-efficient manner by simplifying the second stage design [42]. For example, in [42], a 2-0 architecture is employed. Instead of solely relying on a SAR ADC for the second stage, it is also repurposed as a digital feedforward to diminish the modulator's input range, which relaxes the loop filter constraints and culminates in achieving a state-of-the-art FOM_{Sc} of 179.4 dB.

2) THE STURDY MULTI-STAGE NOISE-SHAPING TECHNIQUE

A significant drawback of MASH lies in the stringent requirement to precisely match the transfer function of the second-stage digital filter, H_2, to the analog NTF_1 of the first stage, so as to ensure proper noise cancellation. To mitigate this matching challenge and relax the required amplifier gains, the sturdy MASH (SMASH) architecture was proposed in [54]. As shown in Fig. 14, establishing an encompassing feedback path combining both stages in SMASH, as opposed to having independent feedback loops in MASH, eliminates the need for the digital filters H_1 and H_2. Consequently, the high-gain constraint on the amplifiers, essential for achieving proper matching between the analog and digital components in MASH, is eliminated by SMASH [54]. The resulting transfer function becomes:

$$\begin{aligned} Y_{out}(z) = {} & STF_1 V_{in}(z) - NTF_1 NTF_2 e_2(z) \\ & + NTF_1(1 - STF_2) e_1(z). \end{aligned} \tag{13}$$

Typically, STF_2 is designed to equal $1 - NTF_2$ in order to ensure that both stage errors are shaped by an identical transfer function. However, this approach no longer completely nullifies the quantization noise of the first stage, thereby affecting SNDR [5]. Although SMASH was initially

proposed for DT configurations, CT implementations have also been demonstrated [55], [56], [57]. Noise-cancelling versions have been introduced as well [55], [58], [59], requiring additional circuit blocks or precise delay matching so as to be able to eliminate the quantization noise of the first stage.

3) NS-SAR QUANTIZER

Another interesting combination is to incorporate a NS-SAR quantizer within a conventional DT $\Delta\Sigma$ loop, harnessing the low power consumption and compact footprint of the NS-SAR alongside the robustness of the DT $\Delta\Sigma$ architecture. This concept has garnered recent attention, as demonstrated in [60], where a 2nd-order NS-SAR is combined with a 1st-order DT integrator. In [61], the DT loop filter complementing the NS-SAR quantizer serves to increase SNDR and input impedance through an auxiliary impedance boosting technique.

4) OPTIMIZATION OF HIGH-ORDER SINGLE LOOP MODULATOR

Despite the appeal of the aforementioned multi-loop structures, the current top FOM_{Sc} are in fact achieved using 3rd- or 4th-order single-loop modulators. To ensure sufficient stability performance in such cases, the NTF sharpness is typically designed to be less aggressive than a pure integrator, thereby limiting out-of-band noise gain and enhancing stability. Notably, four of the papers showcasing FOM_{Sc} in excess of 183 dB follow a similar approach: a single-loop modulator with high-efficiency amplifiers in the loop filter. In DT applications, Lee and Moon [36] employs a 3rd-order loop with pseudo-pseudo differential ring-amplifier based integrators, resulting in a remarkable FOM_{Sc} of 185.3 dB. Similarly, Liu et al. [37] propose a 4th-order structure featuring a cascoded floating inverter amplifier (FIA). In CT scenarios, Mondal et al. [35] introduces a 3-stack operational transconductance amplifier (OTA) to mitigate noise and enhance transconductance within a 3rd-order modulator. Conversely, Lo et al. [34] presents an energy-efficient power domain shift, reducing the supply voltage from 1.8 V to 1 V within a two-stage OTA serving as the loop filter amplifier in a 3rd-order modulator. Chandrakumar's CT design [32] is also a single loop 3rd-order modulator, but differs in that the loop filter is modified with an additional gain stage before the first integrator to reduce the power consumed by the input resistor of the RC integrator, thus yielding a FOM_{Sc} of 184 dB.

5) FEEDFORWARD LOOP STRUCTURE

The most common loop topologies in recent literature include feedforward, which helps reduce voltage swing inside the loop filter, thereby minimizing distortion and easing design constraints for the amplifiers. Recent implementations relying on this approach include [62] which incorporates digital feedforward extrapolation inside a time interleaved structure

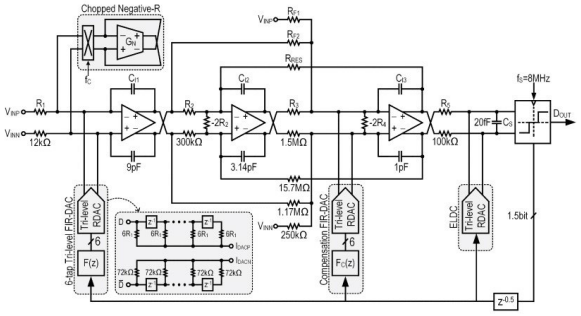

FIGURE 15. Continuous-time $\Delta\Sigma$ modulator with a negative-R assisted first integrator. Reprinted from [68], © 2021 IEEE.

to reduce hardware overhead. Additionally, [63] proposes a modification to the usual CIFF structure that eliminates the internal feedforward, thus relaxing the requirements of the feedforward summing node.

6) CONTINUOUS-TIME LOOP FILTER

The classical implementation of the CT loop filter is based on an active RC integrator. However, designing high-precision modulators imposes stringent noise and linearity requirements, resulting in significant power dissipation in this scenario. To address this issue, [64] proposes the addition of a large capacitor at the amplifier input, creating a passive low-pass filter stage before the integrator. This configuration relaxes the transconductance and swing requirements of the amplifier while converting the parasitic pole into a beneficial noise-shaping one. A different approach combines passive and active stages to reduce the number of power-hungry active integrators. In [65], this method uses two op-amps for a 4th-order modulator.

The negative-R assisted integrator [66] is another solution to reduce power consumption of the active RC integrator. Illustrated in Fig. 15, this method adds an extra negative resistor input path to the integrator's amplifier realized with an active G_m stage. This integrator structure compensates for finite gain by rendering the virtual ground ideal, thereby relaxing the DC gain, bandwidth, noise, and linearity requirements of the amplifier. This technique is reused in [67] and [68], achieving a state-of-the-art FOM_{Sc} of 181.9 dB in the latter instance.

Another design technique for CT loop filters is using a G_mC integrator cell instead of an active RC integrator. The open-loop transconductance lowers power consumption, although the absence of negative feedback limits circuit linearity. Therefore, a linearization technique introduced in [69] and improved in [70] sets the feedback DAC to have the same nonlinear transfer characteristic as the open-loop transconductance. The combination of both circuit blocks thus allows for cancellation of the nonlinearities.

Lastly, the design in [71] combines both filter structures to leverage their advantages: RC integrator for its high linearity, in the most critical first integration stage, and G_mC cells for their high power efficiency, in the subsequent stages.

7) ALIAS REJECTION

Alias rejection is another interesting property of CT ΔΣ modulators. Recent work [72] proposes a reference-switched resistive feedback DAC to maximise this effect, achieving intrinsic anti-aliasing filtration in excess of 80 dB.

B. DESIGN TRENDS IN THE INCREMENTAL ΔΣ MODULATOR

1) MULTI-STAGE CONFIGURATIONS

Recent advancements in ADC design have introduced several improvements to the typical incremental ΔΣ ADC architecture, particularly in multi-stage configurations. One notable configuration is the extended-counting ADC. In this setup, the first stage consists of an incremental ΔΣ ADC, followed by a Nyquist ADC as the second stage [5] as presented in Fig. 16. The unique feature of the extended-counting ADC lies in the readily available total error of the first stage, which, through a feedforward structure, becomes accessible at the output of the last integrator of the loop filter. This total error can then be sent to a Nyquist rate ADC, while the output of the first stage is processed by the decimation filter, allowing for complete pipelined operation [73], [74]. By digitizing the error and subtracting it from the output of the decimation filter, accuracy can be significantly improved. Recent works leveraging this technique include [75], where the first stage comprises a 1st-order, 1-bit incremental ΔΣ ADC extended with a 10-bit SAR reusing the same quantizer and employing a serial two-capacitor DAC. In [76], a three-phase variant reusing the same asynchronous SAR quantizer for each stage, with a power efficient capacitor scaling technique, is presented. Other closely related multi-stage structures explored in recent research include the sturdy MASH [77] and the robust MASH [78]. Additionally, three-stage topologies are introduced in [79], tailored for class-D amplifiers, and more recently in [43], featuring a fifth-order configuration where the first two stages are reconfigured to form the third stage in a hardware-efficient manner.

2) MULTI-PHASE FILTERING

Another interesting technique is to use a multi-phase loop filter able to adjust the properties of the loop filter for different subsets of samples during a conversion. An example involves using slice-based integrators in parallel to optimise the noise/power consumption trade-off [80], [81]. The technique, shown in Fig. 17, consists in disabling some integrator slices as the conversion progresses. The noise of the slice-based integrator increases as some slices are disabled but the contribution of the last samples to the output result holds lower weight. Hence, power consumption can be optimised by gradually relaxing the noise constraints with minimal impact on precision.

Another technique, explored in [82], is to switch the modulator from a 1st-order linear mode to an exponential mode to harness both the benefits of thermal noise suppression in the linear mode and high SQNR in the exponential mode.

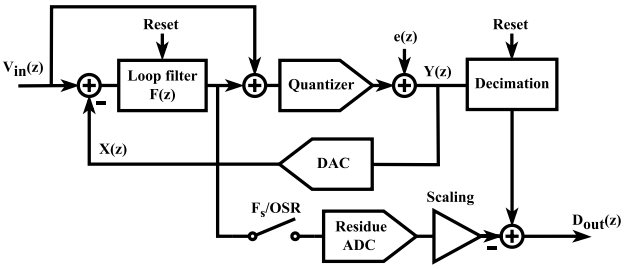

FIGURE 16. Block diagram of the extended-counting ADC.

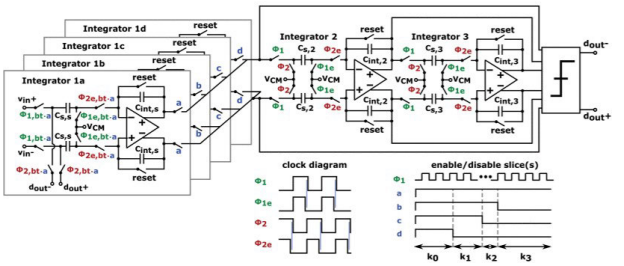

FIGURE 17. Incremental ΔΣ modulator implementing the slice-based integrator. Reprinted from [80], © 2019 IEEE.

This design achieves the highest FOM_{Sc} among the reviewed incremental ADC excluding incremental zoom topology, reaching 176.4 dB. The idea is further explored in [83], including frequency domain analysis.

C. DESIGN TRENDS IN THE NOISE-SHAPING SAR TOPOLOGY

1) CASCADING LOOP FILTERS

The NS-SAR stands out as a remarkably power- and area-efficient topology. However, achieving a high SNDR poses a challenge due to the topology's high sensitivity to loop filter coefficients, particularly in the simpler yet more efficient EF configuration. The practice of cascading loop filters to attain higher-order noise shaping, which is necessary to strive for high SNDR, imposes strenuous matching constraints. To address this, [84] proposes a method for cascading loop filters in a nested manner, thus relaxing matching constraints. This approach has been leveraged in numerous designs, yielding impressive performance. For instance, in [85], cascading a 1st-order stage four times yields a FOM_{Sc} of 182 dB.

Expanding upon this concept, [20] proposes nesting both EF and CIFF feedback paths together. This innovation enables the realization of a 3rd-order loop filter using a single amplifier by merging the residue extraction for both feedback paths, thereby simplifying circuitry and reducing power consumption. The combined use of CIFF and EF structures also leverages their respective advantages: the robustness of the CIFF path reduces NTF sensitivity to amplifier gain variations, while the simplicity of the EF path is maintained. The overall design achieves state-of-the-art performance with a FOM_{Sc} of 182 dB.

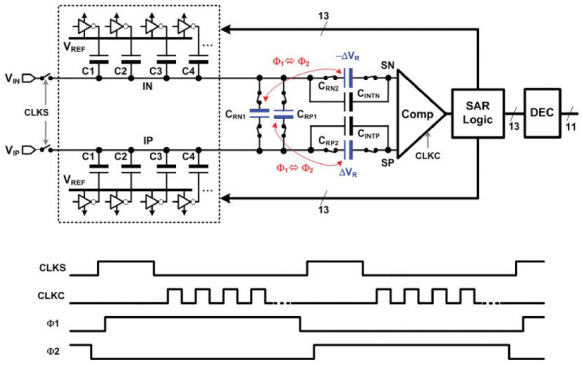

FIGURE 18. Noise-shaping SAR ADC with the capacitor stacking technique. Reprinted from [86], © 2019 IEEE.

2) CAPACITOR STACKING

Another crucial development facilitating the robust order extension technique introduced in the previous section is the capacitor stacking technique. Prevalent in many cutting-edge designs, the capacitor stacking technique was first implemented by [86] as illustrated in Fig. 18. This approach utilizes switching capacitors in series with the signal path as summing elements. While capacitor stacking can enhance the power efficiency of EF structures, as shown in [87], its major impact lies in optimizing CIFF structures. By incorporating a series capacitor at the comparator input, the need for multi-input comparators is eliminated. This innovation is particularly beneficial because multi-input comparators are inherently inefficient, contributing to increased thermal noise and power consumption.

The surveyed CIFF NS-SAR designs clearly demonstrate the effectiveness of capacitor stacking over multi-input comparators. For example, [88] and [89] both present 2nd-order CIFF designs with multi-input comparators achieving a FOM_{Sc} of 171 dB, whereas, in contrast, [90] and [91] showcase comparable 2nd-order capacitor stacking-based designs reaching FOM_{Sc} of 179.4 dB and 181.5 dB, respectively.

Capacitor stacking is also applied in fully passive NS-SAR designs as a summing element with four times amplification, achieving FOM_{Sc} of 178.2 dB in [92] and 182.2 dB in [30]. Additionally, Cheng [33] presents the NS-SAR design with the highest FOM_{Sc} of 184.3 dB, featuring a 4th-order CIFF alternating both passive and active integrators with capacitor stacking.

3) OTHER DESIGN TRENDS

Recently, a CT NS-SAR was proposed for the first time in [93], capitalizing on the power efficiency and anti-aliasing properties of the CT $\Delta\Sigma$. It addresses the timing conflict between the CT integral and the DT SAR quantizer by duty cycling the integrator, allocating 5% of the clock period to SAR quantization, with negligible influence on noise shaping performance.

Additionally, Xie et al. [29] introduces an innovative error feedback-cascaded resonator feedforward (EF-CRFF) topology, enabling NTF optimization through zeros placement, resulting in an impressive FOM_{Sc} of 182.4 dB at OSR of only 5.

Designs aiming to enhance performance and robustness by combining the EF and the CIFF structure are presented in [27] and [94]. In [47], the same idea is applied to a MASH configuration.

Finally, [48] proposes the use of two low-resolution pipelined NS-SAR stages with a high interstage gain (ISG) of 16 to achieve high SNDR while reusing the same amplifier for filtering and ISG.

D. DESIGN TRENDS IN THE ZOOM TOPOLOGY

1) DYNAMIC ZOOM

In the original zoom topology, the coarse quantization defining the zoomed range of the DAC is performed sequentially with the fine $\Delta\Sigma$ stage. This operation in succession severely constrains the bandwidth of the zoom ADC. For instance, initial designs by Souri and Makinawa are capped at 10 S/s [21] and 25 S/s [22]. To address this issue, the dynamic zoom is proposed [95], which involves running both stages concurrently, in parallel. This approach also enables the use of a free-running $\Delta\Sigma$ as the fine stage. Nevertheless, parallelizing both stages introduces a delay before the zoom reference can be updated due to the limited conversion speed of the coarse quantizer. If the input varies rapidly, it may surpass the zoomed range, pushing the modulator beyond its stable bounds. To mitigate this possibility, over-ranging can be used, whereby the zoomed range is enlarged to $\pm$k levels from the coarse quantizer output. This expanded range reduces the risk of being overrun by the input signal. The design in [95] uses this technique to achieve a bandwidth of 20 kHz, sufficient for audio applications. However, the DAC reference level is updated only once every 5 cycles, rendering it vulnerable to out-of-band interferers. The dynamic zoom technique in [40] addresses this issue by refreshing the reference concurrently every clock cycle using an asynchronous SAR coarse quantizer. This faster reference update allows for lower swing and enhanced power efficiency, thereby leading to a state-of-the-art FOM_{Sc} of 183.6 dB at 1 kHz bandwidth.

2) "FUZZ" MITIGATION

Another challenge with zoom ADC is the introduction of out-of-band "fuzz" in the output spectrum, which degrades SNDR [40]. This issue arises from the summation of the outputs of the coarse and fine stages in the digital domain. This digital summation assumes that the STF of the fine ADC is exactly unity, which is not always the case, especially at higher frequencies for CIFF $\Delta\Sigma$ presenting STF peaking [40]. The digital summation then becomes non-ideal, introducing quantization error leakage from the coarse stage into the output. In [40], this problem is addressed with a digital filter replicating the STF at the digital output of the coarse stage, akin to a MASH architecture. Eland et al.

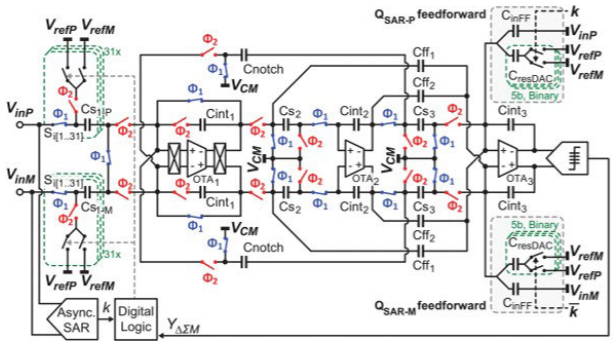

FIGURE 19. Dynamic zoom ADC with analog feedforward path reducing the fuzz issue. Reprinted from [38], © 2021 IEEE.

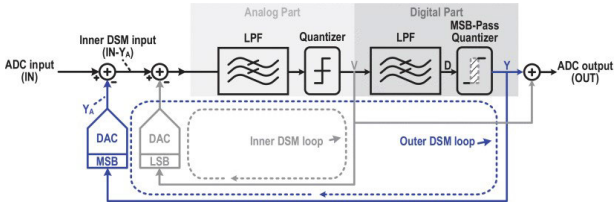

FIGURE 20. Architecture of the nested ΔΣ Modulator. Reprinted from [39], © 2023 IEEE.

[38] proposes the use of an analog residue feedforward path to ensure a unity STF, significantly reducing the fuzz issue. With a 2-bit quantizer, this allows for a 40% OSR reduction, resulting in a state-of-the-art FOM_{Sc} of 183.1dB. The modulator with the additional feedforward path is shown in Fig. 19. Recently, this concept has been revisited in [96] with a fully dynamic zoom using FIA achieving sub 1 μW power consumption and a FOM_{Sc} of 182.2 dB.

3) CONTINUOUS-TIME ZOOM

The advent of dynamic zoom with a free-running ΔΣ fine stage also facilitated the introduction of CT zoom ADC, which aim to leverage the efficient loop filter amplifier and easy drivability properties of the CT ΔΣ architecture [97]. Still, special care must be taken in designing the feedback DAC and the chopping circuitry necessary to suppress 1/f noise. Indeed, CT ΔΣ are more sensitive to DAC waveform non-idealities and chopping artifacts than their DT equivalent. In [97], a novel intersymbol interference (ISI) reduction technique based on matched layout in its DAC and a pseudo-differential inverter-based amplifier are employed, achieving FOM_{Sc} of 181.5 dB at 20 kHz.

Recent works propose using oversampling ADC as coarse quantization stages in CT zoom architectures, with [98] using a NS-SAR and [99] employing a CT ΔΣ modulator. This configuration allows the shaping of the fuzz error of the coarse quantizer, improving SNDR and achieving FOM_{Sc} above 180 dB in both cases. Finally, a highly area-efficient hardware-reusing zoom-incremental-counting ADC with CT ΔΣ fine stage is presented in [100].

4) OTHER DESIGN TRENDS

Among the surveyed works, one recent approach uses FIA-assisted residue extraction, allowing the NS-SAR fine stage to skip 75% of the sampling operations. Combined with a lower OSR, the design reaches a bandwidth of 150 kHz, the fastest in all the assessed zoom topologies [101]. In [102], a self-timed dynamic amplifier-based zoom ADC is introduced that eliminates the need for power-hungry high-frequency clock generation. In [103], an adaptable pole-optimization technique mitigates the performance degradation normally associated with scaling resolution/bandwidth. Furthermore, [104] presents the first pseudo-pseudo-differential incremental zoom design. It employs simple single-ended circuitry to process differential inputs, with a three-phase technique to reduce common-mode noise leakage, resulting in great performance with a FOM_{Sc} of 180.8 dB.

5) AN ALTERNATIVE TO THE ZOOM TOPOLOGY: THE NESTED ΔΣ MODULATOR

A novel approach, distinct from traditional zoom ADC architectures but targeting the same key challenges, is the nested ΔΣ modulator introduced by Guo in [39]. This architecture comprises an inner analog ΔΣ modulator embedded within an outer analog-digital ΔΣ modulator as illustrated in Fig.20. The swing of the inner ΔΣ is suppressed by the outer loop, enabling the same low-power benefits as in the zoom ADC. However, unlike zoom ADC, the nested structure suffers neither from distortion nor from fuzz leakage by virtue of its different loop construction. This architecture surpasses most conventional zoom ADC, achieving a remarkable FOM_{Sc} of 183.5 dB at a 10 kHz bandwidth as well as SNDR of 109.2 dB.

E. DESIGN TRENDS IN THE TIME-DOMAIN ΔΣ MODULATOR

1) VCO-COUNTER ARCHITECTURE

The first generation of oversampling ADC designs making use of TD signal processing is the VCO-counter architecture [105], [106], wherein a VCO performs voltage-to-frequency conversion, and a reset counter provides a digital output proportional to frequency, as depicted in Fig. 21. In this structure, neither feedback nor an integrator is needed. Noise shaping is achieved through the summation of the rising edges at the output of the VCO inside the counter, enacting intrinsic integration. The absence of a feedback path significantly reduces design constraints by eliminating the need for a DAC and its associated linearity and precision challenges. Recent designs leveraging this open-loop oversampling concept include [107], in which a current-controlled oscillator (CCO) with a variable nominal frequency manages to improve power efficiency, and [108], in which a PWM-based voltage-to-time converter precedes the VCO so as to enhance input impedance and linearity, achieving SNDR above 80 dB while consuming only 2.2 μW.

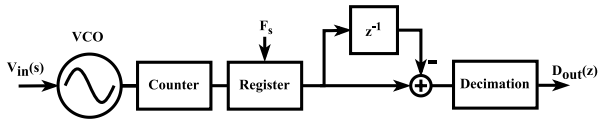

FIGURE 21. Block diagram of a simple implementation of the VCO-counter oversampling ADC.

2) CONTINUOUS-TIME FILTER

A structure introduced in the late 1990s [109] added feedback and a CT integrator upstream of the VCO quantizer, similar to those found in CT ΔΣ modulators. This structural change allows for greater flexibility in loop filter and noise-shaping design. Many recent state-of-the-art designs adopt this structure. Notably, [110] features a capacitive-π network that makes the CDAC independent from the load capacitance of the integrator, thereby reducing capacitor footprint and power consumption. The technique is illustrated in Fig. 22, where the π network is formed of C_L, C_C and C_{DAC} at the output of the G_m stage. The design in [111] improves upon this approach by utilizing a resistive feedback DAC in parallel with the degeneration resistance of the first G_m stage to improve linearity of the system.

3) FULLY TIME-DOMAIN ARCHITECTURE

One drawback of the aforementioned TD architectures is the need for the loop filter to include an active G_m stage. Consequently, part of the signal chain is processed in the voltage domain, which remains subject to limitations in advanced technology nodes with reduced supply voltages. Hence, OTA-less designs have been proposed that use passive RC networks for the loop filter [112]. Other designs employ techniques involving VCO, CCO, and phase detectors to construct analog filters, as explained in [113]. These designs include some of the most efficient and precise TD ΔΣ ADC. For example, the design in [114] introduces a new feedforward structure in a 3rd-order modulator, linearizing the VCO and achieving the highest SNDR in TD ΔΣ of 92 dB with a FOM_{Sc} of 179.1 dB. Furthermore, this highly digital topology, where both quantizer and loop filter are VCO-based, allows for effective layout automation. Zhong's design [115] is fully synthesized and achieves the best FOM_{Sc} for a TD ΔΣ ADC at 180.1 dB. Another fully digital structure is presented in [116], where the loop structure is based on a digital phase-locked loop (PLL) incorporating an array of phase frequency detectors to reduce the VCO center frequency and, consequently, minimize power consumption.

4) MULTI-STAGE ARCHITECTURE

Multi-stage structures are also prevalent, where one or both of the stages is implemented in TD. TD designs where one of the stages still operates in the voltage domain are deemed hybrid in Fig. 11. Employing a TD second stage offers undeniable advantages: the noise shaping from the prior stage and the minimal swing of the quantization error help linearize the VCO without necessitating additional design

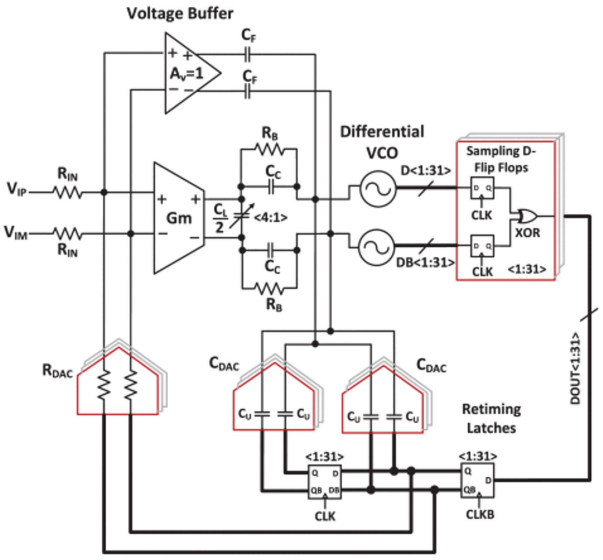

FIGURE 22. Time-domain ΔΣ modulator with VCO quantizer and G_mC integrator. Reprinted from [110], © 2021 IEEE.

tricks. Recent work, such as that in [51] and [52], has delved into MASH structures with both stages implemented in TD. MASH structures combining a DT ΔΣ [50] or a NS-SAR [49] first stage with a VCO-based second stage have also been explored. Furthermore, combinations featuring power-efficient NS-SAR structures have been presented, such as in [117], where a VCO integrator supplements a 2nd-order NS-SAR with an anti-aliasing filter based time-to-voltage conversion between both sections. Finally, the design outlined in [118] integrates a TD comparator within a NS-SAR structure for superior thermal noise performance.

5) AN ALTERNATIVE HYBRID APPROACH: HSIEH'S DESIGN

Among all oversampling ADC designs covered in this survey, Hsieh's topology [31] achieves both the highest FOM_{Sc} and FOM_{Wa} at 186.8 dB and 0.6 fJ/conv-step, respectively. The topology, shown in Fig. 23 consists of two Nyquist SAR quantizers forming the first stage, each handling half of the input swing so as to effectively double the allowable input range. To minimize power consumption, two main techniques are employed. First, the unused of the two quantizers is set to idle mode since each one is responsible for handling a distinct portion of the input range. Second, a low supply voltage of 0.4 V is used.

To enhance SNDR at minimal power overhead, a second stage 1st-order TD incremental ΔΣ reuses as much of the same circuit components as possible. A voltage-controlled delay line (VCDL) within the SAR first stage is reconfigured into a VCO integrator to process the residue error readily available on the SAR CDAC array. After combination of the output of the two successive stages by the digital backend, a SQNR improvement of 24 dB is achieved compared to the SAR first stage only. The overall design operates with

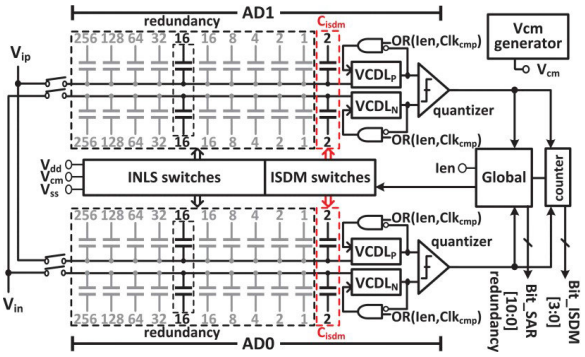

FIGURE 23. Architecture of the design achieving the highest FOM. Reprinted from [31], © 2019 IEEE.

a bandwidth of 135 kHz and a power consumption of just 0.6 μW.

VI. CIRCUIT-LEVEL DESIGN TRENDS

A. AMPLIFIER AND LOOP FILTER DESIGN TRENDS

One of the most critical circuit blocks in $\Delta\Sigma$ modulator design is the loop filter along with its amplifiers. If not designed carefully, distortion and thermal noise caused by the amplifier may significantly degrade the performance of the entire ADC. As for insufficient DC gain, it may result in non-ideal integration, negatively affecting noise shaping and SQNR. Also, insufficient bandwidth can cause settling errors, severely limiting system accuracy. Finally, the amplifier often consumes a significant portion of the power budget of a $\Delta\Sigma$ ADC. For all these reasons, developing amplifier structures to offer more favorable design trade-offs remains a significant research focus.

1) CONVENTIONAL AMPLIFIER

The traditional Miller compensated amplifier is seldom used in recent designs [43], [65]. Instead, designers often prefer single-stage telescopic cascode [50], [82], folded cascode [63], [80], [81], or gain-boosted cascode [62], [70], [76] amplifiers, which offer better power efficiency at the expense of output swing. Another noteworthy amplifier topology for CT $\Delta\Sigma$ modulators is the feedforward compensated OTA. This topology provides higher bandwidth for the same power consumption as a Miller compensated amplifier but introduces more swing in the transient response due to an additional zero in the transfer function [5]. This makes the technique harder to implement in settling-based DT modulators because the additional transient swing needs to settle completely. However, the technique is well suited for CT modulators where the entire waveform is relevant and slowly settling transients don't really matter. Many CT designs make use of this technique to enhance power efficiency [46], [72], [77], [119], [120], [121], including some of the highest FOM_{Sc} recorded [34], [35].

2) INVERTER-BASED AMPLIFIER

The inverter-based, or current-reuse, amplifier was introduced in $\Delta\Sigma$ modulators by Chae [122]. These amplifiers consist of an inverter biased at the center point, which can be used either as the complete amplifier or as an input stage. This design effectively doubles transconductance since both PMOS and NMOS transistors are active simultaneously and contribute to overall transconductance. This improves power efficiency because higher transconductance can be reached for the same bias current. However, this topology is more sensitive to PVT variations and parasitic impedance. Recent designs featuring inverters as amplifiers are presented in [61], [67], [93], [123], and [124]. To achieve higher DC gain, some authors use a current-reuse first stage, within a two-stage OTA [90] or in a cascode structure [38], [40], [64], [97], [103], [125]. A self-bias cascode structure, introduced in [104], reduces power consumption from the bias circuitry.

3) RING AMPLIFIER

The ring amplifier [126] is an innovative amplifier topology that uses a ring oscillator with a dead zone integrated into a feedback loop. The dead zone forms a range where the ring oscillator's output does not change, forcing the output to settle at a fixed value. The advantages of this topology include inherent rail-to-rail output, high slew rate, and excellent scaling with technology nodes. However, there exists a fundamental trade-off between robustness and precision, dictated by the size of the dead zone. Two designs by Lee and Moon [36], [44] use this technique in the surveyed state-of-the-art, with [36] achieving the second-best recorded FOM_{Sc} at 185.3 dB.

4) BUFFER-BASED AND PASSIVE LOOP FILTERS

The source follower integrator [59], [127], illustrated in Fig. 24, is an example of an integrator topology that simplifies design, as it requires only a buffer, a few switches, and capacitors. Many designs also opt for passive filtering using RC or passive switched-capacitor networks as loop filters [49], [89], [112], [128]. The drawback of using passive or buffer-based circuitry is that the integration performed by the circuit is non-ideal, which reduces the effectiveness of the noise shaping.

5) DYNAMIC AMPLIFIER

Dynamic amplifiers are highly popular in recent state-of-the-art designs, as they have the potential to curb the high static power consumption associated with conventional amplifiers. By having its biasing current vary during operation, a dynamic amplifier improves power efficiency as it draws high current only when necessary and limits it during idle periods. Like the ring amplifier, the dynamic amplifier must be used in a settling-based circuit, such as the switched-capacitor integrator of a DT $\Delta\Sigma$ modulator, to be able to reset the bias current variation effectively.

The concept of a variable bias current amplifier was first proposed around 1980 [129], [130], [131]. Its application in modern ADC design was revisited by Chiang et al. [132] in the form of a charge-steering amplifier for pipeline ADC.

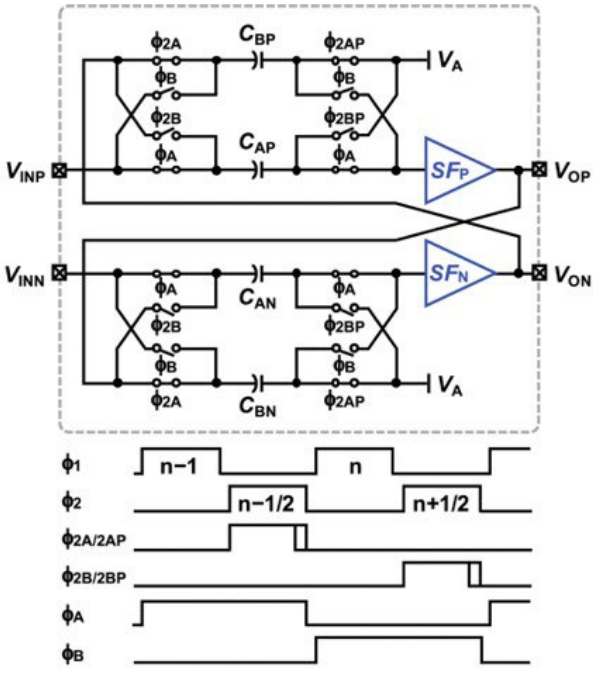

FIGURE 24. Schematic and timing diagram of the source follower integrator. Reprinted from [59], © 2018 IEEE.

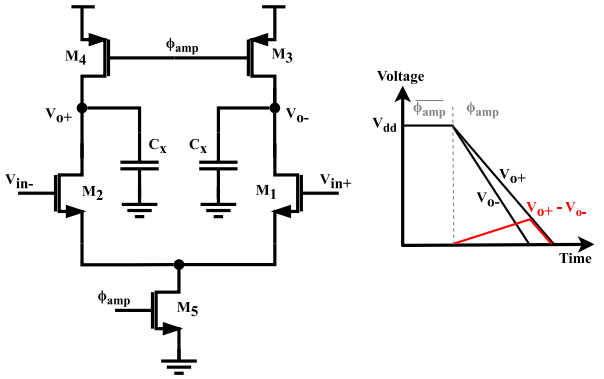

FIGURE 25. Schematic of the charge-steering dynamic amplifier and its simplified output waveforms.

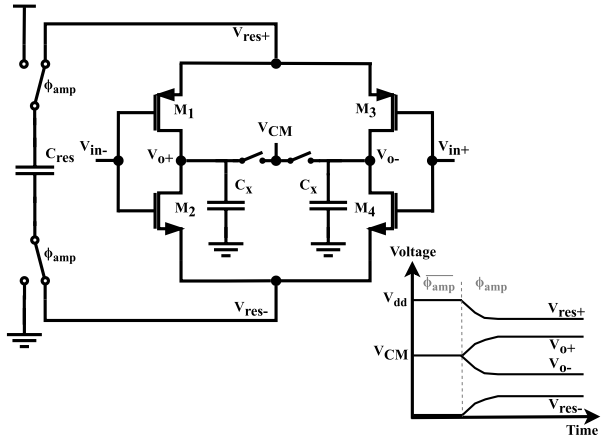

FIGURE 26. Schematic of the floating inverter dynamic amplifier and its simplified waveforms.

The operating principle involves precharging capacitors at the output of a differential pair. During amplification, the charges on both precharged capacitors discharge at a rate proportional to the differential input, thereby generating amplification, as shown is Fig. 25. This idea has been adapted to be used in oversampling ADC [19], [88], [133], notably in Liu's NS-SAR design [28], to help achieve a FOM_{Sc} of 180.1 dB and a FOM_{Wa} of 5.8 fJ/conv-step.

Despite its impressive performance, the charge-steering amplifier has a variable common mode at the output and is sensitive to PVT variations, which makes calibration crucial, as demonstrated in [132]. To address these issues, the floating inverter amplifier (FIA) was first proposed for use in a NS-SAR design by Tang in 2020 [91]. The amplifier, depicted in Fig. 26, consists of two inverters operating as a differential amplifier. A large reservoir capacitor is precharged and used as the power supply during amplification, allowing for floating operation, which directly solves the varying common mode and PVT sensitivity issues of the previous dynamic amplifier design. The initial NS-SAR design of [91] includes a two-stage FIA that achieves ideal 2nd-order noise shaping at low power consumption, reaching a FOM_{Sc} of 181.5 dB.

Many recent designs have adopted and improved upon this amplifier structure, achieving state-of-the-art FOM_{Sc} in excess of 180 dB, such as [20], [33], [37], [96], and [101]. Two key improvements are the use of correlated level shifting and dynamic body biasing, as proposed in [42], which enhance gain and swing while improving transconductance at the end of the amplification phase when the reservoir capacitor is nearly empty. Another significant enhancement is the introduction of an additional operation phase for thermal noise cancellation, as seen in [134]. Also, a dynamic biasing technique incorporating the swing-enhanced FIA is discussed in [135] and [136]. Tang also presents further improvements to his original design in [137]. Other designs using the FIA include [29], [47], [60], [102], [118], [138].

An extension of the dynamic amplifier concept involves altering different amplifier properties dynamically during the amplification phase. For instance, in [139], the concept of incomplete settling [140] is leveraged in a duty-cycled amplifier to control the circuit's gain. The final implementation also includes a power efficient switched biasing circuit. In [84], a multiphase settling technique is introduced that toggles an output resistor on and off during amplification. This method enables a better balance between noise, gain sensitivity, and power efficiency. Similarly, in [45], a segmented integration technique is employed to achieve the same goal. This approach uses two different amplifiers: first, a high slew rate inverter-based amplifier, followed by a low-noise differential pair to complete the integration.

B. NOISE MITIGATION TRENDS

Most oversampling ADC designs are limited by thermal noise, i.e. the majority of the noise budget is allocated to thermal noise, with quantization noise kept relatively small.

This approach is preferable for power efficiency because reducing quantization noise requires less power compared to reducing kT/C noise, which would involve using large capacitors, thereby heavily loading amplifiers and driving circuits. Consequently, circuit design techniques that can help reduce thermal noise efficiently, aside from resorting to large capacitors, are highly sought after for improving SNR at low power.

1) FLICKER NOISE

Flicker noise could be a significant noise source if not addressed properly. However, since it is confined to low frequencies, it can be effectively managed using well-established offset-cancellation techniques such as chopping [141] and auto-zeroing [142]. In CT $\Delta\Sigma$ modulators, however, chopping tends to introduce quantization noise aliasing into the signal, degrading performance [143]. This issue is addressed in [144], where a chopping artifact rejection technique is introduced by setting the chopping frequency to match the sampling frequency.

2) NOISE CANCELLATION

A common approach to reduce thermal noise in circuits is to use noise cancellation [145]. The principle of operation involves sampling the kT/C noise on a capacitor, then subtracting it from the signal path during circuit operation via a switched-capacitor network. Multiple variations of this approach are used in recent oversampling ADC design [20], [47], [134], [146], [147].

For instance, in [134], an additional phase is added to the FIA to allow sampling noise cancellation (SNC), as shown in Fig. 27. The additional capacitors C_{SNC} and switches used for SNC are shown in red. At the end of the sampling phase, the FIA is activated to sample the amplified input change with the sampling noise on C_{SNC}. When the sampling phase ends, the charge transfer begins for both the main sampling capacitor C_S and C_{SNC}. The sampling noise stored on both of these capacitors cancels itself when the charges are transferred to the integrating capacitor C_I. The capacitor ratio between C_S and C_{SNC} must match the amplifier gain for perfect noise cancellation during charge transfer. Hence, some smaller residual thermal noise is expected with the inevitable process mismatches. The thermal noise introduced by the additional circuitry is reduced by a factor of the amplifier's gain, preventing it from degrading performance.

3) MAJORITY VOTING

Another technique introduced in [148] to reduce thermal noise in the NS-SAR quantizer is majority voting. The idea is to repeat one or more of the least significant bit (LSB) comparisons multiple times and take the majority output. This allows for a significant reduction in thermal noise, thus relaxing design constraints. The idea is further optimised in the same work by applying the majority voting technique in a data-dependent manner. The majority voting technique

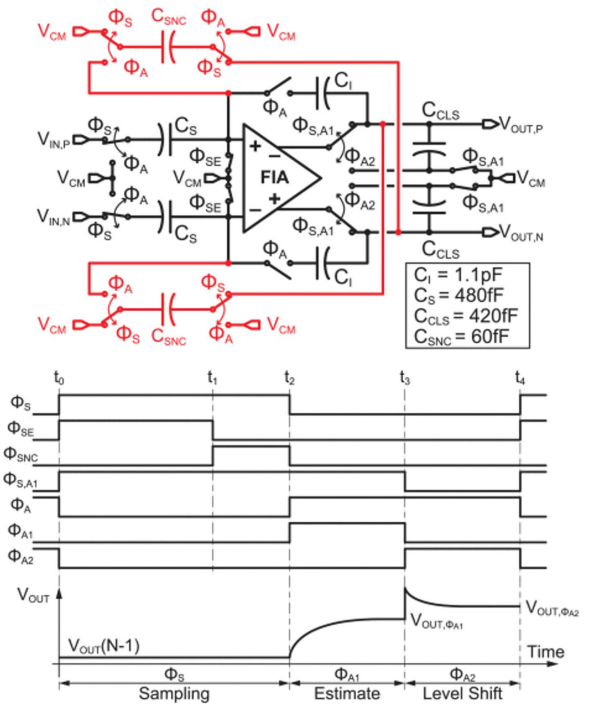

FIGURE 27. Noise cancellation circuit inside a FIA-based loop filter with timing diagram. Reprinted from [134], © 2023 Matsuoka et al., CC BY 4.0.

is only applied when the noise is at a critical level for the SAR comparator. Since the impact of noise depends on the input level, a detector circuit determines when noise becomes critical and majority voting should be applied. Otherwise, power is saved by turning off majority voting.

In [149], the same concept is applied, but only to the LSB, using simplified logic and a digital-friendly circuit that doesn't require an error detector. The drawback is a less efficient implementation of the technique. In [89], an improved tri-level majority voting scheme is introduced by exploiting more information from the comparator and providing an extra decision level. Finally, the technique is used with an 8-fold LSB repetition in [30], where the ADC achieves FOM_{Sc} of 182.2 dB.

C. DAC MISMATCH COMPENSATION DESIGN TRENDS

Mismatch and non-idealities in the feedback DAC are among the most critical limitations of $\Delta\Sigma$ ADC. Since the error correction loop does not shape errors originating in the feedback path, the DAC must be at least as linear as the overall ADC requirements. When high precision is needed, the DAC often becomes the bottleneck because the matching accuracy of the fabrication process is unable to meet the required specifications. Techniques such as laser trimming can be used to improve DAC matching, but at a very significant cost.

1) CALIBRATION

A widely used solution to address the DAC mismatch issue is digital foreground calibration. Foreground calibration occurs while the ADC is not running, either at start-up or in periodic

breaks during operation. This technique uses a lookup table (LUT) encompassing the nonlinear response of the DAC, in order to correct the modulator output as shown in Fig. 28. The LUT can initially be populated by reorganizing the ADC circuit blocks [147], [150], [151], necessitating additional circuitry. Simpler implementations can be realized through the application of a spectrally pure sinusoidal input [152], [153]. However, generating such an input signal on-chip for periodic calibration poses a difficult challenge. To address this conundrum, an alternative implementation using an out-of-band tone was proposed in [154]. An alternative foreground calibration technique is presented in [94] in which a least mean squares filter is used to minimise the impact of quantization noise on mismatch error extraction, simplifying the calibration circuitry and enhancing robustness to process, voltage and temperature variations.

Another approach is the analog calibration of the unit elements of the DAC to improve matching and linearity. An example of this method is presented in [55], where a current-steering DAC has its unit current sources periodically calibrated against a reference, an idea adapted from [155].

2) INHERENTLY LINEAR DAC

To alleviate the need for additional calibration circuitry, a very simple technique to achieve high linearity in the DAC feedback is to use a 1-bit quantizer and a 1-bit DAC. In a 1-bit modulator, only two quantization levels exist, forcing the system to remain perfectly linear after implementation, regardless of how the quantization levels vary with respect to one another. Several design examples leveraging this property are proposed in [37], [64], [75], [135]. However, a 1-bit system is not without its own limitations: higher quantization noise, reduced maximum stable amplitude of the modulator, and increased sensitivity to jitter and DAC waveforms in CT implementations. To avoid renouncing the benefits of multilevel quantization, inherently linear DAC topologies have been proposed. Notably, a DAC architecture where every element is used for each level generation keeps the output linear even with mismatch, as proposed in a 5-level version in [156] and a 13-level version in [157]. A tri-level inherently linear DAC in a SMASH architecture is also proposed in [77]. Finally, a segmentation technique to improve DAC linearity and achievable SNDR is proposed in [158].

3) CONTINUOUS-TIME MODULATOR

CT $\Delta\Sigma$ modulators are particularly sensitive to DAC non-idealities because jitter and waveform symmetry also deteriorate the modulator's performance. Consequently, research on DAC mismatch mitigation has accorded importance to this topology. One widely used technique is to insert a FIR filter before the DAC to smooth out sharp transitions. With smaller transition steps, the DAC becomes less sensitive to jitter since any temporal fluctuation causes a smaller voltage error in the integrator. A differential resetting scheme with a FIR filter

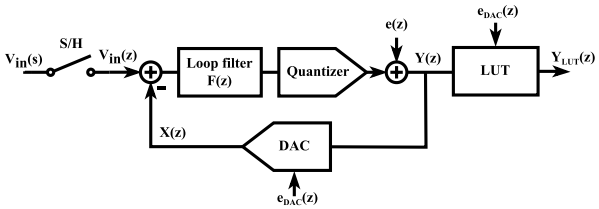

FIGURE 28. Block diagram of the foreground digital calibration of the DAC errors.

DAC is introduced in [121] to improve jitter robustness and DAC linearity. The zap-switch technique is also proposed in [119] with a return-to-open FIR filter DAC to address ISI and transition waveform sensitivity.

4) MISMATCH ERROR SHAPING

Another elegant technique to address the stringent DAC linearity constraint is mismatch error shaping (MES). MES techniques introduce noise shaping to DAC mismatch and nonlinearity in order to diminish their impact on ADC performance. A straightforward approach to achieving this mismatch noise shaping is to shuffle the DAC unit elements for each sample. Indeed, due to mismatch, each DAC element presents a small error relative to the others. Shuffling the DAC elements averages their weight errors over the multiple samples used in the conversion process, by virtue of the strong low-pass filtering provided by the decimation filter. The simplest and most widely used element shuffling scheme is data weight averaging (DWA) [159]. This technique involves rotating the usage of each DAC element in sequence, analogously to a barrel shifter, resulting in 1st-order mismatch shaping.

A limitation of DWA lies in that the simple rotation of DAC elements is highly deterministic, which inevitably introduces spurs in the output spectrum [5]. To mitigate this issue, other element rotation schemes have been proposed to introduce randomness to the element selection algorithm, limiting the spurs but also MES effectiveness. For instance, bidirectional DWA [160] alternating rotation direction or butterfly shuffling [161], a scheme based on the butterfly operation of the fast Fourier transform (FFT), were proposed. In recent state-of-the-art designs, many top-performing ADC leverage DWA or other element shuffling techniques to improve DAC linearity [32], [34], [36], [38], [40].

DAC element shuffling, while attractively simple, merely provides 1st-order MES. An alternate technique is to add a mismatch error feedback, similar to $\Delta\Sigma$ modulation, to allow MES by an arbitrary function. Early works proposed vector-based DAC element selection logic, which included mismatch error feedback with filtering [5], [162]. With this method, selecting a higher-order filter enables achieving arbitrarily high-order MES, albeit at the cost of increased circuit complexity. For instance, a second-order implementation is detailed in [163], where the vector element selection logic is realized with a partial sorter within a slightly modified architecture that requires an

additional filter. In another work, Sun and Cao [164] proposed a novel vector-based MES architecture without the extra filter, enhancing hardware efficiency, MES, and stability performance. More recently, an implementation of vector-based MES in a CT ΔΣ modulator further improves the robustness of Sun's architecture by adding a compensation scheme to the partial sorter [165].

Lately, a similar technique based on subtracting the mismatch error of the previous sample to the current conversion sample to enable 1st-order MES was proposed in [166]. The technique is reused, along with DWA, in [167] to achieve a calibration-free ADC, as the improved linearity from MES is sufficient to meet system requirements. Another design presented in [92] adapts the technique to achieve 2nd-order mismatch shaping [168], reaching SNDR above 90 dB without any calibration.

D. INPUT SWING OPTIMIZATION DESIGN TRENDS

The choice of input swing for an ADC can have a significant impact on the overall performance of the system. Most designs typically make use of the full range of the supplied voltage. However, adjusting the input swing, whether upward or downward, may present notable design trade-offs.

1) BOOSTING THE INPUT SWING

In the surveyed state-of-the-art designs, only two opted to boost the input swing to a value greater than that of the supply voltage. The rationale for maximizing input swing is to enhance SNR without power overhead or, conversely, to decrease power consumption for a given SNR. By increasing the input swing for the same supply voltage, power efficiency is enhanced because it relaxes the noise constraints for a specific SNR specification, given the higher input signal. This allows for smaller thermal noise mitigation capacitors, reducing amplifier loading and consequently lowering power consumption. In contrast, increasing the supply voltage to achieve a higher input swing is not beneficial, as power consumption rises at the same rate as the increased SNR.

This technique is very effective, as evidenced by the design by Hsieh and Hsieh [31] with the top FOM_{Sc}, as discussed in detail in section V-E5. This design is exceptionally power-efficient, featuring a doubled SAR input stage that enables twice the input swing. The other design to boost the input range is Prochet's TD ΔΣ design [114]. It features a CCO-based loop filter with a novel feedforward path that helps linearize the CCO and eliminates the need for an additional DAC. The input swing is increased by raising the DAC reference voltage from the 0.8 V supply to 1.2 V, resulting in a 1.8 V_{pp} differential input swing. The boosted input swing improves SNDR by 2 dB with minimal power penalty, contributing to the design achieving the highest SNDR for a TD ΔΣ at 92 dB.

2) REDUCING THE INPUT SWING

The main drawback of boosting the input swing is that the ADC becomes more difficult to drive. The input buffer feeding into the ADC must be highly linear to avoid distorting the input signal, often requiring a supply voltage higher than the desired swing, leading to substantial power consumption. Therefore, keeping the swing low makes the ADC easier to drive, which can simplify input buffer circuitry and save power. An example of a design following this approach is Lim's CT ΔΣ ADC [144]. This design leverages a capacitively coupled instrumentation amplifier (CCIA) as an in-loop input buffer with high input impedance, as illustrated in Fig. 29. With its 1.8 V supply, it features a 60 mV_{pp} input swing, which can be directly driven by most sensors. This is highly attractive since additional off-chip input amplifiers could easily exceed the power consumption of the entire ADC.

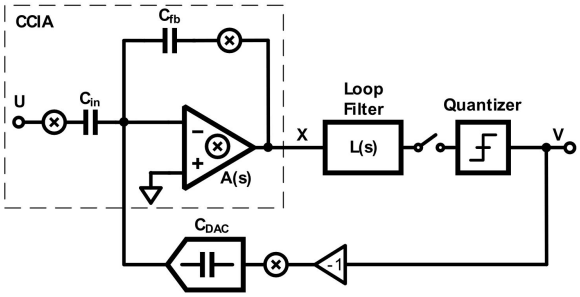

FIGURE 29. Capacitively coupled instrumentation amplifier reducing the input driving requirements of the CT ΔΣ ADC. Reprinted from [144], © 2021 IEEE.

Another design, described in [111], presents a 300 mV_{pp} input swing in a 1 V supply ADC. Here, the design utilizes a TD quantizer with a G_mC loop filter. The G_m amplifier is used directly as the input, providing a high impedance, easy-to-drive terminal. Linearity is improved over the 300 mV input range using an innovative resistive feedback DAC at the source terminal of the input differential pair.

A final example can be found in [61], where an input impedance boosting technique is introduced for the DT loop filter. To minimize charge transfer in the switched-capacitor filter, the sampling capacitor is precharged with the previous output of the modulator just before the sampling phase. Since both voltage values are very similar, charge transfer is minimal, and the input impedance remains high. The input swing for this input stage is 600 mV_{pp} on a 1.3 V supply, and the input impedance reaches several MΩ, allowing for easy drivability.

E. SILICON AREA MINIMIZATION DESIGN TRENDS

The active silicon area of an ADC design is of crucial importance due to its direct impact on cost. In semiconductor foundries, variable costs are mostly proportional to the number of silicon wafers produced. A larger die size will obviously result in a greater unit cost, which can have a very substantial incidence on viability at large-scale production. Hence, in order to maintain market competitiveness, it is essential to employ design techniques that minimize silicon area. This section focuses on the most area-efficient designs

across various technology nodes. Because designs in newer technology nodes are inherently smaller than those in older nodes, comparisons are segregated across technology node sizes.

1) EFFICIENT USE OF HARDWARE

Many designs in the reviewed works leverage hardware sharing to maximize the utilization of on-chip resources. For instance, Zhang et al. [27] introduces one of the smallest surveyed designs, featuring an NS-SAR with a hybrid EF-CIFF feedback path that reuses the same passive integrator for both paths. This design occupies a mere 0.012 mm^2 in a 28 nm technology node. Similarly, another NS-SAR design [90] incorporates a recycling integrator that reuses the same OTA to implement a 2nd-order loop filter, minimizing the area.

Other designs simply employ clever techniques to enhance hardware efficiency. Capacitors, particularly precise ones used in signal paths (e.g., metal-insulator-metal capacitors), tend to occupy significant chip area. To reduce the number of required capacitors, the DT $\Delta\Sigma$ design in [124] uses a buffer and a switching network to store the offset voltage of the integrator amplifier, eliminating the need for the usual auto-zero capacitor and significantly reducing area. Hwang et al. [125] introduces a highly efficient inverter-based amplifier with a self-biasing scheme, reducing the entire amplifier design, including biasing, to just four transistors, along with a few switches and small capacitors. Finally, the novel CT NS-SAR design proposed in [93] and discussed in section V-C3 achieves the smallest surveyed design implemented in a 65 nm node, thanks to its efficient NS-SAR structure with a simple 1st-order loop filter.

2) HIGHLY DIGITAL ARCHITECTURES

Digital circuits are known for their ability to maintain a small area. Processing signals in the digital domain eliminates thermal noise constraints, thereby reducing the need for bulky capacitors. Transistors can also be smaller since no amplifier cells with stringent bandwidth and transconductance requirements are necessary. The topology that maximizes this principle is the TD $\Delta\Sigma$ modulator, which processes signals in the time domain. For instance, the TD $\Delta\Sigma$ discussed in [107], [111], and [112] are among the top three smallest implementations in their respective technologies. Both [111] and [112] utilize a digital-like ring oscillator with a digital phase detector, while [107] employs a highly digital triangular CCO based on a switched capacitor bank.

Another example of a highly digital structure is the coarse stage of the zoom design by Jie et al. [100]. This stage is implemented entirely digitally, utilizing an innovative counter structure based on the digital output of the fine stage. This design is one of the smallest reported, occupying just 0.014 mm^2 in a 28 nm technology node.

3) NOISE MANAGEMENT TECHNIQUES

As previously mentioned, a common solution to reduce thermal noise is to make use of large sampling capacitors, which decrease the kT/C ratio. However, large capacitors necessarily occupy significant area. To alleviate this trade-off, kT/C mitigation techniques discussed in section VI-B can be employed. Another approach used in two of the smallest NS-SAR implementations [19], [28] is to incorporate a dynamic amplifier before the passive filter in the NS-SAR feedback loop. This setup reduces the noise sampled on the filter by a factor proportional to the amplifier's gain, significantly decreasing the required capacitor sizes. In fact, [28] is the smallest of all the surveyed designs with an impressive active area of only 0.0049 mm^2 in a 28 nm node.

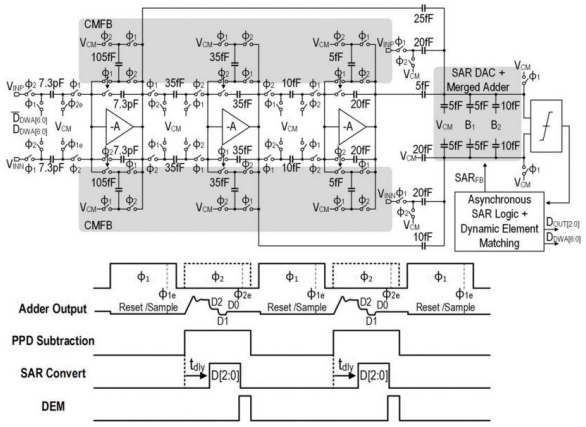

FIGURE 30. Area- and power-efficient 3rd-order DT $\Delta\Sigma$ ADC leveraging pseudo-pseudo-differential amplifiers. Reprinted from [36], © 2022 IEEE.

Another interesting technique used in Lee's design [36] with the second highest FOM_{Sc} is the use of pseudo-pseudo-differential amplifiers. These amplifiers are single-ended but coupled with switches to process signals differentially. One advantage of this approach is the simpler amplifier structure and the inherent flicker noise cancellation, allowing for significant area reduction. The DT $\Delta\Sigma$ design use three of these amplifiers for its 3rd-order loop filter, as illustrated in Fig. 30, yet it remains the smallest implementation in a 180 nm node, occupying only 0.0375 mm^2.

F. PROCESS SCALING MITIGATION DESIGN TRENDS

Recent deep submicron technology nodes are highly power-efficient and allow for packing more features into a smaller area than ever before, at least as far as digital circuits are concerned. Despite the benefits in the digital domain, analog circuits such as ADC are instead presented with significant challenges. On one hand, the reduced supply voltage rail complexifies design due to decreased headroom, making it harder to maintain transistor stacks in the saturation region. On the other hand, reduced transistor length decreases output resistance, which limits gain and worsens matching. These issues are particularly critical in SoC design, where ADC are to be integrated with microprocessors for digital signal processing. The microprocessor is usually the main driver of the choice of a smaller technology node, which forces the ADC to be implemented in the same.

1) AMPLIFIER DESIGN

The primary component affected by technology scaling is the amplifier, where reduced supply voltage becomes a significant challenge. To address this, pseudo-differential amplifiers are often employed. These amplifiers eliminate the tail current source from the differential amplifier, thereby reducing the transistor stack. This approach is commonly seen in inverter-based amplifiers [97], [123], [124]. Inverter-based amplifiers are favored because they effectively double the available transconductance for the same bias current. However, a notable drawback of pseudo-differential amplifiers is the substantial reduction in power supply and common mode rejection ratio, as the branches of the amplifier no longer share the same current.

Similarly, pseudo-pseudo-differential amplifiers, which use the same single-ended amplifier for differential signal processing with alternate clocking, can be employed to reduce the transistor stack and simplify the circuitry [104]. The designs in [36] and [44] also propose pseudo-pseudo-differential amplifiers, but they utilize a ring amplifier as the single-ended amplifier core. This approach makes the circuit even more scaling-friendly, as the ring amplifier presents a predominantly digital structure.

Simple loop filter structures, such as passive and buffer-based filters, limit the need for amplifiers and are also well-suited for digital-friendly, smaller technology nodes. These loop filter structures are covered in section VI-A4, where detailed implementation information is provided.

2) THE TD $\Delta\Sigma$ TOPOLOGY

Another trend particularly well suited for tackling the challenges posed by smaller technology nodes is the TD $\Delta\Sigma$ architecture. Processing information in the time domain allows for the use of digital-like circuitry, which scales effectively with advancing technologies. Additionally, the precision of time domain circuitry improves for smaller technology nodes due to reduced transition times. A prime example of such a design is presented in [115], where a VCO-based $\Delta\Sigma$ modulator is fully synthesized using hardware description language (HDL). The standard cell library is augmented with a few analog cells to facilitate the implementation of the mostly digital architecture. This design, implemented in 28 nm, can be more easily scaled to a smaller node than other designs by reusing the same HDL code and modifying the custom analog cells. Design examples that process information entirely in the time domain are covered in detail in section V-E3.

VII. DISCUSSION

The design trends highlighted in this survey demonstrate the vast diversity and depth of possibilities in oversampling ADC design. A multitude of techniques are suited to achieve varied performance metrics, providing great flexibility in design choices. For instance, NS-SAR ADC excel at achieving outstanding power efficiency for moderate SNDR, while zoom ADC are unmatched for low bandwidth applications requiring very high precision. CT and DT $\Delta\Sigma$ ADC offer a more balanced package, enabling a wide range of performance trade-offs. In any topology, meticulous circuit-level design incorporating efficient loop filters, DAC linearization techniques, and thermal noise mitigation is crucial to achieve cutting-edge performance.

Navigating the diverse, intricate oversampling ADC architectures and implementations can be overwhelming. How does one select the most suitable ADC architecture and implementation parameters for their specific SoC requirements? A method that is applicable on a heterogenous subset of oversampling ADC topologies is to simply compare designs based on a quantitative figure of merit such as FOM_{Sc}. Indeed, FOM_{Sc} captures the essential trade-off between bandwidth, power, and SNDR, which are clearly illustrated by the trendlines in Figures 10 and 11. However, reducing the discussion to only three main performance characteristics may lead to a skewed assessment that overlooks critical elements for SoC implementation.

In research literature, oversampling ADC designs overwhelmingly exclude discussion of the crucial output decimation filter, which is typically implemented off-chip and thus not reflected in the disclosed ADC performance metrics. This omission is of particular significance because common foreground calibration methods used to improve DAC linearity (also often performed off-chip themselves) exacerbate the requirements of the decimation filter, due to an increased signal bit width to handle, all without adverse consequence in terms of FOM. On the contrary, on-chip MES techniques are unfairly penalized in published ADC performance metrics. Indeed, the additional power and area required by on-chip MES are included in the evaluation metrics, whereas the resulting streamlining of the off-chip decimation filter and calibration is not. Similarly, incremental $\Delta\Sigma$ ADC that utilize FIR-based decimation filters, which are simpler and consume less power, do not see these benefits reflected in the FOM when decimation is performed off-chip. In a practical scenario, all components of a SoC must obviously be present on-chip, including the decimation filter and the calibration circuits.

The input driving circuit of the ADC is another element often realized off-chip and thus overlooked in FOM calculations, but that is needed in a practical system. Indeed, most designs in literature do not explicitly include an input buffer amplifier, which would need to be as linear and low in noise as the ADC itself in order to meet requirements, resulting in stringent design constraints and requiring higher power rails than the ADC itself. For the rare designs that include an on-chip buffer, such as [167] and [169], its power consumption ends up being significantly higher than the rest of the entire ADC! CT $\Delta\Sigma$ designs, due to their resistive input impedance and inherent anti-aliasing properties, can relax the input front-end requirements. Certainly, conventional FOM are unable to account for these differences when the input buffer is located off-chip.

An interesting discussion on the topic was initiated by Nauta [170] in the latest ISSCC proceedings. Among other points, he explores the simple case of an amplifier driving a capacitive load representing a basic analog signal processing circuit, in an ADC for example, with a specified SNR requirement. In this scenario, it is shown that the minimal analog power consumption is:

$$P_{min} = \frac{V_{dd}}{V_s} \cdot 8 \cdot k \cdot T \cdot SNR \cdot f, \tag{14}$$

where V_{dd} is the supply voltage, V_s the input swing, k the Boltzmann constant, T the absolute temperature and f the signal frequency. It becomes apparent that a wider input swing V_s relative to supply voltage V_{dd} is beneficial for achieving lower ADC power consumption for a given SNR, thereby improving FOM_{Sc}. However, when the complex and power-hungry input buffer needed to handle a wider input swing is located off-chip, its own impact on total power consumption remains unaccounted for in FOM calculations. Therefore, Nauta proposes introducing a correction factor to FOM_{Sc} as follows:

$$FOM_{Sc+Bu} = FOM_{Sc} + 10 \log \frac{V_{dd}}{V_s}. \tag{15}$$

This modified FOM credits designs for having a smaller input swing, as it should allow for relaxing the specifications of the input buffer, hence decreasing net aggregate system power consumption.

Another factor that remains completely left out by the habitual FOM is the cost effectiveness of the design under consideration. Even so, total implementation cost, which is a function of the semiconductor technology used and of the area footprint of the design, should be of the utmost importance in practice. Indeed, designs implemented using recent technology nodes and occupying large silicon areas may involve a significantly high production cost, making them impractical for most mass-market applications.

To quantify cost effectiveness, it is reasonable to expect that it be proportional to the area of the active design. However, different technology nodes involve different cost scales, depending on their minimum feature size. For illustrative purposes, we propose a cost effectiveness factor (CEF) to be defined as

$$CEF = \frac{A}{tech^2}, \tag{16}$$

where A is the active design area (in μm^2) and $tech$ the technology node critical dimension (in μm). We apply this correction factor to FOM_{Sc} after having normalized it to the average of all designs in the study set to yield:

$$FOM_{Sc+Ar} = FOM_{Sc} - 10 \log(CEF / \overline{CEF}). \tag{17}$$

This adjusted FOM penalizes designs presenting a less area-effective realization while rewarding designs that are likely to offer a cost advantage. It is worthy of mention that CEF as presented is neither intended as absolute nor definitive, but rather as a starting point on an indicative basis for taking into account design cost effectiveness. Indeed, the effects of technology scaling can often manifest in a varied and non-linear manner (e.g., different circuit component types may scale differently across technology nodes, distinct technologies may force the use of different techniques). Furthermore, CEF aims to assess the cost effectiveness of a *design*, not of a specific *implementation*. In other words, FOM_{Sc+Ar} would penalize a design requiring more area than a competitor implemented in the same technology. Ultimately, designers may be interested in such a metric to help them choose a suitable design topology, somewhat independently from the technology node selection. Certainly, any quality metric can only ever be as good as the integrity of its constituent data. For instance, the placement off- or on-chip of auxiliary components such as input buffers, calibration circuitry or decimation filters may cause dramatic and artificial FOM_{Sc+Ar} variation, as the footprint of these parts gets inconsistently counted or not in the total design area. Nevertheless, through careful data validation, some interesting trends can be discovered.

It is also possible to combine the two aforementioned adjustments to generate $FOM_{Sc+Bu+Ar}$ so as to quantify ADC performance while also taking into account the impact of the input buffer as well as the cost effectiveness of the implementation.

These alternative FOM are presented in Fig 31, where the designs are ranked in descending order of FOM_{Sc}. For some designs, the four proposed FOM do not vary substantially. However, other designs significantly benefit from either their low input swing or their area efficient implementation. For instance, Lim's design [144], by virtue of an input swing of only 60 mV, makes the input buffer design straightforward, which boosts its FOM_{Sc+Bu} by 17 dB. Kim's design [90] is very compact, occupying merely 0.12 mm^2 in a 180 nm node, which increases its FOM_{Sc+Ar} by 10 dB. Many designs benefit from their lower than average CEF, such as [64] and [125], or from both criteria, such as [108] and [111]. Interestingly, the top-FOM_{Sc} design by Hsieh and Hsieh [31], previously discussed in section V-E5, is penalized for its wide input swing of 2 V_{dd}, while the second-best FOM_{Sc} design by Lee and Moon [36] is highly area-efficient, surpassing Hsieh's design when using any of the three proposed corrected FOM. The fluctuation in top-ten ranking for the alternative FOM are highlighted in Table 1, showing that several of the highest ranking ADC by FOM_{Sc} are overtaken by other designs when widening the breadth of the FOM to take into account some overlooked parameters.

The top 10 designs for each of the four proposed FOM, as listed in Table 1, are further detailed in Fig. 32. This figure compares the bandwidth and precision performance of these leading designs, while also specifying their architecture and FOM values. It provides a complete overview so as to enable quick identification of the most suitable state-of-the-art designs based on combined precision, bandwidth, power and implementation efficiency requirements.

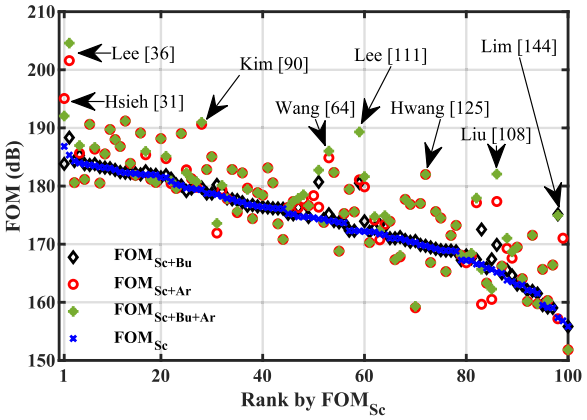

FIGURE 31. Four alternate FOM with different correction factors applied, ordered by FOM_{Sc} rank.

TABLE 1. Best oversampling ADC designs ranked according to various FOM. Blue (red) shading intensity is related to higher (lower) FOM_{Sc} rank for this subset.

Rank	FOM_{Sc}	FOM_{Sc+Bu}	FOM_{Sc+Ar}	$FOM_{Sc+Bu+Ar}$
1	Hsieh [31]	Lee [36]	Lee [36]	Lee [36]
2	Lee [36]	Chand. [32]	Hsieh [31]	Hsieh [31]
3	Cheng [33]	Cheng [33]	Liu [96]	Liu [96]
4	Chand. [32]	Hsieh [31]	Kim [90]	Kim [90]
5	Lo [34]	Guo [39]	Karm. [40]	Karm. [40]
6	Karm. [40]	Lo [34]	Eland [38]	Eland [38]
7	Guo [39]	Karm. [40]	Wang [20]	Lee [111]
8	Mond. [35]	Mond. [35]	Liu [28]	Wang [20]
9	Liu [37]	Liu [37]	Gönen [97]	Liu [28]
10	Eland [38]	Eland [38]	Chae [22]	Gönen [97]

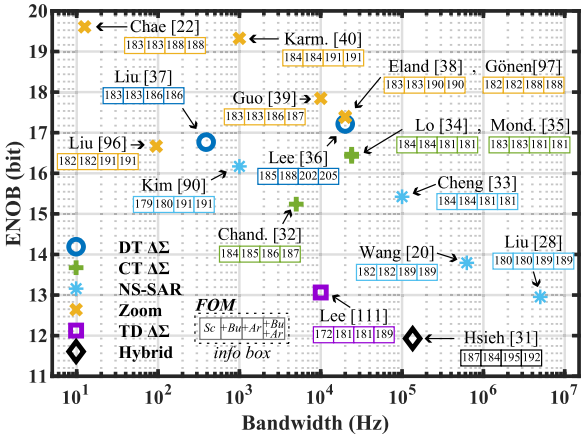

FIGURE 32. Bandwidth and precision performance of the top 10 designs for each FOM, as presented in Table 1. Numerical values for the different FOM are displayed in the info box accompanying each data point.

Although these extra correction factors applied to Schreier's FOM can be very beneficial to designers trying to thin out and select an ADC architecture best suitable for specific needs, there exists no such thing as a perfect FOM. Some applications might find a design with a poor FOM to be the most suitable for their specifications due to idiosyncratic characteristics such as input impedance, decimation filter simplicity, ease of input multiplexing, low latency, superior anti-aliasing, etc. These are all important factors that fail to be simply encompassed in a single FOM equation. Though extremely challenging, this is precisely what sets ADC design apart as such a rich and interesting discipline. Indeed, there can exist as many design possibilities as there can be circuit specification combinations, making custom design often the most appropriate solution.

VIII. CONCLUSION

To conclude, the use of oversampling and noise shaping allows for unparalleled design flexibility at high precision, making the broad family of oversampling ADC the best suited to achieving high SNDR, as has been clearly depicted in Fig. 1 and 10. In the years to come, it appears likely that a promising trend would be innovation focusing holistically on full SoC implementation. With recent technology nodes, digital signal processing is becoming increasingly power-efficient, especially at high precision, since kT/C constraints do not apply in the digital domain. SoC-based ADC are poised to benefit from digitizing the signal as early as possible in the signal chain, with an input swing dictated by the application, thereby reducing the need for a resource-intensive input buffer amplifier. While research projects understandably often focus on specific issues like improving modulator efficiency, it would be refreshing to see systemic innovations targeting the entire signal chain from input front-end to decimation filter.

Digital structures such as the TD $\Delta\Sigma$ topology will most likely play a predominant role in future designs as they scale better with technology and offer more headroom for power efficiency improvement. The main challenge to tackle will be to develop new techniques to linearize the time-domain processing circuit blocks. Dynamic circuits, such as FIA for loop filters, are a well-established trend that will surely continue to evolve, as many of the most power-efficient ADC ever designed incorporate this approach. Exciting and intriguing multi-loop structures combining different topologies are also expected to emerge, leveraging the strengths of multiple structures to achieve varied design trade-offs. One thing is clear: oversampling ADC shall remain unavoidable in high-precision, high-performance data conversion for many years to come.

REFERENCES

[1] C. B. Brahm, "Feedback integrating system," U.S. Patent 3 192 371, Jun. 29, 1965.

[2] H. Inose, Y. Yasuda, and J. Murakami, "A telemetering system by code modulation—Δ – Σ modulation," *IRE Trans. Space Electron. Telemetry*, vol. SET-8, no. 3, pp. 204–209, Sep. 1962.

[3] B. Razavi, "The delta-sigma modulator [a circuit for all seasons]," *IEEE Solid StateCircuits Mag.*, vol. 8, no. 2, pp. 10–15, Jun. 2016.

[4] B. Murmann. *ADC Performance Survey 1997–2023*. Accessed: Apr. 26, 2024. [Online]. Available: https://github.com/bmurmann/ADC-survey

[5] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Hoboken, NJ, USA: Wiley, 2017.

[6] J. M. de la Rosa, R. Schreier, K.-P. Pun, and S. Pavan, "Next-generation delta-sigma converters: Trends and perspectives," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 4, pp. 484–499, Dec. 2015.

[7] J. M. de la Rosa, "Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 1–21, Jan. 2011.

[8] Z. Tan, C.-H. Chen, Y. Chae, and G. C. Temes, "Incremental delta-sigma ADCs: A tutorial review," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 4161–4173, Dec. 2020.

[9] P. A. H. Vardhini and M. L. Makkena, "Design and comparative analysis of on-chip sigma delta ADC for signal processing applications," *Int. J. Speech Technol.*, vol. 24, no. 2, pp. 401–407, Jun. 2021.

[10] M. J. M. Pelgrom, *Analog-to-Digital Conversion*. Cham, Switzerland: Springer, 2013.

[11] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*. Hoboken, NJ, USA: Wiley, 2010.

[12] R. van de Plassche, "A sigma-delta modulator as an A/D converter," *IEEE Trans. Circuits Syst.*, vol. CS-25, no. 7, pp. 510–514, Jul. 1978.

[13] J. Robert, G. C. Temes, V. Valencic, R. Dessoulavy, and P. Deval, "A 16-bit low-voltage CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 2, pp. 157–163, Apr. 1987.

[14] J. Markus, J. Silva, and G. Temes, "Theory and applications of incremental $\Delta\Sigma$ converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 4, pp. 678–690, Jun. 2004.

[15] J. Steensgaard, Z. Zhang, W. Yu, A. Sarhegyi, L. Lucchese, D.-I. Kim, and G. C. Temes, "Noise–power optimization of incremental data converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 5, pp. 1289–1296, Jun. 2008.

[16] T. C. Caldwell and D. A. Johns, "Incremental data converters at low oversampling ratios," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 7, pp. 1525–1537, Jul. 2010.

[17] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, Dec. 2012.

[18] L. Jie, X. Tang, J. Liu, L. Shen, S. Li, N. Sun, and M. P. Flynn, "An overview of noise-shaping SAR ADC: From fundamentals to the frontier," *IEEE Open J. Solid-State Circuits Soc.*, vol. 1, pp. 149–161, 2021.

[19] S. Li, B. Qiao, M. Gandara, D. Z. Pan, and N. Sun, "A 13-ENOB second-order noise-shaping SAR ADC realizing optimized NTF zeros using the error-feedback structure," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3484–3496, Dec. 2018.

[20] T.-H. Wang, R. Wu, V. Gupta, X. Tang, and S. Li, "A 13.8-ENOB fully dynamic third-order noise-shaping SAR ADC in a single-amplifier EF-CIFF structure with hardware-reusing kT/C noise cancellation," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3668–3680, Dec. 2021.

[21] K. Souri and K. A. A. Makinwa, "A 0.12 mm^2 7.4 μW micropower temperature sensor with an inaccuracy of $\pm$0.2 °C (3 σ) from $-$30 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1693–1700, May 2011.

[22] Y. Chae, K. Souri, and K. A. A. Makinwa, "A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV offset," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3019–3027, Dec. 2013.

[23] S. Rao, K. Reddy, B. Young, and P. K. Hanumolu, "A deterministic digital background calibration technique for VCO-based ADCs," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 950–960, Apr. 2014.

[24] Y. Zhong and N. Sun, "A survey of voltage-controlled-oscillator-based $\Delta\Sigma$ ADCs," *Tsinghua Sci. Technol.*, vol. 27, no. 3, pp. 472–480, Jun. 2022.

[25] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

[26] R. H. Walden, "Analog-to-digital converter technology comparison," in *Proc. IEEE GaAs IC Symp.*, Oct. 1994, pp. 217–219.

[27] H. Zhang, X. Wang, N. Li, Z. Jiao, L. Chen, D. Mu, J. Zhang, and H. Zhang, "A 2.5-MHz BW, 75-dB SNDR noise-shaping SAR ADC with a 1st-order hybrid EF-CIFF structure assisted by unity-gain buffer," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 12, pp. 1928–1932, Dec. 2022.

[28] C.-C. Liu and M.-C. Huang, "A 0.46 mW 5 MHz-BW 79.7 dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 466–467.

[29] T. Xie, T.-H. Wang, Z. Liu, and S. Li, "An 84-dB-SNDR low-OSR fourth-order noise-shaping SAR with an FIA-assisted EF-CRFF structure and noise-mitigated push-pull buffer-in-loop technique," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3804–3815, Dec. 2022.

[30] Z. Jiao, H. Luo, J. Zhang, X. Wang, L. Chen, and H. Zhang, "An 84 dB-SNDR 1–0 quasi-MASH NS SAR with LSB repeating and 12-bit bridge-crossing segmented CDAC," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2023, pp. 1–2.

[31] S.-E. Hsieh and C.-C. Hsieh, "A 0.4-V 13-bit 270-kS/s SAR-ISDM ADC with opamp-less time-domain integrator," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1648–1656, Jun. 2019.

[32] H. Chandrakumar and D. Markovic, "A 15.2-ENOB 5-kHz BW 4.5-μW chopped CT $\Delta\Sigma$-ADC for artifact-tolerant neural recording front ends," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3470–3483, Aug. 2018.

[33] K.-C. Cheng, S.-J. Chang, C.-C. Chen, and S.-H. Hung, "A 94.3 dB SNDR 184 dB FoMs 4$^{\text{th}}$-order noise-shaping SAR ADC with dynamic-amplifier-assisted cascaded integrator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 180–182.

[34] C. Lo, J. Lee, Y. Lim, Y. Yoon, H. Hwang, J. Lee, M. Choi, M. Lee, S. Oh, and J. Lee, "A 116μW 104.4 dB-DR 100.6 dB-SNDR CT $\Delta\Sigma$ audio ADC using tri-level current-steering DAC with gate-leakage compensated off-transistor-based bias noise filter," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 164–166.

[35] S. Mondal, O. Ghadami, and D. A. Hall, "A 139μW 104.8 dB-DR 24 kHz-BW CT $\Delta\Sigma$M with chopped AC-coupled OTA-stacking and FIR DACs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 166–168.

[36] C. Y. Lee and U.-K. Moon, "A 0.0375 mm^2 203.5μW 108.8 dB DR DT single-loop DSM audio ADC using a single-ended ring-amplifier-based integrator in 180 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 412–414.

[37] L. Liu, Z. Qin, J. Yin, X. Liao, and Y. Tian, "A 16.8-ENOB, 3.5-μW fourth-order discrete-time delta-sigma ADC for biosignal acquisition applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 71, no. 4, pp. 1749–1753, Apr. 2024.

[38] E. Eland, S. Karmakar, B. Gönen, R. van Veldhoven, and K. A. A. Makinwa, "A 440-μW, 109.8-dB DR, 106.5-dB SNDR discrete-time zoom ADC with a 20-kHz BW," *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1207–1215, Apr. 2021.

[39] Y. Guo, J. Jin, X. Liu, and J. Zhou, "A 372 μW 10 kHz-BW 109.2 dB-SNDR nested delta-sigma modulator using hysteresis-comparison MSB-pass quantization," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2554–2563, May 2023.

[40] S. Karmakar, B. Gönen, F. Sebastiano, R. van Veldhoven, and K. A. A. Makinwa, "A 280μW dynamic zoom ADC with 120 dB DR and 118 dB SNDR in 1 kHz BW," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3497–3507, Dec. 2018.

[41] T. Hayashi, Y. Inabe, K. Uchimura, and T. Kimura, "A multistage delta-sigma modulator without double integration loop," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1986, pp. 182–183.

[42] L. Meng, Y. Hu, Y. Zhao, W. Qu, L. Ye, M. Zhao, and Z. Tan, "A 1.2-V 2.87-μ W 94.0-dB SNDR discrete-time 2–0 MASH delta-sigma ADC," *IEEE J. Solid-State Circuits*, vol. 58, no. 6, pp. 1636–1645, Nov. 2023.

[43] J.-S. Huang, S.-C. Kuo, and C.-H. Chen, "A multistep multistage fifth-order incremental delta sigma analog-to-digital converter for sensor interfaces," *IEEE J. Solid-State Circuits*, vol. 58, no. 10, pp. 2733–2744, May 2023.

[44] C. Y. Lee, P. K. Venkatachala, A. ElShater, and U.-K. Moon, "A pseudo-pseudo-differential ADC achieving 105 dB SNDR in 10 kHz bandwidth using ring amplifier based integrators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 7, pp. 2327–2331, Jul. 2021.

[45] S.-H. Liao and J.-T. Wu, "A 1-V 175-μW 94.6-dB SNDR 25-kHz bandwidth delta-sigma modulator using segmented integration techniques," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2523–2531, Sep. 2019.

[46] M. Fukazawa, T. Oshima, M. Fujiwara, K. Tateyama, A. Ochi, R. Alsubaie, and T. Matsui, "A CT 2–2 MASH $\Delta\Sigma$ ADC with multi-rate LMS-based background calibration and input-insensitive quantization-error extraction," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 2943–2955, Oct. 2021.

[47] H. Zhang, N. Li, J. Wang, Z. Jiao, J. Zhang, X. Wang, and H. Zhang, "A 1.25-MHz-BW, 83-dB SNDR pipelined noise-shaping SAR ADC with MASH 2–2 structure and kT/C noise-cancellation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 10, pp. 3872–3876, May 2023.
[48] S. Oh, Y. Oh, J. Lee, K. Kim, S. Lee, J. Kim, and H. Chae, "An 85 dB DR 4 MHz BW pipelined noise-shaping SAR ADC with 1–2 MASH structure," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3424–3433, Nov. 2021.
[49] S. Tannirkulam Chandrasekaran, S. P. Bhanushali, S. Pietri, and A. Sanyal, "OTA-free 1–1 MASH ADC using fully passive noise-shaping SAR & VCO ADC," *IEEE J. Solid-State Circuits*, vol. 57, no. 4, pp. 1100–1111, Apr. 2022.
[50] M. Sadollahi and G. C. Temes, "A 10-MHz BW 77.9 dB SNDR DT MASH ΔΣ ADC with NC-VCO-based quantizer and OPAMP sharing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 9, pp. 3384–3392, Sep. 2019.
[51] H. Maghami, P. Payandehnia, H. Mirzaie, R. Zanbaghi, H. Zareie, J. Goins, S. Dey, K. Mayaram, and T. S. Fiez, "A highly linear OTA-less 1–1 MASH VCO-based ΔΣ ADC with an efficient phase quantization noise extraction technique," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 706–718, Mar. 2020.
[52] M. Honarparvar, J. M. de la Rosa, and M. Sawan, "A 10-MHz BW 77.3-dB SNDR 640-MS/s GRO-based CT MASH ΔΣ modulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 9, pp. 1519–1523, Sep. 2020.
[53] G. Tan, X. Qin, Y. Liu, M. Guo, S.-W. Sin, G. Wang, Y. Lian, and L. Qi, "A 10 MHz-BW 85 dB-DR CT 0–4 MASH delta-sigma modulator achieving +5 dBFS MSA," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 12, pp. 4781–4792, Dec. 2023.
[54] N. Maghari, S. Kwon, and U.-K. Moon, "74 dB SNDR multi-loop sturdy-MASH delta-sigma modulator using 35 dB open-loop opamp gain," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2212–2221, Aug. 2009.
[55] D.-Y. Yoon, S. Ho, and H.-S. Lee, "A continuous-time sturdy-MASH ΔΣ modulator in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2880–2890, Dec. 2015.
[56] B. Park, C. Han, and N. Maghari, "Correlated dual-loop sturdy MASH continuous-time delta-sigma modulators," *IEEE J. Solid-State Circuits*, vol. 57, no. 10, pp. 2934–2943, Oct. 2022.
[57] L. Qi, A. Jain, D. Jiang, S.-W. Sin, R. P. Martins, and M. Ortmanns, "A 76.6-dB-SNDR 50-MHz-BW 29.2-mW multi-bit CT sturdy MASH with DAC non-linearity tolerance," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 344–355, Feb. 2020.
[58] C. Han and N. Maghari, "Delay based noise cancelling sturdy MASH delta-sigma modulator," *Electron. Lett.*, vol. 50, no. 5, pp. 351–353, Feb. 2014.
[59] Y.-S. Kwak, K.-I. Cho, H.-J. Kim, S.-H. Lee, and G.-C. Ahn, "A 72.9-dB SNDR 20-MHz BW 2–2 discrete-time resolution-enhanced sturdy MASH delta–sigma modulator using source-follower-based integrators," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2772–2782, Oct. 2018.
[60] L. Wang, S. Liu, Y. Zhang, L. Zhong, and Z. Zhu, "A 44-μW, 91.3-dB SNDR DT ΔΣ modulator with second-order noise-shaping SAR quantizer," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 9, pp. 3575–3583, Sep. 2023.
[61] K. Jeong, S. Ha, and M. Je, "A 15.4-ENOB, fourth-order truncation-error-shaping NS-SAR-nested ΔΣ modulator with boosted input impedance and range for biosignal acquisition," *IEEE J. Solid-State Circuits*, vol. 59, no. 2, pp. 528–539, Feb. 2024.
[62] D. Jiang, L. Qi, S.-W. Sin, F. Maloberti, and R. P. Martins, "A time-interleaved 2^{nd}-order ΔΣ modulator achieving 5-MHz bandwidth and 86.1-dB SNDR using digital feed-forward extrapolation," *IEEE J. Solid-State Circuits*, vol. 56, no. 8, pp. 2375–2387, Aug. 2021.
[63] J.-H. Han, K.-I. Cho, H.-J. Kim, J.-H. Boo, J. S. Kim, and G.-C. Ahn, "A 96 dB dynamic range 2 kHz bandwidth 2^{nd} order delta-sigma modulator using modified feed-forward architecture with delayed feedback," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 5, pp. 1645–1649, May 2021.
[64] H. Wang, D. Basak, Y. Zhang, and K.-P. Pun, "A 0.59-mW 78.7-dB SNDR 2-MHz bandwidth active-RC delta-sigma modulator with relaxed and reduced amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 3, pp. 1114–1122, Mar. 2021.
[65] N. Gaoding and J.-F. Bousquet, "A 4th-order 4-bit continuous-time ΔΣ ADC based on active–passive integrators with a resistance feedback DAC," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 6, pp. 744–754, Jun. 2022.
[66] M. Jang, C. Lee, and Y. Chae, "Analysis and design of low-power continuous-time delta-sigma modulator using negative-R assisted integrator," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 277–287, Jan. 2019.
[67] S. Lee, S. Park, Y. Kim, Y. Kim, J. Lee, J. Lee, and Y. Chae, "A 0.6-V 86.5-dB DR 40-kHz BW inverter-based continuous-time delta–sigma modulator with PVT-robust body-biasing," *IEEE Solid-State Circuits Lett.*, vol. 4, pp. 178–181, 2021.
[68] M. Jang, C. Lee, and Y. Chae, "A 134-μW 99.4-dB SNDR audio continuous-time delta-sigma modulator with chopped negative-R and tri-level FIR-DAC," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1761–1771, Jun. 2021.
[69] J. Huang, S. Yang, and J. Yuan, "A 75 dB SNDR 10-MHz signal bandwidth G_m-C-based sigma-delta modulator with a nonlinear feedback compensation technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2216–2226, Sep. 2015.
[70] M. Runge, J. Edler, T. Kaiser, K. Misselwitz, and F. Gerfers, "An 18-MS/s 76-dB SNDR continuous-time ΔΣ modulator incorporating an input voltage tracking G_mC loop filter," *IEEE J. Solid-State Circuits*, vol. 58, no. 8, pp. 2288–2299, Jul. 2023.
[71] J. Kim, Q. Duan, J. Choi, C. Song, and J. Roh, "A 2.16-μW low-power continuous-time delta–sigma modulator with improved-linearity G_m For wearable ECG application," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 11, pp. 4223–4227, Nov. 2022.
[72] S. Patil, R. Theertham, H. Shibata, V. Kozlov, A. Ganesan, E. Burlingame, Z. Li, R. Thakar, Q. Zhang, Y. Yin, and A. Bhat, "A 1-MHz-bandwidth continuous-time delta-sigma ADC achieving >90 dB SFDR and >80 dB antialiasing using reference-switched resistive feedback DACs," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2023, pp. 1–2.
[73] R. Harjani and T. A. Lee, "FRC: A method for extending the resolution of Nyquist rate converters using oversampling," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 4, pp. 482–494, Apr. 1998.
[74] P. Rombouts, W. De Wilde, and L. Weyten, "A 13.5-b 1.2-V micropower extended counting A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 176–183, Feb. 2001.
[75] S.-C. Kuo, J.-S. Huang, Y.-C. Huang, C.-W. Kao, C.-W. Hsu, and C.-H. Chen, "A multi-step incremental analog-to-digital converter with a single opamp and two-capacitor SAR extended counting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 7, pp. 2890–2899, Jul. 2021.
[76] S. Mohamad, J. Yuan, and A. Bermak, "A 102.2-dB, 181.1-dB FoM extended counting analog-to-digital converter with capacitor scaling," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1351–1360, May 2020.
[77] M. A. Mokhtar, A. Abdelaal, M. Sporer, J. Becker, J. G. Kauffman, and M. Ortmanns, "A 0.9-V DAC-calibration-free continuous-time incremental delta–sigma modulator achieving 97-dB SFDR at 2 MS/s in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3407–3417, Nov. 2022.
[78] Y. Wang, S. Dey, T. He, L. Shi, J. Zheng, M. Kareppagoudr, Y. Zhang, K. Sobue, K. Hamashita, K. Tomioka, and G. Temes, "A hybrid continuous-time incremental and SAR two-step ADC with 90.5-dB DR over 1-MHz BW," *IEEE Solid-State Circuits Lett.*, vol. 5, pp. 122–125, 2022.
[79] W. A. Qureshi, A. Salimath, E. Botti, F. Maloberti, and E. Bonizzoni, "An incremental-ΔΣ ADC with 106-dB DR for reconfigurable class-D audio amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 3, pp. 929–933, Mar. 2022.
[80] P. Vogelmann, J. Wagner, M. Haas, and M. Ortmanns, "A dynamic power reduction technique for incremental ΔΣ modulators," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1455–1467, May 2019.
[81] P. Vogelmann, J. Wagner, and M. Ortmanns, "A 14b, twofold time-interleaved incremental ΔΣ ADC using hardware sharing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 11, pp. 3681–3692, Nov. 2020.
[82] B. Wang, S.-W. Sin, F. Maloberti, and R. P. Martins, "A 550-μW 20-kHz BW 100.8-dB SNDR linear-exponential multi-bit incremental ΣΔ ADC with 256 clock cycles in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 1161–1172, Apr. 2019.
[83] P. Kaesser, O. Ismail, J. Wagner, R. F. H. Fischer, and M. Ortmanns, "Frequency-domain analysis of reconfigured incremental ΔΣ ADCs on the example of the exponential phase," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4346–4356, Nov. 2023.
[84] L. Jie, B. Zheng, H.-W. Chen, and M. P. Flynn, "A cascaded noise-shaping SAR architecture for robust order extension," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3236–3247, Dec. 2020.

[85] J. Liu, D. Li, Y. Zhong, X. Tang, and N. Sun, "A 250 kHz-BW 93 dB-SNDR 4th-order noise-shaping SAR using capacitor stacking and dynamic buffering," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 369–371.

[86] Y.-Z. Lin, C.-Y. Lin, S.-C. Tsou, C.-H. Tsai, and C.-H. Lu, "A 40 MHz-BW 320 MS/s passive noise-shaping SAR ADC with passive signal-residue summation in 14 nm FinFET," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 330–332.

[87] P. Yi, Y. Liang, S. Liu, N. Xu, L. Fang, and Y. Hao, "A 625 kHz-BW, 79.3 dB-SNDR second-order noise-shaping SAR ADC using high-efficiency error-feedback structure," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 3, pp. 859–863, Mar. 2022.

[88] Y. Zhang, S. Liu, B. Tian, Y. Zhu, C.-H. Chan, and Z. Zhu, "A 2^{nd}-order noise-shaping SAR ADC with lossless dynamic amplifier assisted integrator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 10, pp. 1819–1823, Oct. 2020.

[89] H. Zhuang, W. Guo, J. Liu, H. Tang, Z. Zhu, L. Chen, and N. Sun, "A second-order noise-shaping SAR ADC with passive integrator and tri-level voting," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1636–1647, Jun. 2019.

[90] G. Kim, S. Lee, T. Seol, S. Baik, Y. Shin, G. Kim, J.-H. Yoon, A. K. George, and J. Lee, "A 1 V-supply 1.85 V_{pp}-input-range 1 kHz-BW 181.9 dB-FOMDR 179.4 dB-FOMSNDR 2^{nd}-order noise-shaping SAR-ADC with enhanced input impedance in 0.18μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 484–486.

[91] X. Tang, X. Yang, W. Zhao, C.-K. Hsu, J. Liu, L. Shen, A. Mukherjee, W. Shi, S. Li, D. Z. Pan, and N. Sun, "A 13.5-ENOB, 107-μW noise-shaping SAR ADC with PVT-robust closed-loop dynamic amplifier," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3248–3259, Dec. 2020.

[92] J. Liu, X. Wang, Z. Gao, M. Zhan, X. Tang, C.-K. Hsu, and N. Sun, "A 90-dB-SNDR calibration-free fully passive noise-shaping SAR ADC with 4× passive gain and second-order DAC mismatch error shaping," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3412–3423, Nov. 2021.

[93] H. Li, Y. Shen, E. Cantatore, and P. Harpe, "A 77.3-dB SNDR 62.5-kHz bandwidth continuous-time noise-shaping SAR ADC with duty-cycled G_m-C integrator," *IEEE J. Solid-State Circuits*, vol. 58, no. 4, pp. 939–948, Apr. 2023.

[94] Q. Zhang, N. Ning, Z. Zhang, J. Li, K. Wu, Y. Chen, and Q. Yu, "A 13-bit ENOB third-order noise-shaping SAR ADC employing hybrid error control structure and LMS-based foreground digital calibration," *IEEE J. Solid-State Circuits*, vol. 57, no. 7, pp. 2181–2195, Jul. 2022.

[95] B. Gönen, F. Sebastiano, R. Quan, R. van Veldhoven, and K. A. A. Makinwa, "A dynamic zoom ADC with 109-dB DR for audio applications," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1542–1550, Jun. 2017.

[96] Y. Liu, X. Wu, X. Yu, J. Hung, L. Lin, P. Chen, and N. N. Tan, "A sub-1 μW 16-bit fully dynamic zoom ADC compatible with free-running and incremental modes using residue feedforward and extended counting techniques," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 71, no. 2, pp. 522–526, Jul. 2024.

[97] B. Gönen, S. Karmakar, R. van Veldhoven, and K. A. A. Makinwa, "A continuous-time zoom ADC for low-power audio applications," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1023–1031, Apr. 2020.

[98] S. Mehrotra, E. Eland, S. Karmakar, A. Liu, B. Gönen, M. Bolatkale, R. Van Veldhoven, and K. A. A. Makinwa, "A 590 μW, 106.6 dB SNDR, 24 kHz BW continuous-time zoom ADC with a noise-shaping 4-bit SAR ADC," in *Proc. IEEE 48th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2022, pp. 253–256.

[99] J. Yoon, M. Jang, C. Lee, Y. Lim, and Y. Chae, "A 243 μW 97.4 dB-DR 50 kHz-BW multi-rate CT zoom ADC with inherent DAC mismatch tolerance," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2023, pp. 1–2.

[100] L. Jie, M. Zhan, X. Tang, and N. Sun, "A 0.014 mm^2 10 kHz-BW zoom-incremental-counting ADC achieving 103 dB SNDR and 100 dB full-scale CMRR," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 1–3.

[101] Z. Wang, L. Jie, Z. Kong, M. Zhan, Y. Zhong, Y. Wang, and X. Tang, "A 150 kHz-BW 15-ENOB incremental zoom ADC with skipped sampling and single buffer embedded noise-shaping SAR quantizer," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 9–11.

[102] Y. Liu, M. Zhao, Y. Zhao, X. Yu, N. N. Tan, L. Ye, and Z. Tan, "A 4.96-μW 15-bit self-timed dynamic-amplifier-based incremental zoom ADC," *IEEE J. Solid-State Circuits*, vol. 58, no. 6, pp. 1646–1656, Jul. 2023.

[103] Y. Liang, J. Ren, L. Chen, H. Lan, J. Song, S. Song, and Z. Zhu, "A reconfigurable 12-to-18-Bit dynamic zoom ADC with pole-optimized technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 5, pp. 1940–1948, May 2023.

[104] Z. Lu, H. Ji, W. Qu, L. Ye, M. Zhao, and Z. Tan, "A 1 V 1.07μ W 15-bit pseudo-pseudo-differential incremental zoom ADC," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2575–2584, Dec. 2023.

[105] M. Høvin, T. S. Lande, A. Olsen, and C. Toumazou, "Novel second-order $\Delta-\Sigma$ modulator/frequency-to-digital converter," *Electron. Lett.*, vol. 31, no. 2, pp. 81–82, Jan. 1995.

[106] J. Kim, T.-K. Jang, Y.-G. Yoon, and S. Cho, "Analysis and design of voltage-controlled oscillator based analog-to-digital converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 1, pp. 18–30, Jan. 2010.

[107] S. Vasishta, K. R. Raghunandan, A. Dodabalapur, and T. R. Viswanathan, "A single-step subranging relaxation oscillator-based open-loop sigma-delta ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 3, pp. 993–1005, Mar. 2023.

[108] L. Liu, T. Qu, P. Wang, Y. Zhang, S. Wu, Z. Hong, and J. Xu, "A 2.2μW PWM-based time-domain sensor interface with 540 mV_{pp} input signal range, 81.6 dB SNDR and 80MΩ input impedance," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 71, no. 4, pp. 1904–1908, Apr. 2024.

[109] A. Iwata, N. Sakimura, M. Nagata, and T. Morie, "The architecture of delta sigma analog-to-digital converters using a voltage-controlled oscillator as a multibit quantizer," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 7, pp. 941–945, Jul. 1999.

[110] A. Mukherjee, M. Gandara, X. Yang, L. Shen, X. Tang, C.-K. Hsu, and N. Sun, "A 74.5-dB dynamic range 10-MHz BW CT-$\Delta\Sigma$ ADC with distributed-input VCO and embedded capacitive-p network in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 476–487, Feb. 2021.

[111] C. Lee, T. Jeon, M. Jang, S. Park, J. Kim, J. Lim, J.-H. Ahn, Y. Huh, and Y. Chae, "A 6.5-μW 10-kHz BW 80.4-dB SNDR G_m-C-based CT $\Delta\Sigma$ modulator with a feedback-assisted G_m linearization for artifact-tolerant neural recording," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2889–2901, Nov. 2020.

[112] S. Li, D. Z. Pan, and N. Sun, "An OTA-less second-order VCO-based CT $\Delta\Sigma$ modulator using an inherent passive integrator and capacitive feedback," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1337–1350, May 2020.

[113] B. Drost, M. Talegaonkar, and P. K. Hanumolu, "Analog filter design using ring oscillator integrators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3120–3129, Dec. 2012.

[114] C. Pochet and D. A. Hall, "A pseudo-virtual ground feedforwarding technique enabling linearization and higher order noise shaping in VCO-based $\Delta\Sigma$ modulators," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3746–3756, Dec. 2022.

[115] Y. Zhong, M. Zhan, W. Wang, X. Tang, L. Jie, and N. Sun, "An 80.2-to-89.1 dB-SNDR 24k-to-200 kHz-BW VCO-based synthesized $\Delta\Sigma$ ADC with 105 dB SFDR in 28-nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2023, pp. 1–2.

[116] Y. Zhong, S. Li, X. Tang, L. Shen, W. Zhao, S. Wu, and N. Sun, "A second-order purely VCO-based CT $\Delta\Sigma$ ADC using a modified DPLL structure in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 356–368, Feb. 2020.

[117] H.-W. Chen, S. Lee, and M. P. Flynn, "An anti-aliasing-filter-assisted 3rd-order VCO-based CTDSM with NS-SAR quantizer," *IEEE J. Solid-State Circuits*, vol. 59, no. 4, pp. 1171–1183, Apr. 2024.

[118] M. Jian, J. Zheng, X. Kong, B. Sun, and C. Guo, "A 73-dB-SNDR 2^{nd}-order noise-shaping SAR with a low-noise time-domain comparator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 71, no. 8, pp. 3645–3649, Aug. 2024.

[119] R. Theertham, S. N. Ganta, and S. Pavan, "Design of high-resolution continuous-time delta–sigma data converters with dual return-to-open DACs," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3418–3428, Nov. 2022.

[120] D. Jeong and C. Yoo, "A 4-MHz bandwidth continuous-time sigma-delta modulator with stochastic quantizer and digital accumulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 7, pp. 1124–1128, Jul. 2019.

[121] M. A. Mokhtar, P. Vogelmann, M. Haas, and M. Ortmanns, "A 94.3-dB SFDR, 91.5-dB DR, and 200-kS/s CT incremental delta–sigma modulator with differentially reset FIR feedback," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 87–90, Sep. 2019.

[122] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009.

[123] P. C. C. de Aguirre, E. Bonizzoni, F. Maloberti, and A. A. Susin, "A 170.7-dB FoM-DR 0.45/0.6-V inverter-based continuous-time sigma–delta modulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 8, pp. 1384–1388, Aug. 2020.

[124] S.-E. Cho, B. Kim, J.-Y. Sim, and H.-J. Park, "Low-power small-area inverter-based DSM for MEMS microphone," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 11, pp. 2392–2396, Nov. 2020.

[125] Y.-H. Hwang, J. Wang, D.-K. Jeong, and J.-E. Park, "An area/power-efficient $\Delta\Sigma$ modulator based on dynamic-boost inverter for multichannel sensor applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 31, no. 9, pp. 1403–1412, Sep. 2023.

[126] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U.-K. Moon, "Ring amplifiers for switched capacitor circuits," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2928–2942, Dec. 2012.

[127] H.-J. Kim, J.-H. Boo, K.-I. Cho, Y.-S. Kwak, and G.-C. Ahn, "A single-loop third-order 10-MHz BW source-follower-integrator based discrete-time delta-sigma ADC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 2, pp. 401–405, Feb. 2023.

[128] H. Wang, F. Schembari, and R. B. Staszewski, "Passive SC $\Delta\Sigma$ modulator based on pipelined charge-sharing rotation in 28-nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 2, pp. 578–589, Feb. 2020.

[129] M. Copeland and J. Rabaey, "Dynamic amplifier for MOS technology," *Electron. Lett.*, vol. 10, no. 15, pp. 301–302, 1979.

[130] B. J. Hosticka, "Dynamic CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-15, no. 5, pp. 881–886, Oct. 1980.

[131] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. De Man, "Adaptive biasing CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-17, no. 3, pp. 522–528, Jun. 1982.

[132] S. W. Chiang, H. Sun, and B. Razavi, "A 10-bit 800-MHz 19-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 935–949, Apr. 2014.

[133] S. Ma, L. Liu, T. Fang, J. Liu, and N. Wu, "A discrete-time audio $\Delta\Sigma$ modulator using dynamic amplifier with speed enhancement and flicker noise reduction techniques," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 333–343, Feb. 2020.

[134] A. Matsuoka, Y. Kumano, T. Nezuka, Y. Furuta, and T. Iizuka, "A 79.2W 19.5 kHz-BW 94.8 dB-SNDR fully dynamic DT $\Delta\Sigma$ ADC using CLS-assisted FIA with sampling noise cancellation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 8, pp. 2759–2763, Dec. 2023.

[135] M. Zhao, Y. Zhao, H. Zhang, Y. Hu, Y. Bao, L. Ye, W. Qu, and Z. Tan, "A 4-μW bandwidth/power scalable delta–sigma modulator based on swing-enhanced floating inverter amplifiers," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 709–718, Mar. 2022.

[136] Y. Zhao, M. Zhao, and Z. Tan, "Fully dynamic zoom-ADC based on improved swing-enhanced FIAs using CLS technique with 1250× bandwidth/power scalability," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 6, pp. 1901–1905, Jun. 2023.

[137] X. Tang, X. Yang, J. Liu, Z. Wang, W. Shi, D. Z. Pan, and N. Sun, "A bandwidth-adaptive pipelined SAR ADC with three-stage cascoded floating inverter amplifier," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2564–2574, Sep. 2023.

[138] R. S. A. Kumar, N. Krishnapura, and P. Banerjee, "Analysis and design of a discrete-time delta-sigma modulator using a cascoded floating-inverter-based dynamic amplifier," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3384–3395, Nov. 2022.

[139] H. Li, Y. Shen, H. Xin, E. Cantatore, and P. Harpe, "A 7.3-μW 13-ENOB 98-dB SFDR noise-shaping SAR ADC with duty-cycled amplifier and mismatch error shaping," *IEEE J. Solid-State Circuits*, vol. 57, no. 7, pp. 2078–2089, Jul. 2022.

[140] E. Iroaga and B. Murmann, "A 12-bit 75-MS/s pipelined ADC using incomplete settling," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 748–756, Apr. 2007.

[141] K.-C. Hsieh and P. Gray, "A low-noise chopper-stabilized differential switched-capacitor filtering technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1981, pp. 128–129.

[142] R. Poujois, B. Baylac, D. Barbier, and J. Ittel, "Low-level MOS transistor amplifier using storage techniques," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1973, pp. 152–153.

[143] S. Billa, A. Sukumaran, and S. Pavan, "Analysis and design of continuous-time delta–sigma converters incorporating chopping," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2350–2361, Sep. 2017.

[144] C. Lim, Y. Choi, Y. Park, J. Song, S.-S. Ahn, S. Park, and C. Kim, "A capacitively coupled CT $\Delta\Sigma$M with chopping artifacts rejection for sensor readout ICs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 8, pp. 3242–3253, Aug. 2021.

[145] R. Kapusta, H. Zhu, and C. Lyden, "Sampling circuits that break the kT/C thermal noise limit," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1694–1701, Aug. 2014.

[146] J. Liu, X. Tang, W. Zhao, L. Shen, and N. Sun, "A 13-bit 0.005-mm^2 40-MS/s SAR ADC with kT/C noise cancellation," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3260–3270, Dec. 2020.

[147] L. Shi, E. Thiagarajan, R. Singh, E. Hancioglu, U.-K. Moon, and G. C. Temes, "Noise-shaping SAR ADC using a two-capacitor digitally calibrated DAC with 82.6-dB SNDR and 90.9-dB SFDR," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 10, pp. 4001–4012, Oct. 2021.

[148] P. Harpe, E. Cantatore, and A. van Roermund, "A 10b/12b 40 kS/s SAR ADC with data-driven noise reduction achieving up to 10.1b ENOB at 2.2 fJ/Conversion-step," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3011–3018, Dec. 2013.

[149] Y.-H. Hwang, Y. Song, J.-E. Park, and D.-K. Jeong, "A fully passive noise-shaping SAR ADC utilizing last-bit majority voting and cyclic dynamic element matching techniques," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 30, no. 10, pp. 1381–1390, Oct. 2022.

[150] M. Sarhang-Nejad and G. C. Temes, "A high-resolution multibit sigma delta ADC with digital correction and relaxed amplifier requirements," *IEEE J. Solid-State Circuits*, vol. 28, no. 6, pp. 648–660, Jun. 1993.

[151] J. R. Shakya and G. C. Temes, "Efficient calibration of feedback DAC in delta sigma modulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 5, pp. 826–830, May 2020.

[152] M. De Bock, X. Xing, L. Weyten, G. Gielen, and P. Rombouts, "Calibration of DAC mismatch errors in $\Sigma\Delta$ ADCs based on a sine-wave measurement," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 9, pp. 567–571, Sep. 2013.

[153] J. Liu, S. Li, W. Guo, G. Wen, and N. Sun, "A 0.029-mm^2 17-fJ/conversion-step third-order CT $\Delta\Sigma$ ADC with a single OTA and second-order noise-shaping SAR quantizer," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 428–440, Feb. 2019.

[154] S. Pavan and R. Theertham, "Improved offline calibration of DAC mismatch errors in delta–sigma data converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 10, pp. 1618–1622, Oct. 2019.

[155] D. W. J. Groeneveld, H. J. Schouwenaars, H. A. H. Termeer, and C. A. A. Bastiaansen, "A self-calibration technique for monolithic high-resolution D/A converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1517–1522, Dec. 1989.

[156] Y. Zhang, D. Basak, and K.-P. Pun, "A highly linear multi-level SC DAC in a power-efficient G_m-C continuous-time delta-sigma modulator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4592–4605, Dec. 2019.

[157] M. Dalla Longa, F. Conzatti, T. Hofmann, J. G. Kauffman, and M. Ortmanns, "An intrinsically linear 13-level capacitive DAC for delta sigma modulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 4, pp. 1291–1295, Apr. 2023.

[158] J.-H. Chung, Y.-D. Kim, C.-U. Park, K.-W. Park, M.-J. Seo, and S.-T. Ryu, "An 81.2 dB-SNDR dual-residue pipeline ADC with a 2nd-order noise-shaping interpolating SAR ADC," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2023, pp. 1–2.

[159] R. T. Baird and T. S. Fiez, "Improved $\Delta\Sigma$ DAC linearity using data weighted averaging," in *Proc. Int. Symp. Circuits Syst.*, vol. 1, May 1995, pp. 13–16.

[160] I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, J. Cao, and S.-L. Chan, "A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8× oversampling ratio," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820–1828, Dec. 2000.

[161] R. W. Adams and T. W. Kwan, "Data-directed scrambler for multi-bit noise shaping D/A converters," U.S. Patent 5 404 142, Apr. 4, 1995.

[162] R. Schreier and B. Zhang, "Noise-shaped multbit D/A convertor employing unit elements," *Electron. Lett.*, vol. 31, no. 20, pp. 1712–1713, Sep. 1995.

[163] A. Yasuda, H. Tanimoto, and T. Iida, "A third-order Δ − Σ modulator using second-order noise-shaping dynamic element matching," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1879–1886, Dec. 1998.

[164] N. Sun and P. Cao, "Low-complexity high-order vector-based mismatch shaping in multibit ΔΣ ADCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 872–876, Nov. 2011.

[165] W. Shi, X. Wang, X. Tang, A. Mukherjee, R. Theertham, S. Pavan, L. Jie, and N. Sun, "A 0.37 mm^2 250 kHz-BW 95 dB-SNDR CTDSM with low-cost 2^{nd}-order vector-quantizer DEM," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2022, pp. 1–2.

[166] Y.-S. Shu, L.-T. Kuo, and T.-Y. Lo, "An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2928–2940, Dec. 2016.

[167] T. Kim and Y. Chae, "A 2.1 mW 2 MHz-BW 73.8 dB-SNDR buffer-embedded noise-shaping SAR ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 12, pp. 5029–5037, Dec. 2021.

[168] J. Liu, C.-K. Hsu, X. Tang, S. Li, G. Wen, and N. Sun, "Error-feedback mismatch error shaping for high-resolution data converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 4, pp. 1342–1354, Apr. 2019.

[169] Y. Guo, J. Jin, X. Liu, and J. Zhou, "A 60-MS/s 5-MHz BW noise-shaping SAR ADC with integrated input buffer achieving 84.2-dB SNDR and 97.3-dB SFDR using dynamic level-shifting and ISI-error correction," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 474–485, Feb. 2023.

[170] B. Nauta, "1.2 racing down the slopes of Moore's law," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 67, Feb. 2024, pp. 16–23.

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