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TOPICAL REVIEW

A Critical Review of Interconnect Options for SIW Technologies

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ABSTRACT Despite extensive research on integrating Substrate Integrated Waveguide (SIW) technologies with conventional transmission technologies such as Microstrip Transmission Line (MSTL), Co-planar Waveguide (CPW), Rectangular Waveguide (RWG), and Coaxial lines, a comprehensive evaluation and design framework has yet to be explored. This review addresses this critical gap by providing a detailed examination of recent advancements in interconnect technologies at millimeter-wave (mmWave) frequencies. The paper identifies unresolved challenges and introduces a Figure-of-Merit (*FoM*) for the first time designed to evaluate and decide the state-of-the-art in interconnect technologies. Furthermore, it proposes a novel design flow that aids interconnect designers by integrating reported advances into a well-defined process. As such, the study provides a basis for further developments, leveraging existing and SIW technologies to ease mmWave system development, along with a commercial perspective.

INDEX TERMS Wideband, millimeter-wave, rectangular waveguide, substrate integrated waveguide, air-filled substrate integrated waveguide, Substrate Integrated Waveguide (SIW) transition, AFSIW transition, microstrip, Co-planar Waveguide (CPW), Coaxial.

I. INTRODUCTION

Various millimeter-wave (mmWave) frequency bands are projected to be used by high-speed wireless sensors and RADAR systems [1], [2], [3]. The classical RWG is a mainstream technology for designing these high-performance systems, but it is not suitable for low-cost and mass production because of its expensive and bulky non-planar structures [4]. The SIW technology has been a popular platform [5], [6], [7], [8] for over two decades and offers a viable alternative to RWG technology [4]. Furthermore, it is actively used in developing high-end microwave systems spanning from gigahertz to terahertz frequency range [9].

The two main types of SIW technologies are used in mmWave applications, namely the one with dielectric-filled technology, SIW, which is most commonly used [5], [10], and the other with dielectric material removed, AFSIW [11], [12], which achieves higher performances in terms of low insertion loss and high power handling capacity [11], [13], [14], [15], [16]. Both these technologies are widely used in the development of next-generation mmWave systems, as evident from the reported papers in the literature [11], [12], [17], and recently filed patents [18], [19], [20]. In developing next-generation communication systems utilizing these technologies, it is often required to interface them with the external systems that rely on interconnect technologies, like MSTL, CPW, RWG, and Coaxial line, to develop upcoming mmWave communication systems. Although these interconnects are fairly documented in the literature; however, their

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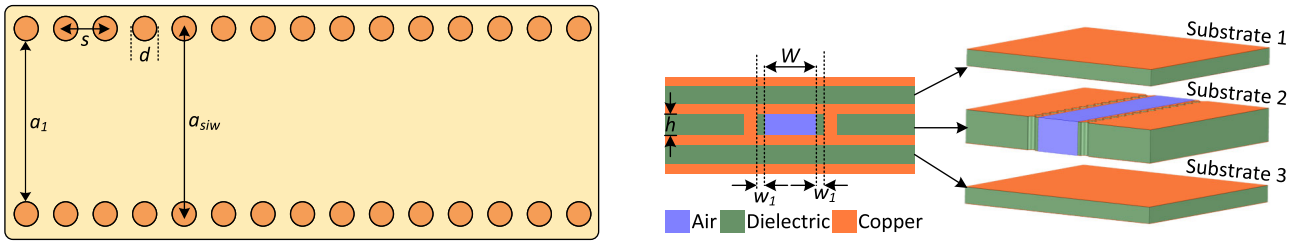


(a) (b)

FIGURE 1. Geometrical Structure: (a) Substrate Integrated Waveguide (b) Air-Filled Substrate Integrated Waveguide.

comprehensive evaluation and design framework are yet to be explored.

Therefore, to address these existing gaps this paper offers the following contributions:

1) Novel Figure-of-Merit (*FoM*): Introduces a *FoM* specifically designed for evaluating millimeter-wave interconnects based on SIW technologies.
2) Comprehensive Review and Evaluation: Utilizing the proposed *FoM* for a rigorous evaluation of existing millimeter-wave interconnects, identifying and reviewing their state-of-the-art designs.
3) Research Gaps and Future Directions: The *FoM*-based analysis identifies critical gaps, and outlines promising areas for future research and commercial perspective.

II. GEOMETRICAL STRUCTURE

A. SUBSTRATE INTEGRATED WAVEGUIDE

The classic SIW employs a double-layer PCB process in which the substrate embeds two parallel rows of metallic via holes that limit the area of wave propagation. Figure 1 (a) shows the structure of SIW with the vias on both sides. Its other geometrical parameters are the width a_1, the diameter of the vias d, and the distance between two successive vias of the same row s, respectively. While, a_1 is the effective width of the SIW defined as the distance between its two vias rows and taken edge to edge, and it is related to the cut-off frequency f_{cSIW} [8], [21], [22] as:

$$a_1 = \frac{c}{2f_{cSIW}\sqrt{\varepsilon_r}} \tag{1}$$

where c is the speed of light in free space, and ϵ_r is relative permittivity, while a_{siw} taken center to center, can be calculated as $a_1 + s\left(0.766e^{\frac{0.4482d}{s}} - 1.176e^{-\frac{1.214d}{s}}\right)$ [22]. The SIW cavity behaves identically to a conventional metallic cavity when $0.5 < d/s < 0.8$ [22]. Furthermore, conditions such as $d < s < 2d$ must be satisfied to avoid the bandgap effect [6], [23], [24], [25], which arises due to periodic structures of vias in SIW.

B. AIR-FILLED SUBSTRATE INTEGRATED WAVEGUIDE

The AFSIW [11], [40] utilizes a multilayer PCB process, as shown in Figure 1(b). Substrates 1 and 3 realize the conducting top and bottom surfaces, while substrate 2 is sandwiched in the middle, which contains an air-filled region W separated by a gap of dielectric slab w_1 and arrays of metallic vias on both sides of the substrate of height h. The cutoff frequency f_{cAFSIW} of the wave traveling in the AFSIW satisfies (2), and it is used to determine the width W [41].

$$tan\left(\frac{w_1\pi\sqrt{\epsilon_r}}{\sqrt{\epsilon_r}}\right) = cot\left(\frac{W\pi f_{cAFSIW}}{c}\right) \tag{2}$$

where, W and w_1 are the widths of air-filled and dielectric-filled regions of AFSIW, respectively (see Figure 1(b)), c is the light's speed, and ϵ_r is the dielectric constant. The via diameter and separation between the center-to-center of the vias used in the AFSIW is determined using the technique described in [24], [25]. Substrates 1 and 3 can be utilized to realize baseband or digital circuits for a more cost-effective wireless system solution.

III. ANALYSIS METHODOLOGY AND PROPOSED FIGURE-OF-MERIT

Several studies on the design of millimeter-wave interconnects for SIW technologies involving MSTL, CPW, RWG, and Co-axial have been reported in the literature [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [42], [43]. It is pertinent to note that this paper focuses specifically on the millimeter-wave range; thus, only works reported in the millimeter-wave band are considered. For brevity, the paper reproduces direct design equations reported in the literature while non-direct/supporting equations are referenced.

A. ANALYSIS METHODOLOGY

To identify the state-of-the-art millimeter-wave interconnect design utilizing SIW technologies, a novel and comprehensive Figure-of-Merit (*FoM*) is introduced using established parameters in the literature, as described in the next Subsection, III-B, which is then used to objectively evaluate millimeter-wave interconnect based on SIW technologies and decide on a state-of-the-art design. The evaluation process is outlined in Fig 2. Once the state-of-the-art design is identified, a thorough analysis is carried out to extract valuable design knowledge, focusing on key aspects such as the physical layout and configuration of the interconnect (design structure), any governing design equations that influence its

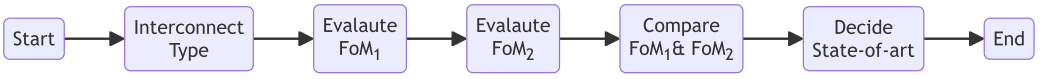


FIGURE 2. Analysis methodology for deciding the state of art for SIW technologies interconnects.

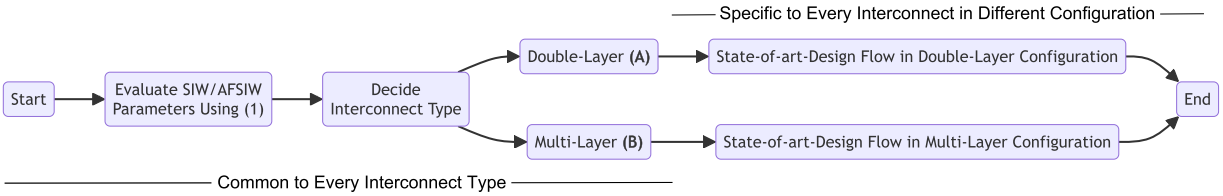


FIGURE 3. High-Level design flow for interconnects utilizing SIW technologies.

TABLE 1. Performance comparison other technologies with SIW technology interconnects.

Ref.	Transition Structure	IL (dB)	BW (GHz)	Design Complexity	Design Equations	Design Flow/Procedure	Optimization Index	Multi-layer	FoM_1	FoM_1
[26]	MSTL to SIW	0.45	14	Low	Yes	Yes	Easy	No	4	31.1
[27]	MSTL to SIW	0.7	6	Low	Yes	Yes	Easy	No	4	8.57
[28]	MSTL to SIW	0.5	9	Low	Yes	No	Easy	No	3	18
[29]	MSTL to SIW	1.4	5	High	No	Yes	Difficult	Yes	2	3.57
[30]	CPW to SIW	0.9	20	High	No	No	Difficult	Yes	1	22.2
[31]	CPW to SIW	0.4	14	Low	No	Yes	Easy	No	3	35
[32]	CPW to SIW	0.75	6	Low	Yes	Yes	Easy	No	4	8
[33]	CPW to SIW	4	3	Low	No	Yes	Easy	No	3	0.75
[34]	CPW to SIW	2.9	2.5	Low	No	Yes	Easy	No	3	0.86
[35]	RWG to SIW	0.55	14.5	High	No	No	Difficult	No	0	26.66
[36]	RWG to SIW	1.0	20	High	No	No	Difficult	No	0	20
[37]	RWG to SIW	0.4	12	Low	No	No	Difficult	No	1	30
[38]	RWG to SIW	0.70	25	Low	Yes	Yes	Easy	No	4	35.71
[39]	Coax to SIW	1.62	43.1	High	Yes	Yes	Difficult	No	2	26.6

performance, and any unique design considerations specific to the design.

These extracted design insights are then incorporated into a comprehensive design flow, consisting of two distinct parts, where the first outlines the higher level design process (See Fig 3) true for all the interconnects, serving as a necessary precursor to the detailed discussion in the second part that showcases the lower level design flow for each of the state-of-the-art interconnect as described in Sections IV and V.

After the design flow is proposed, the critical research gaps especially for their operation in higher millimeter-wave frequencies, and potential future research directions are identified and discussed in each interconnect case, which will pave the way for further advancements and optimizations in this field. These combined approaches, encompassing evaluation, design analysis, and design flow development, eventually streamline the design and development process for high-performance millimeter-wave interconnects involving conventional transmission technologies with emerging SIW or AFSIW.

B. PROPOSED FIGURE-OF-MERIT (FoM)

To propose a Figure of Merit (*FoM*) for evaluating interconnects based on SIW technologies, an extensive literature review was conducted to identify the critical parameters of relevance for interconnect design using SIW technologies [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [42], [43]. Studies such as [26], [27], [32], [38], [39], [42], [43] highlight the importance of design equations and design flow/procedure, which significantly decrease the design cycle time, leading to faster design processes. The inclusion of design equations and procedures inherently reduces the necessity for optimization, as evidenced by cases where design equations render optimizations unnecessary, thus lowering overall optimization efforts. Therefore, having a comprehensive design procedure with relevant design equations is crucial, as it ensures a more efficient design cycle with reduced optimization. While studies such as [29], [30], [38], [42] emphasize the importance of design techniques capable of handling multi-layer configurations, necessary for multi-layer designs in system-on-substrate (SoS) designs. Thus, design techniques must be flexible enough to integrate on multi-layer substrates, reinforcing the need for multi-layer interconnects. The preference for design simplicity over complexity is well-known and widely accepted [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [42], [43]. Moreover, metrics such as bandwidth (BW) and insertion loss (IL) remain critical as these metrics are integral to evaluating the performance of interconnects, and their significance is well-established across multiple studies [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [42], [43]. Therefore, BW and IL are essential parameters that need to be considered alongside design equations and procedures to fully assess the SIW interconnect designs. In conclusion, as made clear from the

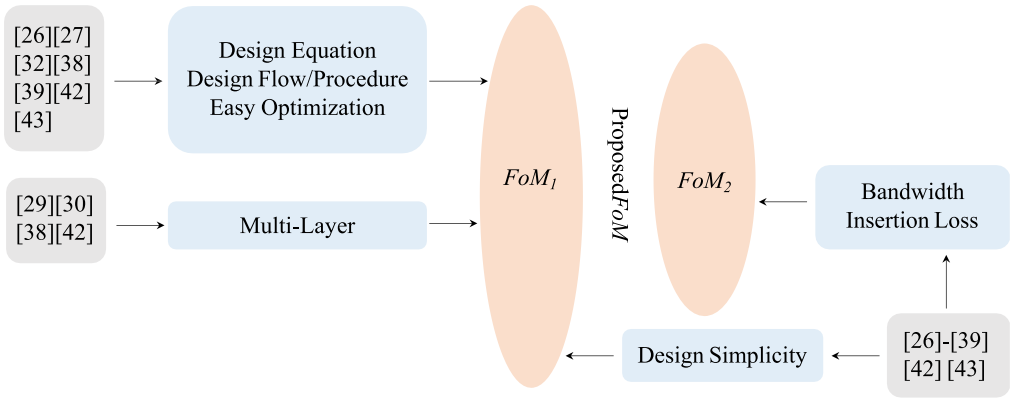


FIGURE 4. Process for the development of the proposed FoM.

discussion above the parameters such as design flow, design equation, design simplicity, easy optimization, and multi-layer capability are important for interconnect design based on SIW technologies, as summarized in Fig. 4.

Based on this literature survey, two *FoMs* are proposed namely FoM_1 and FoM_2 that are developed using the well-established parameters, selected for their relevance and importance in interconnect design. These *FoMs* are then used to comprehensively analyze numerous mmWave interconnects of different types for SIW technologies, covering both qualitative and quantitative features. The FoM_1 utilizes the qualitative aspects, evaluating whether design equations, multi-layer substrate integration, design flow, and design simplicity are utilized, where the design complexity is decided through a well-documented technique reported in the literature [44], [45], [46], [47]. On the other hand FoM_2 examines the quantitative aspects, considering bandwidth and insertion loss, which are foundational metrics for determining state-of-the-art designs as made clear from the discussion above. The expressions for FoM_1 and FoM_2 are described below:

$$FoM_1 = DF[Y/N] + DE[Y/N] + DS[Y/N] + OI[Y/N] + ML[Y/N] \tag{3}$$

where the parameters in (3) are described as follows:

- Design Flow (DF): Scored 1 for a clearly defined and well-documented design flow and 0 for its absence.
- Design Equation (DE): Scored 1 for the presence of design equation, 0 for no equations.
- Design Simplicity (DS): Scored 1 for a design exhibiting ease of fabrication and integration and 0 for complex designs.
- Optimization Index (OI): Scored 1 for easy optimizations and 0 for lengthy optimization processes.
- Multi-Layer Capability (ML): Scored 1 if it supports multi-layer integration and 0 for no multi-layer integration.

$$FoM_2 = \frac{BW[GHz]}{IL[dB]} \tag{4}$$

BW and IL stand for bandwidth and insertion loss, respectively, which are crucial performance [38], [40] to consider when evaluating interconnect performance.

Therefore, FoM_1 and FoM_2 serve as both incentives and rationale for determining the state-of-the-art performance of a particular interconnect design using SIW Technologies involving well-defined parameters established in the literature [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [42], [43].

IV. SIW INTERCONNECTS

SIW interconnects been the subject of extensive study [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [42], [43]. The following subsections describe the two primary kinds of structures—double-layer and multi-layer configurations—for which *FoM* analysis assesses the state of art interconnect design, as explained in section III-B. Every design is reviewed and discussed in terms of equations, design flow, and structural issues, and the state-of-the-art design is discussed in the form of the design flow, backed up by any equation supplied in the state-of-the-art to ease the design process. Finally, the discussion addresses the challenges encountered, unfulfilled research objectives, and promising future directions for SIW interconnects. Considering that this paper focuses specifically on the SIW interconnects operating in the mm-Wave range; therefore, only works reported in the mm-Wave band are considered and included in Table 1.

A. MSTL TO SIW

Several designs from MSTL to SIW transition in double and multi-layer configurations have been reported in the literature [26], [27], [28], [29] as discussed below.

1) DOUBLE LAYER

The *FoM* analysis is applied to evaluate the state-of-the-art interconnects. The results in Table 1 revealed that, among the reported double-layer designs, the interconnect described in [26] achieved the highest performance. As seen in Fig. 5, its structure uses a simple design with a linearly tapered microstrip section to provide effective impedance matching, and the taper width w is related, as indicated in (5). The measured and simulated results for S_{11} and S_{21} [26] in the frequency bands from $25-38$ GHz were achieved as shown in Fig. 6.

$$\frac{1}{w_e} = \begin{cases} \dfrac{\frac{60}{\eta h} ln\left(8\frac{h}{w}+0.25\frac{w}{h}\right)}{b}; w/h<1 \\ \dfrac{120\pi}{\eta h[w/h+1.393+0.667ln(w/h+1.444)]}; w/h>1 \end{cases} \tag{5}$$

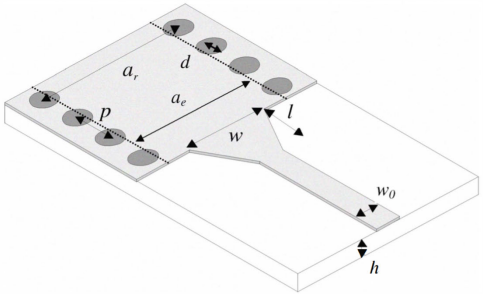


FIGURE 5. MSTL to SIW - double layer [26].

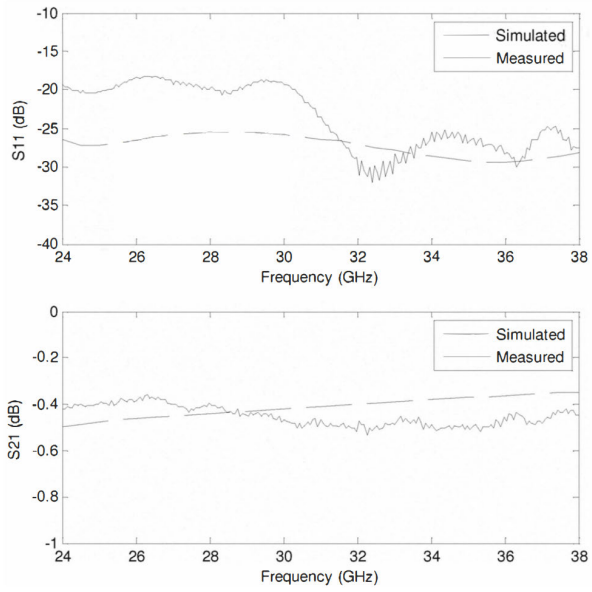


FIGURE 6. Measured and Simulated (S_{11} and S_{21}) [26].

Using the curve fitting technique, the following equation can be derived:

$$\frac{1}{w_e} = \frac{4.38}{a_e} e^{-0.627 \frac{\epsilon_r}{\frac{\epsilon_r+1}{2}+\frac{\epsilon_r-1}{2}\frac{1}{\sqrt{1+12h/w}}}}, \tag{6}$$

where b is the width of the SIW, h is the substrate height,is the free-space impedance, ε_r is the dielectric constant of the substrate, w_e is the width of the waveguide.

By equating (5) and (6), the width w can be determined. The taper length l (see Fig. 5) is taken a multiple of a quarter of wavelength to minimize the return loss and can be expressed as [26].

$$l = 0.25k\left(\frac{\lambda_0}{\sqrt{\varepsilon_{reff}}}\right) = 0.25k\lambda \tag{7}$$

where, $\lambda = \left(\frac{\lambda_0}{\sqrt{\varepsilon_{reff}}}\right)$, λ_0 is the free-space wavelength at the center frequency of operation, and ε_{reff} is the effective dielectric constant of the MSTL, and $k = 1, 2, 3, \ldots,$ and can be optimized in EM solver to achieve the best results for return loss.

These findings, as discussed above, are used, and a design flow is proposed, as shown in Fig. 7. While [26] offers a solid foundation, achieving faster design turnaround, a simplified set of analytical equations is still lacking, making the design process relatively longer. Moreover, the reported work showcases measured results in the lower millimeter wave band, neglecting the higher-end V ($50-75$ GHz) and W ($75-110$ GHz) bands.

Therefore, it is of high interest that simplified equations are to be developed, as well as the applicability of this technique in the higher millimeter wave band is to be demonstrated, the literature is insufficient, and more work is needed to solve these research gaps.

2) MUTLI LAYER

In this configuration of MSTL to SIW interconnect, only one reported work [29] was found. A 3-D configuration and transition parameters are shown in Fig. 8 (a)-(c). The ridges in the transition can be made using one single groove shown in Fig. 8 (c) or some via-hole arrays in Fig. 8 (d); however, the transition remains relatively complex due to its multi-layer nature. The work reports reasonable performance for S_{11} and S_{21} in the lower mm-wave range from 22-28 GHz, as shown in Fig. 9.

The design process followed in the work is not very direct and remains lengthy, [29] utilizes the transverse resonance method (TRM), which is used to calculate the cutoff wavelength λ_c and characteristic impedance. The well-known characteristic impedance equations Z_0 of SIW, ridged waveguide, and MSTL are then used to find the initial dimension by graphically plotting them with respect to the parameter being calculated [38], [48]. After the individual characteristic impedance curves are plotted, the solution of these curves gives initial values for W_2, W_3, and W_4, which need to be further optimized to yield better results.

The design insights presented in [29] were used to propose a design flow shown in Fig. 7. As evident from the reported works that [29] limited research on multi-layer MSTL to SIW showcases a critical research gap in the literature when compared to their well-studied double-layer counterparts.

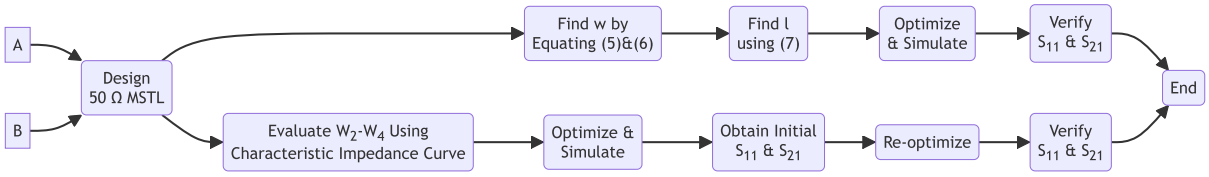


FIGURE 7. Design flow for state-of-art for MSTL to SIW Interconnects.

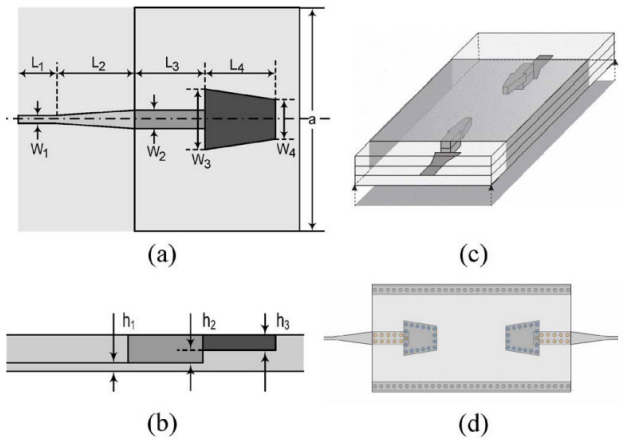


FIGURE 8. MSTL to SIW - Multilayer [29] (a) Top-view (b) Side-view (c) Tri-metric view (d) Top-view transmission system.

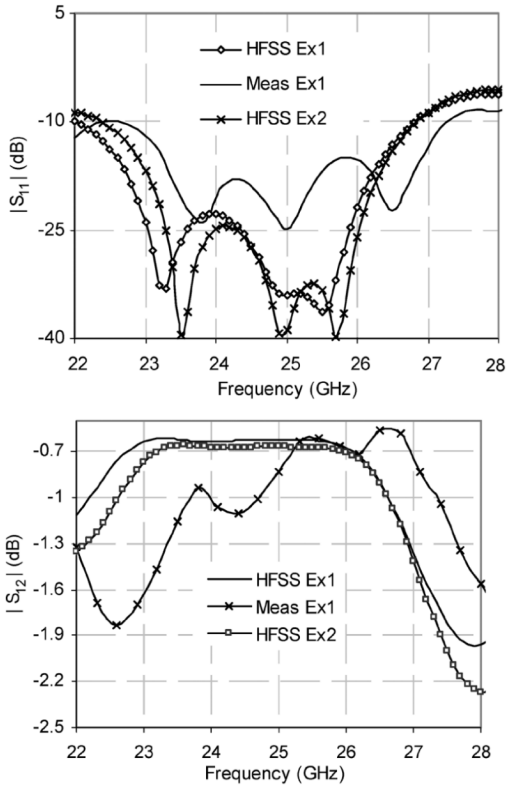


FIGURE 9. Measured and Simulated (S_{11} and S_{21}) [29].

The crucial gap in these works is that they require extensive design optimization processes; moreover, accurate modeling of these multi-layer structures remains challenging due to the complex nature of the interconnect. Moreover, a significant discrepancy is also observed when comparing FoM_1 and FoM_2 of double-layer and multi-layer interconnects, which is due to relatively worse performance as well as a lack of well-defined design process. This underscores the need for improved design approaches tailored explicitly for multi-layer configurations with direct analytical design equations. Furthermore, the interconnect applicability in the V and W bands remains under-reported.

Therefore, it is evident that there is a critical research gap and that it is of high interest to resolve it to pave the way for a fully integrated SoS to support emerging communication applications.

B. CBCPW TO SIW

Extensive research in this category has been carried out [30], [31], [32], [33], [34], a detailed analysis is conducted again and is discussed below.

1) DOUBLE-LAYER

A similar *FoM* analysis is conducted again; Table 1 shows that out of all the double-layer designs provided, the interconnect design from [31] performed the best in terms of FoM_1 and FoM_2. The proposed transition structure can be equivalently set as a generalized impedance inverter (K) in its equivalent form, whose parameter can accurately be extracted using the TRL (Thru, Reflect, Line) calibration technique [31]. In the TRL procedure, the transitions are considered as the two error boxes, which account for port discontinuities at P_1 and P_2 in an EM solver.

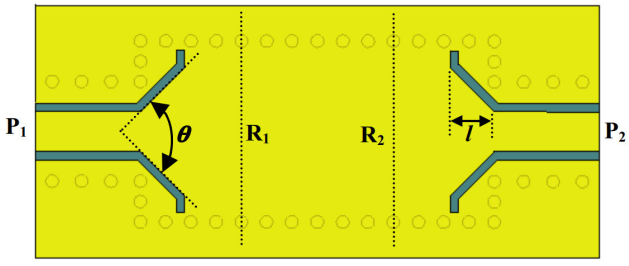


FIGURE 10. CPW to SIW - Double layer [31].

Only two TRL calibration standards—thru and line connections—are utilized in the error box evaluation process. Their S-matrix is then readily computed using 3D EM

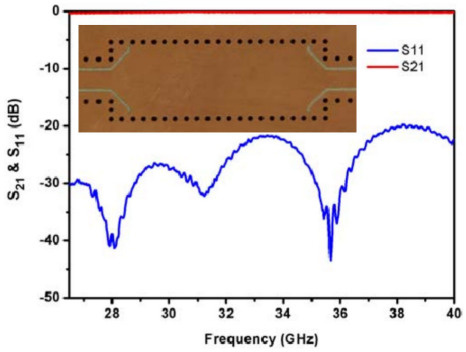


FIGURE 11. Measured results for S_{11} and S_{21} [31].

simulator, and they ultimately yield the propagation constant and normalized impedance of the transition, which is represented as follows:

$$\frac{K}{\sqrt{Z_1 Z_2}} = \sqrt{L} - \sqrt{L-1} \tag{8}$$

where L is the insertion loss of the inverter measured between source and load impedances matched, respectively, to Z_1 and Z_2. The above procedure is used to design a transition using the linear tapering concept. In this case, the parameters that need to be optimized are the angle θ of the taper and the length l of the interconnect (See Fig. 10) [31], as these have a substantial impact on the impedance matching and overall performance of the transition.

The reported work doesn't include straightforward analytical equations to extract these parameters. It follows the process of plotting K for different lengths l and θ to maximize K. This technique is then used to achieve the best results for S_{11} and S_{21} in the frequency range 26-40 GHz, as shown in Fig. 11 with optimized interconnect parameters. The design technique, including the procedural steps, is summarized in the design flow given in Fig. 12 for the CBCPW-SIW interconnect design.

The literature seems well-versed regarding these interconnects, but there is still a literature gap when the analytical design equation for the l and θ is concerned. Furthermore, the interconnects applicability in the higher end of the millimeter wave band, the V and W bands are missing, and the design process relies on a purely parametric process with no analytical design equations. Therefore, there is still a research gap, and future works addressing this issue are of high interest.

2) MULTI-LAYER

In the multi-layer category, authors found a single reported paper [30] in the mm-wave range, and its structure utilizes shorting vias in the interconnect region in the proposed 3-layer transition configuration, as shown in Fig. 13, whereas Fig. 14 explains the E-field gradation in CPW-to-SIW transition. As shown in Fig. 13, the ECPW section plays a role in the intermediary field matching between the horizontal CPW E-field and the vertical SIW E-field as the ridged waveguide. The gradation of the E-field distributions shows that the horizontal CPW E-field is converted to the vertical SIW E-field within a short length of the ECPW from B-B' to D-D', achieving wide bandwidth. The steps and procedure involved in the multilayer configuration is summarized in Fig. 12. The simulated S_{11} and S_{21} for different lengths of ECPW [30] are shown in Fig. 15. The key issue in this is that the parameters can't be extracted through design equations and have to be determined after extensive optimization in an EM solver.

Therefore, a pure parametric technique is available for multi-layer interconnect design in this case, and this limited research on multi-layer interconnects highlights a critical gap in the existing literature. Further efforts are required to address the modeling complexities and optimize the design of multi-layer interconnects to meet the demands of future system-on-substrate technologies. Moreover, the interconnect design applicability is only showcased in the lower millimeter wave range, while its applicability in the higher millimeter wave range, V and W bands, is not examined. Furthermore, when the FoM_1 and FoM_2 analysis of double-layer and multi-layer substrate interconnects are compared, a drastic difference is observed, thus further highlighting the performance gap.

In conclusion, it is readily obvious that there is a critical research gap that needs to be filled to enable the development of a fully integrated SoS to support new emerging applications.

C. RWG TO SIW

In this interconnect category, several reported works in literature [35], [36], [37], [38], a detailed analysis is conducted again and is discussed below.

1) DOUBLE LAYER

A similar analysis is conducted again on the reported works to evaluate state-of-the-art interconnect [35], [36], [37], [38]. Among the reported interconnect, the interconnect [38] reported by the authors achieves the highest FoM in terms of FoM_1 and FoM_2 as given in Table 1 compared to others [35], [36], [37]. As far as its structure is concerned, it relies on a linearly tapered concept (See Fig. 16), where the impedance is gradually transformed. The length of the interconnect L_{SIW} minimizes the insertion loss and leads to excellent impedance matching, is expressed as:

$$L_{SIW} \cong 0.35\sqrt{K_0^2\lambda^2 + K_1^2\lambda^2} \tag{9}$$

$$K_0 = \frac{\frac{(b_1-b_0)}{b_0} - \frac{a_1-a_0}{a_0}\left(\frac{\epsilon_{eff}}{\epsilon_{eff}-\left(\frac{\lambda_0}{2a_0}\right)^2}\right)}{\left(\epsilon_{eff} - \left(\frac{\lambda_0}{2a_0}\right)^2\right)^{\frac{1}{2}}} \tag{10}$$

$$K_1 = \frac{\frac{(b_1-b_0)}{b_1} - \frac{a_1-a_0}{a_1}\left(\frac{\epsilon_{eff}}{\epsilon_{eff}-\left(\frac{\lambda_0}{2a_1}\right)^2}\right)}{\left(\epsilon_{eff} - \left(\frac{\lambda_0}{2a_1}\right)^2\right)^{\frac{1}{2}}} \tag{11}$$

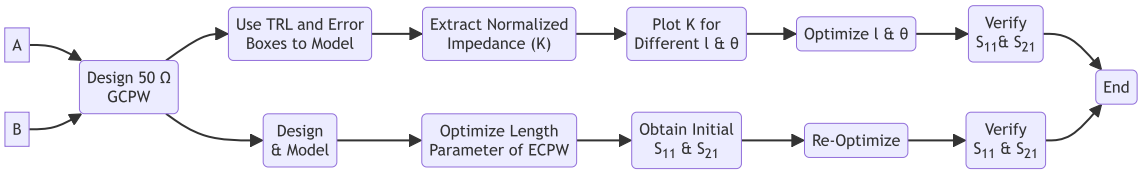


FIGURE 12. Design flow for state-of-art for CPW to SIW Interconnects.

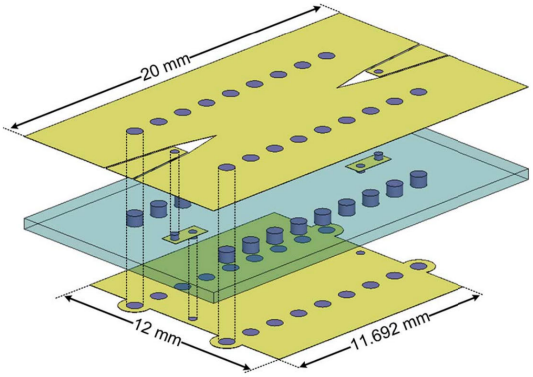


FIGURE 13. CPW to SIW - Multi Layer [30].

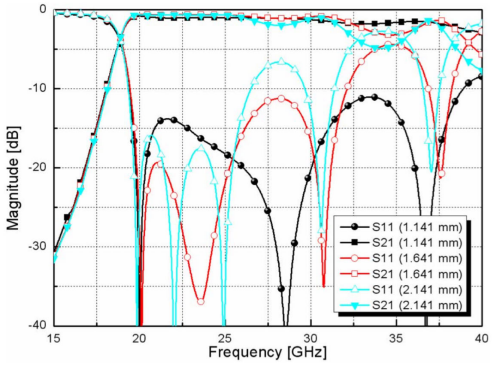


FIGURE 15. Simulated S_{11} and S_{21} for different ECPW length [30].

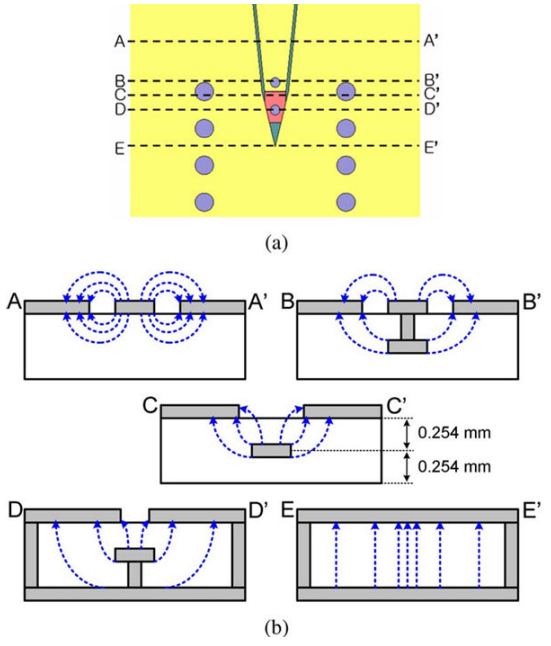


FIGURE 14. Structure of the proposed CPW-to-SIW transition: (a) top view and (b) cross sections showing the E-field gradation [30].

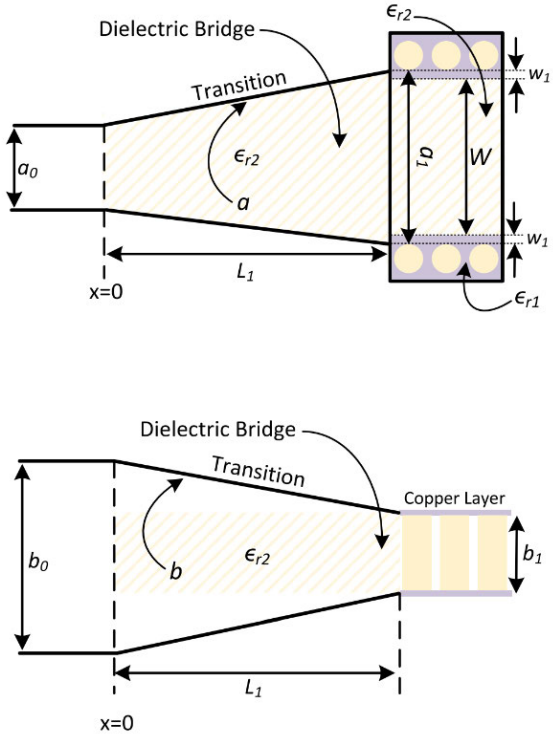


FIGURE 16. RWG to SIW - Double Layer [38].

$$\epsilon_{eff} = A + A^3 \left[\epsilon_{r_1} \left(1 - \frac{t}{b} \right) + \frac{\epsilon_{r_2} t}{b} \right] B \qquad (12)$$

where, b_1 and b_0 represent the width of the RWG and the SIW cavity, while a_1 and a_0 represent the height of the waveguide and SIW cavity respectively, while ϵ_{eff} is the effective dielectric constant of the interconnect and can be known using (12), and while λ_0 is the free space wavelength calculated at the cutoff frequency of the waveguide. The excellent results for S_{11} and S_{21} for the tapered transition [38] are shown in Fig. 17. Considering that the analytical design equations and the interconnect performance are showcased in the higher mmWave bands, it is clear that the literature

TABLE 2. Performance comparison other technologies with AFSIW technology interconnects.

Ref.	Transition Structure	IL (dB)	BW (GHz)	Design Complexity	Design Equations	Design Flow/Procedure	Optimization Index	Multi-layer	FoM_1	FoM_2
[38]	RWG to AFSIW	0.7	25	Low	Yes	Yes	Easy	Yes	5	35.71
[42]	MSTL to AFSIW	0.75	2.3	High	Yes	Yes	Easy	Yes	4	3.0
[43]	MSTL to AFSIW	0.9	14	High	Yes	Yes	Easy	No	4	15.50

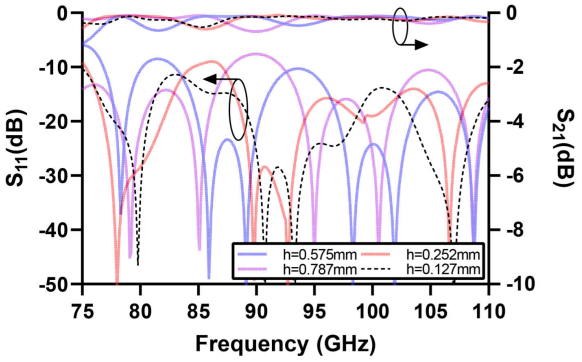


FIGURE 17. RWG to SIW - Double Layer [38].

is adequate. The design steps and procedure, as discussed above, are incorporated, and the state-of-the-art design flow is presented, as shown in Fig. 18.

2) MULTI-LAYER

Although the reported works [35], [36], [37], [38] haven't shown the interconnect integration on a multi-layer substrate. However, in the authors' work, just by adjusting the positioning of the interconnect, it can easily be extended to a multi-layer substrate scenario. The authors [38] have already reported on the analytical equation, which produces good performance and the fact that it can even be expanded to multi-layer scenarios; therefore, it is evident that these interconnects have a research gap and there is a need to showcase the applicability of the interconnect in a multi-layer scenario, which requires to be filled to develop SoS for upcoming areas. Therefore, the literature is inadequate, and more work is needed to showcase multi-layer compatibility.

D. COAXIAL TO SIW

When considering interconnects from coaxial to SIW, the literature is very scarce, with only one reported work found in the mmWave range [39] found. However, the *FoM* analysis is still carried out, and the results are summarized in Table 1.

1) DOUBLE LAYER

The *FoM* analysis is carried out [39], as summarized in Table 1. In this interconnect configuration, the coaxial probe feeds the aperture slot, where electromagnetic (EM) wave changes from TEM mode to TE_{10} mode, as shown in Fig. 19. When the design process of this interconnected is considered, a pure parametric analysis is used. The dimensions of the support pieces are chosen based on mechanical compatibility, while the copper strips (stubs) and an aperture slot are designed to act as an intermediate half-wavelength resonator between the line and SIW. A pure parametric analysis decides their dimensions.

The simulated and measured S-parameters results show a reasonable correlation from the 19.63–62.7 GHz frequency range, as shown in Fig. 20. Although the reported work includes procedural steps; however, these steps rely mainly on parametric analysis. Therefore, it is clear that the reported work mainly utilizes a pure parametric analysis to evaluate all the parameters. Considering the purely parametric process, a design flow is proposed, as shown in Fig. 21. In conclusion, it is clear from the literature that the work is inadequate, and more work is required to extend its applicability to the higher W band. Moreover, future work needs to develop direct analytical design equations.

2) MULTI LAYER

Although the interconnect structure [39] can easily be expanded to a multi-layer design by adjusting the aperture location to achieve the best performance and following the same parametric process. The process is outlined in the design flow chart shown in Fig. 21. Since the literature only uses parametric optimization to achieve adequate results and lacks an analytical equation, more work is required to fill this research gap. Moreover, work must still be done to showcase multi-layer compatibility and pave the way for developing SoS for new applications.

V. AIR FILLED SIW INTERCONNECT

There are very limited reported works [38], [42], [43] in this interconnect category. A similar FoM investigation is carried out to determine the state-of-art and is discussed in detail in the next subsection. Considering the paper focuses primarily on AFSIW interconnects that operate in the mmWave range, only studies published in the mmWave band are taken into account and shown in Table 2.

A. MSTL TO AFSIW

In this case, only a single reported work is available in the literature in both double and Multi-layer cases [42], [43]. However, the *FoM* analysis is carried out, and the results are summarized in Table 2.

1) DOUBLE LAYER

The only reported work consists [43] of an artificial slab along with a classic linearly tapered MSTL; the artificial slabs are used to improve impedance matching, as shown in Fig 22 (a)-(b).

The initial parameters of the interconnect are calculated using (13)-(16), which are further optimized in an EM solver

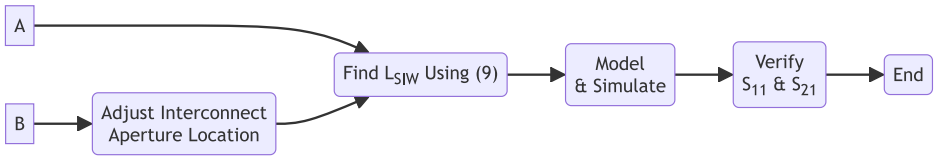


FIGURE 18. Design flow for state-of-art for RWG to SIW Interconnects.

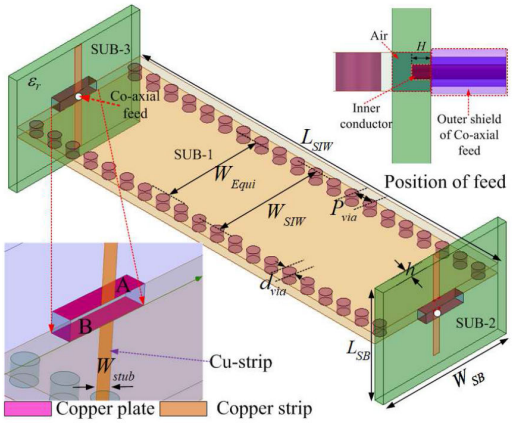


FIGURE 19. Three-dimensional configuration and position of the coaxial line in the transition [39].

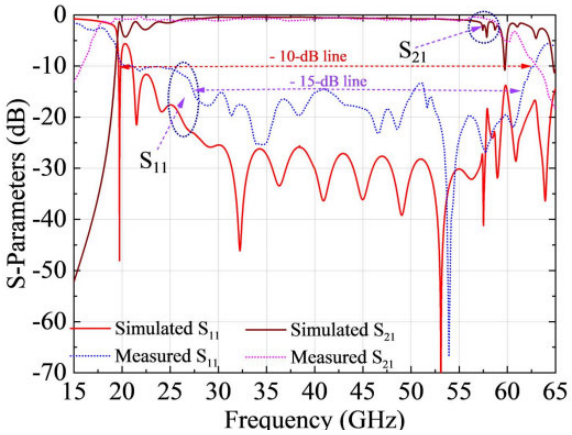


FIGURE 20. S-parameters of the Co-axial-to-SIW transition [39].

to achieve good results for S_{11} and S_{21}. The measured results of the reported interconnect are shown in Fig. 23.

$$W_{tms} = 1.7W_{ms} \tag{13}$$

$$l_{tms} = \frac{\lambda_{ms} f_0}{4} \tag{14}$$

$$w_{ir1}/w_{ir2} = (N-1)(svp_y + l_y) \tag{15}$$

$$h_1 = \left(1 - \frac{\varepsilon_{r_0}}{\varepsilon_r}\right)(h + 2t) \tag{16}$$

Considering all the design findings, a design flow is proposed and is showcased in Fig 24. As evident from the reported work, it is clear that more work is required to develop more accurate design equations so that optimization can be eliminated. Therefore, the literature seems inadequate in this case, and more work is certainly needed. Moreover, the applicability of the technique is to be shown in the higher V and W bands.

2) MULTI-LAYER

The multi-layer interconnect [42] uses a slot coupling method, where a single slot is employed (See Fig. 25(a)) to couple the electric field lines (See Fig. 25(c)). Moreover, to couple the field effectively, a copper line supported by layer $S3$ is introduced between the AFSIW structure (layer $S2$) and the MSTL structure (layer $S4$). This results in improved impedance matching and enhanced E-coupling in the AFSIW (See Fig. 25(c)). In Fig. 26, the S-parameters of the back-to-back transition obtained in simulation and measurement over the frequency range of 27.5 GHz to 29.8 GHz. It is also important to note that the work includes no design equations; a pure parametric flow is relied upon. All the design insights and findings are considered, and a design flow is proposed, as shown in Fig 24.

Although this work provides a path forward, there is much work to be done, especially when the *FoM* analysis is considered, where the difference between the double and multi-layer interconnects is significant. Moreover, the interconnects don't report design equations, which makes the work rely on a parametric process. Furthermore, the technique's applicability is not shown in the V and W bands. Therefore, it is clear that there is a research gap, and future studies need to cover this research gap.

B. CPW TO AIR FILLED SIW

There's no standalone interconnects have been reported in the literature for CPW to AFSIW; instead, all reported interconnects first couple power from CPW to SIW, after the E fields are coupled into the Air filled SIW structure, as shown in Fig. 27 (a)-(b) [11], [49]. In both designs, the first CPW to SIW is designed following the process described in Fig. 12 in multi-layer configuration. In the first case (See Fig. 27 (a)), the interconnect from SIW to air-filled is designed by employing a linear or exponential transition, although its length (L) always remains the point of concern. However, as long as the tapering is smooth, good impedance matching can be achieved, whereas in other cases (See Fig. 27 (b)), windows are etched on the bottom of the substrate 3 for E-wave coupling. From the above discussion, it is very obvious that there exists a critical research gap in the literature as far as these interconnects

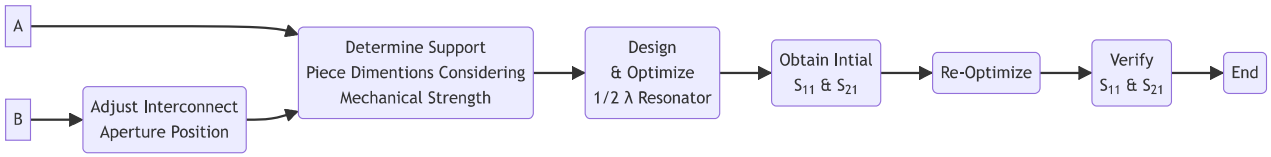


FIGURE 21. Design flow for state-of-art for Coax to SIW Interconnects.

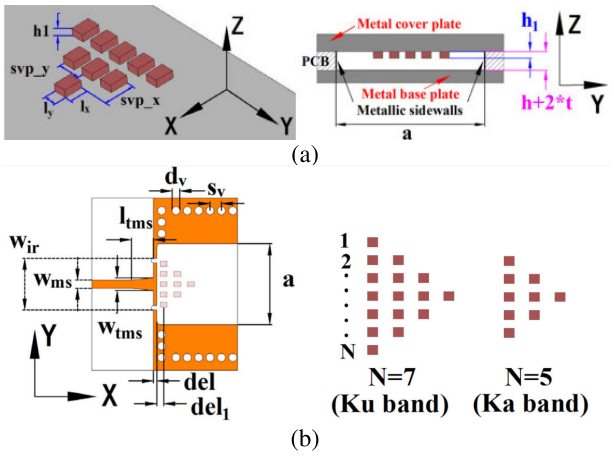


FIGURE 22. MSTL to Air Filled SIW - Classic Double Layer with Supporting Substrates [43].

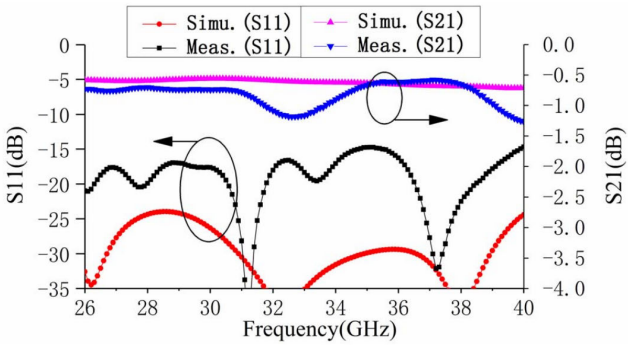


FIGURE 23. Measured and Simulated results for S_{11} and S_{21} [43].

are concerned. Therefore, it is desirable to have a direct interconnect rather than coupling power first to SIW and then to AFSIW. Although the reported [11], [49] can be used to develop interconnect in this, however, a lot of work is needed. Therefore, there is a lot of scope for future work, which is required to fill the existing research gap for developing systems on substrate for emerging applications.

C. RWG TO AIR FILLED SIW

There is one reported work [38] in this transition category; a similar analysis is conducted and is discussed below.

1) DOUBLE LAYER

To evaluate the state of the art, the *FoM* analysis is carried out. The results in Table 1 reveal that the interconnect [38] reported by the authors gains the highest *FoM* score in terms of FoM_1 and FoM_2. The interconnect structure is shown in Fig. 16, which is very simple, where a linearly tapered waveguide feeds the EM Waves in the AFSIW cavity. The transition length L_{AFSIW} is derived, which minimizes the insertion loss and gives excellent impedance matching, is expressed as:

$$L_{AFSIW} \cong 0.35\sqrt{K_0^2\lambda^2 + K_1^2\lambda^2} \tag{17}$$

$$K_0 = \frac{\frac{(b_1-b_0)}{b_0} - \frac{a_1-a_0}{a_0}\left(\frac{\epsilon_{eff}}{\epsilon_{eff}-\left(\frac{\lambda_0}{2a_0}\right)^2}\right)}{\left(\epsilon_{eff} - \left(\frac{\lambda_0}{2a_0}\right)^2\right)^{\frac{1}{2}}} \tag{18}$$

$$K_1 = \frac{\frac{(b_1-b_0)}{b_1} - \frac{a_1-a_0}{a_1}\left(\frac{\epsilon_{eff}}{\epsilon_{eff}-\left(\frac{\lambda_0}{2a_1}\right)^2}\right)}{\left(\epsilon_{eff} - \left(\frac{\lambda_0}{2a_1}\right)^2\right)^{\frac{1}{2}}} \tag{19}$$

The measured and simulated S-parameters for this interconnect are shown in Fig. 28, and a fairly good correlation is achieved. The design steps and procedure, as discussed above, are incorporated, and the state-of-the-art design flow is shown in Fig. 29.

Considering the analytical design equations and the performance of the interconnect, it is clear that the literature is adequate. Therefore, the literature is sufficient in this case.

2) MULTI LAYER

The concept and technique presented in the double-layer case [38] could easily be extended to multi-layer scenarios by adjusting the aperture location and following a similar design flow. However, no reported works have shown the applicability of this technique on multi-layer substrate scenarios. Therefore, the literature is adequate in this case, and more work is needed, especially when SoS applications are considered.

D. COAXIAL TO AIR FILLED SIW

When considering coaxial to air-filled SIW interconnects, no works are reported in the millimeter wave range, which targets this interconnect. Therefore, there is a clear-cut research gap, and there is a lot of scope for future work in both double and multi-layer configurations for developing systems on the substrate for upcoming mmWave communication applications.

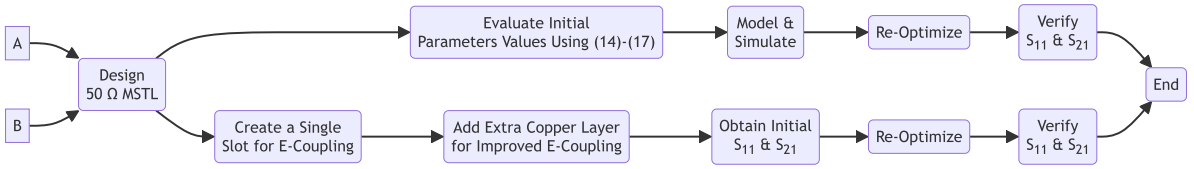
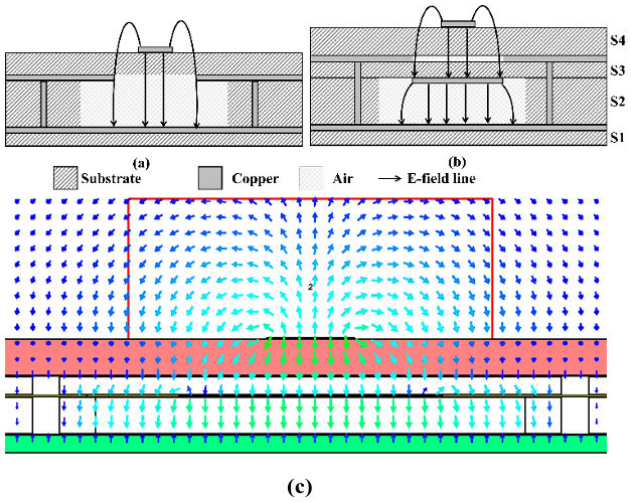


FIGURE 24. Design flow for state-of-art for MSTL to Air-Filled SIW Interconnects.



(c)

FIGURE 25. MSTL to Air Filled SIW - Multilayer [42].

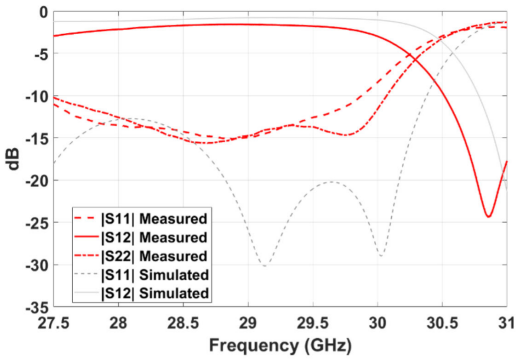
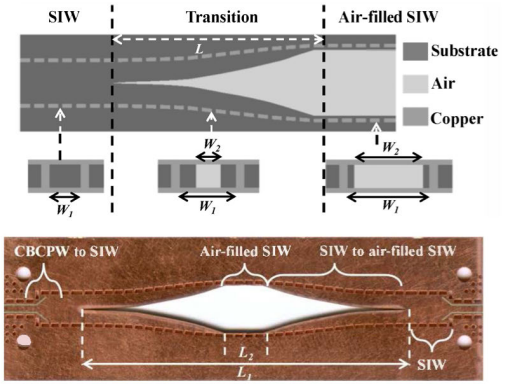
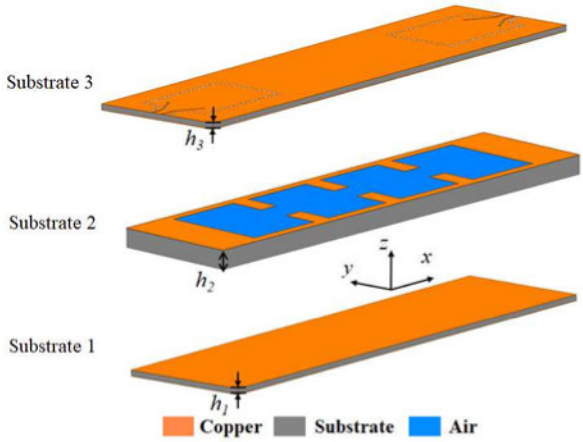


FIGURE 26. Measured and Simulated (S_{11} and S_{12}) [42].



(a) [11]



(b) [49]

FIGURE 27. CPW to AFSIW Transition in Multi-layer Configuration [11], [49].

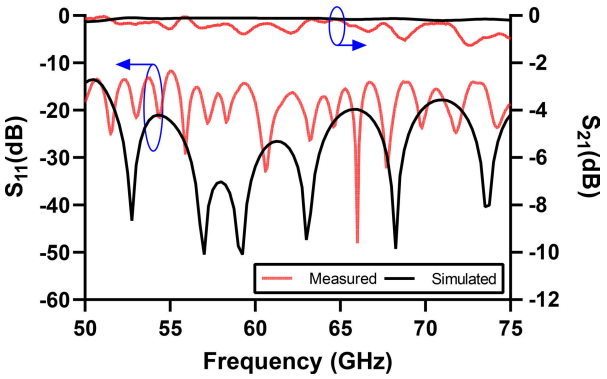


FIGURE 28. RWG to AFSIW - Double layer [38].

VI. RESEARCH GAP AND FUTURE DIRECTION

This section highlights a critical research gap in the design of multi-layer millimeter-wave (mmWave) interconnects. While numerous studies (e.g., [26], [27], [28], [32]) have established analytical equations for double-layer SIW and AFSIW configurations, their application to multi-layer structures remains limited. Conversely, multi-layer interconnect design often relies heavily on purely parametric optimization using electromagnetic (EM) solvers (e.g., [42]).

This necessitates further research encompassing SIW and AFSIW technologies, particularly for multi-layer configurations. A comprehensive investigation that leverages analytical modeling alongside optimization techniques would significantly enhance the performance of on-substrate mmWave systems. The performance metrics, FoM_1 and

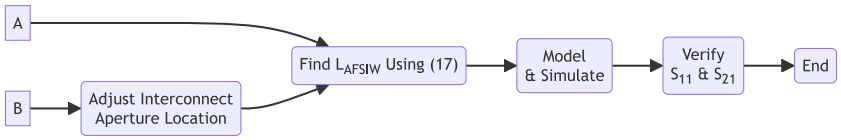


FIGURE 29. Design flow for state-of-art for RWG to Air-Filled SIW Interconnects.

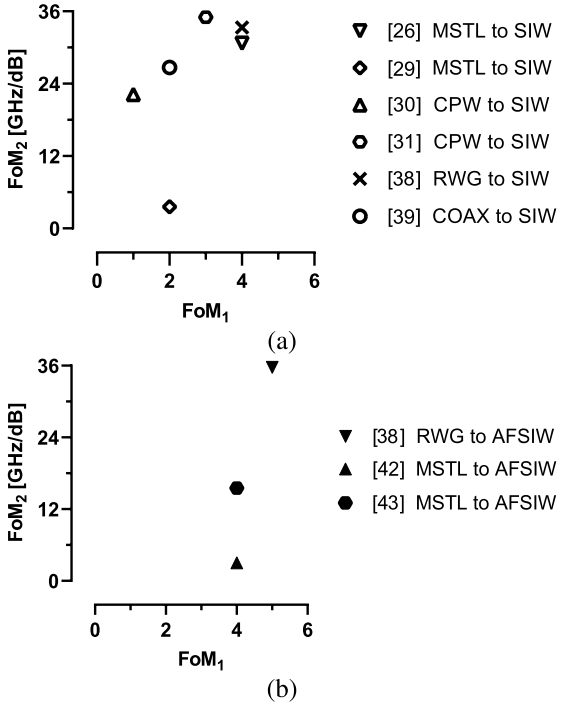


FIGURE 30. FoM Comparative Analysis for different transition technologies (a) SIW (b) AFSIW.

FoM_2, further highlight the research gap. As observed in Figure 30(a) and (b), a significant difference exists between the FoM values for double and multi-layer configurations. Interconnects with higher FoM values in the upper right quadrant of the FoM_2 vs. FoM_1 plot are generally preferred.

For future applications targeting the upper mmWave regime, AFSIW emerges as a promising choice due to its inherently lower losses and broader bandwidth capabilities [38]. However, realizing this potential necessitates addressing certain limitations. Notably, the current literature on high-performance AFSIW interconnects in double and multi-layer configurations remains limited. Furthermore, existing studies, apart from those presented by the authors in [38], exhibit potential performance issues and design complexity challenges associated with AFSIW interconnects. These limitations warrant further investigation to fully harness the potential of AFSIW technology for future mmWave systems.

The findings emphasize the need to bridge the research gap in multi-layer mmWave interconnects. Developing robust analytical models for AFSIW and SIW interconnects in both double and multi-layer configurations, coupled with efficient optimization techniques, will pave the way for high-performance mmWave systems.

Therefore, it is clear that the literature is shallow at a macro level, and more work is needed to fully utilize the SIW technologies, which aim to support the future of millimeter wave communication.

VII. SIW TECHNOLOGY DEVELOPMENT WITH A COMMERCIAL PERSPECTIVE

SIW technologies are predicted for a promising future for high-frequency communication systems. This optimism stems from a compelling alignment between SIW technologies capability and the evolving needs of the industry, as the industry struggles with surging demand for high-bandwidth mmWave systems in telecommunications, automotive radar, aerospace, and defense perfectly matching SIW Technolgies's ability to handle these high frequencies [9]. Moreover, SIW technologies offer a significant advantage in terms of manufacturability, because of its ability to integrate seamlessly with established PCB manufacturing processes, which enables cost-effective mass production, making it a practical choice for large-scale applications with scalability [38].

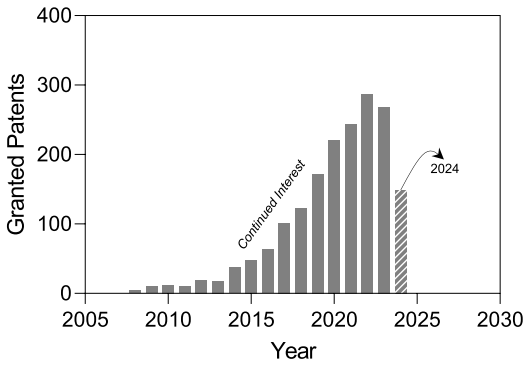


FIGURE 31. Granted Patents for components based on SIW technologies since 2005 (Scopus Data).

Furthermore, developments in substrate materials hold the potential to unlock even greater performance from SIW technologies. The use of innovative materials, such as glass substrates, as evident from a recently granted patent [18], presents an exciting possibility for reducing signal losses and achieving high-performance. This enhanced performance makes SIW technologies an even more attractive candidate for the demanding requirements of emerging applications.

The high data rates, low latency, and robust reliability needed for these next-generation networks are highly favorable to the inherent properties of SIW technologies. This interest is clearly evident from Figure 31, which shows an exponential growth in granted patents for components based on SIW technologies in the recent decade, including contributions from key industry companies such as Huawei [50], Samsung [51], Sony [52], Ericsson [53], Infineon [54], and Honeywell [55].

However, for SIW technologies to achieve full potential utilization, it must address some key challenges. As highlighted in Sections IV, V, and VI, there are limitations in the current understanding of high-performance multi-layer SIW and AFSIW interconnects. Addressing these research gaps and challenges are crucial for unlocking the technology's full potential, along with miniaturization, integration, tunability, and non-linearity issues [9]. Additionally, SIW needs to establish a clear competitive advantage over existing technologies, demonstrating superior performance in these scenarios will be critical for widespread market adoption. Fortunately, strategic partnerships can play a vital role in overcoming these challenges. Collaboration between industry partners and academia can foster further development and full-scale commercialization of SIW technologies.

To summarize, SIW technologies possess a unique combination of strengths that make them highly promising for the future of high-frequency communication systems. Their alignment with industry demands, compatibility with existing manufacturing processes, and potential for performance improvements through material innovations position them for significant growth. By overcoming the challenges related to interconnects, along with miniaturization, integration, tunability, and non-linearity issues [9], while also establishing a clear competitive edge, SIW can solidify its place as a key technology in the development of next-generation communication systems. Strategic industry partnerships will be instrumental in achieving this goal and unlocking the full commercial potential of SIW technologies.

VIII. CONCLUSION

This work addressed the critical challenge of interconnecting SIW technologies with traditional transmission lines at millimeter-wave (mmWave) frequencies. A key contribution is the introduction of a Figure of Merit (*FoM*) for the first time encompassing both qualitative and quantitative aspects to assess the performance of various interconnects in both double and multi-layer configurations. Thus, the *FoM* facilitates the identification of the optimal interconnect solution for specific design requirements.

Furthermore, the work establishes a state-of-the-art design flow for each considered interconnect type, supported by existing design equations. This comprehensive approach streamlines the design process for mmWave SIW technologies interconnects. The proposed FoM not only serves as a valuable design tool but also unveils critical research gaps. The lack of well-defined design methodologies and supporting equations, particularly for higher mmWave frequencies, presents a significant opportunity for future advancements.

This research emphasizes the limitations of current design approaches, especially for multi-layer configurations, which often rely heavily on EM optimizations. The development of analytical solutions represents a promising future direction, as it holds the potential to enable the design of high performance with wider operating bandwidths and lower insertion losses with a short design cycle.

To summarize, this work, through the introduction of the FoMs and the exploration of the design process as well as the identification of research gaps and future direction with a commercial perspective, paves the way for significant advancements in mmWave system integration on substrates. This novel approach offers valuable guidance and tools for researchers and engineers working in this rapidly evolving field.

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