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RESEARCH ARTICLE

Hybrid Digital/Analog Predistorter Architecture With Enhanced Robustness to Hardware Impairments

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ABSTRACT In this paper, a hybrid predistortion architecture that allies the benefits of digital and analog predistortion techniques is investigated. This Hybrid Digital/Analog Predistorter (H-DAPD) uses a low order memory polynomial as a baseband digital predistortion function. To alleviate the complexity of the analog predistorter implementation, an amplitude only predistortion function is adopted. The analog predistortion function is used to perform a coarse linearization of the amplifier. The digital predistortion function is then applied to linearize the system made of the analog predistorter and the power amplifier. The H-DAPD predistortion system is found to be superior to purely analog and to purely digital predistortion systems by combining key advantages present in each of these systems. The robustness of the proposed H-DAPD with respect to the hardware impairments that are typically associated with the implementation of analog predistortion is thoroughly discussed, and shown to be superior to that of conventional hybrid and analog predistortion systems. Experimental validation performed on a commercial power amplifier prototype using 5G new radio (NR) test signals demonstrates the enhanced robustness of the proposed H-DAPD to hardware impairments. It was found that standard compliant adjacent channel leakage ratio is obtained with up to 0.3dB resolution in the analog predistorter's AM/AM function, and up to 3ns delay misalignment between the input and control signals of the analog predistorter. The proposed system is expected to pave the road for future hybrid predistortion systems.

INDEX TERMS Analog predistortion, digital predistortion, memory effects, nonlinear distortions, power amplifiers.

I. INTRODUCTION

In modern communication infrastructure, the power amplifier (PA) exhibits dynamic nonlinear behavior emulated by the amplitude-modulated nature of the signals being transmitted. This issue has been constantly critical given the continuous evolution of wireless communication standards that is driven by the aim to support more users with a wider range of services. This evolution has incessantly resulted in increased signal bandwidths from one generation to the next. As a matter of fact, fifth generation (5G) systems are being designed to handle up to 100MHz of signal bandwidth in the frequency range 1 (FR1) spanning from 410MHz to 7125MHz, and up to 400MHz of instantaneous signal bandwidth in frequency range 2 (FR2) between 24.25GHz and 52.60GHz [1]. These bandwidths pose severe constraints on the electronic circuitry needed to implement the linearization of the power amplifier.

Predistortion is considered as the preferred linearization technique for radio frequency power amplifiers especially for base station applications and gNodeB where the additional power consumption of the predistorter is leveraged by its impact on the amplifier's efficiency. This approach consists of applying, upstream of the PA, a nonlinear function that is complimentary to the nonlinearity exhibited by the power

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amplifier so that the cascade made of the predistorter and the PA operates as a linear amplification system. Conceptually, predistortion can be implemented either in the analog domain or in the digital domain [2], [3]. The radiofrequency (RF) analog implementation of predistortion has been reported using a variety of analog nonlinear circuits such as diodes and transistors [4], [5], [6], [7]. However, the use of such intermodulation generators makes it difficult to update the predistortion function in order to ensure that it continuously matches the nonlinear distortions of the PA. This is especially critical given that the PA distortions can be signal and power dependent in addition to being affected by drifts and aging factors. Moreover, the ability of RF analog predistorter (APD) systems to compensate for power amplifiers distortions in the presence of memory effects remains very limited. For these reasons, baseband digital predistortion techniques have been widely adopted for communication systems infrastructure. However, while the digital implementation of the predistortion function enables the compensation of memory effects and the synthesis of accurate nonlinear functions that lead to better intermodulation distortion reduction compared to the analog implementation, it sets stringent requirements on the transmitter hardware especially in the presence of wideband signals. In fact, the use of a digital predistorter (DPD) introduces wanted nonlinearities causing the bandwidth of the predistorted signal to be typically five times that of the original input signal.

To resolve the above mentioned limitations of analog and digital predistortion techniques, hybrid approaches have been considered [8], [9], [10], [11]. In [8], a predistortion system that combines digital and analog controls was proposed. In this early work, two predistortion layers were successively applied on the input signal. However, both predistortion methods were applied in the analog domain on the envelope of the RF signal through the use of a vector modulator. In [9], analog RF predistortion was augmented by allowing for the compensation of memory effects using a reformulation of the envelope memory polynomial model in order to compensate for mild memory effects. The main limitation of this architecture is that the predistortion function used is restricted to the envelope memory polynomial model. The use of digitally implemented predistortion function along with an analog predistortion function was proposed in [10] and [11]. The authors in [10] proposed the use of a diode based analog predistorter to reduce the out-of-band distortions in a dual-band scenario. A DPD was then used to compensate for the in-band distortions. The joint DPD and APD, recently proposed in [11], uses a diode based analog predistorter to implement a first layer of predistortion aiming at limiting the distortions present in the adjacent channel and is later followed by a bandlimited DPD system, which focuses on the compensation of the residual in-band distortions. In both [10] and [11], the analog predistortion was implemented using a diode based circuit. This negatively impacts the ability of the APD to mimic different nonlinearity profiles, and hence its capability to maintain its performance when the PA nonlinearity profile changes. Hence, the update of the composite predistortion function can only be achieved through the DPD sub-function. In this paper, a hybrid digital analog predistorter (H-DAPD) is proposed in order to address the above mentioned limitations. The proposed predistorter is built using a combination of a DPD followed by an RF APD. The RF APD function is designed using a low complexity digitally controlled memoryless look-up-table structure allowing for easy update when the PA distortions change. This represents a major difference with prior work. The baseband DPD function is built using a low order memory polynomial function that enables memory effects compensation while maintaining a limited bandwidth of the predistorted signal in the digital domain, and ease of update given the limited number of model coefficients. The proposed predistorter allies the advantages of APD (mainly reduction of the sampling rate requirement in the transmit path) and DPD (compensation of memory effects and ease of update). Furthermore, the look-up table used for the analog predistortion function is purely memoryless. This means that it does not include any AM/PM distortions compensation. This reduces the implementation complexity of the APD function, and hence is expected to lead to an enhanced robustness to hardware imperfections when compared to the use of conventional quasi-memoryless look-up tables which include AM/AM and AM/PM compensations. It is important to note here that, in the literature, quasi-memoryless LUTs with complex valued gain (i.e. having AM/AM and AM/PM) characteristics are often referred to as memoryless as long as the LUT is indexed only by the present sample and not the history terms. This subtle but fundamental distinction between memoryless and quasi-memoryless LUTs will have a noticeable positive impact on the proposed predistorter's sensitivity to impairments that are unavoidably observed in analog implementations. Hence, this paper investigates the robustness of the proposed H-DAPD to implementation imperfections of the APD block such as delay misalignment between the input and the control signals and limited gain and phase resolutions. In section II, the proposed H-DAPD is thoroughly discussed and benchmarked to state of the art predistortion techniques. A study of the robustness of the proposed predistorter with respect to the hardware imperfections is presented in Section III along with the experimental validation. The conclusions are summarized in Section IV.

II. PROPOSED HYBRID DIGITAL / ANALOG PREDISTORTER

Hybrid digital baseband / analog RF predistortion architectures appear as a suitable alternative for emerging applications where bandwidth requirements are very demanding. The proposed H-DAPD is depicted in Fig. 1. In this architecture, the input signal (x_{in_DPD}) is applied at the input of the digital predistortion sub-function. The resulting digitally predistorted signal (x_{out_DPD}) is then converted to the analog domain in the main signal path where it will be later up-converted to the RF carrier frequency. The signal x_{out_DPD} is also fed into the analog predistorter's controller, which

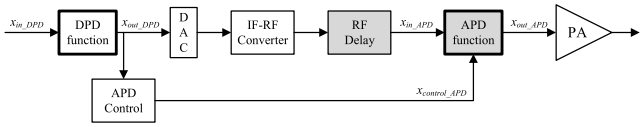

FIGURE 1. Proposed hybrid digital/analog predistortion architecture.

will generate the control signal $(x_{control\_APD})$ of the analog predistortion function. The main signal path includes an RF delay element which is used to synchronize the input signal of the APD (x_{in_APD}) with its control signal.

Hybrid predistortion systems can lead to solutions that combine the benefits of digital and analog implementations. This is maximized in the considered design by using a low complexity analog predistortion function which will be shown to have simplified implementation and better robustness to hardware imperfections. Moreover, the use of this analog predistortion function will perform a coarse memoryless linearization which will make the system composed of the analog predistorter and the nonlinear amplifier behave as a mildly nonlinear system with memory effects. Hence, reducing the nonlinearity order of the digital predistortion function since the spectrum regrowth at the output of the predistorter is of the same order as that of the system being linearized. Accordingly, this will in turn reduce the bandwidth of the digitally predistorted signal and therefore the sampling rate required by the digital to analog converter (DAC) in the transmit path as demonstrated in [12]. Accordingly, the digital predistortion block in the proposed H-DAPD will have low complexity and require slower DAC when compared to a purely digital predistortion system. Thus, the main purpose of the proposed H-DAPD is to relax the requirements on tolerable hardware impairments and improve the performance of analog predistortion systems by combining them with a digital predistortion block. By doing so, it is also possible to relax the requirement on the sampling rate of the digital to analog converter used in the transmit path of digital predistortion systems. Hence, the hybrid approach allows both predistortion functions to cohesively benefit from each other leading to a system level architecture able to extend the use of digital predistortion systems for signals having wider bandwidths that cannot be handled by the sampling rate of state of the art digital to analog converters.

The digital predistortion function can be implemented using a variety of functions commonly used for such purposes. In this work, a conventional memory polynomial function is adopted. Hence, the DPD output signal (x_{out_DPD}) is given by:

$$x_{out\_DPD}(n) = \sum_{i=1}^{N} \sum_{j=0}^{M} a_{ij} x_{in\_DPD}(n-j) \left| x_{in\_DPD}(n-j) \right|^{i-1} \tag{1}$$

where a_{ij} are the complex valued DPD coefficients, M and N are the memory polynomial's memory depth and nonlinearity order, respectively.

It is important to note here that the DPD can be implemented using any of the well-established DPD functions such as generalized memory polynomials, Volterra series, etc. The key factor to consider is that the DPD function will be used to compensate for the residual distortions observed in the cascade made of the APD function and the device under test and hence a reasonably complex function (such as the MP) is an adequate option.

The APD function is built using a memoryless gain model. Typically, memoryless predistortion functions can be implemented using either polynomial functions or more conveniently a look-up-table. The look-up table memoryless gain is a function of the magnitude of the APD input signal $(|x_{in\_APD}(t)|)$. Hence, the APD control block derives the control signal $(x_{control\_APD})$ needed to implement the analog predistorter's memoryless look-up table relationship while taking into account the characteristic of the APD used. For example, when the analog predistorter is implemented using a voltage-controlled attenuator, the APD control block will be used to compute the signal $x_{control\_APD}$ while taking into account the voltage-attenuation characteristic of the APD and the desired gain/attenuation. The APD transfer characteristic is given by:

$$x_{out\_APD}(t) = G_{APD}\left[x_{control\_APD}(t)\right] x_{in\_APD}(t) \tag{2}$$

The control signal of the analog predistorter is function of the power of the input signal (x_{in_APD}) which is in turn function of the DPD output signal (x_{out_DPD}). The APD control unit of the predistorter implements this dependency.

The major sources of hardware imperfections in the analog predistorter are mainly the RF delay element and the APD function accuracy. First, with respect to the delay line to be used to synchronize the signal and control paths of the analog predistortion sub-function. Here, it is impractical to have a perfect time alignment between the two paths. Hence, minimizing the delay misalignment between the two paths and most importantly enhancing the predistorter robustness to such delay misalignment is essential. Therefore, it is important to have a predistorter architecture that can maintain the linearization performance over a realistic range of delay misalignment. Second, the implementation of the analog power-dependent memoryless nonlinear function is often accompanied with limited resolution of the control signals or the implemented gain function. While this limited resolution is imposed by the available components in the market, their impact on the predistortion function performance can be reduced by a proper system-level design.

Accordingly, taking into consideration that the analog implementation of the RF predistortion sub-function is often accompanied with unavoidable hardware imperfections, it is essential to reduce the complexity of this sub-function and devise a structure and an identification approach that will minimize the impact of these hardware imperfections on the overall performance of the H-DAPD. Typical APD functions consist of a quasi-memoryless complex gain function, which includes AM/AM and AM/PM characteristics. In order

to reduce the complexity of the APD function, and hence, enhance its resilience to hardware imperfections, a memoryless scalar gain function is adopted. The memoryless scalar gain function used in this work consists of a memoryless AM/AM only predistortion that is indexed by the input power of the x_{in_APD} signal through the control signal $x_{control\_APD}$. It is important to note that the use of an AM/AM only predistortion function has additional advantages. Since there is no need for a power-dependent phase-shift (AM/PM) predistortion function, the hardware implementation will be much simpler. The scalar gain function can be implemented using a variable gain amplifier or a variable attenuator avoiding the need for the use of phase shifters. In addition to the complexity reduction of the APD function implementation, the use of a reduced complexity scalar-gain analog predistorter reduces the complexity of the APD control algorithm since only one single control signal is needed for the AM/AM function.

To enhance the hybrid predistorter robustness to the hardware impairments originating from the APD function, a two-steps identification procedure is proposed as depicted in Fig. 2. First, both digital and analog predistortion functions are set to unity (by-passed), and only the PA is characterized. The obtained input and output baseband waveforms are processed to synthesize the APD function. The data acquired from this first characterization step is used to synthesize the analog predistortion function, which will be applied to perform a coarse linearization of the DUT. Then, the APD function is applied and a second characterization is performed. In this second characterization, the device under test (DUT) consists of the APD function and the PA. This allows for the capture of the impairments caused by the APD hardware imperfection as part of the data used to synthesize the digital predistortion function. Therefore, the digital predistortion function will attempt to compensate for the additional impairments that are due to the imperfections of the APD function. Hence, the digital predistortion function aims at compensating any residual nonlinearity as well as the PA's memory effects that have not been addressed by the APD function. This sequential identification approach contrasts with common procedures used for the identification of two-box based predistorters where both predistortion sub-functions are derived from the same characterization through a data de-embedding process.

The two-box architecture of the H-DAPD can be adopted to reduce the sampling rate requirements of the digital to analog converter in the signal transmit path [12]. This is because the analog RF predistortion sub-function performs a coarse linearization of the power amplifier. Hence, the resulting partially linearized power amplification system, made of the APD function and the PA, behaves as a mildly nonlinear system, therefore reducing the nonlinearity order needed for the digital predistortion function. In turn, this will reduce the spectrum regrowth in the DPD output signal (x_{out_DPD}), and consequently reduce its effective bandwidth. This will translate into relaxed requirements on the DAC of the signal transmit path.

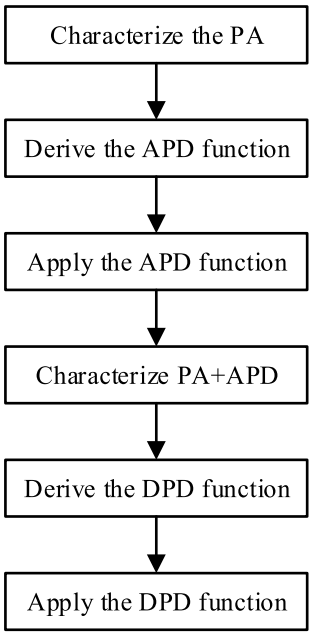

FIGURE 2. Identification procedure for the H-DAPD.

According to the details provided above, it appears that the proposed H-DAPD architecture allies the advantages of DPD systems (ability to synthesize accurate predistortion function) and that of the APD systems (relaxing the sampling rate of the DAC in the signal transmit path).

In order to assess the value of the proposed H-DAPD system, it is important to compare its key features to other predistortion systems. Table 1 presents a summary of the key features of various predistortion techniques. The considered predistortion techniques include the standard digital baseband predistortion (referred to as digital predistortion) [2], the conventional RF analog predistortion (referred to as RF analog predistortion) [2], the digitally assisted RF analog predistortion [9], and the proposed H-DAPD. Fig. 3 presents simplified block diagrams of the digital predistortion, RF analog predistortion and the digitally assisted RF analog predistortion systems.

The key features used to benchmark these various predistortion techniques in Table 1 include the linearization performance, the predistortion function flexibility, the hardware complexity associated with the implementation of each of these techniques, the sampling rate required in the ADC used in the signal transmit path, the sensitivity of the predistorter performance to hardware impairments, and the update complexity.

Baseband digital predistortion often results in high linearization performance due to its high flexibility in terms of predistortion function formulation and its ease of update and its ability to compensate for memory effects. Conversely, RF analog predistortion techniques offer a fairly low flexibility in terms of predistortion function synthesis which impacts their linearization capability, especially in the presence of memory effects, and makes them complex to update.

TABLE 1. Comparison of key features of predistortion techniques.

Features	Digital Predistortion		RF Analog Predistortion		Digitally Assisted RF Analog Predistortion		Hybrid Digital/Analog Predistortion	
Linearization Performance	High	★★★	Low	★	Medium	★★	High	★★★
Predistortion Function Flexibility	High	★★★	Low	★	Low	★	High	★★★
Update Complexity	Low	★★★	High	★	Medium	★★	Low	★★★
Hardware Complexity	Low	★★★	Medium	★★	High	★	Medium	★★
Transmit path ADC Sampling Rate	High	★	Low	★★★	Low	★★★	Low	★★★
Sensitivity to Hardware Impairments	Low	★★★	Medium	★★	High	★	Low	★★★

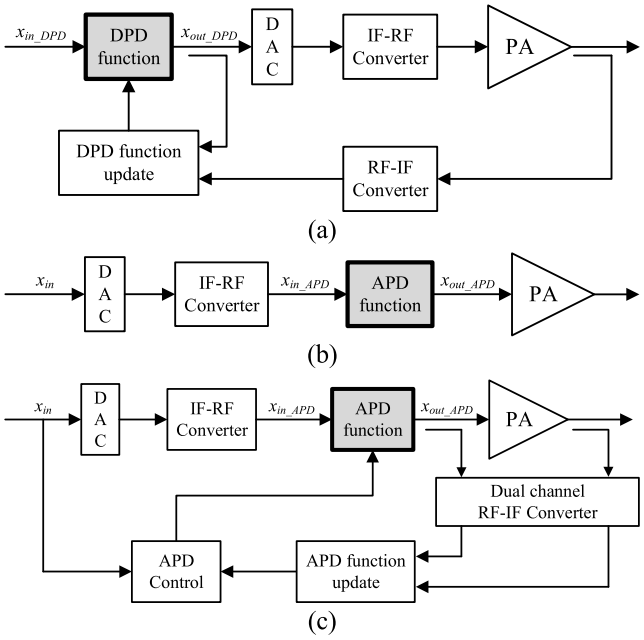

FIGURE 3. Simplified block diagrams of conventional predistortion technique. (a) baseband digital predistortion, (b) RF analog predistortion, (c) digitally assisted RF analog predistortion.

Digitally assisted analog RF predistortion offers better performance than its purely analog counterpart but it does not achieve the high linearization capability of digital predistortion systems. The use of digital control signals enables the digitally assisted RF analog predistortion systems to have some flexibility in the implementation of the predistortion function such that the predistortion function update complexity is lower than purely analog RF predistortion systems. On the other hand, the hardware complexity of digital predistortion is low since it consists of a simple feedback path, and the predistortion function is implemented in the digital domain. However, this sets strict requirements on the sampling rate needed in the digital to analog converter of the signal transmit path. On the other hand, RF analog predistortion technique implements the predistortion function in the analog domain which often results in additional hardware complexity when compared to digital predistortion, but this alleviates the sampling rate constraint on the digital to analog converter in the signal transmit path. This advantage is also shared with the digitally assisted RF analog predistortion technique. However, this latter technique has a more complex hardware implementation than all other predistortion techniques. This is mainly because digitally assisted predistortion requires strict time alignment between the control signal and the transmitted RF signal to ensure acceptable linearization performance. Moreover, the digitally assisted RF predistortion system includes a feedback path that is used to derive the control signals of the analog RF predistorter. Typical analog RF predistortion systems do not have a feedback path, thus limiting the ability to update the predistortion function to track the changes in a PA's behavior. The requirements on the signal sampling rate in the transmit path represent the main drawback of digital predistortion and the main advantage of analog and digitally assisted RF predistortion systems. The proposed H-DAPD attempts to alleviate the limitation in digital predistortion systems by combining the use of a highly nonlinear digitally assisted RF predistortion function with a mildly nonlinear baseband digital predistortion function. Furthermore, analog predistortion techniques are sensitive to hardware impairments. The performance of analog RF predistortion systems heavily relies on their ability to accurately mimic the desired predistortion function, and any impairments will have a direct impact on the linearization performance. On the other hand, the sensitivity of digitally assisted RF predistortion systems to hardware impairments is comparatively higher than that of the purely analog ones due to the need for accurate time delay alignment between the signal in the transmit path and the APD control signals. Moreover, the accuracy and resolution of the predistortion function must be high to meet the stringent linearity requirements of modern communication standards. Lastly, most RF predistortion techniques do not account for the impairments caused within the signal transmit path before the power amplification stage. Conversely, digital predistortion is much less sensitive to hardware impairments since the predistortion function is implemented in the digital domain, and the feedback loop encompasses the signal transmit path to enable compensation for impairments such as IQ imbalance and DC offsets. In the proposed H-DAPD, the presence of the RF analog predistortion creates a sensitivity to said hardware impairments. However, the digital predistortion function allows for relaxing such sensitivity, as will be demonstrated in the next section.

III. HYBRID DIGITAL/ANALOG PREDISTORTER ROBUSTNESS TO HARDWARE IMPAIRMENTS

In this section, the robustness of the H-DAPD system to hardware impairments is investigated. The focus will be on the delay misalignment between the APD input signal (x_{in_APD}) and its control signal $(x_{control\_APD})$, and the limited resolution of the APD function. The study will be carried in three steps. First, the effects of the delay misalignment will be investigated. Then, the effects of the limited resolution in the APD function will be assessed assuming that there is no delay misalignment. Finally, the impact of the coexistence of the above mentioned two types of impairments on the H-DAPD performance will be investigated. In order to evaluate the advantages of the proposed H-DAPD architecture, a conventional hybrid predistorter in which the APD function is implemented as a complex memoryless gain (including AM/AM and AM/PM compensation) is used as a benchmark.

A. DEVICE UNDER TEST AND EXPERIMENTAL SETUP

The device under test utilized includes a commercial evaluation board of a class AB Gallium Nitride (GaN) based power amplifier (model CGH40010-AMP from Wolfspeed). A ZHL-42, from Mini-Circuits, was used as a driver. The DUT considered in this work refers to the power amplifiers lineup made of the power amplifier and its driver. The main test instrument utilized was the Anritsu MS2830A, which is composed of a vector signal generator (VSG) and a vector signal analyzer (VSA). In this instrument, the bits resolutions of the VSG and the VSA are 16 bits, and 14 bits, respectively. Fig. 4 depicts a photograph of the experimental setup.

The signal processing related to the predistortion functions synthesis is performed within a computer environment. For the purpose of this study, the APD function was implemented in Matlab using a realistic look-up table model that allows for the inclusion of hardware imperfections such as delay misalignment and limited resolution. Analog domain implementation of the APD function can be done using an RF vector multiplier, or a voltage controlled attenuator (since only AM/AM compensation is required in the proposed H-DAPD).

The signal that was used in this work is a 40 MHz 5G New Radio (NR) test signal sampled at 153.6MHz and having a peak-to-average-power ratio (PAPR) of 10.4dB. The RF signal was centered at a carrier frequency of 2.425GHz. During the experimental validation, the transmit path's DAC of the VSG and the feedback path's analog to digital converter (ADC) of the VSA were both operating at 153.6 MHz. The DUT's AM/AM and AM/PM characteristics, observed with the 40MHz 5G test signal, are reported in Fig. 5. This figure shows that the DUT exhibits a nonlinear behavior with strong memory effects as inferred from the dispersion of its AM/AM and AM/PM characteristics.

The proposed H-DAP was initially applied to linearize the DUT. In this test, and all subsequent ones, the H-DAPD functions were successively derived as per the flow chart of Fig. 2.

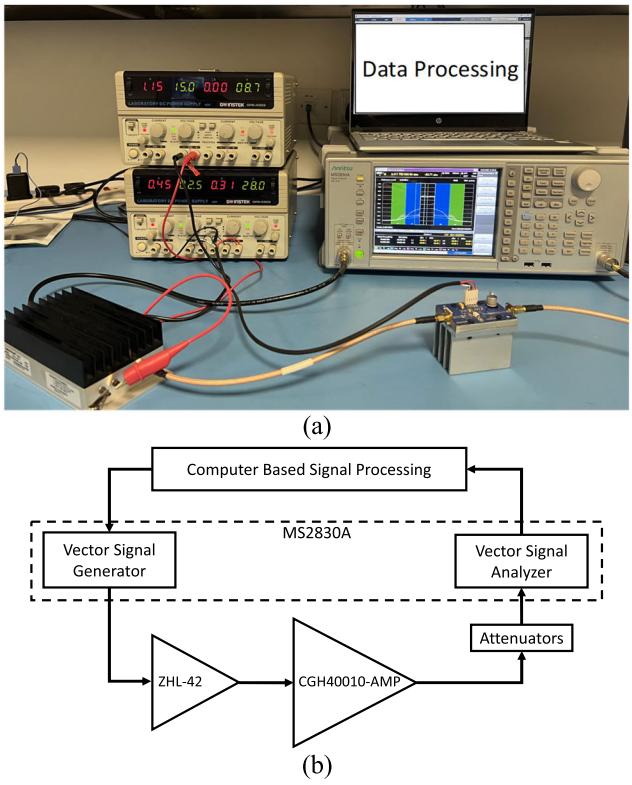

FIGURE 4. Experimental setup. (a) Photograph of the experimental setup, (b) block diagram of the experimental setup.

In both characterization steps of the H-DAPD synthesis, the 5G NR test signal was applied at the input of the system. The time delay between the input and output waveforms was estimated and compensated for. The resulting time-aligned waveforms were then used along with the indirect learning technique to derive the corresponding predistortion function. The APD look-up table was derived using the dynamic exponential weighted moving average algorithm [13]. In these initial results, the APD function used was formulated as a look-up table in which no implementation related hardware impairments were taken in to consideration. In this sense, the resolution of the LUT gain was unconstrained, and it was assumed that the control signal of the APD $(x_{control\_APD})$ is perfectly time aligned with the APD's input RF signal (x_{in_APD}). The resulting AM/AM transfer characteritic of the APD is presented in Fig. 6. The DPD function used in all tests in a memory polynomial having a nonlinearity order $N = 5$ and a memory depth $M = 3$. The coefficients of the memory polynomial model were derived using the least squares method and the pseudo-inverse calculation.

The spectra measured at the output of the amplifier before and after linearization are reported in Fig. 7. This figure shows that the proposed H-DAPD structure is able to linearize the DUT and achieve satisfactory linearity levels. The AM/AM and AM/PM characteristics of the linearized amplifier are depicted in Fig. 8. These characteristics show a perfect cancellation of the nonlinearity and minimal spread in both the AM/AM and AM/PM characteristics.

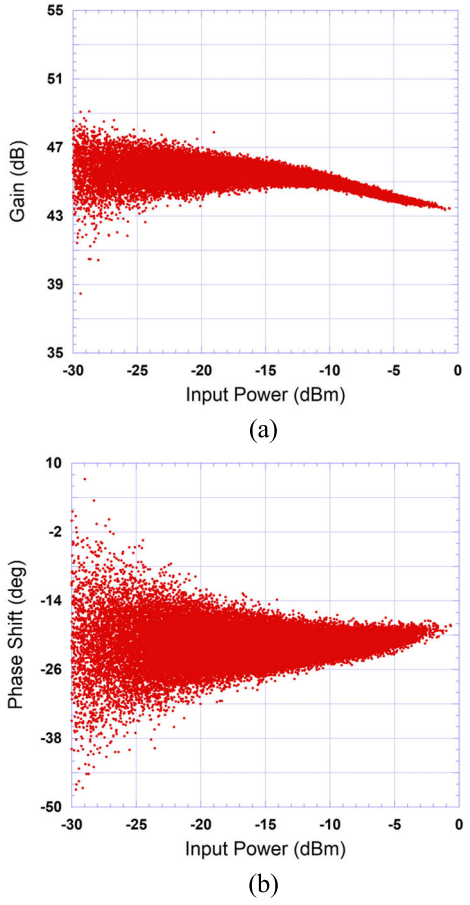

FIGURE 5. Measured characteristics of the DUT. (a) AM/AM characteristic, (b) AM/PM characteristic.

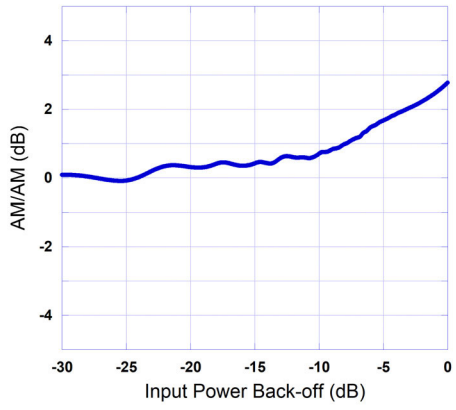

FIGURE 6. AM/AM characteristic of the ideal APD function (no resolution constraint and no time delay misalignment).

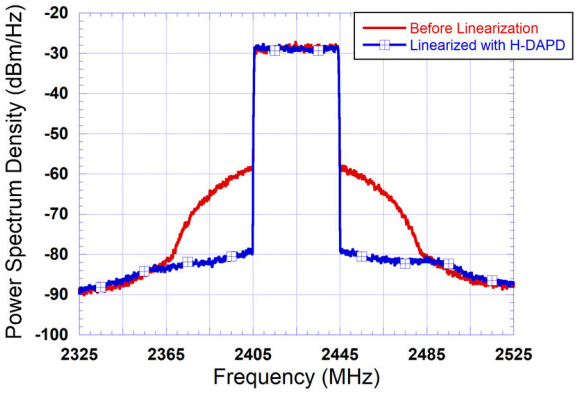

FIGURE 7. Measured spectra at the output of the amplifier.

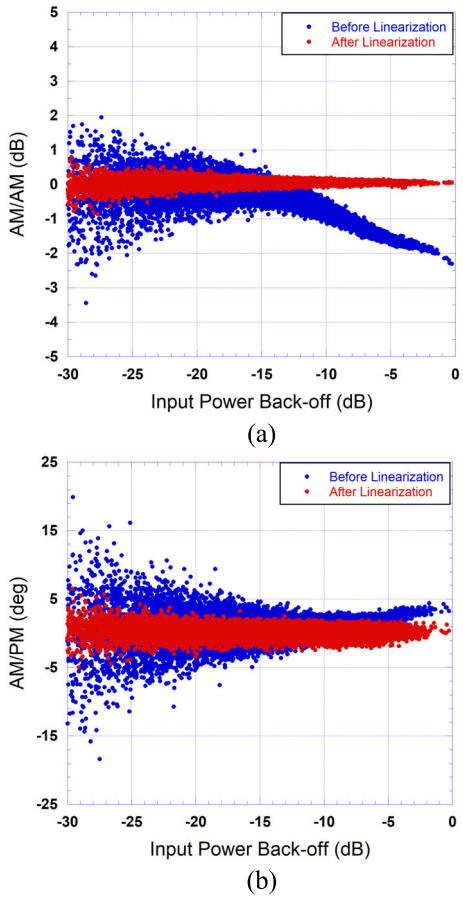

FIGURE 8. Measured characteristics of the DUT after linearization using the H-DAPD. (a) AM/AM characteristic, (b) AM/PM characteristic.

In next sub-sections, the effects, on the H-DAPD performance, of time delay misalignment between the inputs of the APD function and the effects of limited resolution in the APD gain will be investigated. It is important to point out here that the proposed H-DAPD performance will be benchmarked against its counterpart which employs an APD with both AM/AM and AM/PM compensation. It is noteworthy to mention that, in the absence of APD impairments, the performance of the proposed H-DAPD is equivalent to that of a fully digital predistorter. Moreover, the proposed H-DAPD is expected to outperform any state of the art APD in terms of ACLR performance due to the presence of an extra DPD based correction in the H-DAPD, and in terms of features (such as flexibility and adaptability) as described in the previous section. Therefore, it is believe that the only meaningful qunatitative comparison of the H-DAPD is the

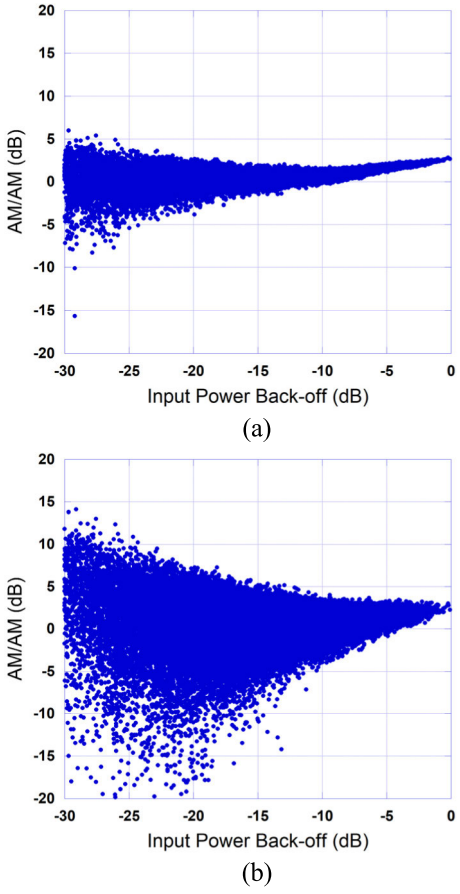

FIGURE 9. Effects of the time delay misalignment on the APD AM/AM characteristic. (a) $\Delta t = 0.65$ns, (b) $\Delta t = 2.60$ns.

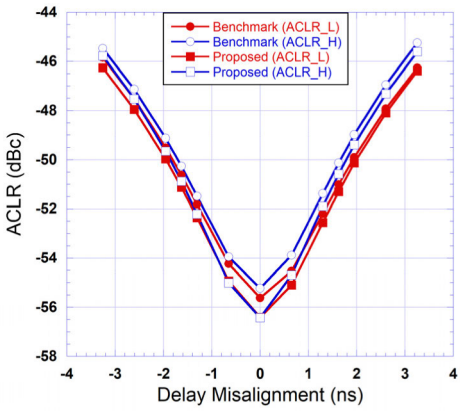

FIGURE 10. Effects of the time delay misalignment on the H-DAPD's ACLR performance.

one where it is compared to a hybrid structure which employs a conventional LUT (including AM/AM and AM/PM compensation). Comparisons of the proposed H-DAPD to purely analog RF predistorters, digitally controlled analog RF predistorters, and digital predistorters can only be qualitative and were thoroughly discussed in the previous section.

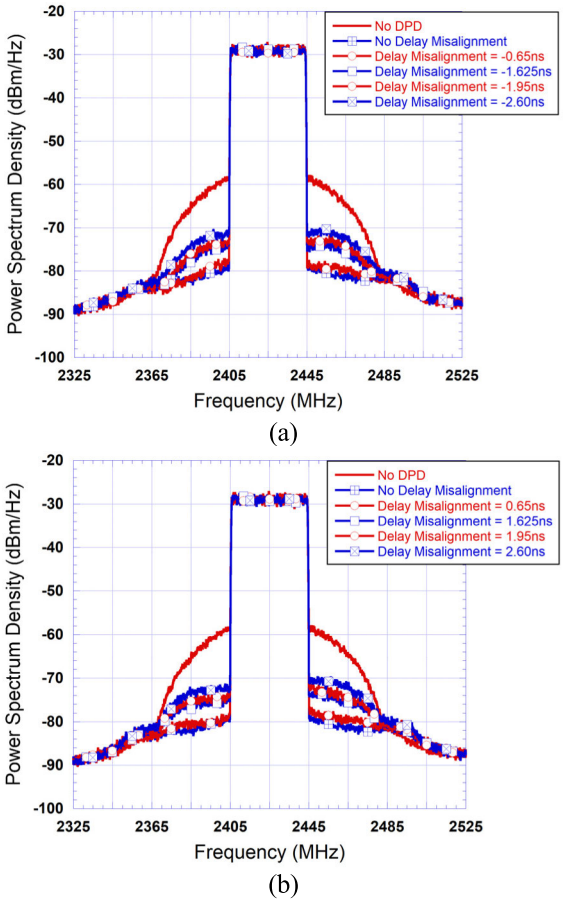

FIGURE 11. Measured spectra at the output of the linearized amplifier using the proposed H-DAPD. (a) with lagging time delay misalignment. (b) with leading time delay misalignment.

B. EFFECTS OF TIME DELAY MISALIGNMENT

The time domain misalignment between the APD control and input signals is investigated by considering a delay (Δt) between these two signals as described by Eq. (3). This delay is to mimic an imperfect time alignment between the control signal branch and the RF path to the input of the APD.

$$x_{out\_APD}(t) = G_{APD}\left[x_{control\_APD}(t + \Delta t)\right] x_{in\_APD}(t) \quad (3)$$

It is important to point out here that the considered delay is solely related to the implementation of the APD function and is independent of the time delay alignment step that is performed following the characterization and data acquisition for the purpose of deriving the APD and DPD functions.

For this study, the PA was initially characterized, and the APD function derived. Later, the APD function was implemented using Eq. (3) for various values of the delay misalignment. Then, the cascade made of the PA and the APD was characterized, and the DPD function synthesized. During this test, the DPD identification step of the H-DAPD identification procedure was performed while a variable delay misalignment (Δt) was introduced between the control signal

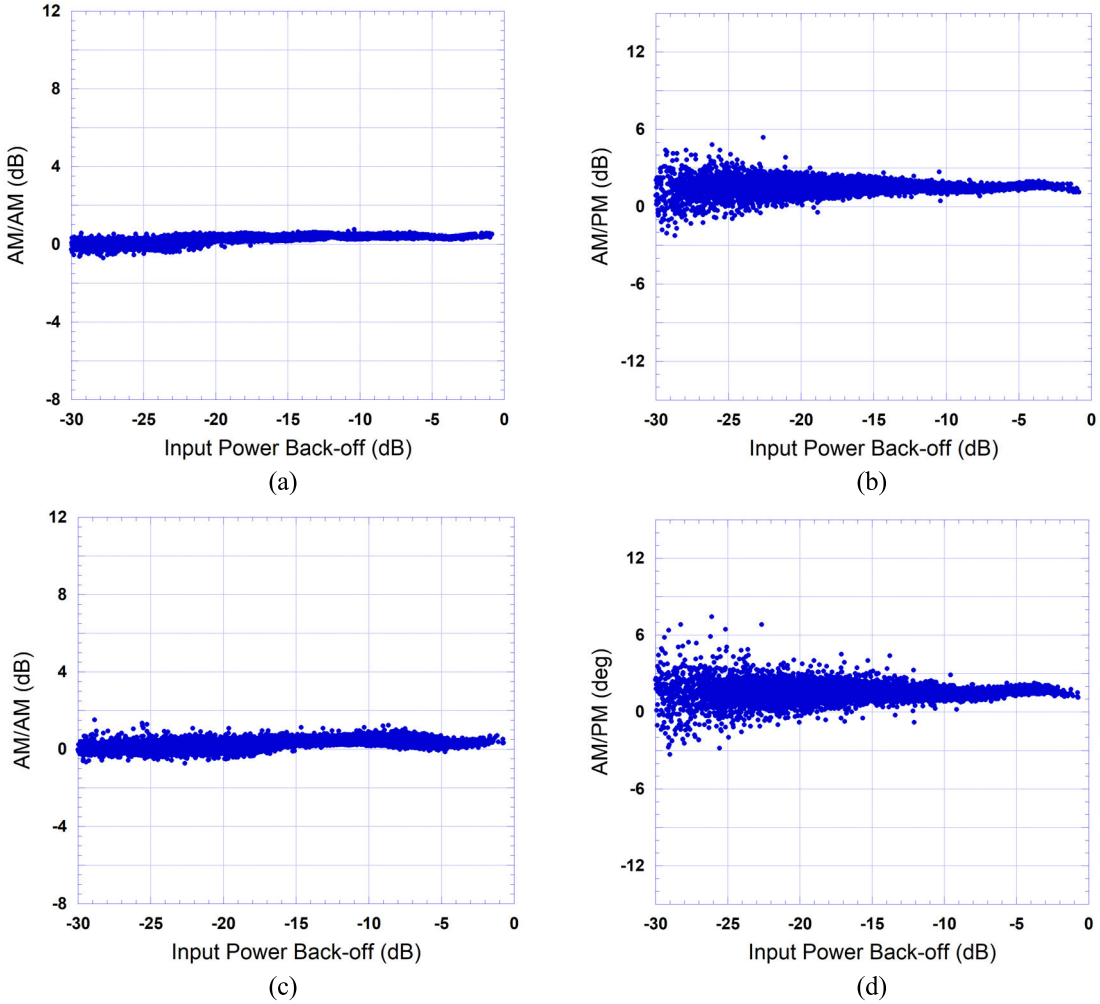

FIGURE 12. AM/AM and AM/PM characteristics of the DUT linearized using the proposed H-DAPD in presence of time delay misalignment in the APD function. (a) AM/AM with $\Delta t = 0.65$ns. (b) AM/PM with $\Delta t = 0.65$ns, (c) AM/AM with $\Delta t = 2.60$ns. (d) AM/PM with $\Delta t = 2.60$ns.

and the input signal of the APD. Finally, the DPD was applied along with the APD to linearize the power amplifiers lineup.

The delay misalignment was varied from $-0.5T$ to $+0.5T$ where T corresponds to the sampling period of the digital signal. This corresponds to an analog delay ranging from $-3.25ns$ and $+3.25ns$ for the test conditions used. The effects of the time delay misalignment on the AM/AM characteristics of the APD are reported in Fig. 9 for the values of $\Delta t =$ 0.65ns and $\Delta t = 2.60$ns. As anticipated, the time domain misalignment between the two signals at the input of the APD translates into a dispersion of its AM/AM charactersitic. The dispersion becomes more pronounced as the value of the delay misalignment increases.

The effects of the time delay misalignment on the adjacent channel leakage ratio (ACLR) performance of the proposed H-DAPD (in which the APD uses only an AM/AM) and the benchmark H-DAPD (in which the APD uses an AM/AM and an AM/PM LUT) was tested. The results, summarized in Fig. 10, show that under no delay misalignment, both DPDs achieve their best performance of around -56dBc. However, as the delay misalignment between the RF input and the control signal of the APD increases, the ACLR performance of the system decreases. As anticipated, the impact of the delay misalignment on both predistorters is quasi-identical. This is expected since both predistorters have comparable architectures and are derived from the same measurements data using the same identification procedure. For a delay misalignment of approximately 3.25ns, the ACLR performance degrades and reaches a level too close to the threshold of -45dBc which is dictated by the 3GPP 5G standards. This sets an upper limit on the delay imperfection that can be tolerated.

The spectra measured at the output of the amplifier when linearized with the proposed H-DAPD are reported in Fig. 11. This figure shows the effects of lagging and leading time delay misalignment which corresponds to negative and positive values of delay misalignment (Δt), respectively. This figure is in agreement with the results of the ACLR reported

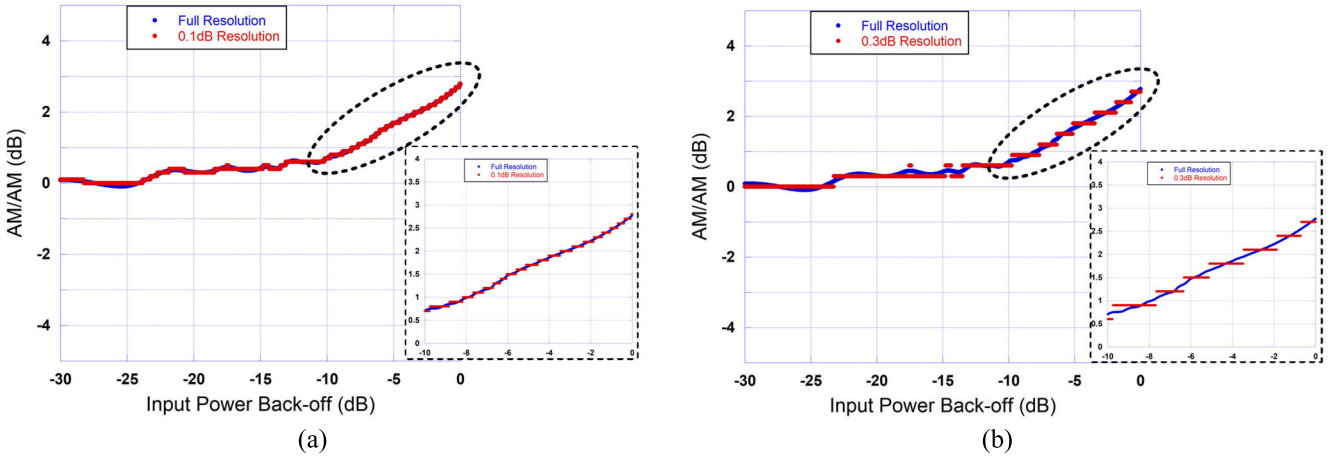

FIGURE 13. Effects of the limited resolution on the APD AM/AM characteristic. (a) 0.1dB resolution, (b) 0.3dB resolution.

in Fig. 10, which shows that the performance degradation is more pronounced for higher delay misalignment irrespective of whether it is leading or lagging.

Samples of the AM/AM and AM/PM characteristics of the cascade made of the proposed H-DAPD and the PA are reported in Fig. 12. These characteristics correspond to the cases where $\Delta t = 0.65$ns and $\Delta t = 2.60$ns. The results of Figure 12 show that the presence of time delay misalignment in the APD characteristics results in residual distortions at the output of the linearized amplifier even after the DPD function is applied. The residual distortions as seen through the AM/AM and AM/PM characteristics of the linearized PA exhibit minor nonlinearity and some dispersion. Both of these effects increase as the time delay misalignment becomes larger.

C. EFFECTS OF LIMITED RESOLUTION IN THE APD FUNCTION

In this section, the effects of the limited resolution on both the AM/AM and AM/PM functions will be investigated. To decouple the effects of such imperfections from the delay misalignment, the results derived in this section correspond to a perfect time alignment between the APD's RF input and control signals. In here, three resolutions of the AM/AM characteristic were considered (namely 0.1dB, 0.25dB, and 0.3dB). Similarly, three resolutions of the AM/PM characteristic were tested (namely 0.9°, 1.8°, and 3.6°). These values correspond to typical resolutions observed in off-the-shelve components that can be used to implement the APD function [14], [15], [16], [17].

To model the limited resolution of the APD function, the AM/AM and the AM/PM corrections were forced to discrete values using the desired resolution by using a nearest neighbor rounding algorithm. Hence, the APD gain G_{APD} of Equation (2) will be replaced by its limited resolution value $\tilde{G}_{APD}$.

TABLE 2. ACLR performance with reduced resolution in APD AM/AM and no delay misalignment and unconstrained phase resolution.

AM/AM Resolution	Ideal	0.10 dB	0.25 dB	0.30 dB
Benchmark ACLR_L (dBc)	−55.62	−54.19	−50.25	−49.01
Benchmark ACLR_H (dBc)	−55.23	−53.61	−49.37	−48.06
Proposed ACLR_L (dBc)	−56.41	−54.81	−50.51	−48.90
Proposed ACLR_H (dBc)	−56.43	−54.43	−49.63	−47.96

Therefore, the output signal of the APD function will be given by

$$x_{out\_APD}(t) = \tilde{G}_{APD}\left[x_{control\_APD}(t)\right] x_{in\_APD}(t) \quad (4)$$

In the presence of limited resolution, the AM/AM characteristic of the APD becomes discontinuous due to the discrete values of the gain. Fig. 13 depicts the AM/AM characteristics of the APD in presence of limited resolution.

Table 2 summarizes the ACLR performance at the output of the linearized amplifier for the proposed and the benchmark H-DAPD under limited amplitude (AM/AM) resolution for the APD function. These results were derived when the AM/PM APD of the benchmark model had an ideal unconstrained resolution, and without a delay misalignment between the APD input and control signals. This table shows that the performance of both H-DAPD degrades with the limited resolution in a similar manner.

At this point, it is worth mentioning that the ACLR performances of the proposed and benchmark hybrid predistorter under no impairments are equivalent to what would be obtained using the same structures in the digital domain. The ACLR obtained under such conditions are −56.4Bc and −55.4dBc, for the proposed and the benchmark H-DAPD, respectively. Conversely, a purely analog predistorter (synthesized using a look-up table model) was able to achieve

TABLE 3. ACLR performance with reduced resolution in APD AM/PM and no delay misalignment and unconstrained amplitude resolution.

AM/PM Resolution	Ideal	0.9 deg.	1.8 deg.	3.6 deg.
Benchmark ACLR_L (dBc)	−55.62	−52.61	−46.87	−41.52
Benchmark ACLR_H (dBc)	−55.23	−51.95	−46.07	−40.77
Proposed ACLR_L (dBc)	−56.41	−56.41	−56.41	−56.41
Proposed ACLR_H (dBc)	−56.43	−56.43	−56.43	−56.43

ACLR levels of −41.9dBc and −39.2dBc in the lower and higher adjacent channels, respectively. This shows that a purely analog predistorter, which is not able to compensate for memory effects, is not suitable for the linearization of the device under test.

Table 3 reports the ACLR performance at the output of the linearized amplifier under limited phase resolution (AM/PM) for the APD function. For these results, no time misalignment was present between the APD input and control signals. Moreover, the resolution of the AM/AM function was unconstrained in this case. These results show that the ACLR performance of the benchmark H-DAPD degrades significantly with the finite resolution of the AM/PM. More specifically, with a resolution of 1.8°, the benchmark H-DAPD performance is reduced to approximately −46dBc. Conversely, the proposed H-DAPD is insensitive to limited resolution in the AM/PM characteristic since it is designed to not compensate for the AM/PM distortions.

The spectra measured at the output of the linearized amplifier when using the proposed H-DAPD with limited AM/AM resolution are reported in Fig. 14. This figure shows that the effects of the limited resolution appears as an increase in the noise floor due to the quantization of the analog predistorter's AM/AM gain values. However, it is important here to keep in mind that the key performance criterion of the linearizer performance is its ability to meet the ACLR specifications of the considered communication standard. This data is reported in Fig. 15 (curves corresponding to unconstrained phase resolution).

Fig. 15 reports the ACLR performance of the proposed H-DAPD along with that of the benchmark H-DAPD. For the case of the benchmark H-DAPD, when the effects of finite resolution on the AM/AM and AM/PM characteristics of the APD are considered concurrently, the ACLR degradation is even more pronounced than the values reported in Tables 2 and 3 since the effects of the limited resolutions on both the AM/AM and AM/PM will add up in the case of the benchmark H-DAPD. However, since the proposed H-DAPD does not include analog compensation of the AM/PM, it is insensitive to the limited phase correction resolution. Fig. 15 summarizes the ACLR at the output of the linearized amplifier for various amplitude and phase resolutions in the APD function. This figure clearly depicts the robustness of the

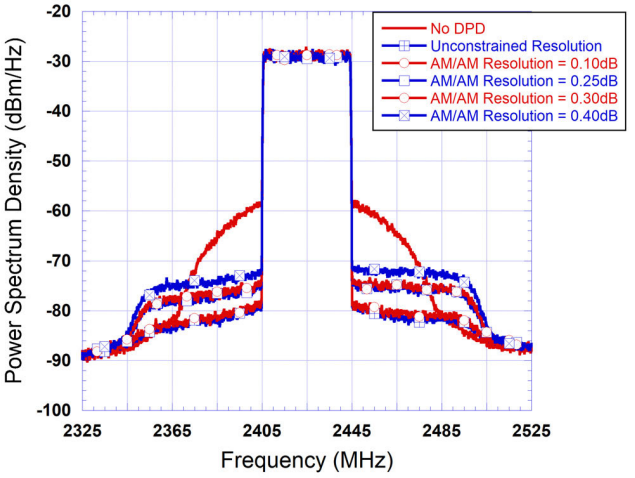

FIGURE 14. Measured spectra at the output of the linearized amplifier using the proposed H-DAPD with limited AM/AM resolution.

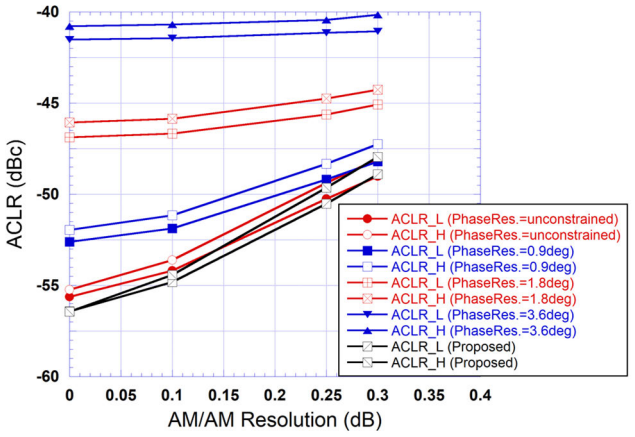

FIGURE 15. Effects of the APD limited AM/AM and AM/PM resolutions on the ACLR performance of the benchmark and proposed H-DAPD architectures.

proposed H-DAPD acquired by eliminating the AM/PM compensation from the APD and implementing it solely in the digital domain. Not only did this approach result in a reduced implementation complexity, but it also made the predistorter more robust to limited resolution in the APD function. In fact, for all considered cases, the ACLR corresponding to the proposed H-DAPD is better than −48dBc. However, the ACLR of the benchmark H-DAPD can be reduced to approximately −40dBc when limited resolutions in the AM/AM and AM/PM characteristics co-exist.

The AM/AM and AM/PM characteristics of the PA linearized using the proposed H-DAPD in the presence of limited resolution in APD sub-function are reported in Fig. 16 for the cases corresponding to 0.1dB and 0.4dB resolutions. This figure shows that a 0.1dB AM/AM resolution has minimal impact on the AM/AM and AM/PM characteristics of the linearized PA. This is in line with the spectra results reported in Fig. 14. However, the AM/AM characteristic obtained when the APD gain resolution is set to 0.4dB shows more

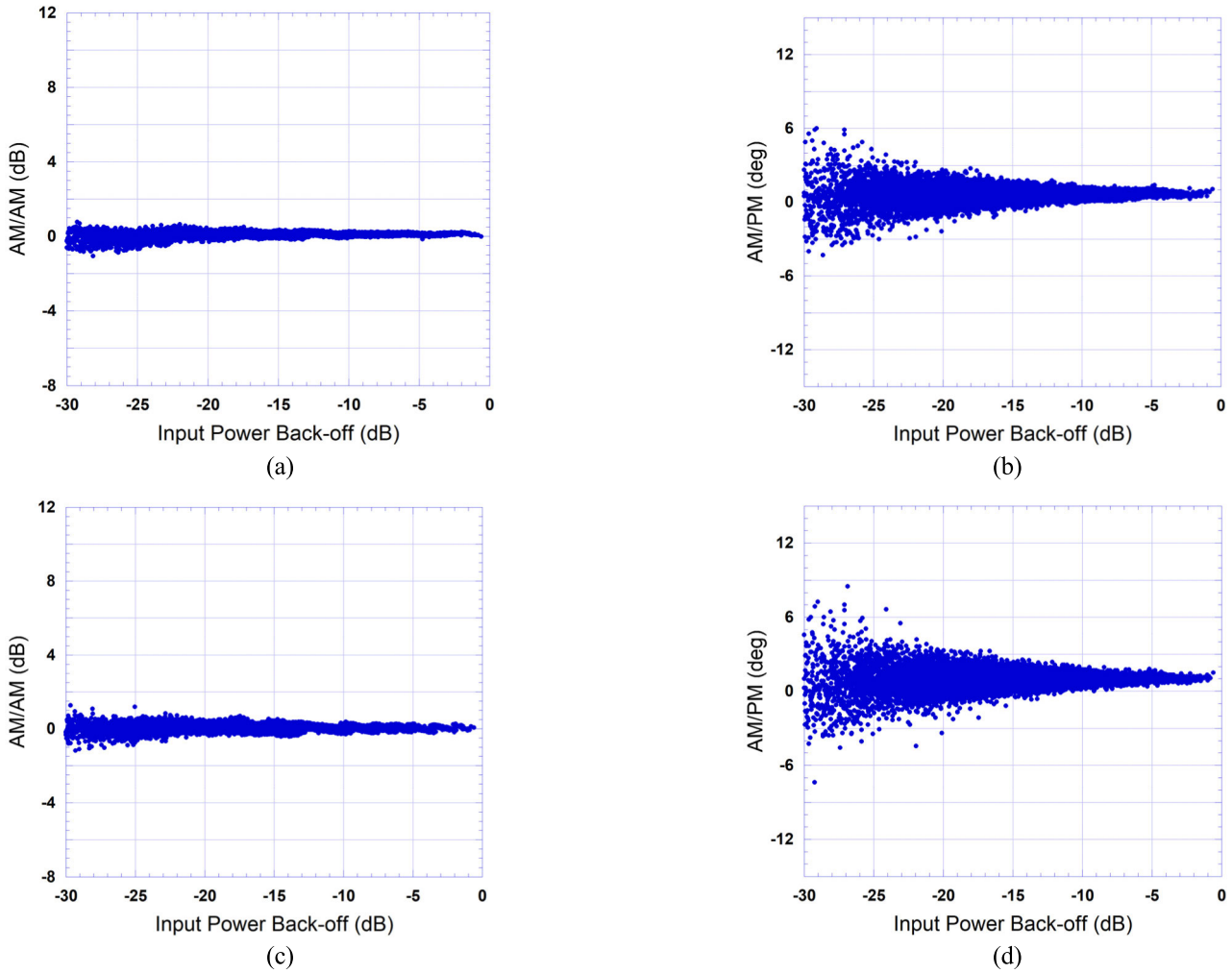

FIGURE 16. AM/AM and AM/PM characteristics of the DUT linearized using the proposed H-DAPD in presence of limited resolution in the APD function. (a) AM/AM with 0.1dB resolution. (b) AM/PM with 0.1dB resolution, (c) AM/AM with 0.3dB resolution. (d) AM/PM with 0.3dB resolution.

dispersion but also noticeable discontinuity due to the discrete values of the APD gains. Similarly, the corresponding AM/PM characteristics depicts the presence of increased dispersion. These characteristics explain the loss of performance observed in the spectra of Fig. 14 and the ACLR results of Fig. 15.

In order to benchmark the proposed H-DAPD against a purely analog RF predistorter, the effects of limited AM/AM resolution and phase resolution were also assessed for the case of the APD. In this case, the APD was modeled using a look-up table with a complex-valued gain to compensate for the AM/AM and AM/PM distortions. The results summarizing the APD performance under constrained amplitude and phase resolutions are reported in Fig. 17. This figure shows that the best performance, obtained under unconstrained resolutions lead to −41.9dBc ACLR which is around 15dB worse than the proposed H-DAPD under the same condition. This is mainly attributed to the fact that the APD does not compensate for memory effects, which are present in the behavior of the device under test. This can also be seen through the imbalance between the ACLR_L and ACLR_H performances. Furthermore, the performance degradation observed as the AM/AM resolution is decreased showcases a similar trend to the proposed H-DAPD but in a more pronounced manner.

D. EFFECTS OF LIMITED RESOLUTION AND TIME-DELAY MISALIGNMENT

In this section, the co-existence of limited resolutions in the APD function implementation and the delay misalignment between the control signal and the RF input of the APD is investigated. The ranges for both imperfections are similar to those considered in the previous subsections. Under these conditions, the output of the APD block will be related to its input through

$$x_{out\_APD}(t) = \tilde{G}_{APD}\left[x_{control\_APD}(t+\Delta t)\right] x_{in\_APD}(t) \quad (5)$$

where $\tilde{G}_{APD}$ is the limited resolution gain, and Δt corresponds to the delay misalignment between the APD control signal and its RF input signal.

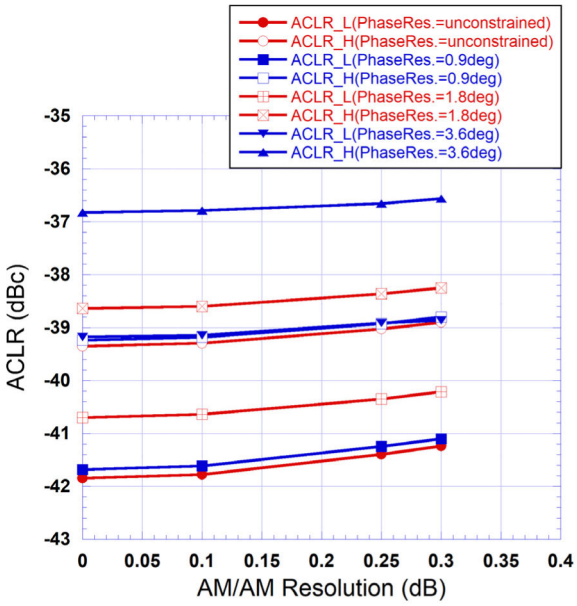

FIGURE 17. Effects of the APD limited AM/AM and AM/PM resolutions on the ACLR performance of the APD.

Fig. 18 presents the AM/AM characteristics of the APD in the presence of limited resolution as well time delay misalignment. These curves are derived for APD resolutions of 0.1dB and 0.3dB. For each of these resolutions, the AM/AM is reported for time delay misalignment of 0.65ns and 2.60ns. In both cases, it appears that the delay misalignment impact revealed through the dispersion of the AM/AM characteristic predominates the impact of the limited resolution. In fact, the impact of the limited resolution can not be discerned in the presence of a significant delay misalignment such as 2.60ns. However, for the 0.65ns case, the impact of the limited resolution in the APD function is revealed especially for high input power levels where the AM/AM curve dispersion is reduced. Indeed, one can clearly observe that for input power back-off levels larger than -10dB, a ripple-like effect is observed especially for the case of 0.3dB resolution. This is mainly due to the discontinuity of the APD characteristic (as previously shown in Fig. 13 (b)).

The effects of concurrent delay misalignment and reduced AM/AM resolution on the performance of the H-DAPD were first investigated under ideal phase resolution of the benchmark DPD. In this first test, the phase correction performed by the APD function of the benchmark H-DAPD via its AM/PM characteristic did not have any resolution constraint. The results summarized in the plots depicted in Fig. 19 show that the benchmark H-DAPD and the proposed one have similar performances and are subject to comparable performance degradation with respect to the delay misalignment, and amplitude resolution.

Fig. 20 reports the ACLR at the output of the linearized amplifier under limited resolution (for both the AM/AM and AM/PM functions) and delay misalignment. Each figure shows the combined effects of limited phase correction

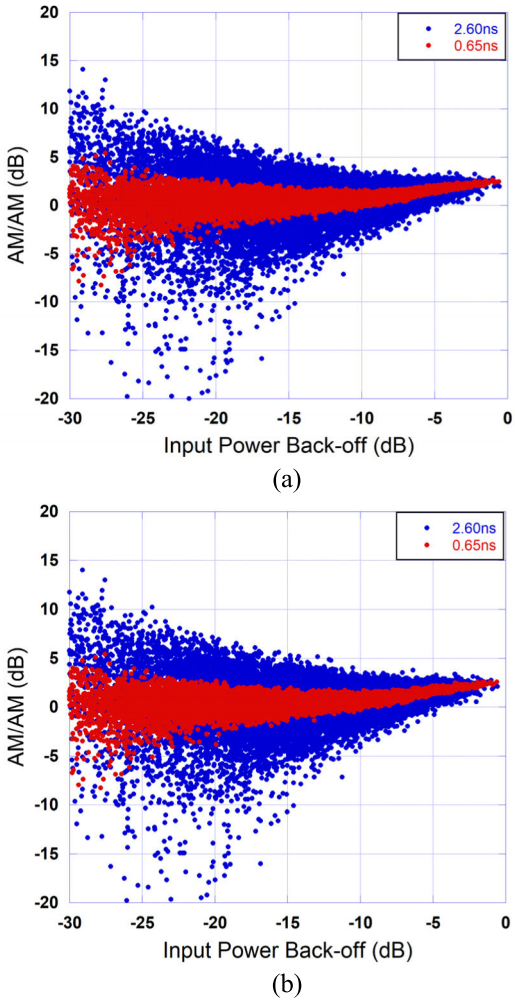

FIGURE 18. Effects of the coexistence of the limited resolution and delay misalignment on the APD AM/AM characteristic. (a) 0.1dB resolution, (b) 0.3dB resolution.

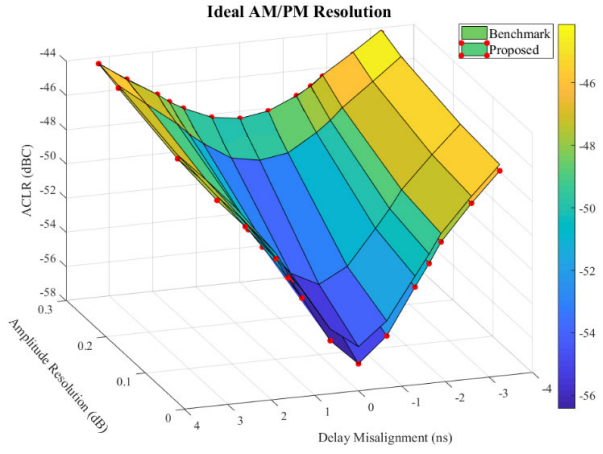

FIGURE 19. Effects of the APD limited AM/AM resolution and delay misalignment on the ACLR performance of the benchmark and proposed H-DAPD architectures.

resolution and delay misalignment for a constant value of the amplitude correction resolution. This figure shows

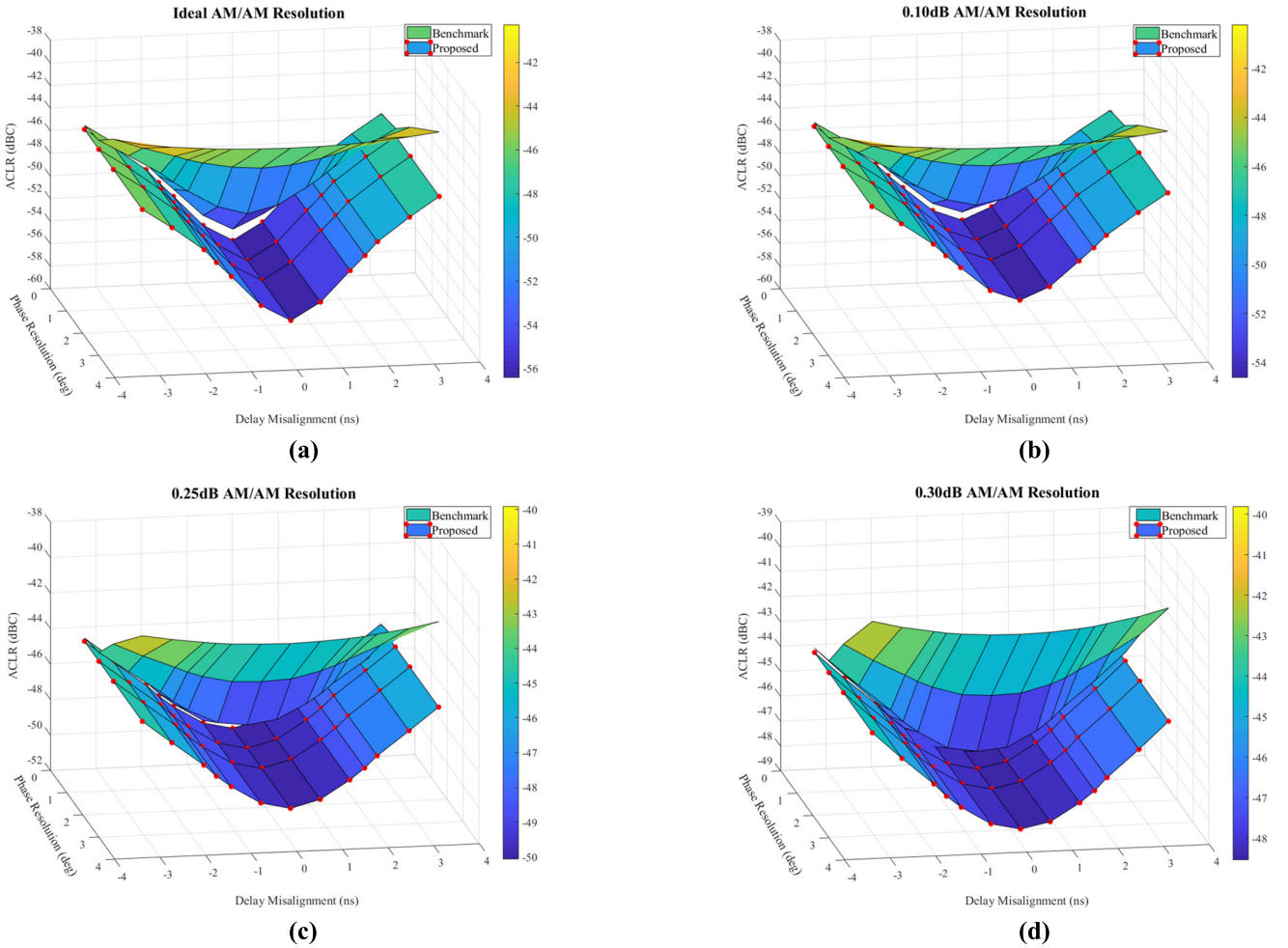

FIGURE 20. Effects of the APD limited resolution and delay misalignment on the ACLR performance of the benchmark and the proposed H-DAPD. (a) ideal AM/AM resolution, (b) 0.10dB AM/AM resolution, (c) 0.25dB AM/AM resolution, (d) 0.30dB AM/AM resolution.

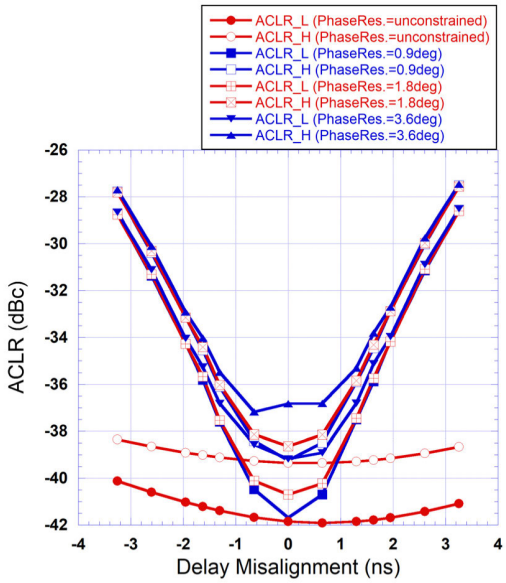

FIGURE 21. Effects of the AM/PM resolution and delay misalignment on the ACLR performance of the APD (unconstrained AM/AM resolution).

that the proposed H-DAPD consistently outperforms the benchmark H-DAPD, and most importantly as the phase resolution becomes worse, the performance degradation of the benchmark H-DAPD becomes more pronounced. However, as anticipated, the proposed H-DAPD performances are independent of the analog predistorter's AM/PM function phase resolution.

The effects of delay mismatch and limited phase resolution were also assessed for the case of the APD having an ideal amplitude resolution. The results are reported in Fig. 21, which shows the ACLR at the output of power amplifier under the considered APD impairments (in the absence of DPD). This figure shows that the APD performance is very sensitive to the phase resolution and that this impact is intensified with the addition of delay misalignment. Most importantly, for a delay of more than 2ns, the ACLR at the output of the linearized amplifier becomes worse than that observed at the output of the amplifier before linearization (-32dBc). Hence, the standalone APD is very sensitive to hardware impairments. Such sensitivity is significantly reduced through the adoption of the proposed H-DAPD system.

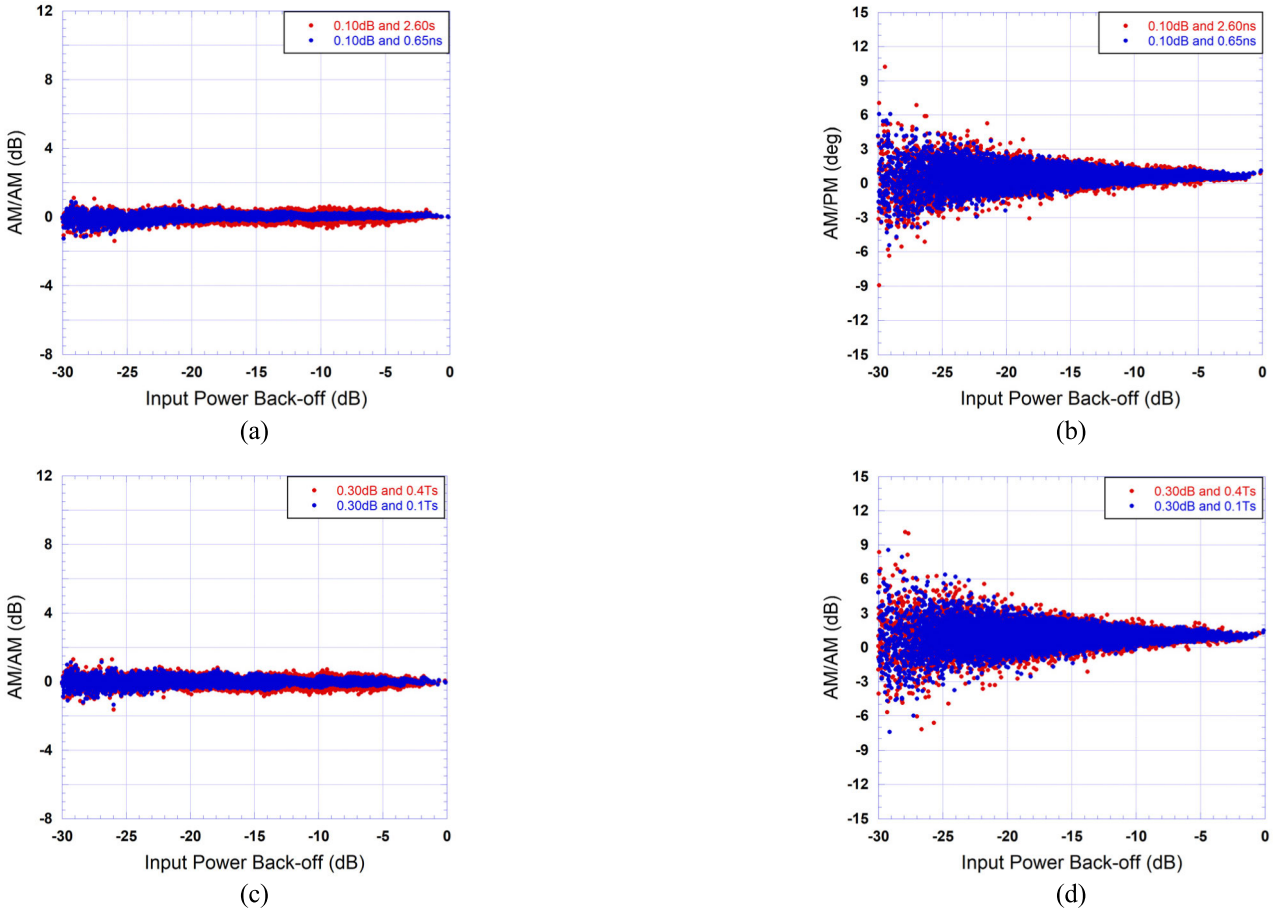

FIGURE 22. AM/AM and AM/PM characteristics of the DUT linearized using the proposed H-DAPD in presence of limited resolution and time misalignment in the APD function. (a) AM/AM with 0.1dB resolution. (b) AM/PM with 0.1dB resolution, (c) AM/AM with 0.3dB resolution. (d) AM/PM with 0.3dB resolution.

Sample AM/AM and AM/PM characteristics of the linearized amplifier using the proposed H-DAPD with coexistent limited resolution and time delay misalignment in the APD function are reported in Fig. 22. These curves correspond to APD's AM/AM resolutions of 0.1dB and 0.3dB and time misalignment of 0.65ns and 2.60ns.

The AM/AM characteristics show an increased dispersion in the presence of the time misalignment. Moreover, as the limited resolution of the APD function changes from 0.1dB to 0.3dB, a ripple-like effect is induced in the AM/AM characteristic of the linearized amplifier. This effect is clearly noticeable for the case of limited time misalignment (0.65ns) but gets covered by the increased dispersion for higher values of time misalignment (2.60ns). Furthermore, one can notice that the impact on the AM/PM characteristic does not show significant dependency on the level of the impairments. This can be explained by the fact that the impairments occur on the APD function which is designed to act only on the AM/AM characteristic of the PA.

The results reported throughout this section demonstrate two main conclusions. First, the proposed implementation of the H-DAPD which confines the compensation of the AM/PM distortions to the digital domain alleviates the requirement for high resolution analog domain phase compensation. Second, while the proposed H-DAPD performance is impacted by the impairments of the analog domain predistorter in terms of time delay misalignment and limited APD's AM/AM resolution, ACLR levels that are 5G NR compliant can be achieved when delay misalignment of up to 3ns coexists with an AM/AM resolution as high as 0.3dB. This robustness to hardware impairments is much less in the case of the conventional H-DAPD where the phase resolution has a significant impact on the linearization performance.

While the experimental validation was carried out only for the FR1 case, it is anticipated that comparable benefits of the proposed technique will be observed in the case of FR2 at millimeter waves where hardware impairments are more critical and the bandwidths of the test signals much wider. In such case, the HDAP is expected to relax the analog predistorter's sensitivity to delay misalignment and limited resolution, and the digital to analog converter's sampling rate in the signal transmit path. This latter is a very valuable given that the maximum signal bandwidth in the 5G FR2 is 400MHz.

IV. CONCLUSION

This paper investigated the use of a hybrid digital/analog predistortion system in which the analog sub-function only includes AM/AM distortions compensation. A two-steps identification technique was used to enable the DPD sub-function to compensate for the residual impairments observed in the cascade made of the APD and the DUT. Compared to benchmark hybrid predistortion functions, the proposed architecture was demonstrated to have enhanced robustness to the hardware impairments that may be present in the implementation of the analog predistortion function including delay misalignment and limited resolution. The proposed hybrid predistortion performance was experimentally assessed using a 40MHz 5G NR signal, and was found to meet the ACLR requirements in the presence of up to 3ns delay misalignment, and 0.3dB AM/AM resolution.

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This paper represents the opinions of the author(s) and does not mean to represent the position or opinions of the American University of Sharjah.

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