RESEARCH ARTICLE

Highly Efficient Isolated Multiport Bidirectional DC/DC Converter for PV Applications

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ABSTRACT This study proposes a novel isolated multiport bidirectional DC/DC converter (IMBC) that combines soft-switching (SS) and resistor-capacitor-diode (RCD) snubber circuits for battery charge and discharge applications in photovoltaic (PV) power systems. The proposed SS circuit operates at zero-current (ZC) switching (ZCS) when the switches are on to reduce the switching losses. The RCD snubber circuit also suppresses the overvoltage when turning off switches. Combining the two circuits also enables a more comprehensive operating range for SS, resulting in low losses and high efficiency. A thorough study of operating systems and design considerations is shown. PSIM illustrates the effectiveness of the suggested control method. A prototype of the suggested IMBC with an output voltage of 120 V and an output power of 150 W is constructed to confirm the viability and efficiency of the suggested topology. The maximum efficacy of the suggested topology in the step-up mode for the PV arrays is about 96.4% at an input voltage of 20.5 V and output power of 150 W. In comparison, the efficiency is about 98.5% in the step-down mode for charging and discharging the battery which is considered a highly satisfactory performance.

I. INTRODUCTION

The development of efficient and isolated power sources (IPSs) has become a vital goal for many power supply innovators. One of the major areas being pushed in terms of compact and simplicity is IPS design. Faster-growing communications systems, computers, and renewable energy require IPSs. All the IPSs require more external elements and intricacy to ensure that the output voltage is truly isolated and regulated. DC/DC converters (DC/DC Cs) have been broadly used in industry to regulate the output voltage and improve power quality. A variety of isolated and non-isolated DC/DC modules have been introduced in the industry depending

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on the applications [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. To satisfy the prerequisites of these applications, several pulse width modulation (PWM) topologies are normally used to execute IPSs. These structures include full-bridge, half-bridge, pull-push, double-switch, single-switch, and flyback topologies, which are listed sequentially from high energy level to low energy level. Each topology has unique properties that make it best suited to a particular energy level.

The hard-switching (HS) of power devices may cause huge switching losses during on and off, thus reducing efficiency and circuit reliability. However, flyback converters (FCs) address some major drawbacks, such as HS and massive voltage spikes (MVS) across the active switch on turn-off owing to the FCs' leakage induction and high current stress. The conduction loss is also sufficiently large to render the

converter ineffective. To achieve high power output, two or more parallel converters are interleaved [11], [12]. To alleviate the problems of HS, an active clamp/snubber circuit is used to attain SS, which can greatly reduce switching loss during switching time and current/voltage stress [13], [14], [15], [16], [17], [18], [19], [20]. However, this configuration requires assisting switches, diodes, and passive elements which increase the price. Voltage surge in the active switch caused by leakage induction of the FC may cause serious damage to the switch. Leakage inductance causes converter power loss and decreases overall efficiency. The operating frequency of this converter is an important factor, the high-frequency process improves the PQ, reduces the converter's size, magnetic element's size, etc. In general, the RCD snubber can effectively prevent the appearance of large VSs via the main switch when turned off, but this leads to a large loss and thus the efficacy of the converter is reduced [21], [22], [23], [24], [25]. Active clamp (AC) circuits are a more attractive solution to this problem [26], [27], [28], [29], [30], [31]. AC topology with FC recovers and outputs leakage power preventing high voltage spikes.

IMBC are popular topologies for low-power applications, up to approximately 500W such as switch-mode power supplies (SMPS). They provide a simple structure and contain very few components, insulation, etc. IMBCs are insulated versions of buck-boost converters that are used in nearly all consumer electronic products such as personal computers, uninterruptible power supply (UPS) units, portable battery chargers, liquid-crystal displays (LCDs) backlights, etc.

In this study, these IMBCs were designed for step-down operations for battery charging using PV arrays used in light-emitting diode (LED) street lighting systems, as shown in Figure 1. IMBCs are highly efficient versions of single-switch FCs. To obtain the desired form of output voltage or current, PWM control is used in converter circuits; thus, the following defects occur: high (voltage stress and conduction losses) in the main switches; the switching power losses (PLs) also rise with the rise in switching frequency (SF); the turn-on and turn-off losses could be an important portion of the total PLs; electromagnetic interference (EMI) in the converter waveforms; the current control mode isn't used; complex control circuits are required.
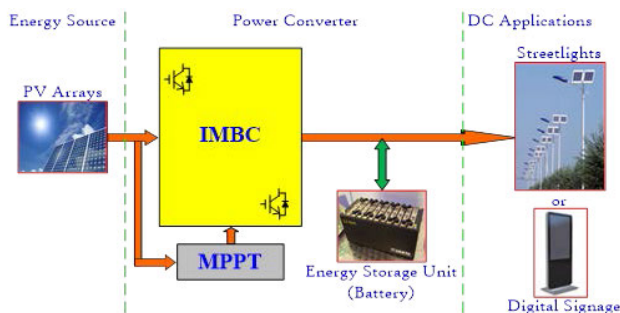

FIGURE 1. Schematic of the suggested IMBC for the studied PV system.

The above defects in the structure of the proposed IMBC circuit can be overcome and minimized if the switches are turned on and off using an SS with an RCD snubber circuit. The drive of the RCD snubber circuit is to suppress the overvoltage when the main switches are turned off and to reduce switching losses. The suggested converter is made to function at a high switching frequency of up to 100 kHz to minimize the size and weight of the passive and magnetic elements. This paper aims to propose a new IMBC configuration that takes into consideration the benefits proffered by both the ZVZCS resonant and the traditional RCD snubber circuit, to save energy and losses as they are in the form of heat and also to achieve high efficiency. The following is a summary of this work's key and innovative contributions:

- The proposed IMBC provides isolation and flexibility for input voltages above and below the battery voltage.
- The RCD circuit also prevents overvoltage when switches are turned off or overvoltage for switching.
- A reduction in the damage caused by overheating of the switches and the safe and reliable operation of the proposed converter.
- Saving energy and losses as well as achieving high efficiency.

This paper gives an overview of SS, especially ZVZCS in an IMBC. The operating principle and steady-state analysis of the suggested IMBC are clarified. Optimal design deliberations for the suggested IMBC are presented. Simulation results of the investigated IMBC and the experimental outcomes are shown in the following sections of this paper.

II. MODELING OF PROPOSED IMBC
A. CIRCUIT DESCRIPTION

The proposed IMBC consists of two MOSFET switches Q_1 and Q_2, an isolated high-frequency (HF) transformer T_r, the rectifier diode D_r, and an output (filter capacitor C_f, and load resistance R_L), as depicted in Figure 2. The switches Q_1 and Q_2 are energetically powered with a short period of dead time, as shown in Figure 4. MOSFET Q_1 and Q_2 and their parasitic capacitors C_{Q1} and C_{Q2} and auxiliary diodes D_{Q1} and D_{Q2} are connected in series with the resonant inductor L_r and leakage inductor L_k in parallel with the input filter capacitor C_{in}, providing SS functions both turn-on and turn-off. The proposed switching cell has no additional current pressure in the chief switches and has lesser extra conduction losses than conventional FCs.

B. MODELING OF RCD SNUBBER CIRCUIT

The circuitry of the RCD snubber involves a resistor R_s, a snubber capacitor C_s, and a snubber diode D_s, as shown in Figure 2. Its main function is to suppress the overvoltage spike and to limit the *du/dt* to reduce the power loss of the switches at the moment of turning off. When the RCD snubber circuit turns off the switching power supply, the current in the transformer leakage inductance L_k will be absorbed by working the engagement diode D_s once the MOSFET drain voltage surpasses the node voltage N, as shown in Figure 2.
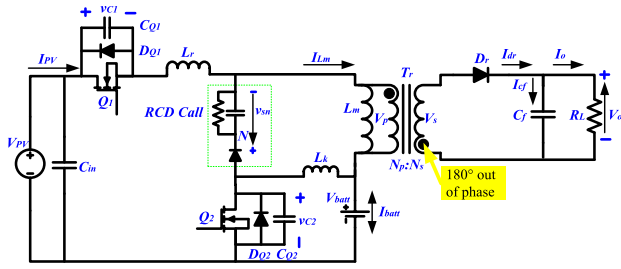
FIGURE 2. The proposed battery charger topology.

After a while, the voltage at the snubber capacitor is close to zero, ready to turn off the power supply. Additionally, in snubber cell analysis, the snubber capacitor must be large enough that its voltage does not alter meaningfully all through one switching cycle. The snubber capacitor used is assumed to be a material that provides low equivalent series resistance. Electrolytic capacitors or tantalum are not acceptable for these reasons [21], [32], [33]. If the parameters of the snubber cell are unreasonably determined, the snubber circuit will not achieve the desired effect and will eventually lead to the destruction of the MOSFET switches.

C. MODELING OF LITHIUM-ION BATTERY

The proposed IMBC circuit needs maximum output power for PV panels $P_{PV(max)} = 75$ W. Important specifications of PV panels are illustrated in Table 1. In the meantime, only the battery cell has a lesser voltage value than the output voltage of the converter. As a result, to boost the outcome voltage or result in the current capacity of a battery cell, multiple battery cells need to be linked in series. Three battery cells are linked in series to make a battery chain, and four battery chains are linked in parallel to form a battery pack, depending on the voltage and current ratings of the battery pack. In other words, 4 series*4 are connected in parallel with the battery pack. Battery parameters and specifications are determined by the manufacturer's datasheet in Table 2. The precise voltage source is labeled by the main equations of a specialized general battery model of a lithium-ion battery as shown in Figure 3, as follows [34]:
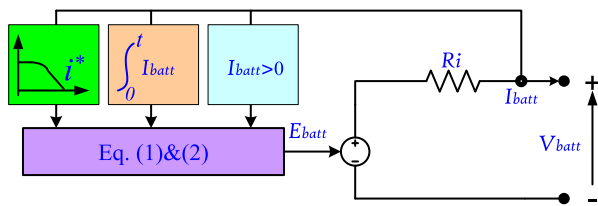

FIGURE 3. Model of the Li-ion battery.

Battery charging voltage:

$$V_{Chg} = V_c - K \frac{Q}{i_t + 0.1Q} \cdot i^* - K \frac{Q}{i_t - Q} \cdot i_t + Ae^{(-Bi_t)} - R \cdot i \quad (1)$$

Battery discharging voltage:

$$V_{Dis} = V_c - K \frac{Q}{Q - i_t} \cdot i^* - K \frac{Q}{Q - i_t} \cdot i_t + Ae^{(-Bi_t)} - R \cdot i \quad (2)$$

where V_c is the battery voltage, R is the internal resistance, K is the polarization voltage constant (V/Ah), i is the battery current, Q is the maximal battery capacity (Ah), i_t is the extracted capacity (Ah), A is the exponential voltage-zone capacity, i^* is the low-frequency current and B is the constant inverse exponential time-zone capacity (Ah^{-1}).

TABLE 1. Specifications of the implemented solar panels prototype.

Parameters	Symbol	Value, Unit
Rated Maximum Power at STC*	P_o	75W
Maximum Power Voltage	V_{mp}	17.5V
Maximum Power Current	I_{mp}	4.29A
Open-circuit Voltage	V_{oc}	22.1V
Short-circuit Current	I_{sc}	4.59A
Solar Calls Type		Poly-crystalline Module
No. of Calls		36(4*9)
Inclination Angle for Panels		47°

STC*: Module Temperature 25 °C and Irradiance 1000 W/m².

TABLE 2. Parameters of battery pack given by the manufacturer.

Specifications	Symbol	One Battery Cell Values	Battery Pack Values (4 Series*4 Parallel)
Capacity Rating	C_n	3.2 Ah	51.2 Ah
Nominal Voltage	V_n	3.2 V	12.8 V
Maximum Charging Voltage	V_{max}	3.8 V	15.2 V
Standard Charging Current	I_{SCC}	1.625 A	6.5 A
Minimum Discharging Voltage	V_{min}	2.6 V	10.4 V
Minimum Discharging Current	$I_{DC(min)}$	6.4 A	25.6 A

D. MODELING OF PWM SEQUENCES

The produced power of the suggested circuit is constantly controlled by a frequency asymmetric PWM control technique as shown in Figure 4, in the case of zero-current SS mode. Figure 4 shows a diagram of the PWM sequence for timing the proposed gate voltage pulses for the MOSFET switches Q_1 and Q_2. The MOSFET switches of the proposed converter are functioned at the identical SF. However, their switch waveforms are shifted in phase concerning each other by $2\pi/N$ radians during the switch time. The advantages of this technology are as a result of harmonic revocation between the main switches high ripple frequency, and low ripple amplitude in the overall income and outcome waveforms.
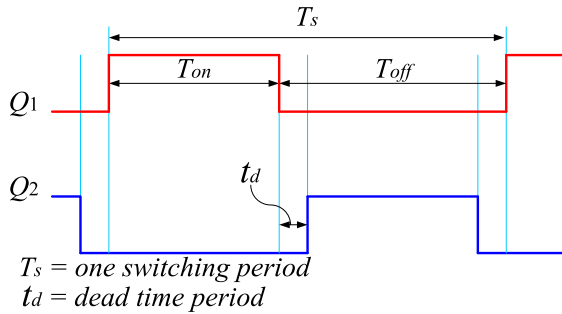
FIGURE 4. Timing pattern sequences of switching gate driving pulses.

III. OPERATING PRINCIPLE OF THE PROPOSED IMBC
A. EQUIVALENT CIRCUITS

The proposed IMBC functions under battery charging (BC) and battery discharging (BD) situations distinctly, as shown in Figure 2. The equivalent circuits of the planned IMBC topology are depicted in Figure 5a&b marked by red lines, respectively. Figure 5a shows IMBC with a magnetic inductor L_m of transformer Tr, which is used as a battery charger. Figure 5b shows IMBC with RCD snubber, which serves as a battery discharger. Using this approach, the proposed IMBC uses fewer elements to achieve BC and BD purposes. To simplify the analysis and avoid the complexity of the suggested converter, the suggested IMBC is supposed to work in continuous connection mode (CCM). The two MOSFET switches Q_1 and Q_2 have the same D, shifted by 0.5 Ts, as shown in Figure 4. Some of the next expectations are ended in one switch period as follows:

1) The input voltage V_{dc} is constant.

2) MOSFETs switches Q_1 and Q_2 are ideal.

3) All diodes are ideal.

4) The C_f is large and adequate to take up that the output voltage V_O is constant and ripple-free.

5) The L_m is large enough to assume that the IL_m on the L_m inductor is constant and much larger than that on the resonant inductor L_r.

6) The L_k of the transformer is ignored since it is much smaller than the L_m.

B. SWITCHING OPERATION MODES
The BC mode:

In steady-state and based on these assumptions, the suggested IMBC functions with six operating methods during a single switching cycle (SC), as shown in Figure 6. Therefore, circuit operations are analyzed into only six operating methods during a single SC in charge mode. The power flow for each functioning mode in the suggested IMBC is illustrated with red lines, as exposed in Fig. 7.

Mode 1: as shown in Figure 7a, in the interval from t_0 to t_1, as shown in Figure 6. Before that, both switches Q_1 and Q_2 were in the off position simultaneously. Since the I_{Lk} current of the leakage inductance is $(-1/2)$ i_{Q2} and the switching current i_{Q1} is a negative value (NV), the D_{Q2} diode
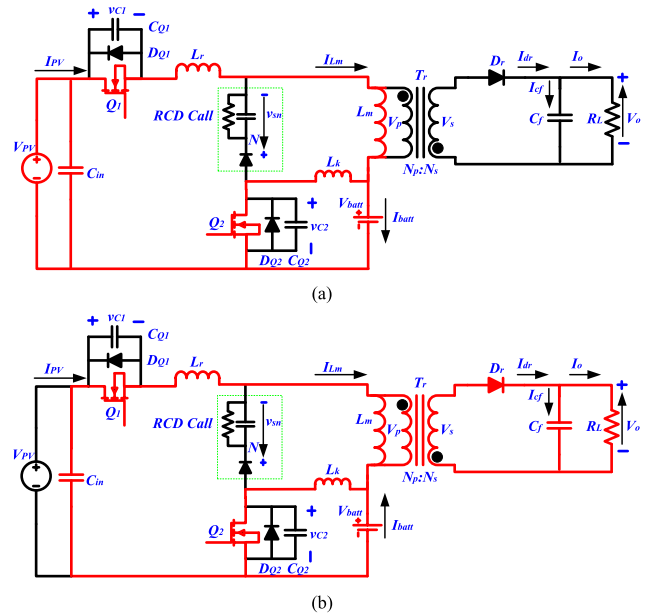

FIGURE 5. Schematic of the equivalent circuits of the proposed IMBC operating in (a) BC mode, and (b) BD mode.
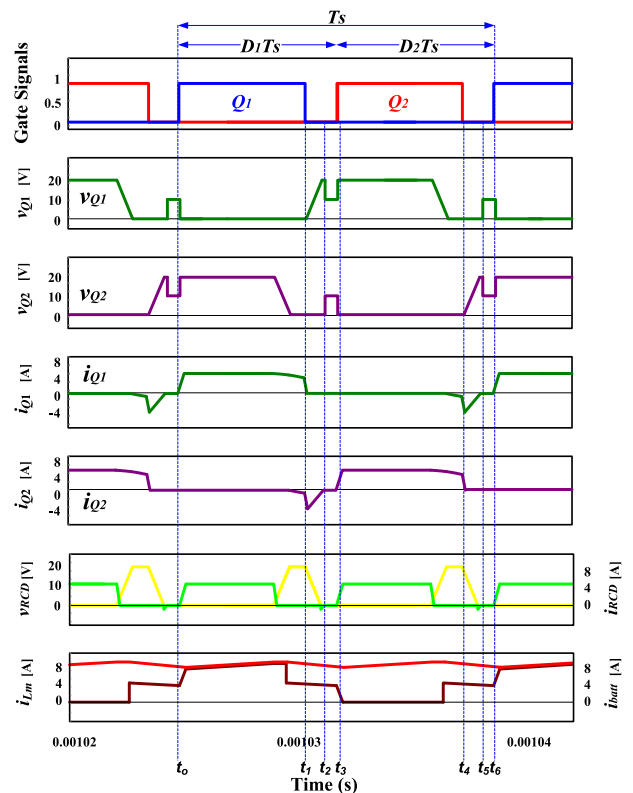

FIGURE 6. Steady-state voltage and current waveforms of the proposed IMBC operating in the BC mode during one SC.

is in the forward-biased condition. When $t \geq t_0$, switch Q_1 is on, and switch Q_2 stays off. The voltage v_{Q1} is equal to 0 V, and the current switching rate i_{Q1} increases abruptly from 0 A to the minimum value of the inductor current i_{Lm}. The V_{PV}
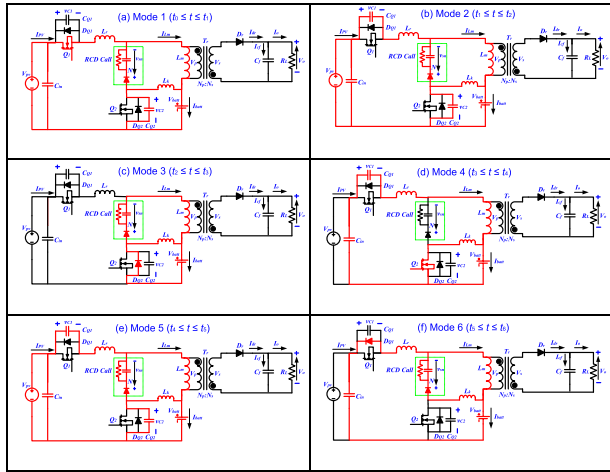
FIGURE 7. Equivalent circuits of the suggested IMBC operating in the charging mode during one switching period.

voltage is approximately supplied on the inductors of L_m and L_r because the inductance of L_m is greater than that of L_k. The current i_{Q1} and i_{Lm} are increased linearly by the input voltage V_{PV}, and the L_m releases energy to charge the battery. Therefore, the D_{Q2} diode is reverse-biased. The ZVS process occurs when Q_1 is on. Therefore, the SL during operation is zero, which is beneficial to reduce EMI, which leads to higher efficiency.

Mode 2: as shown in Figure 7b, in the interval from t_1 to t_2, as shown in Figure 6. The switch Q_1 is off, and Q_2 remains in the off position. L_m and L_r are charging the parasitic capacitor C_{Q1}. Capacitor voltage V_{CQ1} is charging from 0V to $(V_{PV} + V_B)$) because the energy stored in L_m and L_r is large enough to be considered a current source, while V_{CQ2} is discharging from $(V_{PV} + V_B)$ to 0 V. Under this mode, the switching current i_{Q1} and i_{Lm} suddenly drop from the maximum value to 0A, and the current i_{Q2} rate increases rapidly from 0 V to the maximum negative value.

Mode 3: as shown in Figure 7c, in the interval from t_2 to t_3, as shown in Figure 6. At $t \geq t_2$, both switches Q_1 and Q_2 remain off. Since the IL_k current of the leakage inductance is $(-1/2)$ i_{Q1} and the switching current i_{Q2} is an NV, the body diode D_{Q2} is in the forward-biased condition. The IL_k inductor current decreases linearly to release the energy stored in magnetizing inductor L_m to the battery and body diode D_{Q2}.

Mode 4: as shown in Figure 7d, in the interval from t_3 to t_4, as shown in Figure 6. When $t \geq t_3$, switch Q_2 is on, and switch Q_1 stays off. The voltage v_{Q2} is equal to 0V the current switching rate i_{Q2} increases abruptly from 0A to the minimum value of the inductor current i_{Lm}. The V_{PV} voltage is approximately supplied on the inductors of L_m and L_r because the inductance of L_m is greater than that of L_k. The current i_{Q2} and i_{Lm} are increased linearly by the input voltage V_{PV}, and the L_m releases energy to charge the battery. Therefore, the D_{Q1} diode is reverse-biased. The ZVS process occurs when Q_2 is on.

Mode 5: as shown in Figure 7e, in the interval from t_4 to t_5, as shown in Figure 6. The switch Q_1 is off, and Q_2 remains in the off position. L_m and L_{r1} are charging the parasitic capacitor C_{Q2}. Capacitor voltage V_{CQ2} is charging from 0V to $(V_{PV} + V_B)$) because the energy stored in L_m and L_r is large enough to be considered a current source, while V_{CQ1} is discharging from $(V_{PV} + V_B)$ to 0V. Under this mode, the switching current i_{Q2} and i_{Lm} suddenly drop from the maximum value to 0A, and the current i_{Q1} rate increases rapidly from 0V to the maximum negative value.

Mode 6: as shown in Figure 7f, in the interval from t_5 to t_6, as shown in Figure 6. At $t \geq t_5$, both switches Q_1 and Q_2 remain off. Since the IL_k current of the leakage inductance is $(-1/2)$ i_{Q2} and the switching current i_{Q1} is a negative value, the body diode D_{Q1} is in the forward-biased condition. The IL_k inductor current decreases linearly to release the energy stored in magnetizing inductor L_m to the battery and body diode D_{Q1}.

After Q_1 is in the on position, the suggested converter duplicates six identical operating modes during the new switching period. To evade damaging the power MOSFET switch Q_2, the RCD cell is usually connected in parallel with the primary terminal T_r.

The BD mode:

Mode 1 [Figure 9a]: The interval from t_0 to t_1, as shown in Figure 8. Before that, both switches Q_1 and Q_2 were in the off position simultaneously. Since the I_{Lk} current of the leakage inductance is $(-1/2)$ i_{Q1}, the D_{Q1} diode is in the forward-biased condition. At $t \geq t_0$, switch Q_1 is on, and switch Q_2 remains off. The voltage v_{Q1} is 0 V, and the current switching rate i_{Q1} suddenly increases from 0 A to the minimum i_{Lm} of the inductor. Because the D_{Q1} body diode is forward-biased before t_0. So, switch Q_1 is triggered with ZVS at the turn-on transition. The leakage inductor L_k and snubber capacitor C_s are connected in series to generate resonance. The battery supplies power to the magnetizing inductor L_m. Its power is transferred to the secondary side of the transformer T_r and because the rectifier diode D_r is in forward bias stat, it supplies power to the load.

Mode 2 [Figure 9b]: The interval from t_1 to t_2, as shown in Figure 8. The switch Q_1 is off, and Q_2 remains off. At $t \geq t_1$, L_m and L_k begin to flow to charge the parasitic capacitor C_{Q2}, with continuing the snubber capacitor C_s charging across the snubber diode D_s. The voltage of the capacitor V_{CQ1} is charged from 0 V to $(V_o/N + V_B)$ because the energy stored in L_m and L_k is large enough to be considered as a current source. The switching current i_{Q2} rate increases rapidly from 0V to a maximum negative value. On the secondary side of the transformer T_r, the energy stored in the output filter capacitor C_f is discharged to the load.

Mode 3 [Figure 9c]: The interval from t_2 to t_3, as shown in Figure 8. At $t \geq t_2$, both switches Q_1 and Q_2 remain off. At this moment, because the snubber capacitor i_{Cs} current is a negative value, the snubber diode D_s becomes in a forward-biased state. The V_{Cs} then discharge the energy stored in the snubber capacitor C_s back to the load, through leakage

inductance L_k. Since the I_{Lk} current of the leakage inductance is $(-1/2)\, i_{Q2}$, the body diode D_{Q2} is in the forward-biased condition. The inductor current I_{Lk} decreases linearly to release the energy stored in magnetizing inductor L_m to the battery and body diode D_{Q2}. On the secondary side of the transformer T_r, the rectifier diode D_r is in forward bias stat, so it supplies power to the load.

The operation of the proposed IMBC can be analyzed in only six modes during one switching cycle in the discharge mode, as shown in Figure 8. The power flow for each operating mode in the proposed flyback converter is illustrated with red lines, as shown in Figure 9.
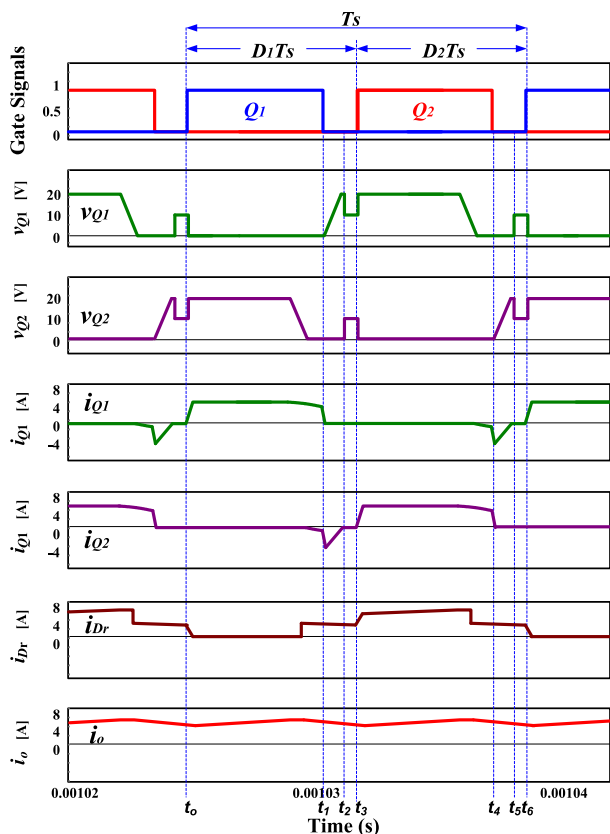

FIGURE 8. Steady-state voltage and current waveforms of the proposed IMBC operating in the battery discharging mode during one switching period.

Mode 4 [Figure 9d]: The interval from t_3 to t_4, as shown in Figure 8. When $t \geq t_3$, switch Q_2 is on, and switch Q_1 stays off. The voltage v_{Q2} is equal to 0V, and the current switching rate i_{Q2} increases abruptly from 0A to the minimum value of the inductor current i_{Lm}. The leakage inductor current i_{Lk} must be driven in a continuous state through the capacitor C_{in} and C_{Q1}, so the capacitor C_{Q1} is discharged and its voltage V_{CQ1} varies from $(V_o/N + V_B)$ to 0V. During this period, the magnetic inductor L_m is in the stored energy state, so L_m releases energy to charge the battery. Because the D_{Q2} body diode is forward-biased before t_3, switch Q_2 is triggered with ZVS at the turn-on transition. On the secondary side of the

transformer T_r, the rectifier diode D_r is reverse-biased due to the 180° phase reversal. The energy stored in the output filter capacitor C_f is discharged to the load.

Mode 5 [Figure 9e]: The interval from t_4 to t_5, as shown in Figure 8. The switch Q_2 is off, and switch Q_1 remains off. At $t \geq t_4$, L_m and L_k begin to flow to charge the parasitic capacitor C_{Q2}, with continuing the snubber capacitor C_s charging across the snubber diode D_s. The voltage of the capacitor V_{CQ1} is charged from 0 V to $(V_o/N + V_B)$ because the energy stored in L_m and L_k is large enough to be considered as a current source. The switching current i_{Q1} rate increases rapidly from 0V to a maximum negative value. On the secondary side of the transformer T_r, the energy stored in the output filter capacitor C_f is discharged to the load.

Mode 6 [Figure 9f]: The interval from t_5 to t_6, as shown in Figure 8. At $t \geq t_5$, both switches Q_1 and Q_2 remain off. At this moment, because the snubber capacitor i_{Cs} current is a negative value, the snubber diode D_s becomes in a forward-biased state. The V_{Cs} then discharge the energy stored in the snubber capacitor C_s back to the load, through leakage inductance L_k. Since the I_{Lk} current of the leakage inductance is $(-1/2)\, i_{Q1}$, the body diode D_{Q1} is in the forward-biased condition. The inductor current I_{Lk} decreases linearly to release the energy stored in magnetizing inductor L_m to the battery and body diode D_{Q1}. On the secondary side of the transformer T_r, the rectifier diode D_r is in forward bias stat, so it supplies power to the load.

After Q_1 is in the on position, the suggested converter duplicates six identical operating modes during the new switching period. To evade damaging the power MOSFET switch Q_2, the RCD cell is usually connected in parallel with the primary terminal T_r.
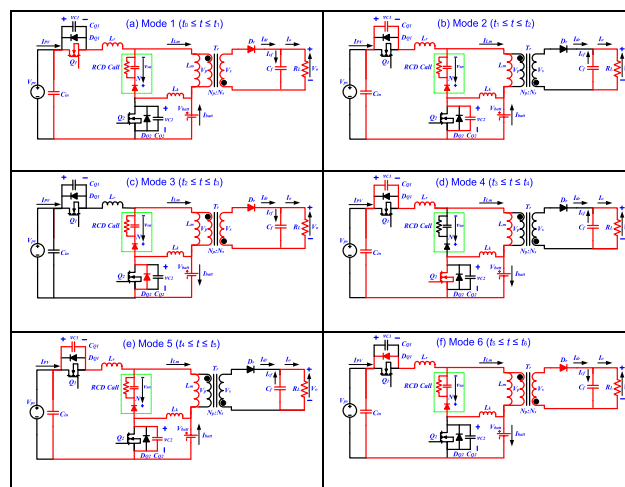

FIGURE 9. Equivalent circuits of the proposed IMBC operating in the discharging mode during one switching period.

IV. OPTIMAL DESIGN PROCEDURES

The proposed IMBC includes SS and an RCD snubber cell for implementing BC and BD functions, as shown in Figure 2.

To design the proposed IMBC, the important parameters include N and D of switches $Q_1\&Q_2$. Below is a brief description of their designs.

A. SELECTION OF TRANSFORMER TURNS RATIO AND DUTY CYCLE

The N must be chosen so that the set time (power-charge time) t_{on} is equal to the downtime (power-discharge time) $T_s - t_{on}$.

$$V_{out} = V_{PV} * \frac{N_2}{N_1} * \frac{t_{on}}{T_s - t_{on}} \tag{3}$$

where $N = N_2/N_1$, and where T_s is the period of the proposed IMBC during a single SC.

The BC mode:

Since the proposed IMBC adopts solar energy as the input source. In daylight, solar energy flows from the solar panels to the battery, using the IMBC as a BC as shown in Figure 5a. To implement solar MPPT, the IMBC can regulate the I_{Batt} charge current to achieve MPPT. During D, the battery voltage V_{Batt} is kept approximately at a constant value. The D_{max} can be specified under the minimum solar output voltage $V_{PV(min)}$ and the maximum battery voltage $V_{Batt(max)}$.

$$V_{PV(min)}D_{(max)}T_s + (-V_{Batt(max)}/N)(1 - D_{(max)})T_s = 0 \tag{4}$$

The D of switches:

$$D_{(max)} = \frac{V_{Batt(max)}}{NV_{PV(min)} + V_{Batt(max)}} \tag{5}$$

The BD mode:

At night, the solar energy stored during the day in the battery flows to the LED street lights, using the IMBC as a BD as shown in Figure 5b.

$$V_{Batt(min)}D_{(max)}T_s + (-V_{out}/N)(1 - D_{(max)})T_s = 0 \tag{6}$$

The D of switches:

$$D_{(max)} = \frac{V_{out}}{NV_{Batt(min)} + V_{out}} \tag{7}$$

The input voltage V_{PV}, the output voltage V_{out}, and battery voltage V_{Batt}; are set in Eqs. (4&6), and the N can be determined.

B. TRANSFORMER MAGNETIZING INDUCTANCE DESIGN

To obtain the design of L_m, the $I_{o(max)}$ is used to obtain L_m, which is the inductor value of the proposed transformer operating at CCM under charging and discharging conditions.

$$L_m = \frac{T_s D_{max}(1 - D_{max})V_{PV(min)}}{2KI_{o(max)}} \tag{8}$$

where K is a ratio that ranges from 0 to 1.

C. TRANSFORMER LEAKAGE INDUCTANCE DESIGN

The leakage inductance calculation is critical in determining the efficiency of the transformer and can be obtained from the data sheet if a pre-constructed transformer is used, or measured after the transformer is created. However, it can be assumed that the L_k is 3% of the magnetizing inductance L_m.

$$L_k \approx 0.03 * L_m \tag{9}$$

D. RCD SNUBBER CIRCUIT DESIGN

In the RCD snubber circuit design, we set the voltage of the V_s at the lowest input voltage. Once V_s is decided, the power in the snubber network is dissipated at the lowest input voltage and is acquired as follows:

$$P_s = \frac{V_{Batt}^2}{R_s} = \frac{1}{2}f_s L_k (I_{Batt-max})^2 \frac{V_s}{V_s - V_1} \tag{10}$$

where R_s is the snubber resistor, $I_{Batt-max}$ is the maximum current via the battery at the lowest input voltage, V_s is the snubber capacitor voltage and is obtained from equation (12) and V_1 is the output voltage of the primary winding. V_s must be greater than V_1 and it is usual to set V_s to be 2.5 times V_1. The leakage inductance is calculated at the SF of the primary winding. Subsequently, R_s of appropriate wattage should be selected based on the power losses.

The maximum voltage ripple of the snubber capacitor C_s is obtained as:

$$\Delta V_s = \frac{V_s}{f_s R_s C_s} \tag{11}$$

The V_s at the lowest input voltage can be obtained from the following equation:

$$V_s = \frac{V_1 + \sqrt{(V_1)^2 + 2f_s R_s L_k (I_{Batt-max})^2}}{2} \tag{12}$$

Then the values of snubber cell components can be successfully determined as shown in Table 4.

E. OUTPUT FILTER CAPACITOR DESIGN

The main factor impacting the amplitude value of the output voltage ripples V_o is the use of a capacitor C_o large enough to satisfy the output current ripple. The output ripple voltage ΔV_o across the output capacitor can be expressed as:

$$\Delta V_o = \frac{I_{o(max)}DT_s}{C_o} \tag{13}$$

Theoretically, the value of the capacitor will be determined according to the output voltage ripple ΔV_o specification.

$$C_o = \frac{I_{o(max)}DT_s}{\Delta V_o} \tag{14}$$

Practical, satisfying the I_o required in equation (13) determines the minimum capacitance that will usually easily satisfy any output ripple voltage specification [35].

V. CALCULATION OF CONVERTER LOSSES AND EFFICIENCY

To analyze the PL and efficiency of the proposed converter, the first step is to summarize the root mean square (RMS) value of currents in the different elements of the proposed converter in Figure 2, as shown in Table 3. The second step is to calculate the losses and efficiency of the proposed converter by writing a code to a MATLAB file. The third step is to take the internal resistance of the various elements of the proposed converter into consideration. MOSFET switches and diodes have this internal resistance only when the switch is turned on mode, but inductors and capacitors lose power when the switches are turned on and off mode.

TABLE 3. RMS currents of the proposed converter elements.

$I_s^{rms} = \dfrac{6n + 2(D-1)}{\sqrt{D}\,(1-D)} I_0$	$I_{C_1}^{rms} = 2I_0\sqrt{\dfrac{1}{D}}$
$I_{D_1}^{rms} = I_0\sqrt{\dfrac{(1-D)}{D_2^2}}$	$I_{C_2}^{rms} = I_0\sqrt{\dfrac{(1-3n)^2(1-D) + (3n-1)^2 D}{D(1-D)}}$
$I_{D_2}^{rms} = 2I_0\sqrt{\dfrac{1}{D_2}}$	$I_{C_f}^{rms} = I_0\sqrt{\dfrac{D(1-D) + (1+D)^2}{(1-D)}}$
$I_{D_r}^{rms} = 2I_0\sqrt{\dfrac{1}{1-D}}$	$I_{N_P}^{rms} = I_0\sqrt{\dfrac{3n(n+1)^2(1-D) + 9n^4 D}{D(1-D)}}$
$I_{C_s}^{rms} = 2I_0\sqrt{\dfrac{1}{D(1-D)}}$	$I_{N_S}^{rms} = I_0\sqrt{\dfrac{(3n+1)^2(1-D) + (2-3n)^2 D}{D(1-D)}}$

The proposed converter efficiency can be determined as follows in Equ. (15):

$$\eta = \frac{P_o}{P_{input}} \times 100\% = \frac{P_o - P_{Losses\_tot}}{P_{input}} \times 100\% \qquad (15)$$

The total PLs are calculated from the conduction of power switches, switching losses, forward diodes, conduction voltage losses, capacitors, and magnetic elements. It can be expressed as follows in Equ. (16):

$$P_{Losses\_tot} = P_{Losses}^{Switches} + P_{Losses}^{Diodes} + P_{Losses}^{Magntics} + P_{Losses}^{Capacitors} \qquad (16)$$

The PL of the switches can be represented as follows in Equ. (17):

$$P_{Losses}^{Switches} = P_{Losses}^{Switching} + P_{Losses}^{Conduction} \qquad (17)$$

In Equ. (18), $P^{Switching}$ is the active switching losses of the switches and is represented as follows:

$$P_{Losses}^{Switching} = 0.5 V_s I_s^{avg} f_s (t_s^{on} + t_s^{off}) \qquad (18)$$

where t_{on} and t_{off} are the rise and fall times of the switch. In Equ. (19), $P^{Conduction}$ is the conduction PL of the switches and is expressed as follows:

$$P_{Losses}^{Conduction} = R_{ds\_on}(I_S^{rms})^2 \qquad (19)$$

The PL of the diodes can be represented as follows in Equ. (20):

$$P_{Losses}^{Diodes} = P_{Losses}^{ForwardVoltage\_D} + P_{Losses}^{Conduction\_D} \qquad (20)$$

In Equ. (21), $P^{ForwardVolatge\_D}$ is the forward voltage losses of the diodes and is given by the following:

$$P_{Losses}^{ForwardVoltage\_D} = \sum_{j=1}^{Number\ ofDiodes} V_{F_{Dj}} I_{Dj}^{avg} \qquad (21)$$

In Equ. (22), $P^{Conduction\_D}$ is the conduction PL of the used diodes which can be written the following:

$$P_{Losses}^{Conduction\_D} = \sum_{j=1}^{Number of\ Diodes} R_{Dj}(I_{Dj}^{rms})^2 \qquad (22)$$

The magnetic components losses are the sum of the conduction losses for coupled inductors expressed as follows:

$$P_{Losses}^{Magnetics} = \sum_{j=1}^{Number of\ Inductors} R_{Lj}(I_{Lj}^{rms})^2 \qquad (23)$$

Finally, the total PL of capacitors is attained as follows:

$$P_{Losses}^{Capacitors} = \sum_{j=1}^{Number of\ Capacitors} R_{Cj}(I_{Cj}^{rms})^2 \qquad (24)$$

The results of the PL analysis and the calculated efficiency of the studied converter are depicted in Figures 10 and 11. Furthermore, the distribution of losses among converter components for $V_{in} = 17.5$V and $V_{in} = 20.5$V at output power $P_o = 150$W are given away in Figure 10 (a) and (b). For $V_{in} = 17.5$V, total losses are measured at 6.74W. Also, P^{Switch} losses are 1.92 W (28% of total losses), P^{Diodes} losses are 2.65W (40% of total losses), $P^{Magntics}$ losses are 1.31W (19% of total losses), and $P^{Capacitors}$ losses are equal to 0.86W (13% of total losses). For $V_{in} = 20.5$V, total losses are measured at 5.61W. P^{Switch} losses are 1.67W (30% of total losses), P^{Diodes} losses are 2.25W (40% of total losses), $P^{Magntics}$ losses are 1.01W (18% of total losses), and $P^{Capacitors}$ losses are equal to 0.68W (12% of total losses). As can be shown, SS causes MOSFET conduction losses higher than switching losses by 6%.
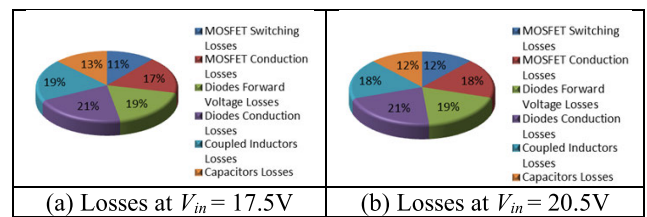

(a) Losses at $V_{in} = 17.5$V	(b) Losses at $V_{in} = 20.5$V

FIGURE 10. Distribution of losses among converter components at output power $P_o = 150$W for two different V_{in}: (a) $V_{in} = 17.5$V & $\eta = 95.7\%$, (b) $V_{in} = 20.5$V & $\eta = 96.4\%$.

The maximal efficacy of the suggested topology varies in the step-up mode of PV modules, due to the current drop at higher voltage levels. The efficiency measured at an input

voltage (IV) of 20.5V and an output power (OP) of 150W is about 96.4%, which is higher than the efficiency measured at an IV of 17.5V. For an IV of 17.5V and OP of 150W, as the current level increases, the PL also increases and the efficiency decreases to 95.7% are shown in Figures 10 and 11.
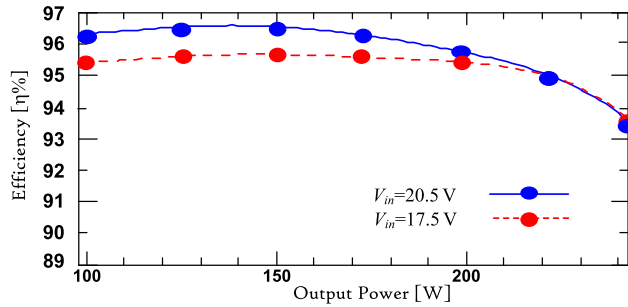

FIGURE 11. The efficacy curve for two different levels IV.

FIGURE 12. Operational modes of P&O algorithm.

VI. RESULTS AND DISCUSSION

A. DESIGN OF P&O ALGORITHM FOR IMBC

In this paper, an IMBC was designed and analyzed for battery charge and discharge applications in PV power systems. The operating modes are controlled by configuring the controller based on load and PV power generation requirements. An MPPT based on perturbation and observation (P&O) algorithm is proposed by including the variation in current, along with the conditional data of voltage, power, and initial value of duty cycle (D) determined by IMBC. The MPPT methods vary depending on the DC-DC converter topology and circuit parameters [36], [37], [38].

This method is based on the PV power (ΔP) variation resulting from a PV voltage (ΔV) variation. In this method, the value of the panel voltage V_{pv} and the PV input current I_{pv} is sensed before the input capacitance C_{in}. From this, the output power of the PV module can be calculated. The MPPT algorithm uses these two values to control the MPP tracking as shown in Equation (25) and Figure 12, under different temperatures and radiation levels.

$$M_{pv} = \frac{\Delta V_{pv}}{\Delta P_{pv}} \times \frac{dP_{pv}}{dV_{PV}} = K \int \frac{dP_{pv}}{dV_{PV}} dt \qquad (25)$$

The scaling factor, M, alters the perturbation size, to calculate the panel input reference point and maintain it at the MPP value, this is done by making a comparison between the calculated PV power (ΔP) value and PV voltage (ΔV) for the moment *n* and moment *n-1*, as shown in Figure 13 the flowchart for the P&O algorithm. If the power difference (ΔP) is zero, take the value of the previous duty cycle (D). If the measured voltage value is less than the previous value, this means that the difference in power (ΔP) is negative, and increases the duty cycle (D), i.e. increasing the voltage reference value (V_{ref}) provided that the voltage comparison is positive, and reduce the duty cycle (D), i.e. reducing the voltage reference value (V_{ref}), if the voltage comparison is negative. If the measured voltage value is greater than the
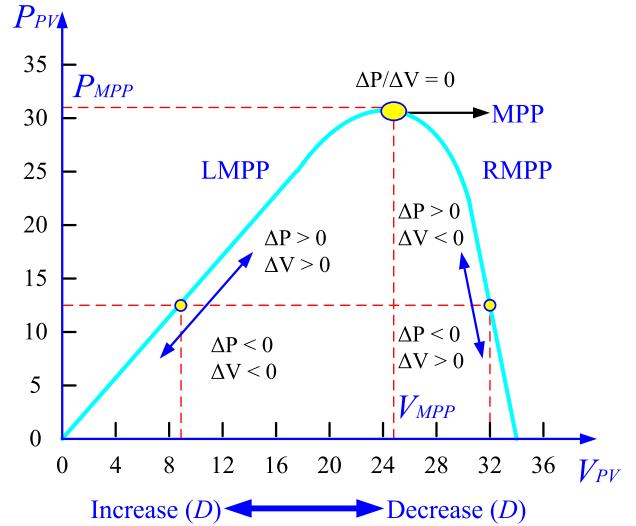
previous value, this means that the difference in power (ΔP) is positive, and increases the duty cycle (D), i.e. increasing the voltage reference value (V_{ref}) provided that the voltage comparison is negative, and reduce the duty cycle (D), i.e. reducing the voltage reference value (V_{ref}) if the voltage comparison is positive. Figure 13 below shows the flowchart of the implementation steps of the P&O-based MPPT algorithm.
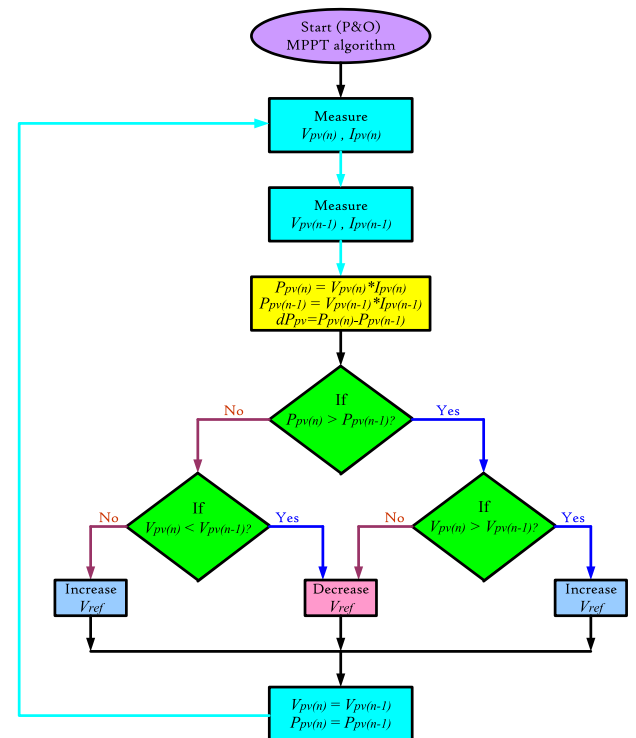

FIGURE 13. Flowchart for P&O algorithm-based MPPT.

The double-loop (DL) average current mode control is a good solution. In the DL architecture, the external loop is a

voltage loop that delivers the current reference to the internal loop. This control needs the sampling of two variables: the output voltage and the inductor current. The internal current and external voltage loop uses a proportional-integral (PI) as shown in Figure 14. To avoid increasing the output voltage above the component rating, the voltage responses of the internal comparators are mapped, which can generate PWM switching pulses to drive converters Q_1 and Q_2, as shown in Figure 14. The OP of the DC/DC converter is sensed and regulated on the word of the voltage and current given to the load to be controlled within the specified limits.
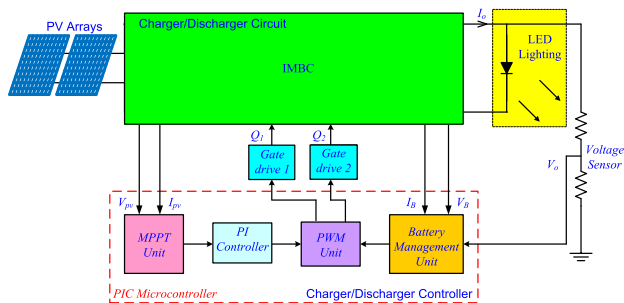

FIGURE 14. Block diagram of IMBC with feedback control.

B. SIMULATION RESULTS

In this study, the simulation was performed for 20 seconds to verify the transient behavior of the IMBC using a PI controller. The PI controller is one of the most commonly used controllers showing good robustness, simplicity in design, and stability in performance including low percentage overshoot and small settling time. In addition, the PI controller's performance heavily depends on its chosen gains to regulate VDC output. The investigated converter model is evaluated by PSIM simulation, as shown in Figure 15. The IV is taken from the PV module (solar panel Poly-crystalline, 75 W, $V_{mp} = 17.5$ VDC, $I_{mp} = 4.29$ A).
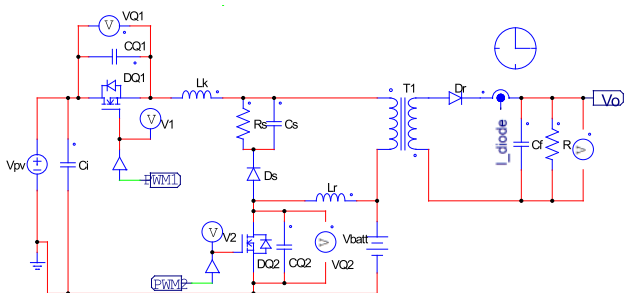

FIGURE 15. PSIM model.

Figure 16 shows the simulation waveforms under full load with an output voltage of 142.5 V and an output current of 1.75 A. Figure 16 also shows the output voltage and output current waveforms at standard irradiance (1000 W/m^2). Figure 17 also displays the BC voltage and current waveforms with a BC voltage of 12 V and a BC current of 6.75 A.
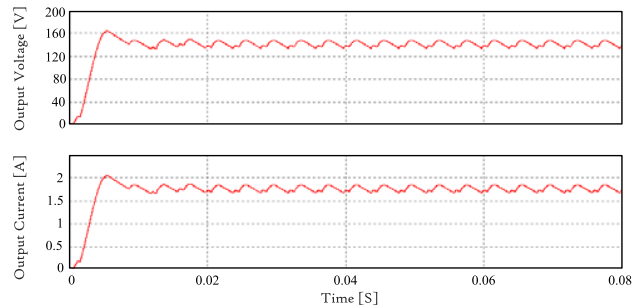

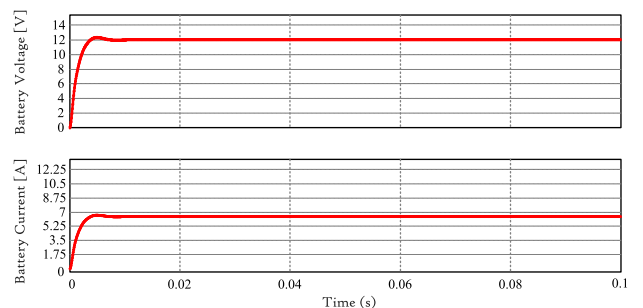**FIGURE 16.** Output voltage and current waveforms of IMBC.

FIGURE 17. BC voltage and current waveforms of IMBC.

C. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed IMBC that uses solar panels as its input source, the solar panel parameters are seen in Table 1. The considered circuit was applied as a prototype to illustrate the operating principle. For this, the prototype is implemented as given away in Figure 18 with the specifications listed below:

FIGURE 18. Experimental setup of IMBC.

● Charger: IMBC
1) Input voltage: $V_{PV} = 17.5$ V∼20.5 VDC (Per solar panel);
2) Maximal input power: $P_{PV(max)} = 75$ W;
3) SF: f_{Q1}&$f_{Q2} = 100$ kHz;
4) Maximal charging current: $I_{BC(max)} = 6$ A;
5) Output voltage: $V_{batt} = 8.8$ V∼12.8 V DC (Lithium-ion battery: 3.2 Ah).

• Discharger: IMBC
1) IV: $V_{batt} = 8.8$ V$\sim$12.8 VDC (Lithium-ion battery: 3.2 Ah);
2) Maximal input current: $I_{BD(max)} = 6.8$ A;
3) SF: $f_{Q2} = 100$ kHz;
4) Maximal output current: $I_{o(max)} = 6.25$ A;
5) Output voltage: $V_{out} = 12$ VDC.

The experimental converter was built as illustrated in Figure 18 employing the element characteristics given in Table 4, following the design process covered in the preceding part as a reference:

TABLE 4. Design specifications and circuit parameters.

Item	Symbol	Value
Input voltage	V_{DC}	17.5V
Switching frequency	f_s	100kHz
Output power	P_o	150W
Output voltage	V_o	120V
Battery voltage	V_B	12V
The dead time of Q_1&Q_2	t_d	1.4µs
Turn ratio of transformer T_r	$N_1: N_2$	1:3
The magnetizing inductance of transformer T_r	L_m	800µH
The leakage inductance of transformer T_r	L_k	7µH
Transformer core T_r		EE-33
Series resonant inductor	L_r	45µH
Resonant capacitor	C_r	16nF
Output filter Electrolytic capacitor	C_f	470µF/25V
Equivalent output resistance	R_L	100mΩ
MOSFET power switches Q_1, Q_2	IRFP220 (N-channel) V_{ces}=600V, I_c=90A	
Snubber resistor R_s	20kΩ	
Snubber ceramic capacitor C_s	470pF	
Snubber diode D_s	HER308 V_{ces}=60V, I_c=10A	
Rectifier Diode D_r	STPS10L60D V_{ces}=60V, I_c=10A	
PIC microcontroller	dsPIC30F2010	

The 150W IMBCs total experimental efficacy at 20.5 V input and 150 VDC output is displayed in Table 5. The MPP was monitored with a precision of roughly 99%, according to the experimental data. Over the whole power spectrum, the IMBC keeps a high level of efficacy with a power efficacy of 96.4%.

TABLE 5. Experimental efficiency results for the full 150-W IMBC.

V_{PV}	V_O	R_L	P_O	η
17.5V	120V	1.5Ω	150W	95.7%
20.5V	120V	1.5Ω	150W	96.4%
23.5V	120V	1.5Ω	150W	97.1%
26.5V	120V	1.5Ω	150W	97.8%
29.5V	120V	1.5Ω	150W	98.5%

A 600V-90A MOSFET is used as two switches operating at an SF of 100 kHz and the duty cycle (D) is changed to prove the principle of operation, as shown in Figures 19&20. The gate drive signal is produced using the PIC dsPIC30F2010 microcontroller circuit. The PWM signal is then delivered to the TLP250 optocoupler circuit to drive the MOSFET power

switches. The observed voltage and current waveforms of the switches Q_1&Q_2 are illustrated in Figures 19(a)–19(f). As can be seen, MOSFETs Q_1&Q_2 are turned off in the ZVS condition which greatly reduces the conduction losses of switching semiconductors using MOSFETs. For step-up mode with the switching frequency level increases, also power loss increases, and the efficiency decreases.
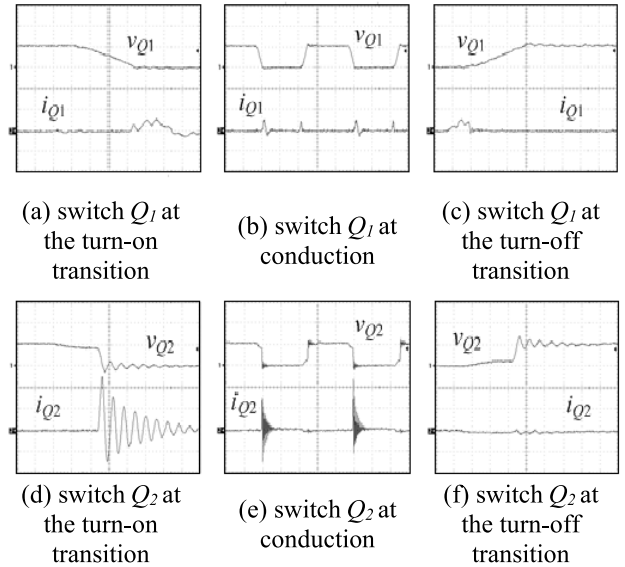

(a) switch Q_1 at the turn-on transition

(b) switch Q_1 at conduction

(c) switch Q_1 at the turn-off transition

(d) switch Q_2 at the turn-on transition

(e) switch Q_2 at conduction

(f) switch Q_2 at the turn-off transition

FIGURE 19. Observed voltage and current waveforms with step-up mode.

The observed voltage and current waveforms of the switches Q_1&Q_2 are illustrated in Figures 20(a)–20(f). As can be seen, MOSFETs Q_1&Q_2 are turned off in the ZVS condition which greatly reduces the conduction losses of switching semiconductors using MOSFETs. For step-down mode with the switching frequency level decreases, also power losses decrease, and the efficiency increases.

Figure 21 describes the results of quantitative total losses analysis among converter components in the IMBC circuit by using MOSFETs. As one can see in the figure, the total losses among converter components can be distributed from the conduction of power switches, switching losses, forward diodes, conduction voltage losses, capacitors, and magnetic elements as the loss's components. The total PL is calculated under the situation of the rated OP of 150W. One can realize that the overall PL of the IMBC is 5.61W in the step-down mode and 6.74W in the step-up mode.

Figure 22 shows the measured efficiency curves for the suggested converter topology. The maximum efficiency of the suggested topology is about 98.5% at OP of 150 W, in a step-down mode of battery charging and discharging for the suggested IMBC.

Table 6 comprehensively compares the proposed IMBC and other similar systems in recent years. Table 6 now includes comparisons with seven related works, each related to our work in one or more aspects. Numerical values are

TABLE 6. Comparison of other existing topologies with the proposed IMBC.

No.	Parameters	Ref. [35]	Ref. [39]	Ref. [40]	Ref. [41]	Ref. [42]	Ref. [43]	Ref. [44]	Proposed
1	Converter used	BIHC	IBC	BDC	DSCI	TPDB	IBC	SICBC	IMBC
2	Input voltage, V_{in}	20V	48V	20V	24V	24V	30V	36V	12-30V
3	Max. output voltage, V_{out}	80V	96V	200V	206.3V	199.72V	100V	300V	150V
4	Max. voltage gain, G	4	2	3-10	8.6	8.32	3.33	8.33	5-12.5
5	No. of switches	6	4	5	2	3	2	2	2
6	Switching frequency, f_s	10kHz	20kHz	20kHz	20kHz	25kHz	40kHz	20kHz	100kHz
7	No. of coupled inductors	3	Interleaved	Not required	1	Transformer	2	3	Transformer
8	Efficiency	96%	96%	95.7%	98.23%	92.2%	97%	96-98%	98.5%
10	Input source	Battery	Battery	Battery	Battery	Photovoltaic	Photovoltaic	Photovoltaic	Photovoltaic

(a) switch Q_1 at the turn-on transition

(b) switch Q_1 at conduction

(c) switch Q_1 at the turn-off transition

(d) switch Q_2 at the turn-on transition

(e) switch Q_2 at conduction
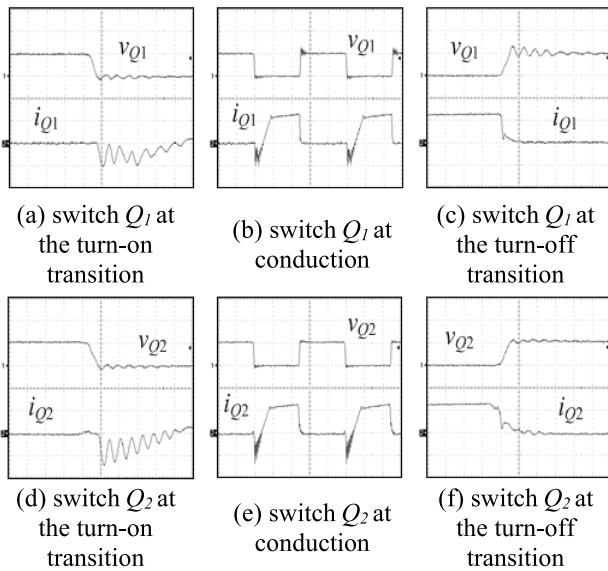
(f) switch Q_2 at the turn-off transition

FIGURE 20. Observed voltage and current waveforms with step-down mode.
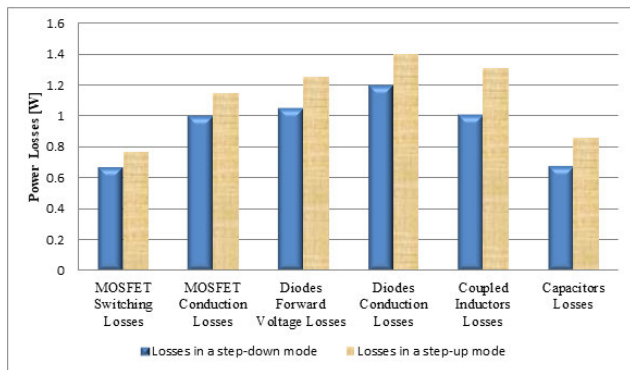
FIGURE 21. Distribution of total losses among converter components.
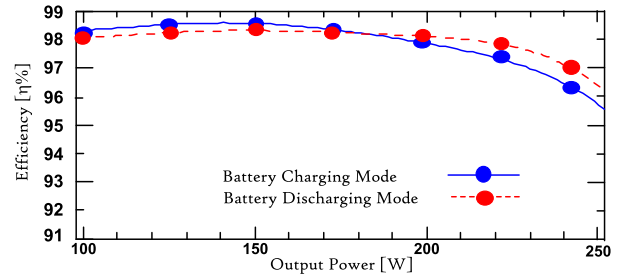
FIGURE 22. The measured efficiency curves of the proposed converter topology.

VII. CONCLUSION

In this paper, a prototype of the proposed SS IMBC with an RCD snubber circuit is built and implemented. The main disadvantage of an FC is the high voltage rise at off and poor conversion efficacy due to the presence of leakage inductance. This paper reviews novel topologies to overcome these shortcomings. Therefore, it uses SS cell with IMBC to implement ZVS and ZCS features under the operating transitions of the main switch (Q_1) and the auxiliary switch (Q_2). Hence, the switching losses and EMI of the main and auxiliary switches can be reduced, and the efficiency can be increased. The investigated converter is controlled by traditional fixed-frequency PWM technology. Thus, the investigated converter integrates the benefits of PWM and ZCS technologies without other current stresses compared to the traditional hard-switching method, which improves converter performance and maintains high efficacy. Simulation results show that an SS IMBC yields better efficiency for the same power ratings. The simulation results of the proposed converter are further validated by providing experimental results from a 150 W prototype setup of the proposed IMBC. It is noted that the regulated 120 VDC voltage is maintained at the output. The maximum efficacy of the investigated topology in a step-up mode of PV modules is about 96.4% at an input voltage of 20.5 V and an OP of 150 W. In comparison, the efficiency is about 95.7% at an input voltage of 17.5 V and an OP of 150 W under different loading conditions for

also added for comparison as shown in Table 6. From these numerical values, the proposed IMBC topology has a higher efficiency.

the investigated IMBC. Moreover, the efficacy is about 98.5% in a step-down mode for BC and BD, which is considered a quite satisfactory performance.

ABBREVIATIONS

List of abbreviations used in this manuscript:

AC	Active Clamp.
BC	Battery Charging.
BD	Battery Discharging.
CCM	Continuous Connection Mode.
DC	Duty Cycle.
DC/DC Cs	DC/DC Converters.
DL	Double Loop.
EMI	Electro-Magnetic Interference.
ESR	Equivalent Series Resistance.
FCs	Flyback Converters.
HS	Hard Switching.
IMBC	Isolated Multiport Bidirectional Converter.
IPSs	Isolated Power Sources.
IV	Input Voltage.
LCDs	Liquid-Crystal Displays.
LEDs	Light-Emitting Diodes.
LV	Low Voltage.
MPPT	Maximum Power Point Tracking.
MS	Main Switch.
MVS	Massive Voltage Spike.
NV	Negative Value.
OP	Output Power.
OVR	Output Voltage Ripple.
P&O	Perturb & observe.
PFC	Power Factor Correction.
PI	Proportional-Integral.
PIC	Programmable Interface Controllers.
PLs	Power Losses.
PV	Photo Voltaic.
PWM	Pulse Width Modulation.
RCD	Resistor-Capacitor-Diode.
RCs	Resonant Capacitors.
RES	Renewable Energy sources.
RF	Resonance Frequency.
RIs	Resonant Inductors.
RMS	Root Mean Square.
SC	Switching Cycle.
SF	Switching Frequency.
SMPS	Switch-Mode Power Supplies.
SS	Soft Switching.
UPS	Uninterruptible Power Supply.
ZCS	Zero Current Switching.
ZVS	Zero Voltage Switching.

ACKNOWLEDGMENT

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