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RESEARCH ARTICLE

A 60 GHz Broadband LNA With Joined Variable Gain Control and Switching in 22 nm FD-SOI

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ABSTRACT This paper investigates a 60 GHz low-power broadband low noise amplifier (LNA) with variable gain control. To prove the concept, the circuit is implemented in a 22 nm fully depleted silicon on insulator (FD-SOI) CMOS technology. It supports broadband operation at 60 GHz achieved by gain peaking (gain distribution) technique. By tuning some key matching networks of the amplifier, the peak gain of each stage was distributed to different frequencies resulting in an overall broadband frequency response. The circuit consists of three cascaded cascode amplifier stages. Matching networks were optimized regarding bandwidth and noise figure. The transistor back-gate was used for LNA designs to switch the circuit to low-power standby mode. This avoids the problems of front-gate based switching regarding voltage breakdown and circuit stability. Additionally, simultaneous realization of variable gain control at such high frequencies was achieved via the back-gate. Compared to the front-gate based, the back-gate based variable gain control can deliver a continuous fine-tuning of the gain while requiring less accuracy or resolution of the control voltage. In the measurement, The gain was successfully tuned from 20 dB down to −25 dB via the back-gate. At a DC power of 8.1 mW from a nominal supply of 1 V, the LNA provides a peak gain of 20 dB, a bandwidth of 18.5 GHz, and a minimum noise figure of 3.3 dB. When biased at a reduced DC supply of 0.4 V, the presented circuit consumes only 2.5 mW of DC power, and still provides a power gain of 10 dB and a minimum noise figure of around 4.5 dB. By switching to standby mode, the LNA consumes 850 µW of DC power at the nominal supply and 240 µW at the reduced supply. The LNA compares well against previously reported designs by showing the lowest noise figure with competitive gain, bandwidth and DC power. To the authors' knowledge, this is the first 60 GHz LNA featuring joined variable gain control and switching capability via solely back-gate biasing.

INDEX TERMS 22 nm FD-SOI, 60GHz, broadband, CMOS, cascode circuit, gain peaking technique, low-power, LNA, switching, variable gain, millimeter-wave.

I. INTRODUCTION

In recent years, the increasing demand for high transmission data rates and low latencies has posed significant challenges to existing wireless communication systems. Thanks to the large bandwidth available at millimeter-wave (mmW) frequencies, wireless systems can provide high channel capacity of communication and play an important role in satisfying the rapidly increasing requirements on data rate and latency. The unlicensed bands around 60 GHz provide great opportunities for high-speed applications supporting up to multi-Gb/s data transmission. Due to the high free

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space path loss (FSPL), 60 GHz wireless systems are ideally suitable for short-range, small-area deployment, which does not require a large area coverage and reduces the interference between adjacent wireless systems. As the first active component in a wireless receiver, the LNA is a critical block of mmW frontends because of the requirements of high gain, low noise, high linearity and high frequency of operation, which set the overall system performance in terms of sensitivity and signal-to-noise ratio (SNR). Beyond satisfying the general system performance requirements, low cost and low DC power are also of central importance [1].

A. BROADBAND TECHNIQUES

For short-range wireless applications, multiple license-free 60 GHz band-sets were released by different countries and regions worldwide spanning from 57 GHz to 66 GHz [2]. Recently, the US FCC (Federal Communications Commission) further empowers short-range radars by allowing radar operation in the 57-64 GHz band [3]. Since the actual set of bands released for operation varies with the geographical regions, it is beneficial from the perspective of development and distribution costs that 60 GHz frontends are capable of supporting broadband or multi-band operation. Multiplexing of chipsets operating in different frequency bands, single broadband chips and single multi-band chips are the possible ways to support multi-standard operation. The approach of multiplexing different chips requires integrating mm-wave frontends at the package level, which increases the cost while decreasing the performance. In contrast, broadband or multi-band designs can easily support multiple standards in diverse operating regions, consume less silicon area and have a lower packaging cost.

In recent years several LNAs working at 60 GHz mm-wave bands were reported [1], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. In [10] a broadband LNA operating at 63.5 GHz to 91 GHz using pole-converging technique for bandwidth extension was presented. LNAs reported in [1], [4], [8], and [11] have introduced dual-resonance impedance matching technique for broadband designs. The *gain peaking* or *gain distribution* techniques are widely used in common amplifier designs to achieve multi-band or broadband characteristics: single-band matching networks are engineered to distribute the peak gain response of gain stages at different target frequencies to obtain a cumulative broadband or multi-band gain response from a multi-stage amplifier. Compared to the dual-resonance matching technique, the gain peaking technique is easier to implement and enables better optimization flexibility in terms of gain, gain flatness and bandwidth, since the gain peaking frequencies can be individually tuned without affecting others. This is attractive for broadband or multi-band LNA designs. However, it is important to investigate the impact of the gain degradation associated with inter-stage impedance mismatches on the noise figure (NF) of the amplifier, because the matching networks are designed to realize a conjugate matching at one single frequency, while leaving the impedance unmatched at other frequencies. This is intuitively problematic in terms of the noise performance, particularly in the first stages of an LNA.

To provide a quantitative design guideline for this approach, this paper presents an analysis of the impact of mismatch losses on noise performance and shows the potential of such a technique for the implementation of LNAs. To prove the concept, the design and analysis of a 60 GHz broadband LNA operating at 60 GHz is presented. Similar to the proposed design, [7], [9], [12] presented broadband LNAs using gain peaking technique. However, these designs rely on low-Q matching networks realized by low-k transformers and capacitors, which widen the bandwidth of each individual gain stage and reduce the impact of impedance mismatch on the noise performance. In contrast, this paper investigates a more direct approach to gain peaking design which only relies on the natural bandwidth of first-order single-frequency matching networks while still delivering useful noise performance over a high frequency band. A similar design methodology was first introduced in our early work [14] at lower frequencies, this design not only improves the circuit energy efficiency and noise performance but also features additional switching and gain tuning capabilities via the transistor back-gate.

B. VARIABLE GAIN CONTROL

In indoor short-range scenarios, the transmitter (Tx) needs sufficient transmitting power to serve the required amount of area. Depending on the relative location between the Tx and Rx, the signal amplitude received by the Rx could vary. The overall Rx gain should be tuned to provide a proper signal amplitude in the baseband for digital processing. In common procedures, a separate variable-gain-amplifier (VGA) is integrated into the Rx chain. Implementing the variable gain technique in the LNA could give the Rx operator another degree of freedom to optimize the overall dynamic range of the receiver. The work in [15] used a parallel transistor tank to achieve the variable gain control. Reference [16] realized a variable gain LNA by adding some shunt transistors as attenuators. These approaches could only achieve limited states of amplifier gain due to the limited numbers of parallel gain stages or attenuators. Works in [17], [18] have introduced a current steering technique for continuous gain control relying on an auxiliary transistor controlling the DC current. All the works mentioned above are relying on the transistor front-gate for gain control. In contrast, this work utilizes the transistor back-gate for gain control. In comparison to the front-gate, the back-gate has less sensitivity in controlling the transistor channel and biasing current but a wider gate voltage tuning window (0-2V) resulting in a comparable gain tuning range. This allows the users to continuously fine-tune the LNA gain for its best value, and reduces the performance requirement of gain control circuits supplying the biasing voltage, because less accuracy of the control voltage is required. Works reported

in [19] and [20] have introduced a similar back-gate based variable gain control technique. However, the accomplished gain tuning range in these designs is lower compared to this design, due to the lack of co-optimization of front-gate and back-gate biasing. The sensitivity of gain tuning with respect to the back-gate voltage is highly dependent on the front-gate voltage. In this design, the front-gate biasing was chosen to achieve high tunability via the back-gate.

C. LOW-POWER STANDBY MODE

Energy efficiency is also an essential design parameter, since circuits become power-hungry when moving to higher frequencies. The work [11] applied a switching method via front-gate in its LNA for energy-saving, when the LNA is at its idle time. This work proposes a fast switching based on the back-gate. The presented LNA can be switched into low-power sleep mode via the back-gate for a short period of idle time. Compared to back-gate switching, the drawbacks of using front-gate for switching are breakdown problems associated with stacked transistors, stability and the complexity of switching circuits [21]. During the switching progress, due to the high supply voltage, the devices with stacked transistors require a synchronized tie-down of all the voltages to avoid breakdown. A slightly unsynchronized or non-properly defined tie-down profile of the voltages will cause excessive overload voltage leading to breakdown. This increases the complexity of switching circuits supplying the biasing voltages. Furthermore, switching speed and stability are always trade-offs by front-gate switching. Circuit stability is always a major concern for RF circuit design. To ensure the best stability, large DC stabilization capacitors (RF shunt) are usually placed at transistor gate biasing nodes. However, to increase the switching speed less stabilization capacitance is wanted. By applying the back-gate for fast switching, this problem can be avoided. Designers can attach large stabilization capacitance to the front-gate for the best stability while optimizing the back-gate for fast switching with less shunt capacitance. Furthermore, using back-gate for switching could reduce the systems complexity due to reduced IO signals and the corresponding IO circuits for switching purposes. Only one back-gate voltage is needed for the switching task on the top level.

This paper investigates a switchable broadband 60 GHz LNA. The broadband characteristics are realized by distributing the peak gains of different gain stages at different frequencies. For the first time, transistor back-gates are used to switch the LNA into standby mode at its idle time for energy-saving. Moreover, at the same time, transistor back-gates here are utilized to accomplish variable gain control via back-gate for an LNA.

II. NOISE PERFORMANCE AND IMPEDANCE MATCHING

This section reviews the impact of impedance matching at the input and output port of amplifiers on their noise figure, as well as the effect of impedance mismatches on the noise figure of multi-stage amplifiers.

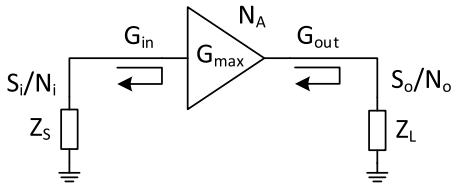

FIGURE 1. Noise analysis of an amplifier with mismatches at input and output.

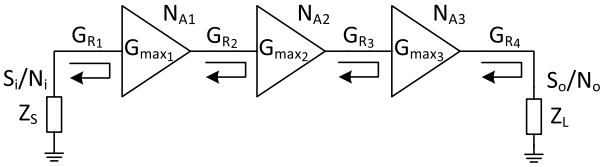

FIGURE 2. Noise analysis of three-stage amplifier with impedance mismatches.

For an amplifier of transducer power gain G between a source of impedance Z_S and load of impedance Z_L, it is possible to write the gain as

$$G = G_{in} \cdot G_{max} \cdot G_{out} \tag{1}$$

where G_{max} is the maximum gain achievable under optimum matching of the amplifier to source and load, G_{in} and G_{out} are matching factors, which indicate the gain losses due to mismatches and they are smaller than unity. For a unilateral amplifier, G_{in} and G_{out} will be independent from one another and function of Z_S and Z_L, respectively.

To illustrate how the mismatch coefficient impacts the noise factor of an amplifier, we consider the schematic in Fig. 1: a signal source of impedance Z_S feeds a signal of power S_i to an amplifier of gain G – factorized as in (1) – which in turn drives a load of impedance Z_L. As the matching factors G_{in} and G_{out} depend on the amplifier and the source and load impedance, by definition the signal power delivered to the load will be $S_o = G \cdot S_i$. The signal source and amplifier are both noisy and contribute with noise powers N_i and N_A, respectively, to the matched load. For a signal power delivered to the load of S_o, the signal-to-noise ratio (SNR) at the load can be written as

$$\frac{S_o}{N_o} = \frac{G_{in} G_{max} G_{out} S_i}{G_{in} G_{max} G_{out} N_i + G_{out} N_A} \tag{2}$$

which allows to express the noise factor of the amplifier as

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{G_{in} G_{max} N_i + N_A}{G_{in} G_{max} N_i} = 1 + \frac{N_A}{G_{in} G_{max} N_i} \tag{3}$$

This shows how the noise factor of an amplifier does not depend on the matching to its load. This aspect can be leveraged in the design of multi-band LNAs, because it allows to tolerate some inter-stage mismatch without degrading excessively the noise factor.

Fig. 2 shows a three-stage amplifier with impedance mismatches at input and output and between stages. $G_{max_{1,2,3}}$

are the maximum gains of each stage and $G_{R_{1,2,3,4}}$ are the matching factors. The SNR at the load can be expressed as in (6), shown at the bottom of the page. As in the single-stage case, the noise factor of the three-stage amplifier can be written as in (7), shown at the bottom of the page.

Applying

$$\frac{N_A}{N_i} = (F-1)G_{in}G_{max} \tag{4}$$

from (3) in (7) results in

$$F = F_1 + \frac{F_2-1}{G_{max_1}G_{R_1}} + \frac{F_3-1}{G_{max_1}G_{max_2}G_{R_1}G_{R_2}} \tag{5}$$

This quantifies how the amplifier gain and impedance mismatches impact the noise factor of a three-stage amplifier, such as the circuit presented in this paper. For well-matched input, output and inter-stage, all G_{R_x} will be approximately equal to 1, and the noise after the first stage will be strongly suppressed by the G_{max} of the stages. Furthermore, equation (5) shows a useful option for broadband or multi-band LNA design: it is possible to realize broadband operation by optimizing the gain of some stages to multiple bands without strongly affecting the noise performance at one or other frequencies, also referred to as gain peaking. In a broadband LNA with gain-peaking at two frequencies, the input and output impedance are matched for both frequencies for practical system-integration reasons, but it is possible to place the peak gain of each stage at target single frequencies by allowing an inter-stage mismatch at one or another band. As an example, assume that the output of the first stage is matched at frequency f_1 leaving frequency f_2 unmatched, and the output of the second stage is matched at f_2 leaving f_1 unmatched. As a consequence, the mismatch degrades the noise performance of the second stage at f_2 – as quantified in (3). However, thanks to the high suppression from $G_{max_1}G_{R_1} \approx G_{max_1}$ the impact of F_2 will be suppressed, maintaining an acceptable noise performance at f_1 and f_2. Section III-C and in particular Table 1 provides a complete quantitative and experimental example of an implementation of this technique.

For ultra-wide and multi-band designs having gain-peaking at more than two frequencies, and more than three stages of amplifiers are needed, equation (5) can be extended for an N-stage amplifier as follows

$$F = F_1 + \frac{F_2-1}{G_{max1}G_{R_1}} + \cdots + \frac{F_N-1}{\prod_{i=2}^{N} G_{max_{i-1}}G_{R_{i-1}}} \tag{8}$$

In a simple yet general case, each band will be matched once between pairs of stages. With (8), it must be noted that it is increasingly challenging to apply single-band inter-stage matching in a long multi-band chain because of the accumulation of the negative effect of poor noise factors $F_N - 1$.

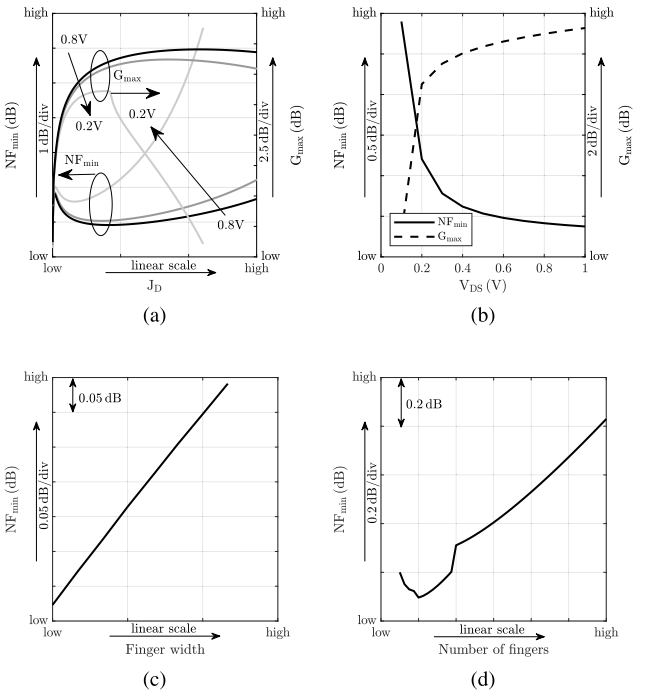

FIGURE 3. Simulated (a) NF_{min} at 60 GHz versus drain current density J_D for different drain-source voltages V_{DS} (0.8 V, 0.5 V, 0.2 V) (b) versus drain-source voltage V_{DS} (c) versus transistor finger width (d) versus transistor number of fingers.

III. CIRCUIT DESIGN

To prove the concept of the inter-stage matching approach presented in the previous section, the LNA was realized in the GlobalFoundries 22FDX® technology. In this section, the related design considerations of the LNA design will be shown.

A. FIELD-EFFECT TRANSISTOR

The noise performance of a transistor core consisting of several parallel transistor units depends on the bias current density, finger width and number of fingers of each transistor unit, and total transistor size. In order to illustrate the optimum bias and layout configuration for the available technology, the corresponding features of the transistor are investigated in this section. For a low gate resistance and consequently a better noise performance, transistors with

$$\frac{S_o}{N_o} = \frac{G_{max_1}G_{max_2}G_{max_3}G_{R_1}G_{R_2}G_{R_3}G_{R_4}S_i}{\left\{\left[(N_iG_{R_1}G_{max_1}+N_{A1})G_{R_2}G_{max_2}+N_{A2}\right]G_{R_3}G_{max_3}+N_{A3}\right\}G_{R_4}} \tag{6}$$

$$F = \frac{S_i/N_i}{S_o/N_o} = 1 + \frac{N_{A1}}{N_i}\cdot\frac{1}{G_{max_1}G_{R_1}} + \frac{N_{A2}}{N_i}\cdot\frac{1}{G_{max_1}G_{max_2}G_{R_1}G_{R_2}} + \frac{N_{A3}}{N_i}\cdot\frac{1}{G_{max_1}G_{max_2}G_{max_3}G_{R_1}G_{R_2}G_{R_3}} \tag{7}$$

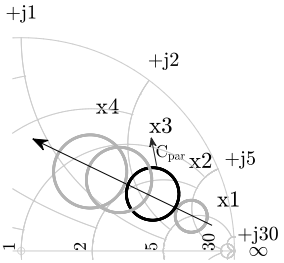

FIGURE 4. Simulated noise circle (NF = 2.6 dB) versus total transistor size at 60 GHz (multiple times of unit transistor core).

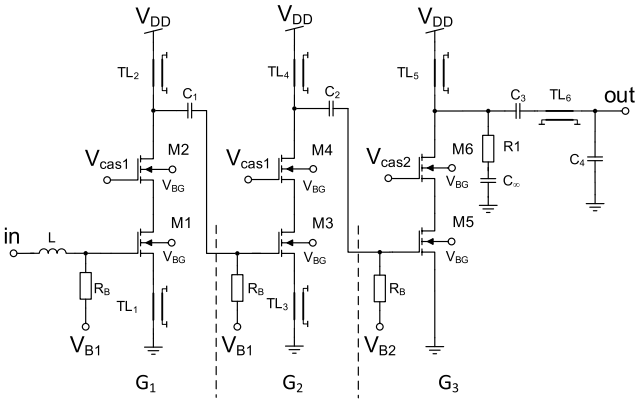

FIGURE 5. Circuit schematic of the presented LNA based on three stages of cascode amplifier $M_{1,2}$, $M_{3,4}$ and $M_{5,6}$.

double-sided gate contacts were used [22]. Fig. 3a shows the relationship between the minimum noise figure (NF_{min}) and drain current density J_D at 60 GHz. The NF_{min} first decreases as the current density increases because of an increasing transconductance g_m and reaches its minimum. As the current density further increases, the NF_{min} grows again for the dominant contribution of channel thermal noise at higher current levels. The drain current density J_D was optimized for a low-noise operation and low DC power. Fig. 3a also indicates that the optimum current range for low noise and the transistor performance remains almost unchanged in certain cases with a lowered drain-source (V_{DS}) voltage. This allows us to optimize the V_{DS} for lower DC power. Fig. 3b describes the relation between noise performance, gain and V_{DS} at the chosen optimum current density. As the V_{DS} decreases, the gain and minimum noise figure decrease slowly before a certain point. An operating voltage above 0.4 V will be sufficient for high gain, low noise, and low power operation.

Fig. 3c illustrates the NF_{min} in terms of the finger width. Because of the impact of the poly-silicon resistance of the gate, the NF_{min} increases with the finger width. Theoretically, it would be optimal to use the minimum finger width allowed. However, with the device lifetime taken into account, as a trade-off, a larger finger width is needed to allow a sufficient number of vias at the drain and source to avoid early electromigration failures. By doing so, the simulation shows that for the chosen finger width the degradation of NF_{min} is as little as about 0.14 dB. The NF_{min} has a strong relation to the number of fingers used in the transistor. The NF_{min} first decreases and reaches its minimum, and with the finger number further increasing, the NF_{min} increases again due to the increasing loss of interconnections using the bottom copper layer, which distributes the signal at the transistor gate to each single finger of the transistor. The number of fingers has been chosen to result in minimum noise. The channel length of the transistors was optimized for the peak f_{max} of the technology.

B. CASCODE GAIN CELL

The cascode circuit was chosen as the gain stage of the LNA. Thanks to the additional common-gate (CG) stage and the resulting higher output impedance, the power gain is higher than that of a normal common-source (CS) amplifier [23]. The cascode amplifier has also better reverse isolation because of the additional isolation of the CG stage. The CS and CG stages have the same transistor size. By sweeping the number of transistor units – which results in different total transistor widths – within the cascode circuit, simulations were run to investigate the relationship between total transistor size and noise performance. Fig. 4 shows the simulated constant noise circles at NF = 2.6 dB with different numbers of transistor units at 60 GHz. A large transistor size could bring the noise circles closer to the 50 Ω source resistance circle (unity circle) at 60 GHz and requires a low-Q impedance matching with higher bandwidth. Additionally, the diameter of the noise circles increases with the transistor size being larger. As a result, a large transistor can be matched for optimal noise over a larger bandwidth. However, the simulation does not include the negative effect in terms of capacitive, resistive and inductive parasitics from the laterally growing interconnections between small transistor units when the transistor size increases. The parasitic capacitance C_{par} will move the noise circles upwards. The larger parasitic inductance of a wide transistor core originating from transistor interconnection lowers the accuracy of the modeling, which is done by neglecting the inductive parasitics. Furthermore, a large transistor core requires metal filling due to density restrictions, which brings more parasitic effects and reduces further the modeling accuracy. Especially, the dense filling of thick metals will cause excessive electromagnetic coupling. Additionally, a large transistor core biased at optimal current density requires a proportionally high DC power; to optimize the design for low DC power for mobile systems, a decision regarding noise matching and power consumption was made: two transistor units were selected. After adding the layout parasitic capacitance at the transistor gate, the noise circle will be closer or crossing the unity circle in Smith-chart, which allows using only one single low-loss inductor for noise matching. This reduces the loss at the input of an LNA benefiting the overall noise performance.

C. CIRCUIT IMPLEMENTATION

The circuit schematic of the proposed LNA is shown in Fig. 5. The LNA consists of three cascode amplifier stages.

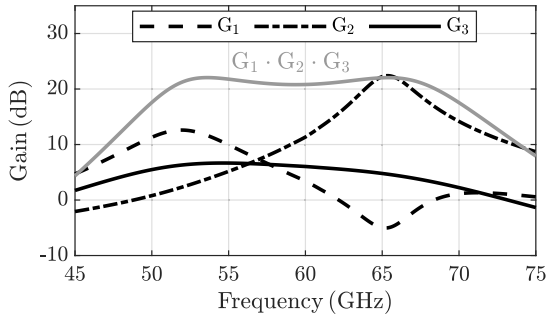

FIGURE 6. Distributed peak gains of the three stages at different frequencies to realize broadband characteristic. G_1-G_3 are the simulated gains of the three amplifier stages.

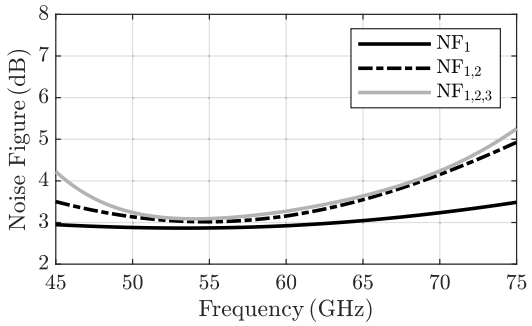

FIGURE 7. Simulated noise figures after gain stage G_1, G_2 and G_3.

TABLE 1. Simulated performance of each amplifier stage.

Stage1				
Freq. (GHz)	G_{R_1} (dB)	G_{max_1} (dB)	G_{R_2} (dB)	NF_1 (dB)
52	−0.57	13.28	−0.11	2.87
65	−0.06	13.21	−18.16	3.05
Stage2				
Freq. (GHz)		G_{max_2} (dB)	G_{R_3} (dB)	NF_2 (dB)
52		17.29	−14.94	4.17
65		23.35	−1.10	7.86
Stage3				
Freq. (GHz)		G_{max_3} (dB)	G_{R_4} (dB)	NF_3 (dB)
52		6.80	−0.49	14.73
65		4.91	−0.12	6.27
Freq. (GHz)	**Cal. NF_{tot} (dB)**		**Sim. NF_{tot} (dB)**	
52	**3.12**		**3.12**	
65	**3.64**		**3.64**	

The channel length and gate width of the transistors $M_{1\text{-}6}$ as discussed in the previous section were optimized for low noise, high gain, and low power.

To reduce losses and consequently improve the noise performance, a simple input matching network consisting of one single inductor was used to transform the 50 Ω source impedance to the optimum noise source impedance $Z_{op,noise}$ at the first gain stage. Inductive source degeneration was applied at the first stage of the LNA in order to bring the optimum impedance $Z_{op,noise}$ for noise matching and the optimum impedance $Z_{op,power}$ for power matching closer to each other, which makes simultaneous matching of power and noise possible.

To obtain a broadband gain response, the frequency behavior of the gain for each stage was engineered as shown in Fig. 6. Simple single-band matching networks consisting of a shorted parallel line and a series capacitor were used for both inter-stage impedance matching networks. The peak gains of the first and second stages were split to 52 GHz and 65 GHz by tuning the matching networks. Thanks to the high suppression $G_{max_1}G_{R_1}$ of the noise factor F_2 of the second stage as explained in (5) and bias in a low-noise mode of the transistors, the degradation of the noise performance associated with the high mismatch loss at the input of the second stage at the upper corner of the frequency band is moderate. The input noise matching of the LNA was mainly optimized for around 65 GHz, because the noise performance of the transistor at lower frequencies is generally good, and noise optimized for around 65 GHz could compensate the slight noise performance degradation to the device. Table 1 gives the simulated stand-alone performance of each amplifier stage in terms of G_{max}, G_R and noise figure (NF), with the same symbol conventions of Section II and Fig. 2. Since the input of the second stage is matched at around 52 GHz, the noise performance of the second stage at 65 GHz suffers from the high mismatch and has a sub-optimal NF. In contrast, the third stage has a poor NF at 52 GHz because of its matched gain at 65 GHz. Applying the simulated values in (5) results in the calculated total noise figure (Cal. NF_{tot}) of the three-stage LNA. The results obtained with (5) show a good agreement with the simulated total noise figure (Sim. NF_{tot}) of the amplifier chain, where the stage amplifiers are in cascade. Fig. 7 illustrates how the simulated noise figure changes at different frequencies after gain stages G_1, G_2 and G_3 are connected to the chain. An increment less than 1 dB of the noise figure at the upper frequency of 65 GHz was observed after the second gain stage G_2. This is however still comparable with the noise figure at 52 GHz. A dual-resonance matching network was implemented at the output of the LNA to ensure broadband impedance matching. An RC network was connected in parallel to the output of the LNA to improve the bandwidth at the cost of some gain.

The transistors $M_{1\text{-}4}$ were biased at an optimum drain current density for their lowest minimum noise figure (NF_{min}); in contrast, the transistors $M_{5,6}$ of the last stage were biased in deep class-AB with a lower drain current density with no input signal, to achieve a higher input 1-dB compression point iP_{1dB}. Furthermore, the transistor back-gates were merged and used for variable gain control. The back-gate voltage can be varied from 0 V (standby mode) up to 2 V (active).

IV. MEASUREMENT RESULTS

The chip micro-photograph of the fabricated LNA is shown in Fig. 8. The core of the circuit occupies 0.2 mm^2

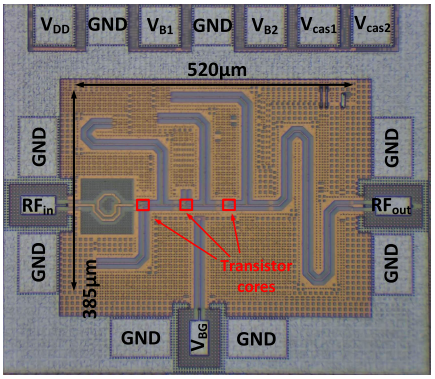

FIGURE 8. Micro-photograph of the LNA.

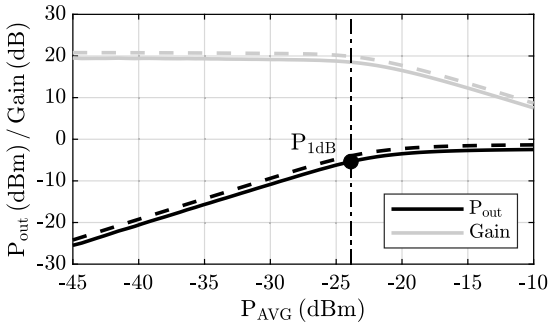

FIGURE 11. Measured and simulated large-signal performance at 60 GHz of the LNA for $V_{DD} = 1.0$ V.P_{AVG} is the available generator power at the input. (solid lines: measurement, dashed lines: simulation).

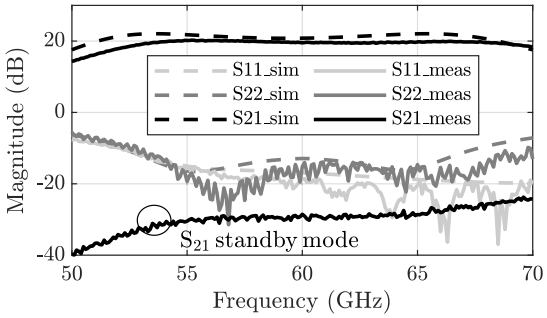

FIGURE 9. Measured and simulated small-signal response of the LNA for $V_{DD} = 1.0$ V.

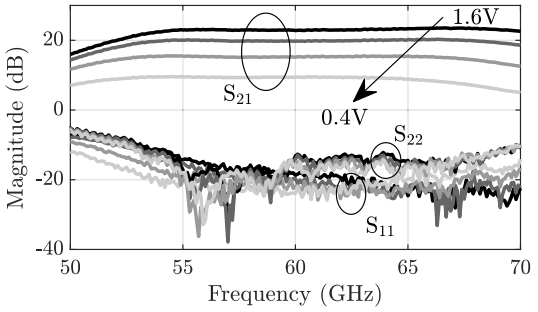

FIGURE 12. Measured forward gain, S_{11} and S_{22} over frequency for different V_{DD} values (0.4 V, 0.6 V, 1.0 V and 1.6 V).

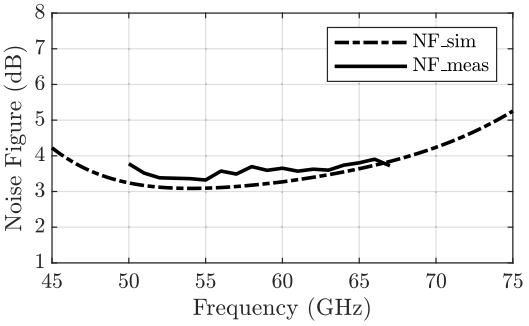

FIGURE 10. Measured and simulated noise figure of the LNA for $V_{DD} = 1.0$ V.

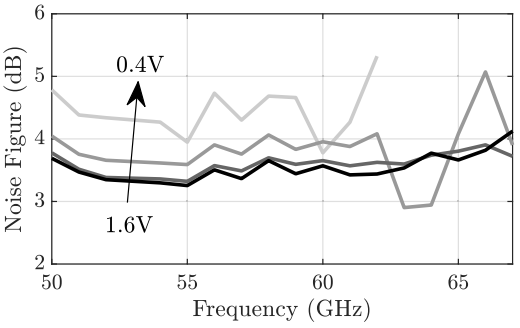

FIGURE 13. Measured noise figure for different V_{DD} values (0.4 V, 0.6 V, 1.0 V and 1.6 V).

(520 µm × 385 µm). Its size can be further reduced if the transmission lines are folded. The LNA was biased with $V_{DD} = 1$ V, $V_{B1} = 250$ mV, $V_{B2} = 150$ mV, $V_{cas1} = 750$ mV and $V_{cas2} = 650$ mV. The back-gate voltage V_{BG} is 2 V when the circuit is in active mode, and 0 V when the circuit is in standby mode. The total DC power is 8.1 mW and decreases to 0.85 mW when the circuit is in standby mode. Both small- and large-signal characterizations were performed on-chip, and the presented results include the losses of the chip pads.

Fig. 9 shows the measured and simulated small-signal S-parameters of the LNA at a nominal supply voltage of 1 V. The measured $|S_{21}|$ shows a flat broadband characteristic with a gain of around 20 dB. The measured −3-dB bandwidth (BW_{-3dB}) is 18.5 GHz from 51.5 GHz to 70 GHz. This is limited by the measurement setup which only supports frequencies up to 70 GHz. The LNA could achieve a measured 1-dB gain flatness from 53 GHz to 69 GHz resulting in a 16 GHz −1-dB bandwidth. The measured $|S_{11}|$ has a broadband frequency response due to the well-chosen transistor size and simple single-inductor matching, and is below −10 dB from 52 GHz to 70 GHz. The upper boundary is limited by the measurement equipment. Thanks to the dual-resonance matching, the output of the LNA shows a dual-peak response at 56 GHz and 64 GHz resulting in a broadband matching: the $|S_{22}|$ is below −10 dB from 52.5 GHz to 70 GHz. Tie the back-gate control voltage V_{BG} down to 0 V, the circuit enters low-power standby mode, and has a gain of below −25 dB. The measured small-signal performance

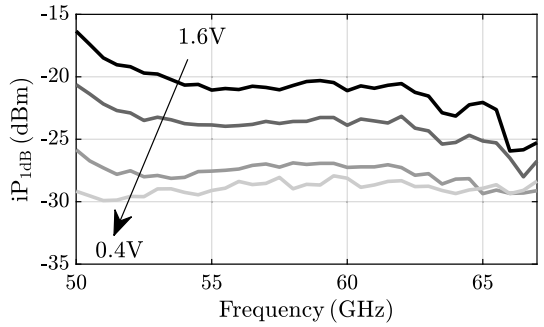

FIGURE 14. Measured iP_{1dB} over frequency for different V_{DD} values (0.4 V, 0.6 V, 1.0 V and 1.6 V).

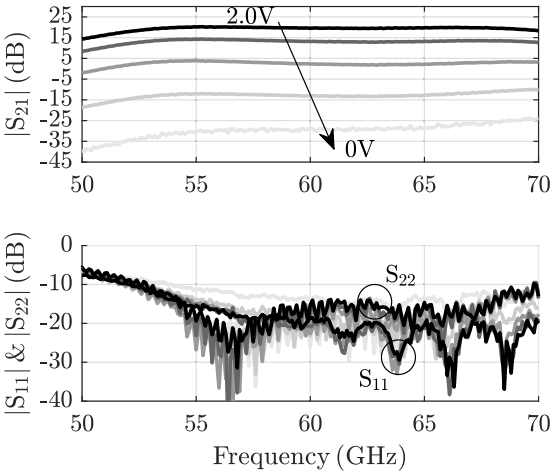

FIGURE 15. Measured forward gain, S_{11} and S_{22} over frequency for different V_{BG} values (0 V, 0.5 V, 1.0 V, 1.5 V, 2.0 V).

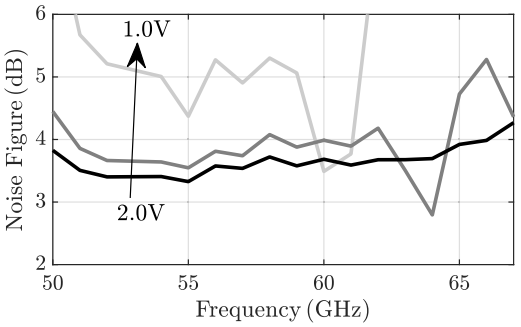

FIGURE 16. Measured noise figure for different V_{BG} values (1.0 V, 1.5 V and 2.0 V).

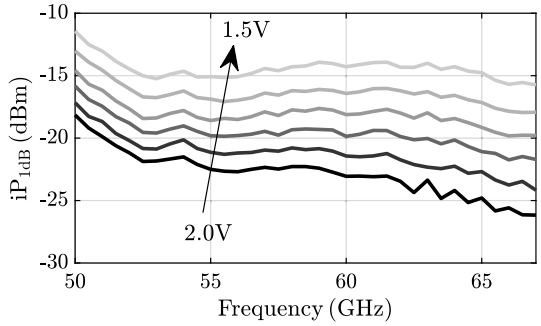

FIGURE 17. Measured iP_{1dB} over frequency for different V_{BG} values (1.5 V to 2.0 V, step 0.1 V).

shows a good agreement with the simulations for both input and output matching and gain.

The measured and simulated NF at nominal bias $V_{DD} = 1$ V are shown in Fig. 10. Due to the measurement setup, the NF was characterized up to 67 GHz. The minimum NF is 3.3 dB. The measured NF is below 4 dB in the entire measurement frequency range from 50 GHz to 67 GHz. The measurements match well with the simulations.

Fig. 11 shows the large-signal performance at 60 GHz and a nominal supply voltage of 1 V. The circuit has an input-referred 1-dB compression point (iP_{1dB}) of −23.9 dBm. The LNA provides a saturated output power of about −2.5 dBm.

The performance of the LNA in terms of small-signal and large-signal behavior under different supply voltages (1.6 V, 1.0 V, 0.6 V and 0.4 V) was also tested. The presented circuit is able to operate from a significantly reduced supply, down to 0.4 V, corresponding to a minimum power consumption of 2.5 mW. The results are shown in Figs. 12 to 14. The forward gain of the LNA decreases with the supply voltage, and a sufficient gain of around 10 dB at the frequencies of interest can still be obtained at a supply voltage of 0.4 V. The port matchings at the LNA input and output ports show they are robust against wide variations of the supply voltage, as they are not impacted significantly by them. Fig. 13 shows the measured NF for different supply voltages as well. For lower supply voltages, the noise performance degrades due to the reduction of the gain. An NF of about 4.5 dB can still be delivered with a supply of 0.4 V. Operating the LNA with a higher supply voltage than the nominal voltage 1 V does not bring significant improvements to the NF, but the gain is higher. The measured iP_{1dB} over frequency for different V_{DD} values is depicted in Fig. 14. Due to the reduced supply, and consequently the reduced voltage headroom in the gain stages, the LNA compresses earlier at a lower supply voltage. For $V_{DD} = 0.4$ V the iP_{1dB} is around −30 dBm.

To test the variable gain control via back-gate, small-signal and large-signal measurements under different back-gate voltages were also conducted. The results are shown in Figs. 15 to 17. Note that the actual voltage tuning step used in the measurement is smaller than the one shown here. The results presented here are selected among the entire set of results to show a clear behavior of gain tuning. The LNA gain decreases as the back-gate voltage decreases due to the reduction of biasing current. The gain of the LNA can be varied from −25 dB to 20 dB using back-gate. Fig. 16 presents the relationship between NF and back-gate voltage. The NF decreases with the back-gate voltage due to the lack of gain. A back-gate voltage of below 1.5 V increases the NF significantly. At $V_{BG} = 1$ V, the NF rises to 5-6 dB. However, this is probably not critical, because the gain will be tuned

TABLE 2. State of the Art of LNAs operating in 60 GHz bands.

Ref.	Process	Freq. (GHz)	Broadband Tech.	Gain (dB)	BW_{-3dB} (GHz)	NF_{min} (dB)	iP_{1dB} (dBm)	P_{DC} (mW)	Area (mm^2)	VGA[†]	FoM
[7]	65 nm CMOS	52.2-63.1	Gain-Distribution	17.4	10.9	3.95	−14.2@ 57 GHz	10	0.26	No	1466
[9]	65 nm CMOS	54.4-90	Gain-Distribution	17.7	35.6	5.4	−15.4@ 65 GHz	19	0.37	No	1289
[12]	65 nm CMOS	60-90	Gain-Distribution	14.2	30	6.3	−10@77 GHz	33.5	0.45	No	721
[11]	22 nm FD-SOI	49.8-68.1	Dual-Resonance	18.1	18.3	4.4	−21.1@60 GHz	3.6	0.39	No[s]	1452
[17]	90 nm CMOS	50-67	Dual-Resonance	17.1	17	5.8	−25@60 GHz	5.7	0.6	FG	273
[1]	65 nm CMOS	54-66[+]	Dual-Resonance	12.8	12[+]	3.6	−6@60 GHz	8.8	0.33	No	5056
[16]	40 nm LP-CMOS	55-65	No	19.8	10	6	−29.5@60 GHz	18	0.22	FG	20
[18]	28 nm CMOS	47.4-61.5	No	20.5	13.8	4.3[♯]	−23.6	20.9	0.41	FG	191
[8]	28 nm LP-CMOS	54.5-72.5	Dual-Resonance	13.8	18	4	−12.5@60 GHz	24	0.38	No	669
[4]	90 nm CMOS	50-67[++]	Dual-Resonance	16.8	17[++]	5.4	−26@60 GHz	5.7	0.6	No	145
[10]	65 nm CMOS	63.5-91	Pole-Converging	13.3	27.5	6.4	−14.3@80 GHz	12	0.24	No	540
[13]	45 nm RF-SOI	55.5-69.1[♭]	N/A	20.4	13.6	5	−23.6@60 GHz	8.6	0.14[*]	No	350
This	22 nm FD-SOI	[H]51.5-70[++] [L]50.8-70[++]	Gain-Distribution	20.2[H] 13.1[L]	[H]18.5[++] [L]19.2[++]	3.3[H] 3.5[L]	−23.9[H] −14.3[L] @60 GHz	8.1[H] 5.5[L]	0.2[*]	BG[s]	856[H] 2138[L]

[*]: core area excluding the pads [H]: high gain @ V_{BG} = 2 V [L]: low gain @ V_{BG} = 1.5 V [+]: limited by data provided [++]: limited by measurement setup
[♯]: simulated result [♭]: estimated from figure [†]: FG(front-gate) BG(back-gate) [s]: switchable

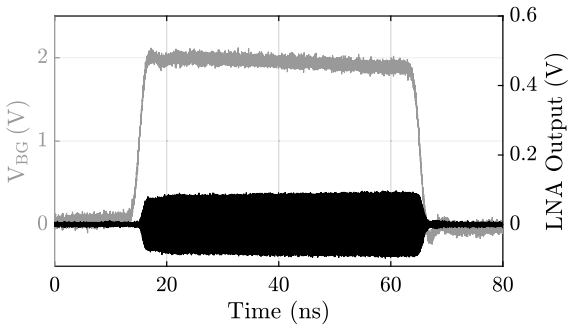

FIGURE 18. Demonstration of dynamic switching via back-gate.

down only when the LNA receives a strong input signal and the receiver tends to saturate. In such a case, the SNR is good enough to tolerate the drop of NF. Fig. 17 demonstrates the improved LNA dynamic range by tuning the back-gate voltage. By lowering the V_{BG}, the biasing current of the transistors are lowered. This decreases the LNA gain and increases the iP_{1dB}. In the measurement, an improvement of about 10 dB is achieved for the iP_{1dB} by reducing the V_{BG} from 2 V to 1.5 V.

As already mentioned, the back-gate control voltage can be used to switch the entire LNA between low-power standby and active mode. Fig. 18 demonstrates the dynamic behavior of the LNA under a 10 MHz square-wave V_{BG} signal. The LNA was fed by a 60 GHz RF signal at the input during the test. The waveforms of the control signal and LNA output were captured by a high-end real-time oscilloscope. The measurement shows that the LNA can be switched between two modes within 3 ns. Note that the actual time of switching should be faster because the slope of the control signal is not sharp limited by the available lab equipment. An internal on-chip driver can be implemented to overcome this problem.

V. CONCLUSION

In this paper, a switchable back-gate tuned variable gain 60 GHz LNA with a broad operating band and low DC power is presented and investigated. To prove the concept, it is implemented in a 22 nm FD-SOI CMOS technology. The circuit consists of three cascode stages. The impact of mismatch losses was discussed and quantified with a theoretical analysis of the relation between mismatch and noise performance of single-stage and multi-stage amplifiers. The results illustrate the potential of using a gain peaking technique to realize broadband operation for LNA designs. Applying this method, single-band matching networks have been introduced for the inter-stage matching of the LNA to realize the broadband characteristic. At the input of the LNA, a single-inductor matching network was applied for low loss and better noise performance. At the output of

the LNA, a dual-resonance matching network was used to obtain matching and gain simultaneously around 56 GHz and 64 GHz. The proposed LNA consumes a DC power of 8.1 mW from a nominal supply voltage of 1 V at a nominal back-gate voltage V_{BG} of 2 V. With a reduced supply voltage, the DC power can be lowered to only 2.5 mW while the LNA still provides a sufficient gain and noise figure. In this work, back-gate control was investigated for such an LNA to enable variable gain capability and save energy. Leveraging the back-gate biasing voltage, the threshold voltage of the transistors can be tuned, consequently enabling control of the biasing current and gain. Compared to the front-gate based variable gain control, the back-gate based scheme can also deliver continuous gain tuning but has lower requirements on the gain control circuits in terms of accuracy or resolution. The measurements have shown that the LNA gain can be tuned continuously from −25 dB to 20 dB via the back-gate biasing voltage. The measurements have also demonstrated that the iP_{1dB} can be improved by tuning down the back-gate voltage. By lowering the back-gate voltage from 2 V to 1.5 V, the iP_{1dB} was improved by about 10 dB. Furthermore, the capability of the fast switching between active and low-power standby mode via back-gate has been proven. When there is no data transmission ongoing, the LNA can be switched to standby mode at its idle time to save energy. The switching time is less than 3 ns. The back-gate switching could solve the problems of front-gate switching in terms of breakdown, stability and complexity of switching circuits. From a nominal supply voltage of 1 V, the LNA consumes only 850 µW of DC power when it is switched to low-power standby mode. For a reduced supply of 0.4 V, the LNA draws 240 µW of DC power in standby mode. If a long period of idle time is expected, as the second tier of switching, the supplies can be tuned down to reduce the DC power to zero. Table 2 compares the presented LNA design to previously reported LNAs operating in 60 GHz mmW bands. In high gain mode ($V_{BG} = 2$ V), it provides one of the highest gain and the lowest noise figure measured for a competitive DC power. Moreover, the presented LNA shows an outstanding bandwidth of 18.5 GHz under consideration of high gain. Beyond this, the LNA has also a good in-band gain flatness. It has an in-band 1-dB flat band of 16 GHz ranging from 53 GHz to 69 GHz. By tuning the back-gate voltage V_{BG} to 1.5 V, the LNA can be switched to low-gain mode. The power gain drops down to 13.1 dB while showing an improved iP_{1dB} of −14.3 dBm and lower DC power of 5.5 mW. Comparing the figure-of-merit (FoM) [8],

$$\text{FoM} = \frac{G \cdot \frac{\text{iP}_{1\text{dB}}}{\text{mW}} \cdot \frac{\text{BW}}{\text{MHz}}}{(F-1) \cdot \frac{\text{P}_{\text{DC}}}{\text{mW}}} \tag{9}$$

where G and F are the power gain and noise factor in linear scale, the presented circuit outperforms most of the designs reported when operating in low-gain mode. However, in high-gain mode, the circuit only shows a moderate FoM. To the best of the authors' knowledge, this is the first 60 GHz LNA accomplishing simultaneous fast switching and variable gain control via back-gate biasing.

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