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RESEARCH ARTICLE

FEOL Monolithic Co-Integration of FeFET and CMOS on 8-Inch Wafer Using Laser Spike Annealing With Implementation of an FeFET Inverter

BOHYEON KANG, (Member, IEEE), JEHYUN AN, (Member, IEEE), JONGSEO PARK, (Member, IEEE), GIRYUN HONG, (Member, IEEE), BEOMJOO HAM, (Member, IEEE), JAESEONG PYO, SUNG-MIN AHN, (Member, IEEE), AND ROCK-HYUN BAEK, (Member, IEEE)

Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang 37673, Republic of Korea

Corresponding authors: Sung-Min Ahn (josh21@postech.ac.kr) and Rock-Hyun Baek (rh.baek@postech.ac.kr)

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ABSTRACT Ferroelectric devices and monolithic three-dimensional integration technology (M3D) with good CMOS process compatibility have emerged as promising solutions to scaling issue at the device and system levels, respectively. In this study, we developed a monolithic co-integration scheme, which sequentially fabricates CMOS devices and ferroelectric field-effect transistors (FeFETs) on the front-end-of-line (FEOL) area of the same 8-inch wafer. To fabricate FeFETs after CMOS device fabrication and achieve co-integration on the FEOL area, an etch-back process was developed to remove thick oxide over a wide area. FeFET fabrication involves the selective laser spike annealing (LSA) in the source/drain region of the FeFET to implement the low thermal budget process crucial for monolithic integration. In our test, LSA resulted in a lower sheet resistance compared to conventional rapid thermal annealing (RTA), thus validating its performance for dopant activation. The monolithic co-integration completed by incorporating this LSA was evaluated by measuring the electrical characteristics of CMOS, FeFET and FeFET inverter, which was first fabricated in this work. By developing this monolithic co-integration, this work offers an opportunity to integrate diverse new devices in addition to the FeFET with CMOS and achieve further advancements in technology.

INDEX TERMS Co-integration, FeFET inverter, ferroelectric field-effect transistor (FeFET), front-end-of-line (FEOL), laser spike annealing, monolithic integration.

I. INTRODUCTION

For decades, scaling strategies have led to advancements in complementary metal-oxide-semiconductor (CMOS) technology. However, due to continuous scaling, the limitations of scaling have become evident, including restricted device performance and high–power consumption. Various solutions are currently being implemented to overcome these limitations, one of which is the device-level approach, which involves the introduction of devices based on new concepts [1]. The feasibility of any new device technology is determined by its compatibility with the CMOS process and whether it can exhibit unique functionality that is difficult to implement with existing CMOS technology. From this perspective, ferroelectric devices are notable candidates, demonstrating distinctive characteristics

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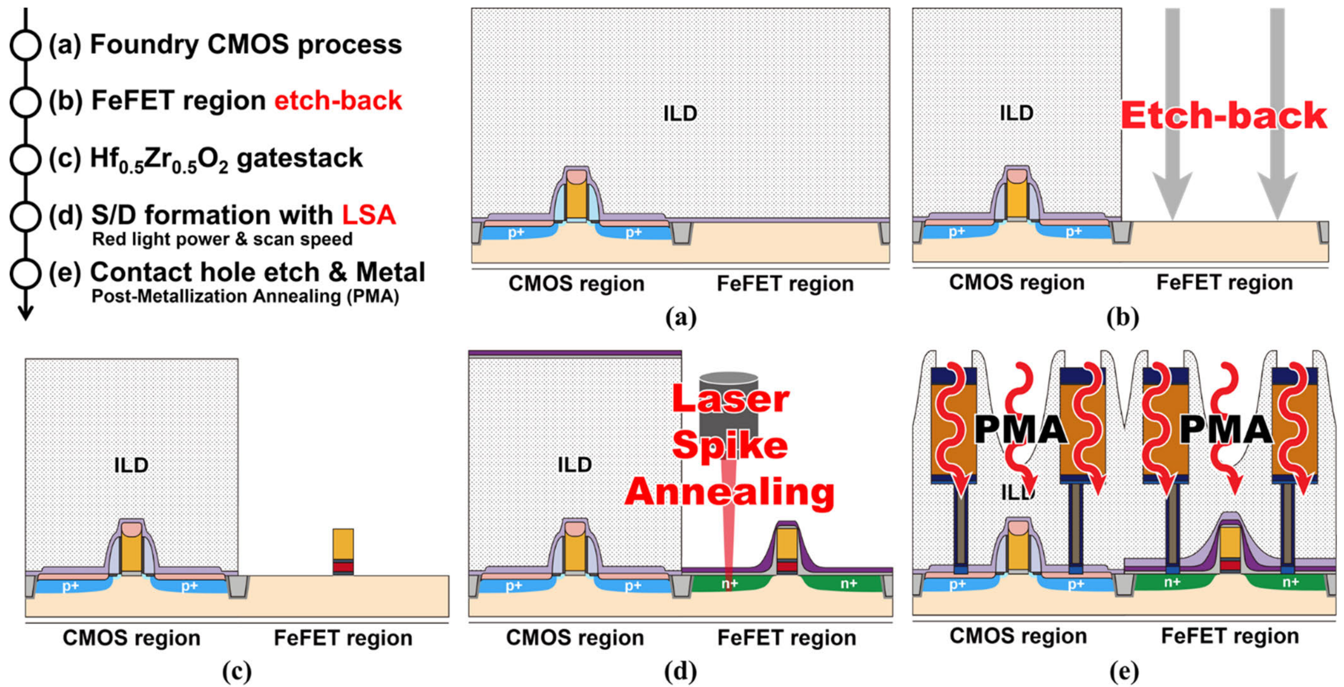


FIGURE 1. Co-integration process flow and corresponding schematics of each processing step ((a)–(e)). Etch-back and laser spike annealing (LSA) are the critical processes for the co-integration.

of spontaneous polarization without the need for an external electric field [2], [3]. This property has enabled the development of innovative negative-capacitance field-effect transistors (NCFETs) with a subthreshold slope (SS) below 60 mV/dec [4], [5], [6], [7], [8] and memory devices based on the hysteresis property induced by altering the internal polarization of the ferroelectric [9], [10], [11], [12], [13]. In addition, hafnium zirconium oxide (HZO) is a suitable ferroelectric material owing to its good ferroelectricity and compatibility with CMOS processes [14].

Another solution for sustaining Moore's law involves a system-level approach. Monolithic 3D integration technology (M3D) has emerged as a solution to address the scaling challenges. While various 3D integration methods such as wire-bonding, interposer, and through-silicon vias (TSVs) are under investigation, monolithic integration stands out for its potential for high-density integration facilitated by extremely small inter-tier vias [15], [16]. M3D enables the creation of extremely dense integrated circuits and offers design flexibility by utilizing nanometer-scale inter-tier vias instead of larger TSVs with diameters in the range of several micrometers. Moreover, inter-tier vias offer higher electrical performance than TSVs, which are associated with significant parasitic capacitance and mechanical stress [16]. Therefore, monolithic integration helps mitigate the scaling issues from a system perspective.

However, implementing monolithic integration is challenging due to its vulnerability to high process temperatures, as it requires fabricating multiple device types on the same wafer. To successfully implement stable monolithic integration, it is essential to employ low-temperature processes to prevent the deterioration of previously manufactured devices [15], [16]. Laser spike annealing (LSA) has recently gained a lot of attention as a promising candidate for low thermal budget processes. LSA offers the advantage of selectively applying annealing to specific regions, making it particularly suitable for monolithic integration compared to rapid thermal annealing (RTA), which uniformly heats the entire wafer. Owing to these benefits, LSA has been investigated for various applications in device fabrication, including dopant activation, damage removal in ion implantation (I/I), crystallization, and post-deposition annealing [17], [18], [19], [20].

An innovative solution to current issues is merging these device- and system-level approaches. Despite the excellent prospects of ferroelectric devices, changing the existing CMOS ecosystem using only new devices is time-consuming and expensive. A more practical approach is to replace a part of the CMOS device with new devices using monolithic integration. So, several studies have attempted to develop co-integration of CMOS device and different types of devices [21], [22]. However, these studies have not fully addressed the need for stable monolithic integration through low-temperature processes. Additionally, the proposed schemes are limited to specific materials and structures.

Therefore, in this study, we developed a monolithic co-integration process incorporating the LSA to ensure the low thermal budget. Using this process, we integrated ferroelectric FETs (FeFETs) with CMOS devices on the FEOL

area of the same 8-inch wafer. LSA was used as a substitute for RTA in the source/drain (S/D) manufacturing process of FeFETs to manage high process temperature. Also, an etch-back process was developed to sequentially fabricate the FeFETs on the FEOL area after CMOS process. FEOL monolithic integration on the bulk Si substrate allows the use of high-quality Si substrate and the standard back-end-of-line (BEOL) process of CMOS. Using this monolithic co-integration, this work presents a novel FeFET inverter composed of a co-integrated FeFET and CMOS, which can constitute a nonvolatile memory system based on its unique ferroelectric properties. Furthermore, in addition to the FeFETs, any novel devices can be incorporated with CMOS using this co-integration process. This paper presents an innovative approach for advancements in semiconductor technology, particularly for the co-integration of new devices with conventional CMOS processes.

II. MONOLITHIC CO-INTEGRATION AND CHARACTERIZATIONS

A. CO-INTEGRATION OF FEFET AND CMOS ON FEOL AREA

CMOS devices and FeFETs were integrated simultaneously into the front-end-of-line (FEOL) region of an 8-inch wafer to utilize both types of devices. The manufacturing process proceeded sequentially, with the CMOS devices fabricated first using an established foundry process, followed by FeFET fabrication. Fig. 1 shows the flow of the entire co-integration process used in this study. Figs. 2(a) and (b) show the results after CMOS process in the foundry, corresponding to Fig. 1(a).

In Fig. 2(a), the CMOS and FeFET regions are visibly distinguished, with distinct active and field areas present in each. The active area corresponds to the Si substrate where the devices are fabricated, whereas the field area serves to isolate individual devices with SiO_2. Notably, the gate structure is exclusively present in the active area of the CMOS region, whereas the FeFET region exhibits only an active area devoid of the gate structure. Fig. 2(b) shows a cross-sectional perspective, revealing a 700-nm-thick interlayer dielectric (ILD). The foundry CMOS process was modified by adding a protective step to exclude the silicidation process from being applied to the FeFET region, thus facilitating the production of FeFETs in the subsequent steps. The inset in Fig. 2(b) shows the oxygen and nitrogen distributions measured using energy-dispersive X-ray spectroscopy (EDS). Specifically, only the silicon oxide and nitride layers were deposited on the FeFET region during CMOS device fabrication, with no indication of silicide formation, effectively preserving the active area of the FeFET region.

To remove the thick ILD deposited over a wide area and expose the Si substrate for FeFET fabrication adjacent to the CMOS region, an etch-back process was developed, as depicted in Fig. 1(b). Subsequently, FeFET gate structures were fabricated on the active areas of the FeFET region following the completion of the etch-back process (Fig. 1(c)).

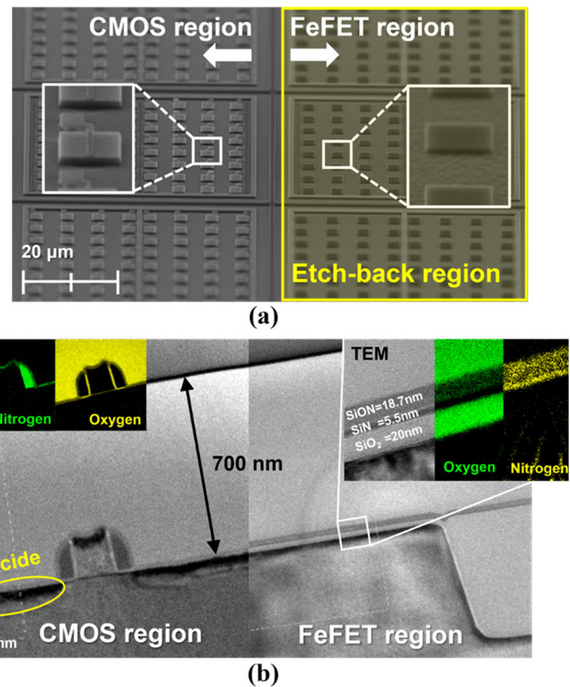


FIGURE 2. Results of processing in the foundry corresponding to the process step shown in Fig. 1(a): (a) Top view of boundary between CMOS region and FeFET region measured by SEM and (b) Cross-sectional view of the CMOS and FeFET regions measured using a TEM. The inset shows the EDS images, which show the distributions of each element.

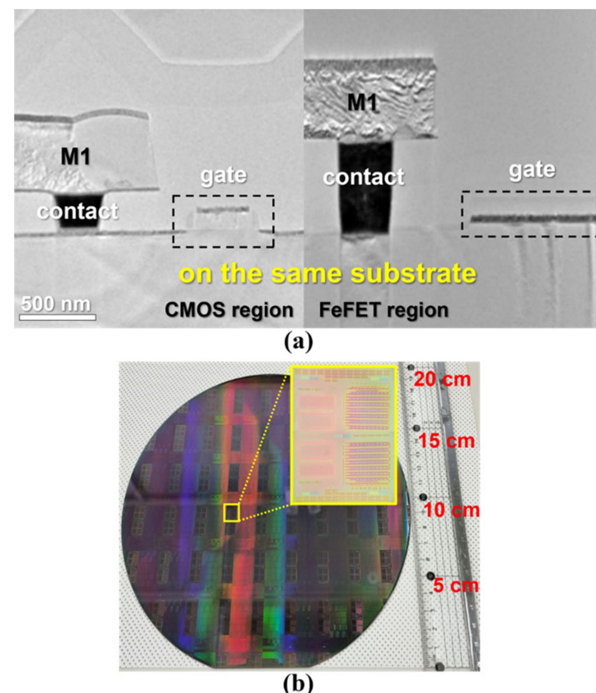


FIGURE 3. (a) Cross-sectional view of CMOS and FeFET regions after completion of fabrication up to Metal 1 line (M1), corresponding to the process step shown in Fig.ure 1(e). (b) An 8-inch wafer with completed co-integration. The inset image shows an optical microscope view of the circuit layout.

SiO_2 3.3 nm thick was deposited by plasma-enhanced atomic layer deposition (ALD) at 150 °C for 20 min, followed by the

deposition of 10 nm TiN via sputtering at 300 °C for 10 s. Subsequently, 30 nm of HZO was deposited using thermal ALD at 270 °C for 4000 s, followed by the deposition of an additional 10 nm of TiN via sputtering at 300 °C for 10 s. Gate etching was performed by BCl_3/Cl_2 plasma etching at an $Ar:Cl_2:BCl_3$ ratio of 1:1:3 for 50 s.

After gate formation, S/D regions were created using LSA (Fig. 1(d)). To demonstrate LSA, an 8-inch p-type Si (1 0 0) wafer was used as the substrate, and P-ions were implanted with a dose of 4.6×10^{15} cm^{-2} and at energies of 25, 35 and 45 keV using a high-current ion implanter (Axcelis, G-1510). A red ($\lambda = 613$ nm) laser (APS System, VisAA) was used. The size of the focused beam injected into the sample was 160×100 μm^2. Scan speeds of 10 and 100 mm/s were applied. The distance between two adjacent scan paths was fixed at 80 μm, yielding a 50% overlap of the scan path. The laser power emitted onto the sample was measured using a power meter embedded in the laser system (VisAA).

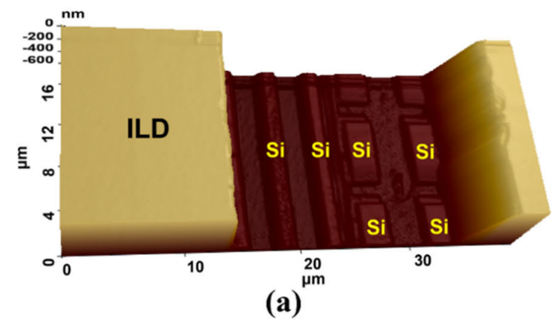
Following S/D creation with LSA, the ILD was deposited, and metal lines were formed, as shown in Fig. 3(a), which corresponds to the process step shown in Fig. 1(e). In this stage, the CMOS device and FeFET were interconnected to form a circuit. Fig. 3(b) shows the final monolithic co-integration result with the FeFET and CMOS devices on the same 8-inch Si wafer. These results demonstrate the successful implementation of the monolithic co-integration scheme.

B. PHYSICAL AND ELECTRICAL CHARACTERIZATIONS

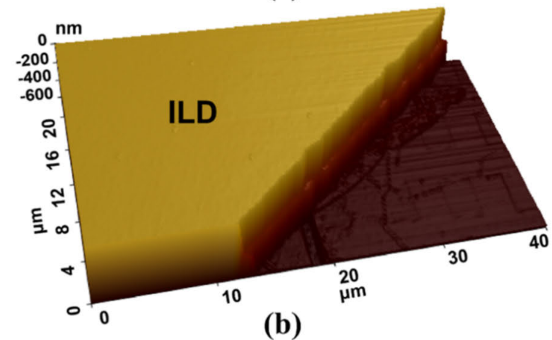
The cross-sectional morphology and thickness of each layer were measured using high-resolution transmission electron microscopy (HR-TEM; JEOL JEM-2100F) and high-resolution field-emission scanning electron microscopy (FE-SEM; JEOL JSM 7401F). An elemental analysis was performed using energy-dispersive X-ray spectroscopy (EDS). The surface morphology and surface roughness were measured using atomic force microscopy (AFM; Oxford, Jupiter XR). The dopant (P) distribution was determined using secondary ion mass spectrometry (SIMS; CAMECA, IMS 6F). The sheet resistance of the annealed samples was measured using a four-point probe resistivity measurement system (AIT, CMT-SR2000N). The current–voltage (I–V) characteristics and voltage transfer characteristics of the FeFET inverter were measured using a Keysight B1500A semiconductor device analyzer. A waveform generator and fast measurement unit (WGFMU) module (B1530A) was used for the fast I–V measurements.

III. RESULTS AND DISCUSSION

There are two primary requirements to establish a monolithic co-integration with FeFET and CMOS on the FEOL area: (1) Exposing the Si substrate within the FeFET region for FeFET fabrication without damaging the Si surface and (2) applying low process temperatures to avoid damaging the previously manufactured devices. For monolithic integration, because both the CMOS and FeFET fabrication processes occur consecutively on the same wafer, a scheme to avoid damaging the previously manufactured devices during subsequent manufacturing steps should be adopted. In particular,



(a)



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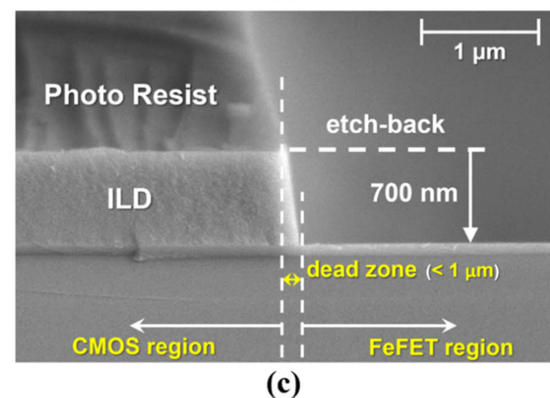

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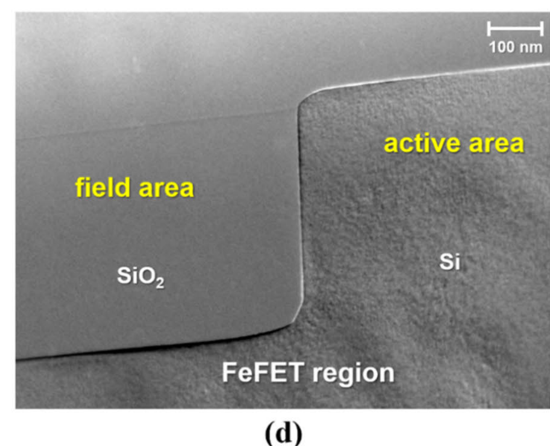


(d)

FIGURE 4. Results of the etch-back process: AFM images captured after wet etching for (a) 40 s and (b) 80 s; (c) SEM image presenting the boundary between the CMOS and FeFET regions, highlighting the narrow dead zone 8 VOLUME XX, 2017 under 1 μm. (d) TEM image showing the exposed Si surface of FeFET region devoid of oxide and nitride stacks observed in Fig. 2(b).

because high processing temperatures can cause device failure, LSA has been introduced as an alternative to RTA to prevent high-temperature processing during S/D annealing.

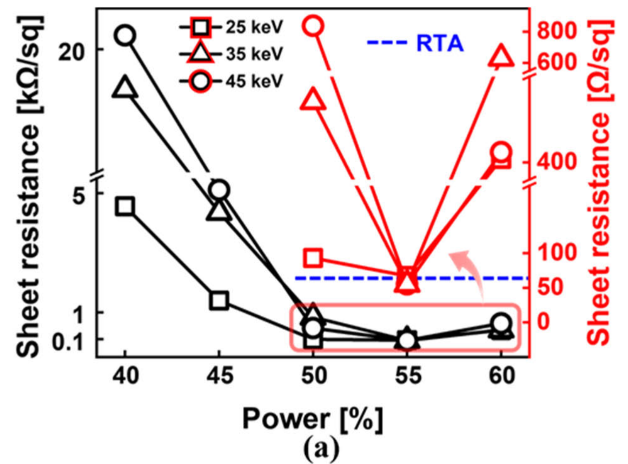
Furthermore, when the wafers are fab-out from the foundry after the CMOS process, a thick ILD is deposited to protect the wafer. To manufacture FeFETs on the same Si substrate, it is necessary to remove this ILD within the FeFET region. However, unlike typical etching processes that target narrow areas, this process requires the removal of a thick material over a wide area spanning tens of micrometers. If a thick material is etched at an angle, it can result in a greater loss of the FeFET region compared to etching a thin material. Therefore, it is important to etch this ILD as close to vertical as possible to minimize the "dead zone," which is an area unusable for device manufacturing. Moreover, a wide etching area can cause variations in the etched thickness between the regions adjacent to the boundary of the CMOS and FeFET regions and regions farther away from it. To address these problems, we introduced a two-step etching process. Initially, a region of approximately 600 nm was removed via dry etching to ensure vertical etching, followed by wet etching to achieve a smooth surface.

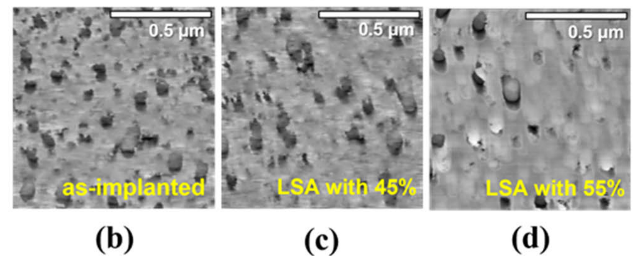
Figs. 4(a) and (b) show the surface structure after wet etching measured using an AFM. Wet etching for 80 s (Fig. 4(a)) resulted in an excessive etching of SiO_2, leading to a significant difference in surface height between the active area composed of Si and the field area composed of SiO_2. In contrast, wet etching for 40 s (Fig. 4(b)) resulted in a minimal difference in the surface height between the active and field areas. Consequently, the wet-etching duration was set to approximately 40 s, and the etch-back process was completed by applying a subsequent cleaning process. Fig. 4(c) shows the result of the etch-back process. Clearly, the 700-nm-thick ILD was successfully etched, with only a small dead zone of less than 1 μm. Fig. 4(d) shows the surface of the FeFET region, illustrating the disappearance of the oxide and nitride layers observed in Fig. 2(b) and the clear exposure of the Si substrate surface.

TABLE 1. Matching the percentage of the maximum power to the actual power measured by the power meter.

	Power					
%	40	45	50	55	60	100
W	16	18	20	22	24	40

The key process in this work is LSA for the S/D activation of the FeFET, which differentiates from other previous work and completes low-temperature stable monolithic integration. LSA is an essential process for monolithic integration to reduce the thermal budget. Unlike RTA, which heats the entire wafer, LSA selectively irradiates a laser beam only on specific areas of the wafer for annealing. So, it is possible to anneal without damaging the previously manufactured elements. We evaluated the performance of LSA for dopant activation on a non-patterned wafer. A continuous-wave laser with a wavelength of 613 nm was utilized, allowing us to adjust the laser output power as a percentage of the maximum power of the laser source, which was 40 W.





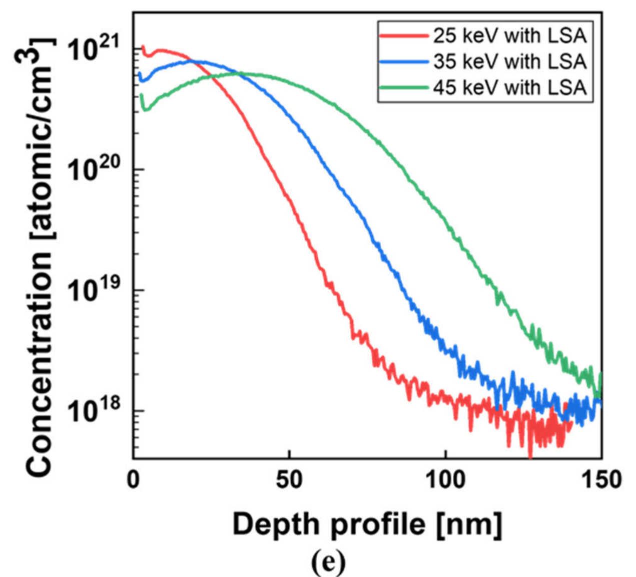


FIGURE 5. (a) Sheet resistance of the test samples, subjected to multiple conditions of I/I energies (25, 35 and 45 keV) and various LSA powers on non-patterned wafers, compared with the RTA case; AFM images showing the surface of Si (b) without annealing with an I/I energy of 25 keV and after LSA at a power of (c) 45% and (d) 55%; (e) Dopant (P) distribution from the Si surface measured by SIMS.

TABLE 1 shows the corresponding actual power measured by the power meter for each percentage value. Test samples were prepared with LSA applied to a non-patterned wafer at a scan speed of 100 mm/s, and they were divided into

three groups based on I/I conditions: energies of 25, 35 and 45 keV were employed with a dose of 4.6×10^{15} cm^{-2}. Fig. 5(a) shows the sheet resistances measured after annealing at various output powers to assess the efficiency of LSA for dopant activation. At a laser power of 40%, dopant activation was insufficient, resulting in high sheet resistances. With the increase in the laser power, dopant activation improved, leading to a decrease in the sheet resistance. In particular, at laser powers exceeding 50%, the sheet resistance decreased significantly, reaching values of less than 1 kΩ/sq. Remarkably, the lowest sheet resistance was attained at a power of 55% for all doping energies, measuring 67, 57 and 55 Ω/sq for energies of 25, 35 and 45 keV, respectively. The values at the I/I energies of 35 and 45 keV were lower than that obtained with RTA at 1000 °C for 10 s (64 Ω/sq). This indicates that the LSA process effectively activates dopants for S/D formation and can be a practical substitute for RTA.

In addition, annealing with a laser of adequate power can produce the effect of curing the surface of Si damaged by I/I. Figs. 5(b), (c) and (d) show the as-implanted Si surface with an I/I energy of 25 keV and the Si surface after annealing at a laser power of 45% and 55%, respectively. Annealing at the power of 55% notably reduced the damage to the Si surface whereas 45% power did not reduce the damage. The root-mean-square (RMS) roughness of the surface as-implanted and annealed at 45% power were 1.3 and 1 nm, whereas it decreased to 0.6 nm after annealing at the power of 55%. In other words, LSA at a laser power of 55% has an effect of curing surface defects, which can reduce the scattering centers and improve the electrical properties.

Meanwhile, in cases where dopant activation was insufficient (at powers $< 50\%$), higher sheet resistances were observed with higher doping energies (35 and 45 keV) at the same laser power (Fig. 5(a)). This is similar to the results obtained when applying RTA and can be attributed to the different dopant distributions depending on the I/I energy (Fig. 5(e)). When the laser power was low, little energy contributing to dopant activation was transmitted to the deep region; therefore, dopant activation occurred primarily near the surface. For a doping energy of 25 keV, where the amount of dopant on the surface was greater than that at 35 and 45 keV, the sheet resistance exhibits lower value than that at the other I/I energies.

However, when dopants were adequately activated (e.g., at a power of 55%), the sheet resistances were similar to each other, regardless of the doping energy. With laser power increasing, the energy delivered to the deep region for dopant activation increased, and the sheet resistance gradually decreased. Ultimately, at sufficient laser power levels, the dopant activation energy provided by LSA could be transmitted to a sufficient depth, resulting in similar sheet resistances regardless of the dopant distribution. However, an excessive laser power can degrade the electrical characteristics, causing an increase in the sheet resistance. This suggests the existence of an optimal laser power for effective dopant activation; for this non-patterned wafer, the power of 55% is considered as the optimal laser power.

In addition to the laser power, an optimal I/I energy should be determined for the integration process. Given our integration process where I/I is performed simultaneously in both the S/D area and the gate structure of FeFETs, the I/I energy should be set to prevents excessive dopant penetration into the HZO layer. Using the *Sentaurus* technology computer-aided design (TCAD) tools, we determined that the optimal energy to protect the gate structure and form the S/D is 30 keV.

TABLE 2. Table showing the LSA conditions for patterned wafer testing.

	#1	#2	#3	#4	#5	#6	#7	#8
Scan speed [mm/s]	10	10	10	10	100	100	100	100
Power [%]	25	30	35	40	25	30	35	40

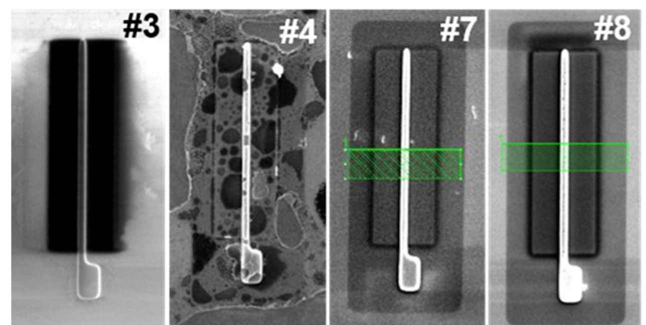


FIGURE 6. Images of the gate structure after LSA.

Like I/I energy, LSA conditions should be evaluated with respect to the process integration. Despite the demonstration of LSA on a non-patterned wafer, when LSA is incorporated into the process integration, the outcomes may differ from those observed when LSA is applied to a flat wafer. Hence, to introduce LSA into the co-integration, it is crucial to demonstrate its characteristics when applied to a patterned wafer where the device structure is formed. To determine suitable LSA conditions for a patterned wafer, LSA was conducted under various conditions by adjusting the laser scan speed and output power (TABLE 2).

In cases without the pattern, the substrate was effectively annealed at an output power of 55% (Fig. 5(a)). However, when patterns were present, increasing the output power to 55% caused damage to the wafer. Therefore, for patterned wafers, the output power for the experiment was reduced to a range of 25%–40%. In TABLE 2, Conditions #1 to #4 involved a low scan speed, with #3 and #4 resulting in device damage (Fig. 6), particularly under Condition #4, which resulted in severe damage. Conditions #5 to #8 utilized a high scan speed, with only minor scorching observed under Condition #8, while the overall outcomes were satisfactory. Low scan speeds, such as 10 mm/s, resulted in a higher energy delivery to the wafer; therefore, even a low laser power can destroy the device with the same material. This makes it

difficult to precisely control the energy delivery to the device by restricting the range of available power. In addition, a low scan speed increases the processing time. Consequently, Condition #7, which ensures stable annealing at maximum power and high speed, was chosen as the suitable LSA condition and applied to the integration process.

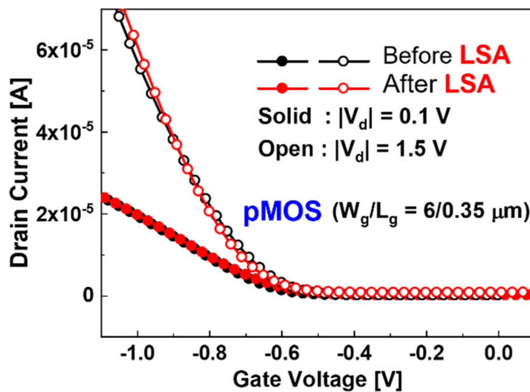


FIGURE 7. Drain current of pMOSFET fabricated in the foundry measured before and after LSA.

The results of the monolithic co-integration were assessed through electrical measurements. First, it is important to verify the performance of previously manufactured devices, as it is a key point for completing monolithic integration using LSA. Therefore, we evaluated whether the CMOS device's performance is affected by the LSA process. Fig. 7 shows a comparison of the drain current of the CMOS device measured immediately after the fabrication at the foundry with the results obtained after LSA. Notably, the current characteristics remained nearly identical before and after LSA, indicating that the CMOS device characteristics were unaffected by the LSA. Consequently, with the integration of LSA into the FeFET manufacturing process, monolithic co-integration was established to produce subsequent FeFETs without compromising the characteristics of the existing CMOS device. After demonstrating the CMOS device, the drain current of the FeFET was evaluated.

Fig. 8(a) shows the I_d–V_g curves of $Hf_{0.5}Zr_{0.5}O_2$-nFeFET obtained using conventional and fast I–V measurements. In the case of the conventional I–V measurement of the FeFET, owing to the trapping that occurs during the measurement, V_{th} of the reverse sweep is positively shifted compared with the forward sweep. Therefore, an I_d–V_g double-sweep is observed in the clockwise direction [23]. Fast I–V measurements, which are used to minimize the trapping effect, revealed only the polarization characteristics of the ferroelectric material. In the reverse sweep, V_{th} shifted negatively compared with that in the forward sweep and exhibited a counter-clock wise (CCW) loop, which is a ferroelectric characteristic. In other words, with the use of fast I–V measurements, the trapping effect was significantly reduced, leaving only polarization and exhibiting ferroelectric characteristics. Fig. 8(b) shows the n-FeFET I_d–V_d curves measured using the fast I-V measurement. The negative differential resistance (NDR) effect, in which I_d decreases as the V_D increases, appears due to the polarization of the ferroelectric material.

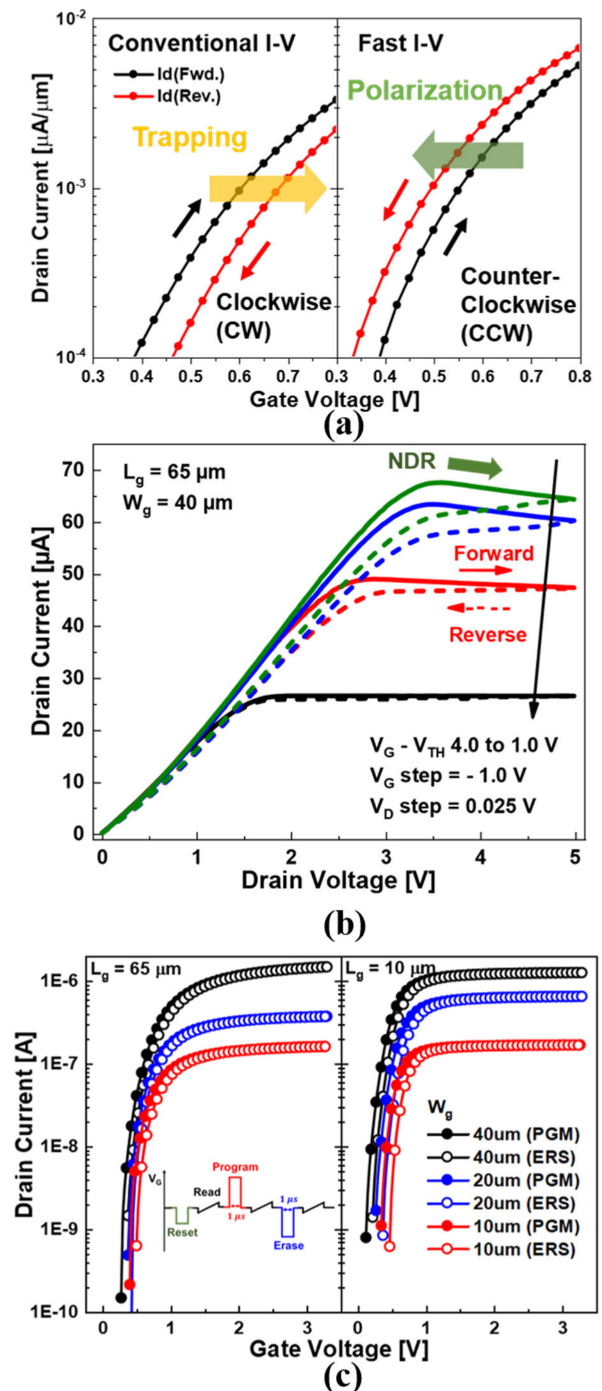


FIGURE 8. (a) Comparison of n-FeFET $I_d - V_g$ curves obtained using conventional I – V and fast I – V measurement methods, (b) $I_d - V_d$ curves of *n*-FeFET. The NDR is shown at forward sweep. (c) Program (PGM) and Erase (ERS) waveforms to observe ferroelectric characteristics, and $I_d - V_g$ curve of HZO-FeFET with $L_g = 65\mu$m and 10μm, respectively ($V_d = 100$mV).

To implement the memory device, the FeFET should have memory characteristics such as difference in V_{th} according

to Program/Erase (PGM/ERS) state switching. Fast I–V measurements and a pulse generator were used to evaluate the memory characteristics of the ferroelectric device. A PGM/ERS pulse was applied to the gate, and the change in V_{th} was measured. Before applying the PGM and ERS pulse to the gate, a reset pulse was given to initialize the ferroelectric state for accurate measurements, and then a PGM pulse of 8 V was applied for 1 μs. Moreover, an ERS pulse of −6 V was applied for 1 μs for the ERS state (Fig. 8(b)). In the PGM state, V_{th} shifts in the negative direction; in the ERS state, the ferroelectric operation can be confirmed through a positive shift in V_{th}. The current level did not change with the PGM/ERS state, and only the difference in the dimensions affected the drain current level.

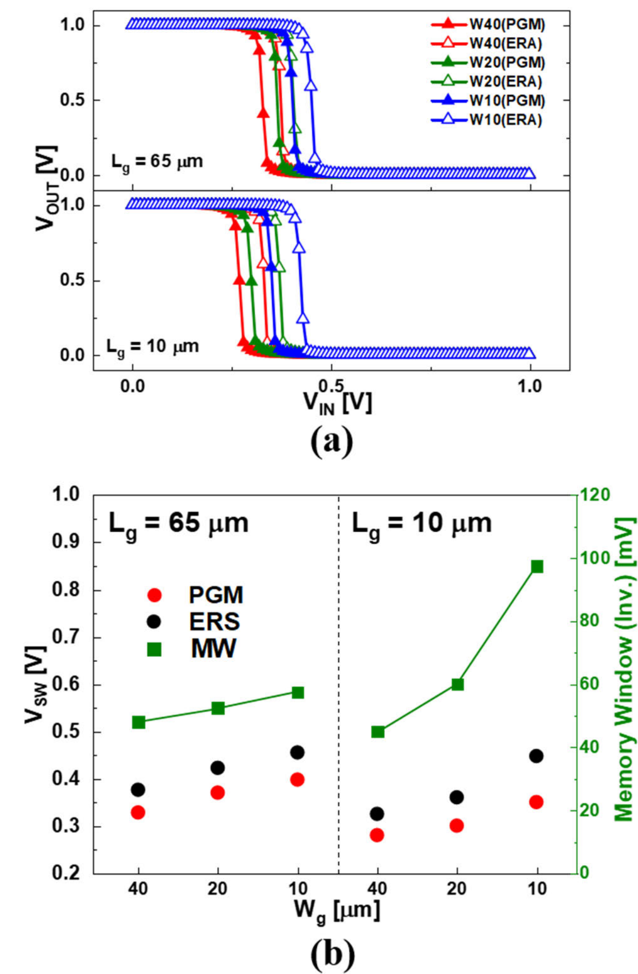


FIGURE 9. (a) Voltage transfer characteristics (VTC) of the inverter (pMOSFET +nFeFET) with various W_g/L_g (V_{dd} = 1 V), (b) Switching threshold voltage (V_{SW}) and memory window (MW = $V_{SW,ERS} - V_{SW,PGM}$) of the inverter with respect to the nFeFET dimensions.

As a result of the co-integration, we developed a novel inverter composed of both FeFET and MOSFET, called FeFET inverter. Fig. 9(a) shows the voltage transfer characteristics (VTC) of the FeFET inverter manufactured using our co-integration method. The switching threshold voltage (V_{SW}), which is the value of V_{IN} at which V_{OUT} is converted from one to zero, can be adjusted by changing the PGM/ERS state of the FeFET. Curves of the same color are measured from the same inverter and show different V_{SW} determined by the "program" and "erase" states of the FeFET. Fig. 9(b) shows V_{SW} with respect to the PGM/ERS state and memory window (MW) of the inverter, which is the difference in V_{SW} between the PGM and ERS states. In an FeFET inverter composed of FeFETs with the same length, the smaller the width, the greater the V_{SW} value, regardless of the PGM/ERS state. In addition, for the same width, the longer the length, the higher the V_{SW} value. V_{SW} exhibited a trend similar to that of V_{th} of the nFeFET within the inverter, depending on the nFeFET dimensions. With the decrease in the gate width of the nFeFET, the MW increased. The MW of the FeFET inverter, including the shortest nFeFET with both the width and length being 10 μm, was the highest at 97.5 mV, which is sufficient to operate a memory system with nonvolatile characteristics.

IV. CONCLUSION

In this study, we achieved a FEOL monolithic co-integration of FeFET and CMOS devices by introducing LSA. Two key processes are the etch-back to expose the Si substrate and enable the FEOL co-integration, and LSA to ensure low process temperatures for stable monolithic integration. The etch-back process removed the 700 nm-thick ILD nearly vertically, resulting in a narrow dead zone less than 1 μm between the CMOS and FeFET region. In addition, this process also successfully secured the active area for FeFET fabrication. In a test on non-patterned wafer, LSA achieved a lower sheet resistance than conventional RTA at a 55% of maximum laser power (22 W), indicating effective S/D activation. To introduce LSA into the process integration, we optimized the LSA conditions to 35% of maximum power (14 W) and a scan speed of 100 mm/s on a patterned wafer. Following the FeFET fabrication, electrical measurements confirmed that the characteristics of previously manufactured CMOS device remained unchanged before and after the LSA process. In addition, the FeFET demonstrated memory characteristics based on the V_{th} shift depending on the PGM/ERS state, and the FeFET inverter exhibited a MW of 97.5 mV at maximum in VTC, which is sufficient to operate a memory system. Ultimately, this work provides an opportunity for integration of other new devices, in addition to FeFETs, with CMOS by developing the monolithic co-integration scheme. It can be an innovative solution to current challenges and enables further progress in semiconductor technology.

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BOHYEON KANG (Member, IEEE) received the B.S. degree in electrical engineering from Pusan National University, Republic of Korea, in 2019, and the M.S. degree in electrical engineering from Pohang University of Science and Technology (POSTECH), Republic of Korea, in 2021, where he is currently pursuing the Ph.D. degree in electrical engineering.

His research interests include developing monolithic co-integration of CMOS with novel devices using laser annealing and characterization of gate stack for reliability and new device with new materials (ultra-high k and ferroelectric) beyond CMOS.

JEHYUN AN (Member, IEEE) received the B.S. degree in electrical engineering from Pohang University of Science and Technology (POSTECH), Republic of Korea, in 2019, where he is currently pursuing the integrated M.S. and Ph.D. degree in electrical engineering.

His research interests include the reliability of cryogenic memory (DRAM core cell and Peri) and characterization of gate stack for reliability and developing new device with new materials (ferromagnetic) and structures beyond CMOS.

JONGSEO PARK (Member, IEEE) received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, Republic of Korea, in 2021, and the M.S. degree in electrical engineering from Pohang University of Science and Technology (POSTECH), Pohang, Republic of Korea, in 2023, where he is currently pursuing the Ph.D. degree in electrical engineering.

His research interests include characterization of gate stack for reliability and developing new device with new materials (ultra-high k, ferroelectric, and ferromagnetic) and structures beyond CMOS.

GIRYUN HONG (Member, IEEE) received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, Republic of Korea, in 2023. He is currently pursuing the M.S. degree in electrical engineering with Pohang University of Science and Technology (POSTECH).

His research interests include optimization of new device structures through the deposition of novel materials (ultra-high k and ferromagnetic) and improvement of material contact characteristics.

BEOMJOO HAM (Member, IEEE) received the B.S. degree in electrical engineering from Pohang University of Science and Technology (POSTECH), Pohang, Republic of Korea, in 2023, where he is currently pursuing the M.S. degree in electrical engineering.

His research interests include characterization of gate stack for reliability and developing new device with new materials (ultra-high k and ferroelectric) and structures beyond CMOS.

JAESEONG PYO received the B.S. degree in electrical engineering from Pusan National University, Pusan, Republic of Korea, in 2024. He is currently pursuing the M.S. degree in electrical engineering with Pohang University of Science and Technology (POSTECH).

His research interests include optimization of new device structures through ALD with new materials (ultra-high k and ferroelectric).

SUNG-MIN AHN (Member, IEEE) received the B.S. and M.S. degrees in physics from Korea University, in 1998 and 2000, respectively, and the Ph.D. degree in physics from Seoul National University, Seoul, Republic of Korea, in 2010. He was a Senior Research Engineer with the Imaging Solution, System LSI Division, Samsung Electronics, Yongin, Republic of Korea, from 2005 to 2008. As a Postdoctoral Scientist, from 2010 to 2013, he worked on spintronic materials of nanowire with Institut d'Electronique Fondamentale (IEF), Université Paris Sud, France, from 2010 to 2011, and developing low-energy magnetic logic with the Department of Materials Science and Engineering, Massachusetts Institute of Technology (MIT), USA, from 2012 to 2014. He was a Principal Engineer (Advanced TD) with the Semiconductor Research and Development Center, Samsung Electronics, Hwaseong, Republic of Korea, from 2014 to 2019, a Senior Process Engineer (New Technology Leader) with Applied Materials, Sunnyvale, CA, USA, and a Technical Manager with Nova Ltd., from 2019 to 2021. He is currently with Pohang University of Science and Technology (POSTECH), Pohang, Republic of Korea, with a focus on electrical engineering. Over 20 years, his work has mainly covered from material synthesis to characterization, optimization for emerging devices-based STT/SOT-MRAM, racetrack memory, PC-RAM, FeRAM, and their hybrid applications (co-integration).

ROCK-HYUN BAEK (Member, IEEE) received the B.S. degree in electrical engineering from Korea University, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from Pohang University of Science and Technology (POSTECH), Pohang, Republic of Korea, in 2006 and 2011, respectively. From 2011 to 2015, he was a Postdoctoral Researcher and a Technical Engineer with SEMAT-ECH, Albany, NY, USA. From 2011 to 2017, he was an Assistant Professor of electrical engineering with POSTECH, where he is currently an Associate Professor. From 2015 to 2017, he was a Senior Device Engineer with the Samsung Research and Development Center (Pathfinding TEAM), Republic of Korea. His research interests include advanced logic devices (fin, gate-all-around, nanosheet FETs, and vertical FET), materials (Si, SiGe, and Ge), memory (3D-NAND and DRAM peri), 3DIC (TSV and M3D), and unit circuit characterization based on electrical measurement, TCAD, and machine learning technique.