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RESEARCH ARTICLE

# A 42.7Gb/s Optical Receiver With Digital Clock and Data Recovery in 28nm CMOS

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**ABSTRACT** This paper presents a broadband optical receiver that employs multiple bandwidth extension techniques in analog front-end (AFE) and has efficient digital clock and data recovery (CDR). The AFE is implemented exclusively with inverter-based stages. It consists of a shunt feedback transimpedance amplifier followed by a continuous time linear equalizer (CTLE) and variable gain amplifier (VGA). High $R_F$ value, 400Ω, was employed to have better sensitivity at the cost of narrow bandwidth. Total AFE bandwidth is extended by 5.5X with CTLE peaking, series inductances between each AFE stage, and active inductor loads in the CTLE output and VGA stages. Quarter-rate, phase-locked loop (PLL) based digital CDR is implemented for clocking. The resolution of a digitally controlled oscillator (DCO) is optimized at 9-bit to balance jitter and hardware cost from the CDR. Multi-phase clock generation is accomplished by a delay locked loop (DLL). Fabricated in 28nm CMOS, the 42.7Gb/s optical receiver achieves an optical modulation amplitude (OMA) sensitivity of −3.6dBm at a bit error rate (BER)$<10^{-12}$, 10MHz CDR bandwidth, and 3.4pJ/bit energy efficiency.

**INDEX TERMS** Bandwidth extension techniques, broadband AFE, DCO resolution, digital CDR phase noise modeling, optical receiver.

## I. INTRODUCTION

Soaring amount of data use from artificial intelligence (AI), 5G network, Internet of Things (IoT), and mobility growth accelerates ultrahigh speed data transmission in data centers [1]. Electrical link systems which have been predominantly used in the past decades are now facing challenges to support data centers with lower-cost and energy-efficient solutions [2]. As more channel loss occurs at higher data rates in electrical backplane system, it requires many equalization techniques which consume area and power to compensate intersymbol interference (ISI) and dispersion. Data centers require new medium which can support rapid increase on bandwidth. Nowadays, optical link systems are employed in most of data centers since it can support high data rates with low power. A general block diagram of an optical transceiver is shown in Fig. 1. Optical transmitter converts serialized electrical data into an optical domain, which transfers through an optical fiber. Optical receiver, then, converts high-speed optical signal to an electrical domain with a photodiode (PD). This is followed by transimpedance amplifier (TIA) and voltage amplifier such that the data can have a sufficient signal in order for a comparator to detect the bit stream correctly. Over past decades, numerous researches have been done to optimize front-end performance [3], [4], [5], [6], [7]. Moreover, advanced CMOS technology such as FinFET, as well as bandwidth extension techniques, helps push the date-rate furthermore [8], [9], [10]. However, due to unavoidable trade-offs between gain, bandwidth and noise, challenges still exist

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in designing analog front-end (AFE). This paper introduces high bandwidth AFE with multiple bandwidth extension techniques.

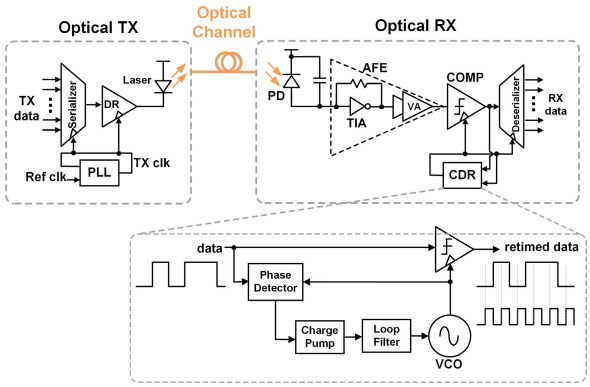


**FIGURE 1.** General optical transceiver.

Another receiver challenge involves designing a clocking system. Pin count is a critical factor in link system implementation due to packaging costs. Since clock and data recovery (CDR) does not require reference input clock signal, it can be a cost-efficient solution for a clocking system. However, conventional analog CDR shown in Fig. 1 confronts many challenges. First, due to an analog loop filter, CDR is not able to take full advantage of scaled technologies. Second, analog components are susceptible to process, voltage, and temperature (PVT) variations. Also, they are not area-efficient. Digital CDR has gained more attention since it can overcome those aforementioned challenges encountered by conventional CDR. Digital synthesis in submicron CMOS technology allows loop filter to be implemented digitally. In addition to resolving the issues mentioned above, a digital loop filter (DLF) provides programmability for loop dynamics with a simple digital bit configuration. However, due to digital implementation, quantization noise is unavoidably added to the clock jitter. Detailed phase noise analysis of the proposed digital CDR is addressed later in this paper.

In our previous work [11], we presented a 42.7Gb/s optical receiver that employs broadband AFE and digital CDR. This article is an extension of previous work, which is organized as follows: Section II provides a brief overview of the proposed receiver architecture. Design considerations and circuit implementations of AFE for wideband applications are described in Section III. Section IV focuses on digital CDR illustrating phase noise modeling, and multi-phase clock generation. Receiver measurement results from a 28nm CMOS prototype are presented in Section V. Finally, Section VI concludes this paper.

## II. RECEIVER ARCHITECTURE

Fig. 2 shows top-level block diagram of the proposed optical receiver, which consists of AFE, and CDR. The AFE block is composed of TIA, continuous time linear equalizer (CTLE), and variable gain amplifier (VGA). A shunt feedback TIA (SF TIA), consisting of a simple inverter with a feedback resistor ($R_F$), converts PD current to a voltage signal. The average photo-current is subtracted from DC offset cancellation (DCOC) with pull down NMOS transistor forming a feedback loop. The SF TIA is followed by CTLE, which provides bandwidth extension, enabling high transimpedance gain with reducd noise. CTLE has a digital tunability which helps to compensate PVT variations. VGA provides additional amplification for sampler banks to determine the correct bits. Series passive peaking employed between each AFE stage and active inductor loads at CTLE output and in each VGA stage are employed to extend AFE bandwidth. AFE output is sampled by data and edge slicer banks that consist of double-tail sense amplifier followed by SR latch [12] to provide the signal and phase information for CDR. After being demultiplexed from quarter-rate to 1/16$^{th}$ rate, each data pattern is buffered out and fed to a bit error rate tester (BERT). More details on circuit analysis and implementation of AFE are discussed further in Section III.

A quarter-rate, digital CDR consists of slicer banks (four data samplers, four edge samplers), demultiplexers, bang-bang phase detector (BBPD), DLF, LC-DCO, and delay locked loop (DLL). Quarter-rate architecture implemented in this prototype relaxes the VCO clock frequency, and demultiplexing early and late signal from BBPD eases the clock speed of DLF. CDR locking is done by detecting the phase difference between incoming data signal and oscillator clock signal from BBPD and using a feedback loop to adjust the phase of the oscillator. Loop filter, which is entirely synthesized, compares early and late signals and provides 9-bit digital output to control DCO. DCO generates differential clock signals, and DLL provides 8-phase clock signals for quarter-rate CDR logic operation. More details on phase noise estimation, optimum DCO resolution bit selection, and circuit implementations are presented in Section IV.

## III. ANALOG FRONT-END

A detailed AFE block diagram is shown in Fig. 3, which is implemented exclusively with inverter-based amplifier stages that offer high $g_m$ utilization and allow for an overall simple architecture. The AFE is powered with an external 1V supply. At this power supply voltage level, the inverter-based input TIA provides higher gain relative to regulated cascode (RGC) TIA designs [4]. The inverter-based CTLE that follows offers better area efficiency over CML-based topologies. While not implemented in this prototype, improved PVT robustness is also possible with adaptive supply regulation [13]. Low-complexity bandwidth extension with active inductor loads, utilized at the CTLE output and in each VGA stage, is realized by shorting the inverter stages input and output and adding series gate resistors. Stable operation is ensured with the global DC offset cancellation and local VGA common-mode feedback loops, with simulations showing close to 80° phase margins.

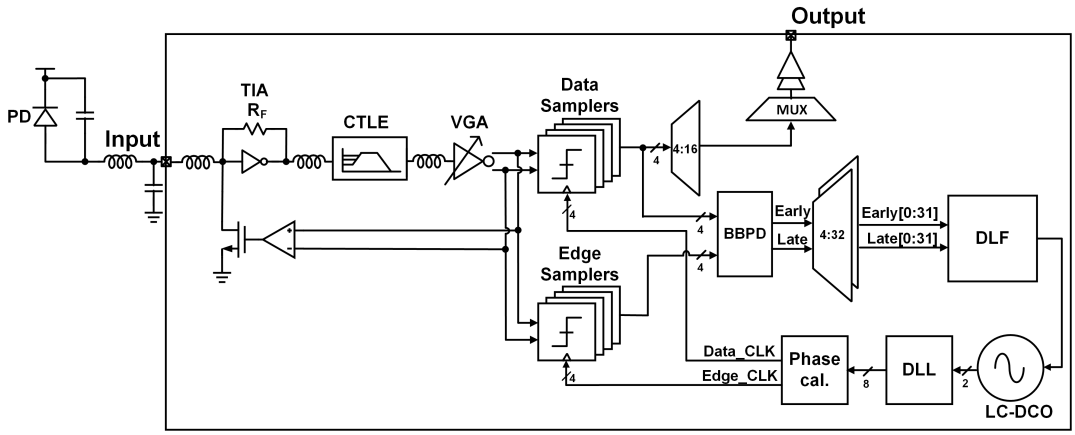


**FIGURE 2.** Proposed optical receiver architecture.

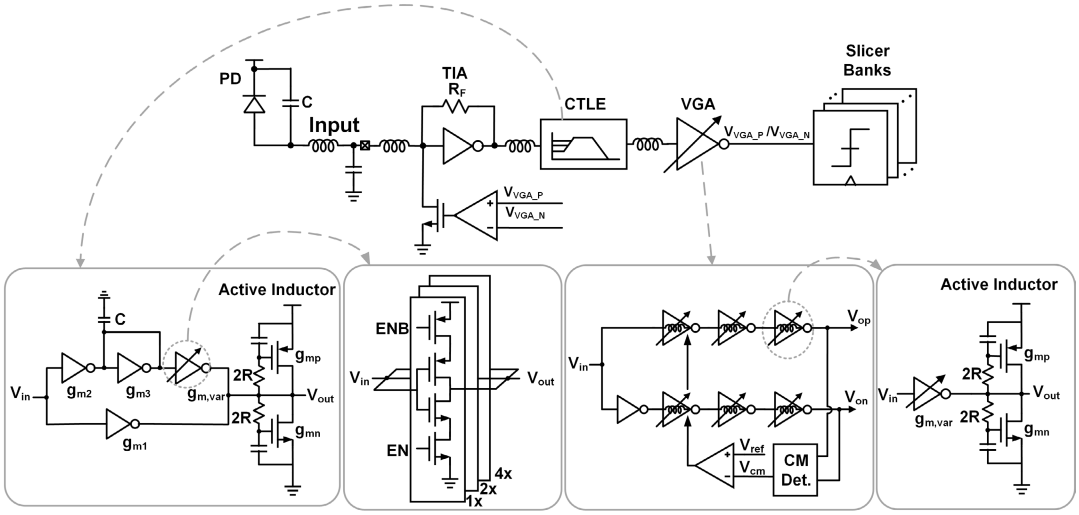


**FIGURE 3.** Analog front-end.

### A. TRANSIMPEDANCE AMPLIFIER (TIA)

Theoretically, a simple resistor connected to the ground can be used as TIA. However, a direct trade-off between transimpedance gain, bandwidth, and noise performance limits its availability. To improve gain-bandwidth (GBW) product, topologies with active components have been employed: RGC TIA [4], and inverter-based SF TIA. Better SNR performance of SF TIA over RGC TIA [10] makes it attractive to our design. A schematic of SF TIA, its small signal, and a noise model is shown in Fig. 4. $C_{in}$ denotes the total capacitance seen at an input node of TIA, $C_F = C_{GD}$, $C_L$ represents total sum of capacitance at output node of TIA, and $R_{out}$ states TIA output resistance. The transimpedance of SF TIA can be represented by

$$Z_T(s) = \frac{(R_F C_F s + 1 - g_m R_F) R_{out}}{\alpha s^2 + \beta s + \gamma}, \tag{1}$$

where $\alpha = (R_F R_{out})(C_F C_L + C_L C_{in} + C_{in} C_F)$, $\beta = [R_F(1+g_m R_{out})C_F + R_{out} C_L + (R_F + R_{out})C_{in}]$, and $\gamma = 1 + g_m R_{out}$. The second-order system can be characterized by two parameters: natural frequency ($\omega_n$) and damping factor ($\zeta$)

$$\omega_n^2 = \frac{1 + A}{R_F R_{out}(C_F C_L + C_L C_{in} + C_{in} C_F)} \tag{2}$$

$$\zeta = \frac{1}{2} \frac{R_F(1+A)C_F + R_{out} C_L + (R_F + R_{out})C_{in}}{\sqrt{R_F R_{out}(1+A)(C_F C_L + C_L C_{in} + C_{in} C_F)}}, \tag{3}$$

where $A = g_m R_{out}$. Assuming a Butterworth response for maximally flat frequency response, TIA bandwidth ($\omega_{3dB}$) becomes [14]

$$\omega_{3dB} = \omega_n = \sqrt{\frac{g_m}{R_F(C_F C_L + C_L C_{in} + C_{in} C_F)}}. \tag{4}$$

Not only the frequency response of transimpedance but also the analysis on noise sources matters in AFE design. Input referred noise model is widely used to find the TIA specifications that provide optimum signal-to-noise-ratio (SNR). Noise from TIA occupies most of the noise profile in AFE since noises from the following stages are suppressed by transimpedance gain. The feedback resistor and amplifier noise components determine the input-referred noise current

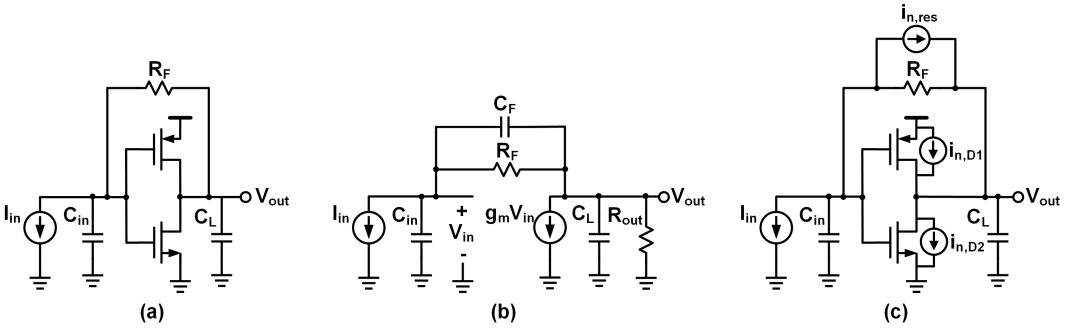


**FIGURE 4.** Inverter-based TIA: (a) circuit diagram, (b) small signal model, and (c) noise model.

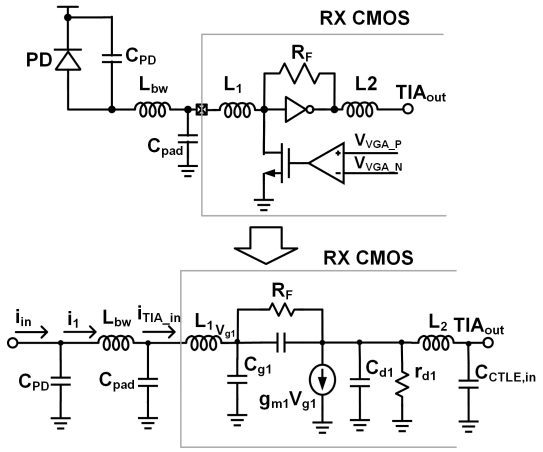


**FIGURE 5.** TIA circuit with input network.

spectrum, which can be expressed in [15]

$$\overline{I_n^2}(f) = \overline{I_{n,res}^2}(f) + \overline{I_{n,amp}^2}(f) = \frac{4kT}{R_F} + \frac{4kT\gamma}{g_m R_F^2} + \frac{4kT\gamma(2\pi C_T)^2}{g_m} \times f^2, \quad (5)$$

where $g_m$ is the transconductance of an inverter in TIA, $k$ is the Boltzmann constant, $T$ is the absolute temperature, and $\gamma$ is the MOSFET thermal noise factor.

More importantly, there is a condition where $R_F$ cannot be above by [16]

$$R_F \leq \frac{A\omega_A}{C_{in}\omega_{3dB}^2}, \quad (6)$$

where $\omega_A$ is 3dB bandwidth of amplifier. Equation (6) explains that $R_F$ has an inverse-quadratic relationship with 3dB bandwidth of TIA. Once input sensitivity is decided from (5), TIA bandwidth and $R_F$ value would be determined. In addition to numerical analysis mentioned above, design iterations with post-simulation are required to accommodate the parasitics from layout.

Although aforementioned analysis includes all parasitics in TIA, an overall frequency response will be different if TIA is connected to PD with bond wire. Fig. 5 shows SF TIA with optical to electrical interface. For bond wire applications, it is inevitable to have a parasitic inductance interfacing photodiode to CMOS chip. In this prototype, it is estimated to have 300pH. By considering optical to electrical interface, TIA transfer function can be acquired with the product of two groups: one with the transfer function from PD current to input to the TIA ($H_0$), and the other from TIA input current to TIA output voltage ($Z_{TIA}$). The transfer function of SF TIA including the input network is given by (7) and (8), as shown at the bottom of the next page, which is based on previous TIA analysis [17]. By including the interface between PD and TIA, the proposed TIA transfer function adds an additional pole that reflects more of a practical case. $R_F$ value has to be considered such that the proposed receiver can support high data rates. After iterative post-layout simulations considering the trade-offs, 400Ω was employed as $R_F$ value to support over 40Gb/s data rate. High $R_F$ allows better sensitivity at the cost of narrow bandwidth. By simulation, TIA offers 7GHz of bandwidth which is roughly 1/5$^{th}$ of the total BW, and the input-referred rms noise current is estimated to be $3\mu A_{rms}$. Narrow bandwidth of TIA itself can be extended by the following multiple bandwidth extension techniques.

### B. CTLE

The first bandwidth extension technique applied in AFE is utilizing an adjustable CTLE peaking technique. The equalization strengths can be adjusted by tuning the transconductance of one of two different paths, which is illustrated in Fig. 3. CTLE provides peaking by subtracting the low-frequency signal component by utilizing a top-path low-pass filter [18], and adjustable 7dB low-frequency gain allows to compensate for PVT variations. The transfer function of CTLE is given by

$$\frac{v_{out}}{v_{in}}(s) = -(g_{m1} - g_{m,var}\frac{g_{m2}/g_{m3}}{1+sC/g_{m3}})Z_L$$
$$Z_L = \frac{1}{G_m}\frac{1+sRC_{gs}}{1+sCgs/G_m} = \frac{1}{G_m}\frac{1+s/\omega_z}{1+s/\omega_T}, \quad (9)$$

where $G_m = g_{mp} + g_{mn}$, $C_{gs}$ is total inverter gate capacitance, and $\omega_T$ is the transit frequency of an inverter. As explained in (9), de-emphasis level can be adjusted with $g_{m,var}$. For frequency range $\omega \ll \omega_T$, this impedance can be

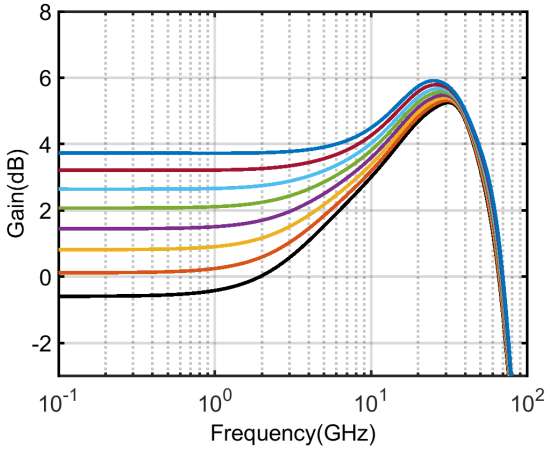


**FIGURE 6.** Simulated CTLE frequency response.

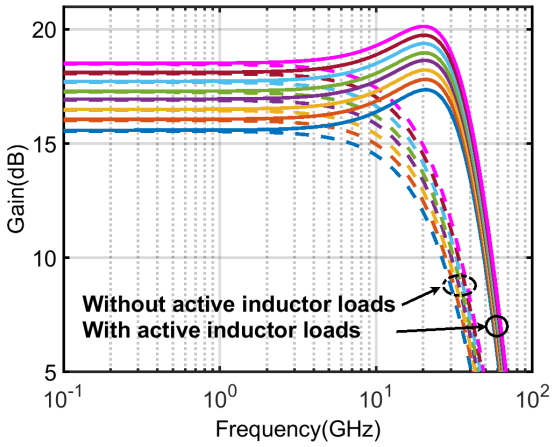


**FIGURE 7.** Simulated VGA frequency response.

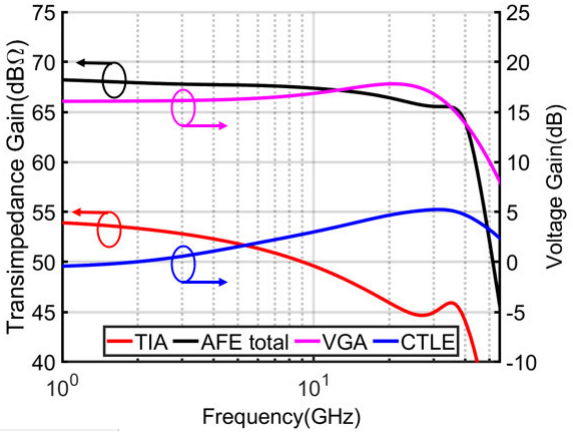


**FIGURE 8.** Simulated overall AFE frequency response.

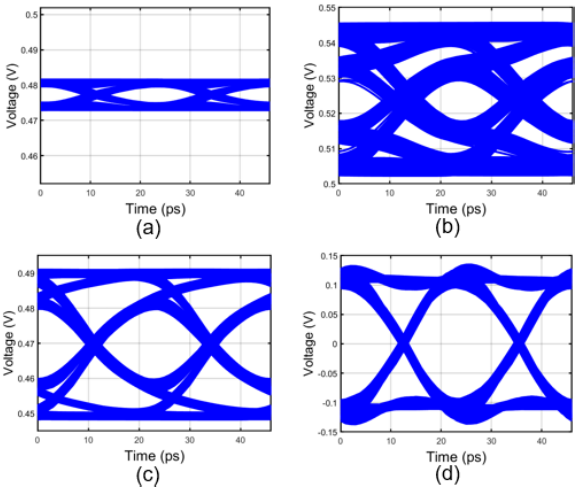


**FIGURE 9.** Post-extracted simulated 42.7 Gb/s eye diagrams at the output of (a) PD, (b) TIA, (c) CTLE, and (d) VGA.

approximated to

$$Z_L \approx \frac{1}{G_m}(1 + s/\omega_z) = \frac{1}{G_m} + s\frac{R}{\omega_T}. \tag{10}$$

### C. VGA

The VGA block, shown in Fig. 3, is configured with cascaded inverter-based amplifier stages. Each amplifier stage has an active inductor load that is the same as the one in the CTLE output stage. A common-mode feedback loop assists to place the bias point in the middle of the output swing and equalize the gain of the positive and negative signal paths. The transfer function of a VGA block is

$$\frac{v_{out}}{v_{in}}(s) \approx -2 \times (g_{m,var}Z_L)^3. \tag{11}$$

Fig. 7 represents the frequency response of VGA block. It shows that VGA provides not only the gain that is tunable with 8 settings, but also the peaking which helps bandwidth extension.

The overall frequency response is plotted in Fig. 8. Although TIA itself has a high $R_F$ value advantageous for noise reduction at the cost of narrow bandwidth, the following

$$H_0(s) = \frac{i_{TIA,in}(s)}{i_{in}(s)} = \frac{i_1(s)}{i_{in}(s)}\frac{i_{TIA,in}(s)}{i_1(s)} = \frac{1}{1 + sC_{PD}(sL_{bw} + Z_0)}\frac{1 + sC_{g1}R_I}{1 + s(C_{g1} + C_{PD})R_I + s^2L_1C_{PD} + s^3L_1C_{PD}C_{g1}R_I} \tag{7}$$

$$Z_{TIA}(s) = \frac{v_{TIA,out}(s)}{i_1(s)} = -Z_fZ_{l,1}\frac{g_{m1} - 1/Z_f}{g_{m1}Z_{l,1} + 1}\frac{1}{1 + s\frac{C_{g1}(Z_{l,1}+Z_f)+C_{d1}Z_{l,1}}{1+g_{m1}Z_{l,1}} + s^2C_{g1}C_{d1}\frac{Z_{l,1}(Z_{l,1}+Z_f)}{1+g_{m1}Z_{l,1}}}\frac{1}{sC_{g2}Z_{s,1}} \tag{8}$$

$$\textit{where}\quad Z_O = \frac{1}{sC_{pad}}||(sL_1 + Z_{o1}), Z_{o1} = \frac{Z_{l,0} + Z_f}{1 + g_{m1}Z_{l,0} + sC_{g1}(Z_{l,0} + Z_f)}, Z_{l,0} = 1/(sC_{d1})||r_{d1}, Z_f = R_F||[1/(sC_{gd1}),$$

$$R_I = \frac{R_F}{g_{m1}r_{d1} + 1}, Z_{l,1} = 1/(sC_{d1})||r_{d1}||Z_{s,1}, Z_{s,1} = sL_2 + 1/(sC_{CTLE,in}),$$

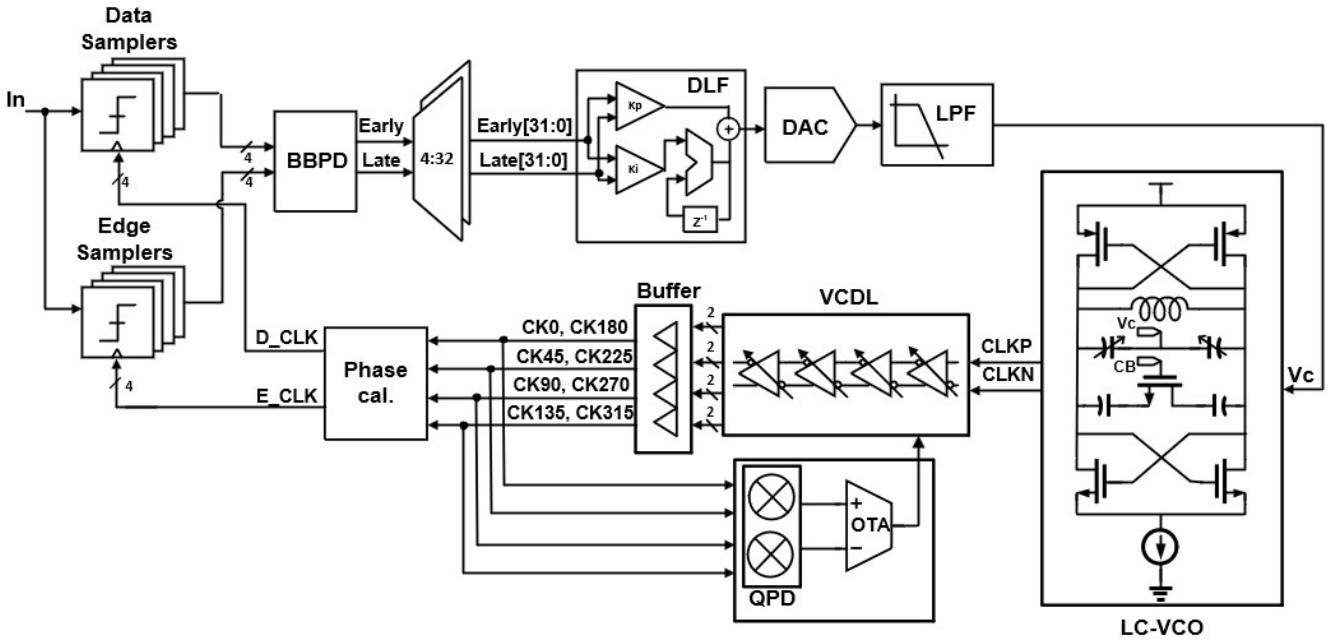


**FIGURE 10.** Digital CDR block diagram.

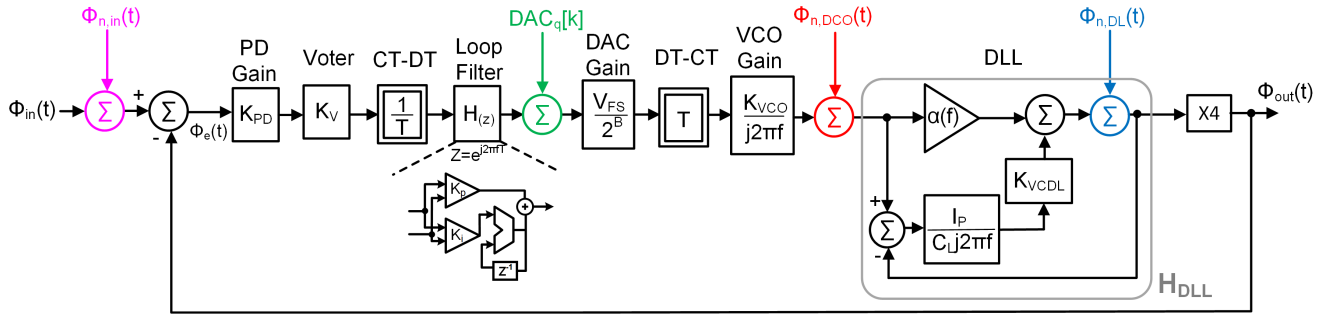


**FIGURE 11.** Linearized quarter-rate CDR phase noise model.

stages help to increase the bandwidth. CTLE provides a 5dB peaking at 30GHz by subtracting a low-frequency signal with active inductor load, and VGA offers 2dB peaking with active inductor loads. Series passive inductors also assist bandwidth extension by a factor of 2X. Overall, the proposed AFE provides 38.7GHz bandwidth with 67.5dBΩ transimpedance gain. Fig. 9 shows the resulting 42.7 Gb/s eye diagrams at the output of PD, TIA, CTLE, and, VGA. In this design, TIA bandwidth is limited to 7GHz to achieve $3\mu A_{rms}$ input-referred noise. 0.35UI of ISI-induced jitter was measured at TIA output. However, this pattern-dependent jitter has been reduced to 0.12UI and 0.08UI at the output of CTLE and VGA, respectively thanks to bandwidth extension techniques applied in this design.

## IV. DIGITAL CDR

The detailed block diagram of digital CDR is shown in Fig. 10. DLF controls the loop dynamics of CDR by providing gains ($K_i$, $K_p$) for integral and proportional paths independently. DAC is employed as a sub-circuit of LC-DCO to convert the digital output of the loop filter into an analog voltage. Tunable RC low-pass filter followed by LC-VCO filters out voltage noise generated by the DAC. In order to support high data rates with low jitter, an LC-VCO is chosen due to its lower phase noise relative to a ring-based VCO. LC-VCO additionally features a cap bank for wide-range operation. DLL generates eight-phase clock signals from a delay line. It achieves equal spacing by adjusting the load capacitance of the delay cell in a negative feedback manner. We begin by analyzing the phase noise in the CDR and presenting the loop dynamics along with the associated parameters. Finally, we address the circuit implementation of the DLL in this section.

### A. CDR PHASE NOISE

Digital implementation of loop filter causes quantization noise which adds jitter to clock signal. There exists an optimum point where the total jitter is minimized in terms of hardware cost, DAC resolution. Phase noise modeling is reported here to investigate the optimum. The phase noise

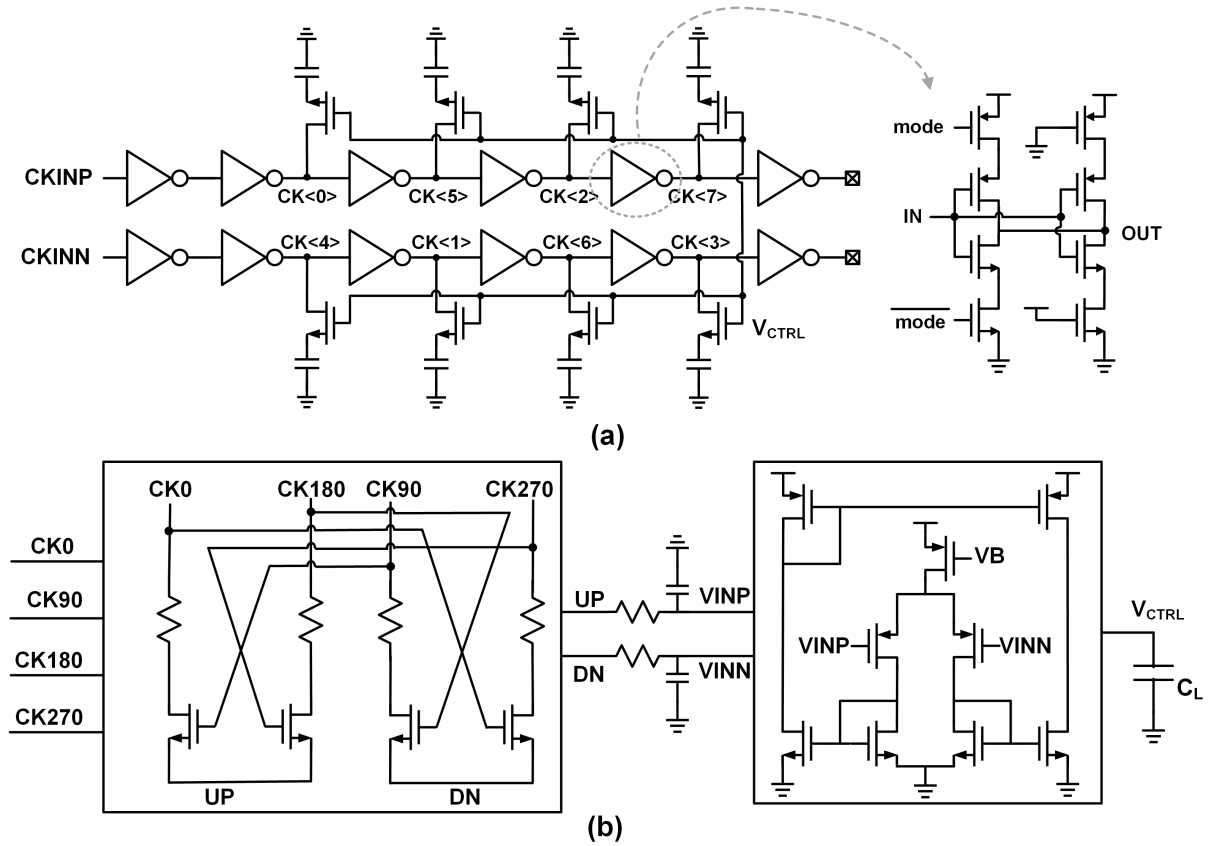


**FIGURE 12.** DLL schematics: (a) VCDL, (b) QPD, and OTA.

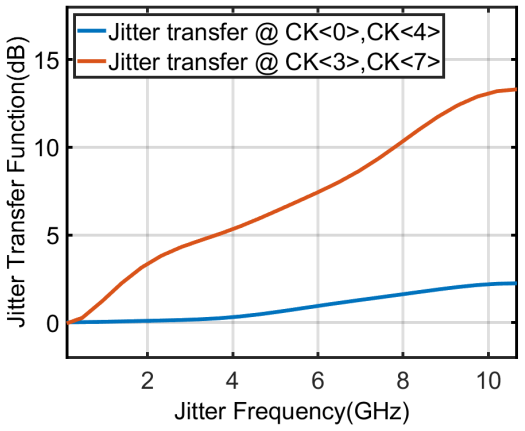


**FIGURE 13.** Simulated delay line jitter transfer response.

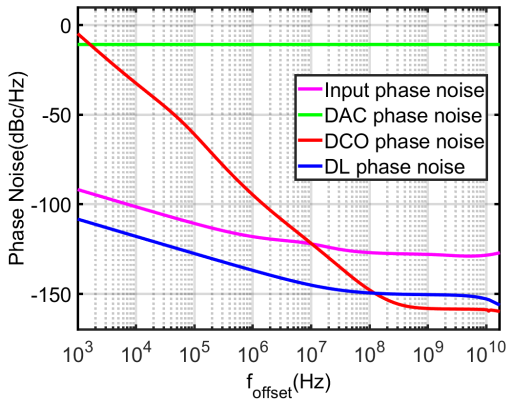


**FIGURE 14.** Simulated phase noise profiles.

model for the proposed digital CDR is depicted in Fig. 11. Four major noise sources are included in the modeling: Input noise, DAC quantization noise (DAC QN), DCO random noise (DCO RN), and delay line random noise (DL RN). DCO is modeled as DAC followed by VCO and converting from discrete to continuous domain requires a scaling factor of T, where T denotes reference period. Also, scaling factor 1/T is required to convert early and late signals from BBPD into a discrete form such that DLF can process. A simple majority voter is included and the X4 term following DLL block indicates that the proposed CDR is a quarter-rate system.

DLL has all-pass nature in terms of jitter transfer [19]. However, when it comes to high-speed clocking, we need to consider the jitter amplification factor ($\alpha$) in delay line that has a bandwidth-limited characteristic. Thus, in terms of jitter transfer response, delay line inludes a high-pass filter feature which amplifies high-frequency component [20]. Simulation was done to examine the jitter amplification factor in the proposed clocking system. Delay line in DLL consists of a chain of inverter cells with tunable load capacitance as

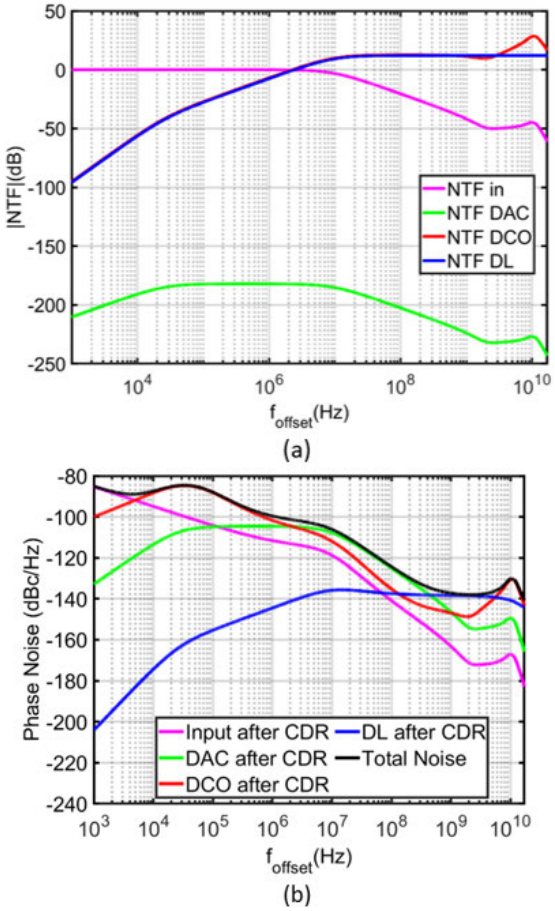


**FIGURE 15.** Phase noise simulation: (a) noise transfer functions and (b) overall phase noise.

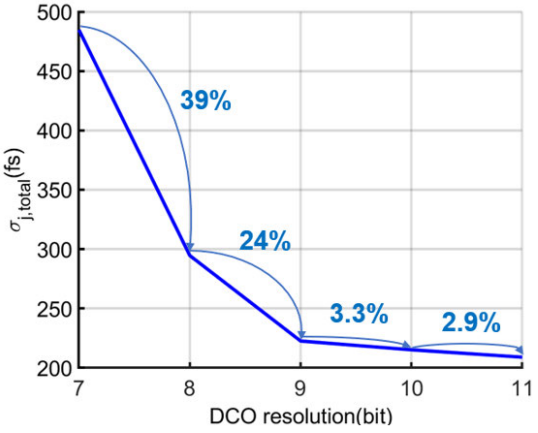


**FIGURE 16.** Simulated jitter ($\sigma_{rms}$) as a function of DCO resolution.

**TABLE 1.** CDR parameters.

| Param. | Value | Unit |
|---|---|---|
| $K_{PD}$ | 1.9 | per UI |
| $K_V$ | $\frac{1}{8}$ | - |
| $K_i$ | $\frac{1}{2^{10}}$ | - |
| $K_p$ | 2 | - |
| $K_{DAC}$ | $\frac{0.6}{2^9}$ | $\frac{V}{code}$ |
| $K_{VCO}$ | $10^9$ | $\frac{Hz}{V}$ |

illustrated in Fig. 12 (a). An impulsive jitter is provided by input clock source, which results in jitter in subsequent edges on the clock network. Jitter transfer function can be acquired by taking Fourier Transform of the jitter impulse response assuming the response is linear. Simulation result, as shown in Fig. 13, indicates minimal amplification at low jitter frequencies, with amplification increasing as the frequency rises. Also, it is confirmed that the magnitude of jitter amplifies as the signal passes through more stages. Considering jitter amplification, the following steps explain how the individual noise sources affect jitter performance. The open loop gain (LG) of the system in Fig. 10 can be represented by

$$LG(f) = 4(K_{PD})(K_V)H(e^{j2\pi fT})(\frac{V_{FS}}{2^B})(\frac{K_{VCO}}{j2\pi f})H_{DLL}(f). \tag{12}$$

The DLL transfer function ($H_{\mathrm{DLL}}(f)$) is

$$H_{DLL}(f) = \frac{\alpha(f) + (\frac{I_P}{j2\pi fC_L})(K_{VCDL})}{1 + (\frac{I_P}{j2\pi fC_L})(K_{VCDL})}. \tag{13}$$

DAC exhibits quantization noise with a uniform power spectral density of 1/12, while random noise such as thermal or flicker noise from the DCO follows Leeson's phase noise model with −121.8 dBc/Hz at 10 MHz frequency offset. Including the phase noise of the analog front-end and delay line, Fig. 14 illustrates four major phase noise sources. After deriving individual noise transfer functions by using Mason's rule, the output phase noises contributed from each noise source have been acquired, and the total phase noise can be obtained by summing up all the noise components.

$$NTF_{in}(f) = \frac{\phi_{out}}{\phi_{n,in}} = \frac{LG(f)}{1 + LG(f)} \tag{14}$$

$$NTF_{DAC}(f) = \frac{\phi_{out}}{q_{DAC}} = \frac{4(\frac{V_{FS}}{2^B})T(\frac{K_{VCO}}{j2\pi f})H_{DLL}(f)}{1 + LG(f)} \tag{15}$$

$$NTF_{DCO}(f) = \frac{\phi_{out}}{\phi_{n,DCO}} = \frac{4H_{DLL}(f)}{1 + LG(f)} \tag{16}$$

$$NTF_{DL}(f) = \frac{\phi_{out}}{\phi_{n,DL}} = \frac{4}{1 + LG(f)} \tag{17}$$

$$S_{\phi_{out}}^{\phi_{n,in}}(f) = S_{\phi_{n,in}}(f)|NFT_{in}(f)|^2 \tag{18}$$

$$S_{\phi_{out}}^{DAC_q}(f) = S_{DACq}(f)(\frac{1}{T})|NFT_{DACq}(f)|^2 \tag{19}$$

$$S_{\phi_{out}}^{\phi_{n,DCO}}(f) = S_{\phi_{n,DCO}}(f)|NFT_{DCO}(f)|^2 \tag{20}$$

$$S_{\phi_{out}}^{\phi_{n,DL}}(f) = S_{\phi n,DL}(f)|NFT_{DL}(f)|^2 \tag{21}$$

$$S_{\phi_{out}}^{Total}(f) = S_{\phi_{out}}^{\phi_{n,in}}(f) + S_{\phi_{out}}^{DAC_q}(f) + S_{\phi_{out}}^{\phi_{n,DCO}}(f) + S_{\phi_{out}}^{\phi_{n,DL}}(f) \tag{22}$$

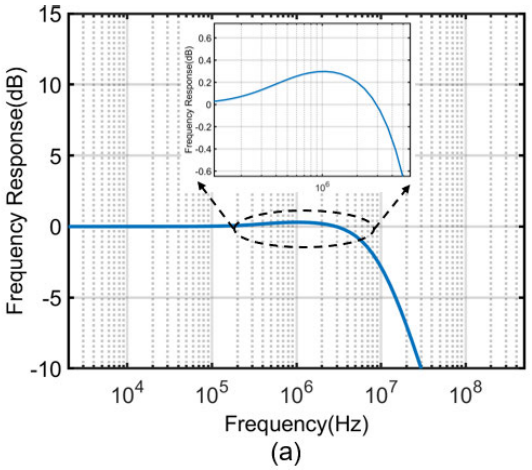


**FIGURE 17.** Simulated jitter transfer function.

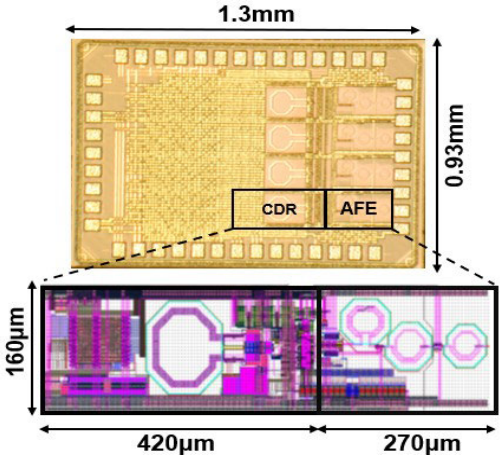


**FIGURE 18.** Chip micrograph with layout details.

Fig. 15 represents individual noise transfer functions and overall phase noise. By integrating up to Nyquist frequency, proposed CDR with 9-bit DCO resolution is estimated to have 231fs of $\sigma_{rms}$ value. Increasing the resolution of the DCO helps reduce DAC quantization noise, albeit at the expense of higher hardware costs, larger DAC layout size. To achieve optimum jitter performance considering the cost, simulation was done by sweeping DCO resolution. Fig. 16 reveals that jitter decreases as DCO resolution increases since DAC QN reduces. 9bit is an optimum since there is a rapid jitter reduction until 9bit. Increasing the resolution furthermore has marginal effect on reducing jitter but increasing layout size. In addition to jitter generation, investigating phase error observed at the PD ($\phi_e$) is also important since it determines the BER performance [21]. The phase noise from the phase error can be acquired by

$$S_{\phi_e}^{Total}(f) = S_{\phi_{n,in}}(f) + S_{\phi_{out}}^{DAC_q}(f) + S_{\phi_{out}}^{\phi_{n,DCO}}(f) + S_{\phi_{out}}^{\phi_{n,DL}}(f). \quad (23)$$

Compared to phase noise from jitter generation in (22), phase noise with regard to phase error considers unfiltered input noise ($S_{\phi_{n,in}}(f)$). Converting phase noise from the phase error to time domain, the proposed receiver is estimated to have 670fs$_{\text{rms}}$ of random jitter.

### B. CDR LOOP DYNAMICS

The digital CDR's open loop gain (LG) in Fig. 10 was described in (12). Since CDR loop dynamic is determined by DLF parameters, it is better to express LG with $K_i$ and $K_p$.

$$LG(z)|_{z=e^{j2\pi fT}} = 4(K_{pd})(K_V)(K_p + \frac{K_i}{1-e^{-j2\pi fT}})(\frac{V_{FS}}{2^B})(\frac{K_{VCO}}{j2\pi f})\alpha(f) \quad (24)$$

By substituting (24) into (12), jitter transfer function (JTF) for the proposed CDR is acquired as shown in Fig.17. JTF presents that CDR has 10MHz bandwidth with 0.3dB jitter peaking. Phase detector gain ($K_{PD}$) can be acquired from simulation by transmitting random data on the proposed CDR and averaging enough early and late information from BBPD. $K_v$ is set to 1/8, which illustrates a majority voting factor. Other CDR parameters used in phase noise modeling and jitter transfer function are summarized in Table 1.

### C. DLL

Multiphase clock signals are generated by DLL. As shown in Fig. 10, DLL consists of voltage controlled delay line (VCDL), quadrature phase detector (QPD), and operational transconductance amplifier (OTA). More information on sub-circuits of DLL is described in Fig. 12. An additional switch enables wide-range operation of 40-60Gb/s. Equal phase spacing of 8 clock signals is acquired from negative feedback of DLL. Since DLL is running inside of CDR loop, DLL loop bandwidth, 153MHz, should be high enough such that it does not interrupt main CDR loop dynamics. DLL bandwidth is represented by

$$\omega_{DLL} = \frac{I_{CP}K_{VCDL}}{2\pi C_L}\omega_{ref}, \quad (25)$$

where $I_{CP}$=350uA, $K_{VCDL}$=14ps/V, $C_L$=330fF, and reference frequency is 10.675GHz.

## V. MEASUREMENT RESULTS

The multi-channel optical receiver prototype was fabricated in a 28nm CMOS process. Fig. 18 shows the chip micrograph and the layout details of a single RX channel that occupies 0.11mm$^2$ active area. The receiver optical test setup is illustrated in Fig. 19. The RX chip was wire-bonded to a InGaAs/InP PIN-PD. A M8195A generates a pseudo-random binary sequence (PRBS) pattern to drive a Mach-Zehnder modulator (MZM) with a DC laser source input. This modulated output signal is then coupled to the PD. By sweeping the source laser power, OMA sensitivity is acquired at a certain BER. CDR frequency acquisition is achieved by initializing the LC-VCO coarse cap-bank and fine varactor DAC control codes and then allowing the closed-loop digital PLL-based CDR to achieve phase lock. The measured BER versus input optical power curve, as depicted

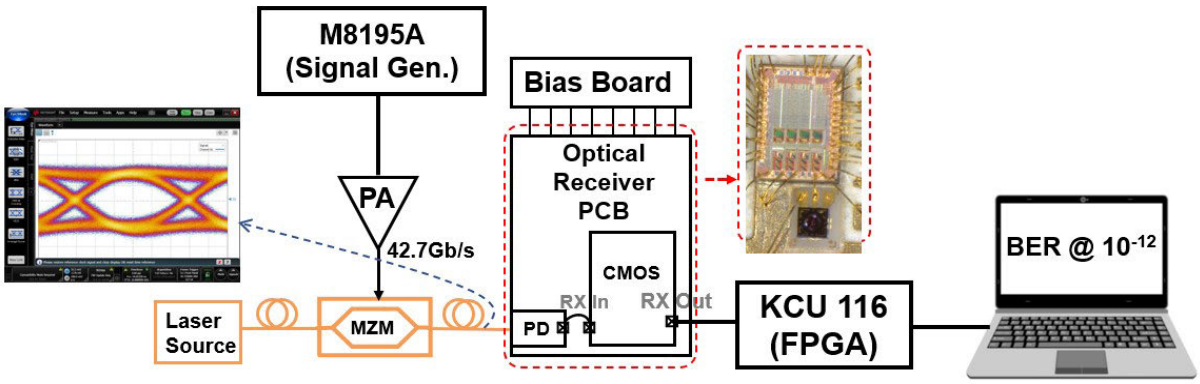


**FIGURE 19.** Optical test setup.

**TABLE 2.** Comparison table.

| | [22] | [23] | [24] | [25] | [26] | [27] | This Work |
|---|---|---|---|---|---|---|---|
| Technology | 14nm CMOS | 28nm CMOS | 28nm CMOS | 32nm SOI | 40nm CMOS | 65nm CMOS | 28nm CMOS |
| Data rate (Gb/s) | 56 | 25 | 40 | 25 | 25.78 | 26 | 42.7 |
| PD resp. (A/W) | - | 0.8 | 0.6 | 0.5 | 0.5 | 0.4 | 0.8 |
| OMA Sens. (dBm) @BER $10^{-12}$ | -4[a] | -6.8 | -1.9 | -10.9 | -10.6[b] | -7.3 | -3.6 |
| Efficiency (pJ/b) | 2.2 | 0.17 | 3.4 | 4.4 | 9.8 | 5.4 | 3.4 |
| Gain (dBΩ) | - | - | 75 | - | - | 72 | 67.5[c] |
| BW (GHz) | - | - | 27 | - | - | 20.4 | 38.7[c] |
| Area ($mm^2$) | 0.06 | 0.0018 | 0.009 | 0.06[d] | 3.72 | 0.81 | 0.11 |

[a]Measured @BER $10^{-11}$ [b]44$\mu A_{PP}$ converted to -10.6 [c]Simulation [d]RX core area

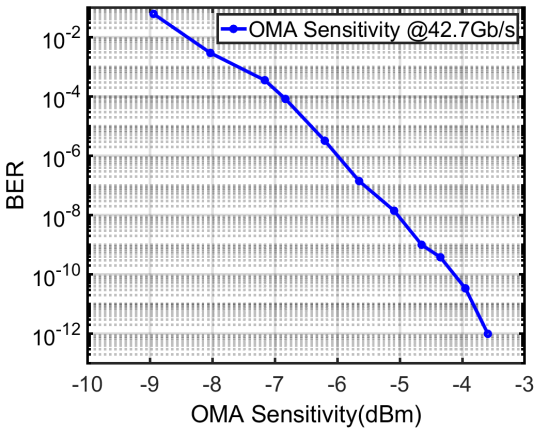


**FIGURE 20.** Measured OMA sensitivity.

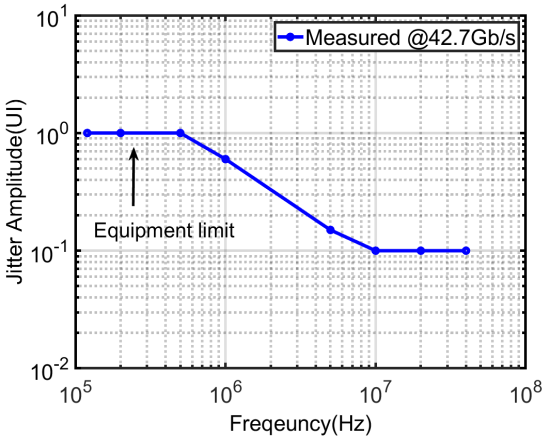


**FIGURE 21.** Measured jitter tolerance.

in Fig. 20, reveals that at a 42.7 Gb/s data rate, the receiver achieves OMA sensitivity of −3.6dBm at BER of $10^{-12}$. Jitter tolerance is also measured with sinusoidal jitter applied at different jitter frequency/amplitude levels by modulating the signal generator delay. Jitter tolerance can be reported up to a 1UI jitter amplitude due to equipment limitations. Fig. 21 provides a jitter tolerance plot measured at a BER of $10^{-12}$ with 42.7 Gb/s PRBS data. It shows that CDR has 10MHz of bandwidth with 0.1UI of high-frequency jitter tolerance. The performance summary and the comparison with other optical receivers are shown in Table 2. Among planar CMOS

process receivers designed with a CDR, this work achieves the highest data rate. The presented broadband AFE with bandwidth extension techniques allow the prototype receiver to achieve high bandwidth with comparable gain.

## VI. CONCLUSION

This paper presents a 42.7 Gb/s optical receiver fabricated in 28nm CMOS. An inverter-based shunt feedback TIA cascaded with CTLE and VGA topology was employed for the AFE, and it shows 67.5dBΩ with 38.7GHz of 3dB bandwidth. CDR with optimum 9bit DLF was implemented to balance jitter and hardware cost. The receiver is wire-bonded to PIN PD, and the measured OMA sensitivity at 42.7Gb/s is −3dBm with a power efficiency of 3.4pJ/bit.

## ACKNOWLEDGMENT

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## REFERENCES

[1] Cisco. (2018). *Cisco Annual Internet Report (2018–2023) White Paper*. [Online]. Available: https://www.cisco.com/c/en/us/solutions/collateral/executive-perspectives/annual-internet-report/white-paper-c11-741490.html

[2] S. Fathololoumi et al., "1.6 Tbps silicon photonics integrated circuit and 800 Gbps photonic engine for switch co-packaging demonstration," *J. Lightw. Technol.*, vol. 39, no. 4, pp. 1155–1161, Feb. 15, 2021.

[3] J. Proesel, A. Rylyakov, and C. Schow, "Optical receivers using DFE-IIR equalization," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 130–131.

[4] S. M. Park and H.-J. Yoo, "1.25-Gb/s regulated cascode CMOS transimpedance amplifier for gigabit Ethernet applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 112–121, Jan. 2004.

[5] T. Takemoto, H. Yamashita, T. Kamimura, F. Yuki, N. Masuda, H. Toyoda, N. Chujo, K. Kogo, Y. Lee, S. Tsuji, and S. Nishimura, "A 25-Gb/s 2.2-W optical transceiver using an analog FE tolerant to power supply noise and redundant data format conversion in 65-nm CMOS," in *Proc. Symp. VLSI Circuits (VLSIC)*, Jun. 2012, pp. 106–107.

[6] C. Kromer, G. Sialm, T. Morf, M. L. Schmatz, F. Ellinger, D. Erni, and H. Jackel, "A low-power 20-GHz 52-dBΩ transimpedance amplifier in 80-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 885–894, Jun. 2004.

[7] P.-C. Chiang, J.-Y. Jiang, H.-W. Hung, C.-Y. Wu, G.-S. Chen, and J. Lee, "4 × 25 Gb/s transceiver with optical front-end for 100 GbE system in 65 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 573–585, Feb. 2015.

[8] D. Patel, A. Sharif-Bakhtiar, and A. C. Carusone, "A 112 Gb/s −8.2 dBm sensitivity 4-PAM linear TIA in 16 nm CMOS with co-packaged photodiodes," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2022, pp. 1–2.

[9] S. Daneshgar, H. Li, T. Kim, and G. Balamurugan, "A 128 Gb/s, 11.2 mW single-ended PAM4 linear TIA with 2.7 $\mu$Arms input noise in 22 nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1397–1408, May 2022.

[10] I. Ozkaya, A. Cevrero, P. A. Francese, C. Menolfi, T. Morf, M. Brändli, D. M. Kuchta, L. Kull, C. W. Baks, J. E. Proesel, M. Kossel, D. Luu, B. G. Lee, F. E. Doany, M. Meghelli, Y. Leblebici, and T. Toifl, "A 64-Gb/s 1.4-pJ/b NRZ optical receiver data-path in 14-nm CMOS FinFET," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3458–3473, Dec. 2017.

[11] H. Kang, I. Kim, R. Liu, A. Kumar, I.-M. Yi, Y. Yuan, Z. Huang, and S. Palermo, "A 42.7 Gb/s optical receiver with digital CDR in 28 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2023, pp. 9–12.

[12] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18 ps setup+hold time," in *Proc. IEEE Int. Solid-State Circuits Conference. Dig. Tech. Papers*, Feb. 2007, pp. 314–605.

[13] K. Zheng, Y. Frans, K. Chang, and B. Murmann, "A 56 Gb/s 6 mW 300 $um^2$ inverter-based CTLE for short-reach PAM2 applications in 16 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.

[14] E. Säckinger, *Broadband Circuits for Optical Fiber Communication*. Hoboken, NJ, USA: Wiley, 2005.

[15] D. Li, G. Minoia, M. Repossi, D. Baldi, E. Temporiti, A. Mazzanti, and F. Svelto, "A low-noise design technique for high-speed CMOS optical receivers," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1437–1447, Jun. 2014.

[16] S. S. Mohan, M. D. M. Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, Mar. 2000.

[17] J. Kim and J. F. Buckwalter, "A 40-Gb/s optical transceiver front-end in 45 nm SOI CMOS technology," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, pp. 1–4.

[18] K. Zheng, Y. Frans, S. L. Ambatipudi, S. Asuncion, H. T. Reddy, K. Chang, and B. Murmann, "An inverter-based analog front-end for a 56-Gb/s PAM-4 wireline transceiver in 16-nm CMOS," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 12, pp. 249–252, Dec. 2018.

[19] B. Razavi, "The delay-locked loop [a circuit for all seasons]," *IEEE Solid StateCircuits Mag.*, vol. 10, no. 3, pp. 9–15, Mar. 2018.

[20] B. Casper and F. O'Mahony, "Clocking analysis, implementation and measurement techniques for high-speed data links—A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 1, pp. 17–39, Jan. 2009.

[21] H.-C. Lee, "An estimation approach to clock and data recovery," Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, USA, 2007.

[22] I. Ozkaya, A. Cevrero, P. A. Francese, C. Menolfi, M. Braendli, T. Morf, D. Kuchta, L. Kull, M. Kossel, D. Luu, M. Meghelli, Y. Leblebici, and T. Toifl, "A 56 Gb/s burst-mode NRZ optical receiver with 6.8 ns power-on and CDR-lock time for adaptive optical links in 14 nm FinFET CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 266–268.

[23] S. Saeedi and A. Emami, "A 25 Gb/s 170 $\mu$W/Gb/s optical receiver in 28 nm CMOS for chip-to-chip optical communication," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, pp. 283–286.

[24] L. Szilagyi, M. Khafaji, J. Pliva, R. Henker, and F. Ellinger, "40-Gbit/s 850-nm VCSEL-based full-CMOS optical link with power-data rate adaptivity," *IEEE Photon. Technol. Lett.*, vol. 30, no. 7, pp. 611–613, Apr. 15, 2018.

[25] A. Rylyakov, J. E. Proesel, S. Rylov, B. G. Lee, J. F. Bulzacchelli, A. Ardey, B. Parker, M. Beakes, C. W. Baks, C. L. Schow, and M. Meghelli, "A 25 Gb/s burst-mode receiver for low latency photonic switch networks," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3120–3132, Dec. 2015.

[26] J. Wang, Q. Pan, Y. Qin, X. Chen, S. Hu, R. Bai, X. Wang, Y. Cai, T. Xia, Y. Zhang, J. Ma, N. Qi, and P. Y. Chiang, "A fully integrated 25 Gb/s low-noise TIA+CDR optical receiver designed in 40-nm-CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 10, pp. 1698–1702, Oct. 2019.

[27] Q. Pan, X. Luo, Z. Li, Z. Jia, F. Chen, X. Ding, and C. P. Yue, "A 26-Gb/s CMOS optical receiver with a reference-less CDR in 65-nm CMOS," *J. Semiconductors*, vol. 43, no. 7, Jul. 2022, Art. no. 072401.

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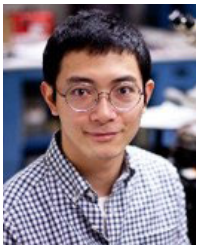

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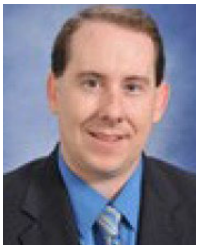

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