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RESEARCH ARTICLE

Enhanced Switched Capacitor Nine-Level Inverter (ESC9LI) Featuring Boost Capability and Streamlined Component Configuration

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ABSTRACT This research presents an innovative design for a switched capacitor inverter, integrating two capacitors, Eleven switches, with one input supply. The proposed configuration successfully attains nine unique voltage states, achieving a voltage gain of two. A separate control unit for capacitor management is no longer necessary with the introduction of the improved SC nine-level inverter (ESC9LI). The management of capacitor charging and discharging is exclusively governed by the activation and deactivation states of the switches. Additionally, the proposed design utilizes fewer components and DC voltage sources, resulting in a higher resultant voltage. The suggested inverter design significantly reduces the necessity of capacitors, switches, and diodes. Power devices' voltage stress is precisely minimized even with the enhanced output voltage. Moreover, only four active devices are conducting per voltage level. Overall, minimizing the number of active devices conducting per voltage level in multilevel inverter circuits offers several benefits including improved efficiency, reduced losses, lower harmonic distortion, enhanced reliability, and simplified control. Consequently, lower-voltage power devices can be employed, leading to a reduction in overall power loss. The control technique employed in the ESC9LI is the level shifted Pulse Width Modulation (LSPWM). The paper presents a detailed comparative study, examining multiple similar topologies. Simulation findings under various operating settings are presented and evaluated against real-time data acquired from an experimental working model.

INDEX TERMS ESCMLI, MLI, LSPWM, phase-disposition, SCMLI, THD.

I. INTRODUCTION

There are fewer components and only a single input power supply used by the nine-level inverter proposed in [1] compared to previous multilevel inverters that have been established. This streamlining lower intricacy and enhances effectiveness in transforming DC to high-frequency AC power. To realize the nine distinct output levels, though, 2 diodes, 9 switches, two capacitors, and one power supply are linked in series and parallel. The topology provided in [2] provides benefits such as enhanced output voltage, a basic voltage balancing method, pulse generation flexibility, and enhanced performance when compared to existing topologies. Nevertheless, the voltage stress and design complexity of the MLI become exceedingly intricate as the number of voltage levels increases. A novel nine-level inverter configuration introduced in [4] utilizes switched capacitors (SCs) connected in series/parallel. It comprises 12 switches and two SCs, offering advantages such as reduced component count, quadruple-boost capability, and limited switch voltage stress. In [5], a novel architecture for boost inverters is introduced, which can produce a voltage waveform with

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nine levels. With this configuration, automated voltage balancing between the capacitors is achieved by using only one DC input in conjunction with two SCs. In [6], a boost-type multilevel inverter with a SC structure is introduced. This configuration provides benefits such as output voltage boosting, multilevel output generation, and a compact design with a minimal component count. Using only one DC supply and 8 switches, the design shown in [7] produces an output voltage with nine levels. Notably, it does not require an H-bridge at the back-end. However, this configuration does necessitate three diodes and three capacitors. A novel arrangement for compact SCMLI is presented in [8]. This design not only has self-regulating voltage, in addition to power enhancement features and enhancing functions, but it also uses a level-shifted multicarrier PWM approach. Nonetheless, the CSCMLI topology requires a total of eleven switches, including one bidirectional switch. A novel boost multilevel inverter topology, leveraging switched-capacitor technology, is introduced in [9]. This topology offers advantages such as voltage gain, self-voltage balancing, and reduced voltage stress. However, it requires a total of eleven switches, including one bidirectional switch, and three capacitors. In [10], describes a novel cross-connected SC module. The floating capacitors (FCs) are optimally connected to the supply source using a design that includes 4 switches and a pair of diodes in this part of the design. By employing the C3SC cell, a nine-level inverter is achieved with only ten switches and two FCs. Specifically for low-voltage usages, an innovative nine-level inverter design architecture is discussed in [11]. However, this proposed topology does not possess voltage boosting capability. A compact SCMLI with efficient modulation techniques is described in [12]. Nonetheless, this proposed topology utilizes a total of 10 switches, including one bidirectional switch and two diodes. In [13], proposes a transformer less T-type nine-level hybrid boost inverter. This inverter combines both the boosting stage and the multilevel inversion stage, resulting in improved efficiency and higher power density. The hybrid nine-level inverter topology introduced in [14] allows for extended utilization of the DC-bus and functionality within the region of overmodulation. Nonetheless, the recommended setup requires the integration of a pair of DC power supplies to acquire the desired result. In [15], highlights the positive aspects of the SC-MLIs, which can achieve the required voltage levels using fewer DC sources and effectively utilize capacitor voltages. However, the voltage boosting factor in SC-MLIs is typically low. Numerous nine-level quadruple boosting circuit designs that utilize SC are outlined in [16], [17], and [18]. Source DC voltage is potentially multiplied by a factor of 4 by employing these inverters; no extra boost conversion step is necessary. Nonetheless, these designs use larger amounts of power components to deliver the prescribed output. Additionally, in [18], the individual switches experience high voltage stress.

An SC-based MLI is presented in the context of [19], which reduces the voltage stresses on power devices. Nonetheless, this layout requires a smaller amount of power electronics switches, but with a larger number of capacitors and diodes to provide a desired resultant voltage. In [20], a nine-level inverter with single-stage voltage step-up capabilities is demonstrated. To accomplish twofold voltage boosting, this design includes 9 switches (9S) with 3 self-balancing capacitors. A new version of the SCMLI with nine different levels and lower capacitance can be witnessed in [21]. However, to provide the expected outcome, this design employs 13 switching devices. In [22], a single-source multilevel inverter with nine levels is presented. This architecture lowers the quantity of essential components and uses input suppliers through switched capacitors, which have self-charging and naturally balancing capabilities. Despite this, it uses a single diode, 10 switching devices, a solitary DC source, and 2 SCs that act as virtual DC sources. A nine-level SC-based enhanced MLI is detailed in [23]. When contrasted with similar configurations, this one offers fewer number of switches, but it requires three capacitors and two diodes to achieve nine different voltage states and offer a voltage amplification equal to twice the input voltage. Nevertheless, this enhancement entails a heightened design cost attributed to the inclusion of extra capacitors and diodes The utilization of diodes prohibits bidirectional power flow in certain renewable energy applications. Figure 1(a) displays the SCMLI inverter topology as reported recently [23], comprising 10 switches and 2 diodes with a boosting gain of two. Based on the literature review, there is an opportunity to develop new inverter topologies that require fewer components while still achieving high boosting factors. Building upon [23], the proposed topology depicted in Figure 1(b) accomplishes a reduction of two diodes while maintaining the same number of output voltage levels and boosting gain. This advancement results in a further reduction in component count, on-state switches, and gate drivers. It focuses on utilizing a single DC voltage source, eliminating the need for additional diodes and floating capacitors, generating up to nine voltage states with only 11 switches and two capacitors, providing a voltage gain of twice the input voltage, ensuring self-balancing of the switched capacitor voltage, and reducing the voltage rating of the switching elements.

The objective of this study is to present an innovative inverter configuration utilizing the switched-capacitor method, facilitating bidirectional power flow with minimal components and ON state switches. Additionally, a strategy for reducing the number of conducting switches and gate drivers is proposed. Moreover, the operation involves only four active devices conducting per voltage level, offering numerous benefits in multilevel inverter circuits. These advantages include increased efficiency, reduced losses, minimized harmonic distortion, enhanced reliability, and simplified control mechanisms.

The benefits of the suggested configuration include:

- Utilization of merely four active devices per voltage level during operation, leading to a decrease in both on-state switches and gate drivers

TABLE 1. ESC9LI Switching States.

Switches											C		Vout
S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	C1	C2	
											⇩	⇩	$2V_{dc}$
											⇩	-	$1.5V_{dc}$
											⇧	⇧	V_{dc}
											⇧	⇩	$0.5V_{dc}$
											⇧	⇧	0
											⇩	⇧	$-0.5V_{dc}$
											⇧	⇧	$-V_{dc}$
											-	⇩	$-1.5V_{dc}$
											⇩	⇩	$-2V_{dc}$

OFF ON

- Absence of diodes, thereby allowing bidirectional power flow in specific renewable energy scenarios
- Employment of fewer components overall
- Reduced voltage stress on the switches
- Doubling of the input voltage for the output voltage
- Self-balanced FC voltages, eliminating the need for voltage/current sensors

The structure of this article is as proceeds. Following an introduction, Section II describes the ESC9LI layout, its states of operating condition and control method applied to the ESC9LI. In Section III, Comprehensive Comparison study with recent MLI topologies and total standing voltage. Power loss analysis is presented in section IV. The testing findings are laid out and addressed in Section V and Section VI outlines the conclusion.

II. ESC9LI CIRCUIT TOPOLOGY

A. CIRCUIT CONFIGURATION

In Fig. 1(a), the diagram illustrates a recently published nine-level SCMLI topology as discussed in [23]. This configuration employs 10 switches, 2 diodes, and three capacitors, resulting in a boosting gain of two. Expanding upon the findings presented in [23], this paper introduces a novel ESC9LI topology (refer to Fig. 1(b)) featuring eleven switches and only two capacitors. By streamlining the process of charging and discharging capacitors, the recommended ESC9LI lowers the total quantity of input supply. Using regulated operations in both series and parallel modes, the capacitors may balance themselves independently. This structural characteristic

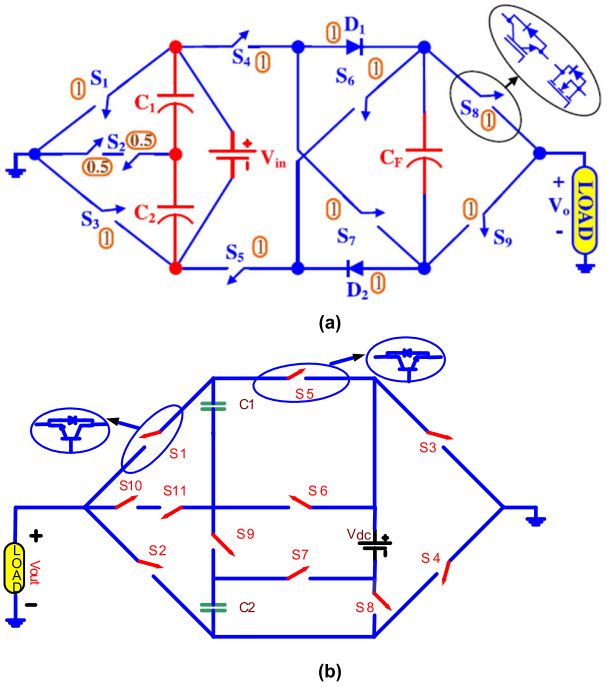

FIGURE 1. 9 level (a) SC9LI presented in [23] and (b) Proposed ESC9LI circuit diagram.

enables the avoidance of additional power supply requirements. This topology yields a high-quality output voltage with minimal harmonic distortion, making it suitable for a diverse range of applications. Nine different voltage levels (±2Vdc, ±1.5Vdc, ±0.5Vdc, ±Vdc, and 0 Vdc) have been produced by the system.

Each of the quasi-square waveform's Fourier decomposition (V_{oi}) might be described as,

$$V_{oi} = \frac{2V_{dc}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \frac{\cos(k\theta_i)}{k} \sin(k\omega t) \tag{1}$$

In this case, (ω) represents the output's angular frequency. Based on the theory of waveform formation, the resulting voltage may be portrayed as,

$$V_{out} = \sum_{i=1}^{4} V_{oi} \tag{2}$$

Hence, the Fourier decomposition of the resultant voltage (V_{out}) may be expressed as,

$$V_{out} = \frac{2V_{dc}}{\pi} \sum_{k=1,3,\ldots}^{\infty} \sum_{i=1}^{4} \frac{\cos(k\theta_i)}{k} \sin(k\omega t) \tag{3}$$

B. STATES OF OPERATING CONDITION

The operational modes of various devices are detailed in Table 1, which includes the on and off cycles of switches and the charging and discharging conditions of capacitors. The color red indicates that the switch is off, while the color green indicates that it is on. Upward and downward arrows stand for both the charging and the discharging state of a

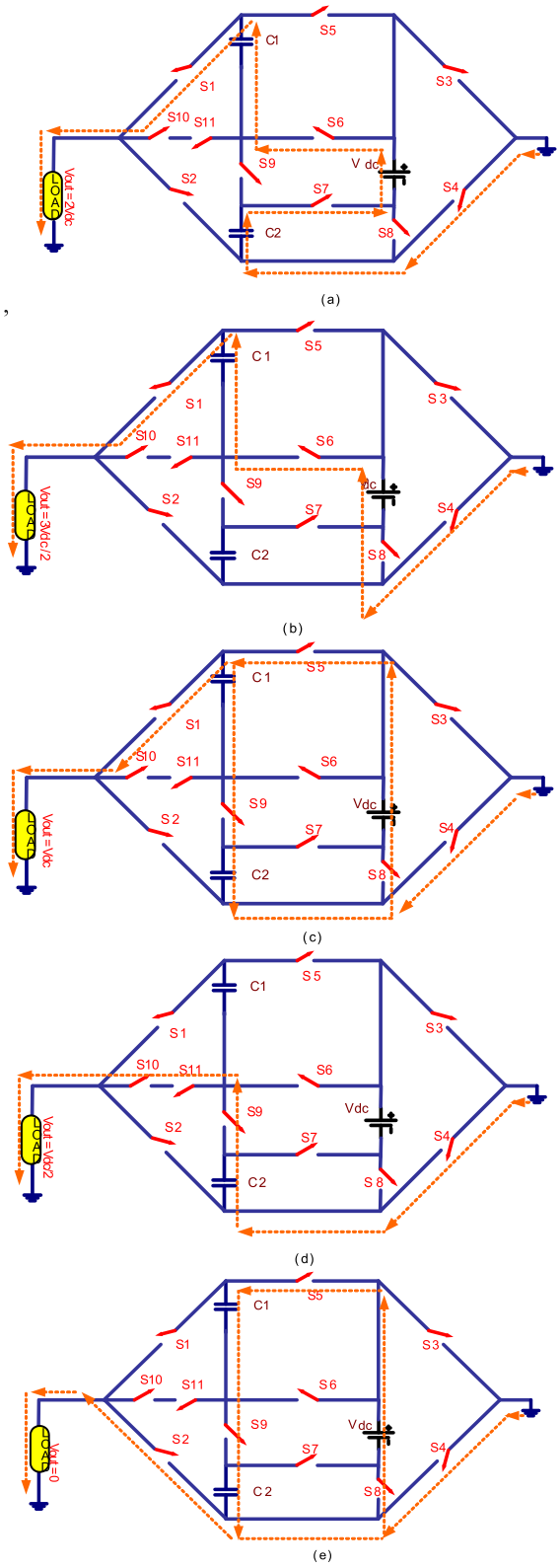

FIGURE 2. Current path for proposed inverter (a) $2V_{dc}$ level (b) $1.5V_{dc}$ level, (c) V_{dc} level (d) $0.5V_{dc}$ level (e) $0V_{dc}$ level.

capacitor, correspondingly. For each positive voltage level and zero, Figure 2 (a) to (e), shows the current directions of the designed ESC9LI structure.

The configuration has eleven switches, but only four of them must be active for the intended result to be achieved. This minimizes losses and simplifies the switching process.

To avert unintended short circuits, the switches are crafted with anti-parallel diodes that stay in a non-forward biased state. The suggested topology guarantees the prevention of source short-circuits by choosing a switching state that takes into account all conceivable scenarios.

Table 1 provides an overview of the various operation modes of the suggested MLI. Fig. 2 depicts the operation states for 2Vdc, 1.5Vdc, Vdc, 0.5Vdc, and 0Vdc. Fig. 2 shows that switches S1, S4, S6, and S7 are engaged in switching state-1.

So, the inverter's output is +2Vdc. Switching state 2 corresponds to a +1.5Vdc voltage output whenever switches S1, S4, S6 and S8 are maintained in their active positions. After shifting to state 3, the exact voltage output is +Vdc as long as switches S1, S4, and S9 are held in the on position. In switching state 4, the suitable voltage output is +Vdc whenever either S4, S9, S10 and S11 are held on. In switching state 5, the suitable voltage output is 0Vdc whenever either S1, S4, and S9 are held on. In addition, Table-1 displays the rest of the operational modes of the established ESC9LI.

C. CONTROL METHOD APPLIED TO SC9LI

The fundamental operational principles of the proposed SC9LI are established through the implementation of the Level Shifted (LS)-PWM scheme. (L-1) carriers with the same frequency and highest possible amplitude were employed to build an L-level MLI [24], [25], [26], [27], [28], [29]. As evident in Figure 3a, the carrier signal is an instance of in-phase synchronization between carriers above and below the zero-axis. The reference signal takes a sinusoidal form, and each of the eight triangular carriers shares a consistent maximum magnitude and a frequency of 2 kHz. In Fig. 3(a), the modulating signal is denoted as S_{ref}.

The "phase disposition" (PD) approach arranges these carriers in sequential phases. Accordingly, an activation pulse is immediately produced if a sinusoidal reference signal exceeds triangular carriers as assessed by a comparator. The relevant switching signals are consequently produced by utilizing the appropriate logic circuits. Figure 3(b) shows the gate pulses for each of the eleven switches that contribute to the ESC9LI.

A phase opposition disposition PWM methodology, which uses this carrier configuration, surpasses traditional LSPWM methods pertaining to spectrum efficacy. Fig. 3 (a) depicts the distribution of carriers Ca1-Ca4 above the zero level and carriers Ca5-Ca8 just below. For positive values, the carrier sequence is constructed as follows: $0 \leq VCa1 \leq 1 \leq VCa2 \leq 2 \leq VCa3 \leq 3 \leq VCa4 \leq 4$, while for negative values, it is structured as follows: $0 \geq VCa5 \geq -1 \geq VCa6 \geq -2 \geq VCa7 \geq -3 \geq VCa8 \geq -4$.

Each carrier is synchronized with the next in the sequence. Consequently, the initial driving signals are created directly

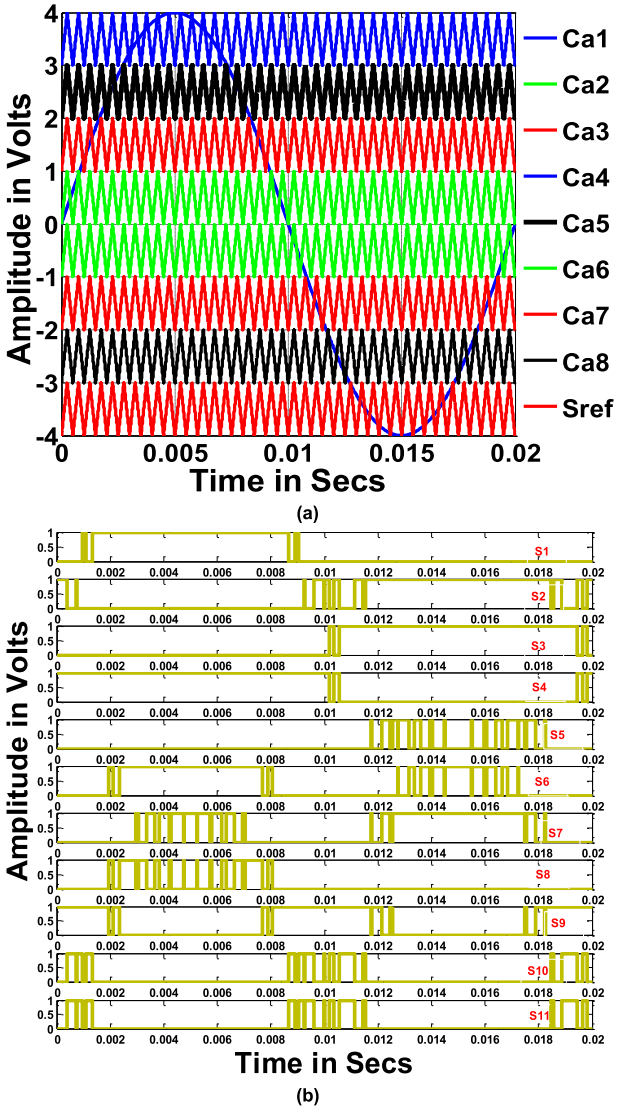

FIGURE 3. ESC9LI PD mechanism switching design a) arrangement of carriers b) the pulses for each switch.

by contrasting Sref with the signals of the carriers Ca1–Ca8 employing comparators. Furthermore, appropriate logical operators are utilized in producing switch gate pulses (S1-S11). Fig. 3(b) depicts the generated pulses for the S1-S11 switches.

III. COMPARISON STUDY WITH RECENT MLI TOPOLOGIES AND TOTAL STANDING VOLTAGE

A. COMPREHENSIVE COMPARISON

An extensive comparison is given to illustrate the efficacy of the proposed ESC9LI setup. Taking into account the total number of capacitors, dc sources, switches, diodes, the maximum conducting switches, boosting factor, Active devices, maximum voltage of capacitor, maximum voltage stress of switches, number of switches in the conducting path, maximum output voltage, total blocking voltage, number of devices in the charging loop, self-balancing ability, voltage input and output, power output and the percentage of efficiency. The ESC9LI is compared to other similar inverter configurations in Table 2, which features information from [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [15], [16], [18], [19], [20], [21], [22], [23], [25], [26], and [27]. As provided in table 2 the NC values for the suggested inverter arrangement are noticeably reduced in comparison to [2], [6], [7], [9], [16], [19], [20], and [23] and same those for other configurations described in the relevant research. Within the chosen configurations, all these configurations utilize 1 DC power sources whereas [22] alone uses one power source with a rating of 2 Vdc. In contrast to other presented topologies, it becomes evident that the proposed topology employs a reduced number of switches and diodes (NSW+ND) to achieve the 9-level output, except for the topologies mentioned in [20]. Nevertheless, these particular topologies require a higher NC, thereby resulting in an increased component count for the inverter configurations.

The table 2 clearly shows that the proposed topology eliminates the need for diodes, similar to other configurations mentioned in the relevant research, with the exception of the configuration presented in [1], [5], [7], [10], [15], [16], [18], [19], [20], [22], [23], and [27]. Most of the cases diodes restricts the reverse or regenerative power flow. The ESC9LI allows for the activation of no more than four switches per level. In the proposed inverter structure and the topologies described in [5], [22], and [23], the MCS exhibits a significant decrease compared to other topologies mentioned in the literature. However, it should be noted that the configurations presented in [5], [22], and [23] necessitate a higher number of components when compared to the suggested design. Furthermore, active devices including switches and diode are noticeably less compared to other topologies mentioned in the literature. Maximum Voltage rating of the capacitors is half of the input voltage in the proposed configuration. Number of switches in the conducting path also less compared to many configurations presented in the literature. Total blocking voltage of switches is very less compared to all the topologies presented in the literature. % η outperforms all previously reported literature. It is noticed from Table 2 that the recommended ESC9LI functions more effectively than the existing MLIs.

B. TOTAL STANDING VOLTAGE OF ESC9LI

A crucial aspect in assessing the cost of an MLI involves the capacity of the switch to handle blocking or standing voltage. Blocking voltage refers to the maximum potential difference that can be averted when a switch is open. The overall cost of the inverter lowers proportionally with the blocking voltage (BV).

As shown in Figure 4, the BV (Blocking Voltage) of ESC9LI is calculated using Figure 2. It is then presented in the form of charts. The switches, S1-S4, in the ESC9LI experience the highest voltage stress of 2Vdc (twice the input dc supply), as depicted in Figure 4. As demonstrated in the

TABLE 2. Comparison With Recently Reported Similar MLIs.

MLIs	NC	NDS	NSW	ND	NSW +ND	MCS	BF	AD (S+D)	MVc (Vdc)	MVSS (Vdc)	NSCP	MOV (Vdc)	TBV (Vdc)	NDCL	SB	Vo/Vin (Vdc)	Pout (W)	%η
[1]	2	1	9	3	12	5	2	6	0.5	2	5	2	11.5	3	Y	2/1	NA	94.18
[2]	3	1	12	0	12	5	1	6	0.5	1	6	1	5	3	N	1/1	250.1	92.3
[3]	2	1	12	0	12	7	2	7	0.5	1	5	2	5.5	4	Y	2/1	15.57	80.6
[4]	2	1	12	0	12	7	4	6	2	2	6	4	5.25	4	Y	4/1	NA	87.2
[5]	2	1	10	2	12	4	2	4	0.5	2	4	2	5.5	2	Y	2/1	2000	95
[6]	4	1	12	0	12	6	4	6	2	4	5	4	6	4	Y	4/1	50	96
[7]	3	1	8	3	11	6	4	4	2	4	3	4	5.75	3	Y	4/1	500	93
[8]	2	1	11	0	11	8	2	7	0.5	1	7	2	11	4	Y	2/1	400	94
[9]	3	1	11	0	11	6	2	6	1	2	5	2	5	4	Y	2/1	100	96.5
[10]	2	1	10	2	12	5	2	7	0.5	1	5	2	9	4	Y	2/1	400	97.12
[15]	2	1	10	1	11	5	4	5	2	4	4	4	5.75	4	Y	4/1	500	94.3
[16]	3	1	11	2	13	5	4	6	4	6	5	4	8	8	Y	4/1	1000	93.97
[18]	2	1	13	1	14	5	4	6	2	4	5	4	7.75	4	Y	4/1	390	90.94
[19]	4	1	9	3	12	5	4	6	3	3	5	4	5.25	4	Y	4/1	1000	95.2
[20]	4	1	9	1	10	6	2	7	1	2	5	2	5	4	Y	2/1	1200	97.5
[21]	2	1	13	0	13	6	2	6	0.5	2	5	2	6	5	Y	2/1	NA	95.5
[22]	2	1	10	1	11	4	2	4	1	4	4	4	4	2	Y	4/2	100	95
[23]	3	1	10	2	12	4	2	6	0.5	4	4	2	5.5	4	Y	2/1	1000	97.27
[25]	2	1	11	1	12	6	4	7	2	4	6	4	4.25	5	Y	4/1	786.3	96.37
[26]	2	1	09	2	11	5	4	6	2	4	5	4	6	3	Y	4/1	157	96.95
[27]	2	1	10	01	11	5	4	5	2	4	2	4	6.25	3	Y	4/1	-	-
Proposed	2	1	11	0	11	4	2	4	0.5	2	4	2	3.25	3	Y	2/1	600	98.86

NC: Number of capacitors, NDS: Number of DC sources, NSW: Number of switches, ND: Number of diodes, MCS: maximum conducting switches, BF= Boosting Factor, η = Efficiency

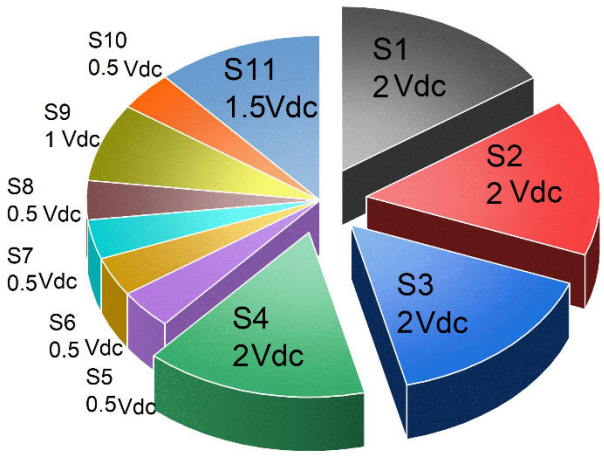

FIGURE 4. BV on switches on each individual switch.

aforementioned figure, the BV of S9 is equivalent to the input voltage. Likewise, the BV of switches S5-S8 is half of the input voltage. One and a half times the input voltage is the BV of switch S11. To determine the overall BV of all switches, a similar method is employed. The Total Blocking Voltage (TBV) is equal to 13 Vdc since it represents the sum of all blocking voltages across all devices. Additionally, it is observed that not all switches need to be rated for high voltage; only a select number of them require this rating.

IV. ANALYSIS OF POWER LOSSES

In the study portion, the power losses of the inverters are estimated. These losses include switching losses (P_{SL}), conduction losses (P_{CL}), and ripple losses of capacitors (P_{RL}).

A. CONDUCTION LOSSES

Conduction losses include power losses produced by power device on-state resistance and diode conduction voltage drop. The nine operational modes of the suggested inverters are portrayed by four equivalent circuits in Fig. 5 (a)–(d). Switches' on-state resistance is denoted by $R_{ON,Switch}$, Load resistance is represented by R_L, and the equivalent series resistance of each capacitor is denoted by ESRC, assuming the anti-parallel diodes have the conduction voltage drop $V_{d,Diode}$ and internal resistance $R_{i,Diode}$. R_{eq} represents the equivalent resistance of the power device, and the equivalent voltage drop of the diode is represented by $V_{d,Diodeeq}$.

$$P_{CL} = \frac{2}{\pi}\sum_{i=1}^{4}\left[\left(\frac{V_{out} - V_{d,Diodeeq}}{R_{eq} + R_L}\right)^2 \times R_{eq} \times (\theta_{i+1} - \theta_i)\right] \tag{4}$$

B. SWITCHING LOSSES

Turn-on and turn-off activities develop switching losses. The following formula will be employed to estimate the switching losses of the i^{th} switch:

$$\begin{aligned} P_{SL,ON,i} &= f_s \int_0^{t_{on}} v_{switch,i}(t)\, i(t)\, dt \\ &= f_s \int_0^{t_{on}} \left(\frac{V_{switch,i}}{t_{ON}} t\right)\left[-\frac{I_i}{t_{ON}}(t - t_{ON})\right] dt \\ &= \frac{f_s V_{switch,i} I_i t_{ON}}{6} \end{aligned} \tag{5}$$

$$
\begin{aligned}
&P_{\mathrm{SL,OFF},i} \\
&\quad = f_{\mathrm{s}} \int_0^{t_{\mathrm{off}}} v_{\mathrm{switch},i}\,(t)\, i\,(t)\,\mathrm{d}t \\
&\quad = f_{\mathrm{s}} \int_0^{t_{\mathrm{off}}} \left(\frac{V_{\mathrm{switch},i}}{t_{\mathrm{OFF}}} t\right) \left[-\frac{I_i}{t_{\mathrm{OFF}}}\,(t - t_{\mathrm{OFF}})\right] \mathrm{d}t \\
&\quad = \frac{f_{\mathrm{s}} V_{\mathrm{switch},i} I_i t_{\mathrm{OFF}}}{6}
\end{aligned} \tag{6}
$$

The variable fs represents the switching frequency of the i-th switch. $V_{switch,i}$ denotes the voltage stress on the switch, while I_i represents the current flowing through the i-th switch. t_{ON} and t_{OFF} refer to the turn-on and turn-off times of the switch, respectively. The overall switching losses of the suggested inverter are possibly to be calculated as

$$
P_{\mathrm{SL}} = \sum_{i=1}^{11} \left(P_{\mathrm{SL},ON,i} + P_{\mathrm{SL,OFF},i}\right) \tag{7}
$$

Based on the study indicated earlier, the suggested topology has a low switching frequency and voltage stress. This is beneficial in reducing the switching loss of the inverter.

C. RIPPLE LOSSES

Capacitor voltage fluctuations are the source of ripple loss. The voltage ripple may be determined by calculation.

$$
\Delta V_{\mathrm{rip}} = \frac{V_{\mathrm{dc}}\,(2\pi - 3\theta_3 - \theta_4)}{2\pi f_{\mathrm{out}} R_{\mathrm{L}} C} \tag{8}
$$

Two capacitors' ripple losses can be computed as follows:

$$
P_{\mathrm{RL}} = \sum_{j=1}^{2} C_{\mathrm{j}} \Delta V_{\mathrm{rip}}^2 f_{\mathrm{out}} \tag{9}
$$

Considering that the inverter's overall ripple loss is

$$
P_{\mathrm{RL}} = \frac{V_{\mathrm{dc}}^2\,(2\pi - 3\theta_3 - \theta_4)^2}{2\pi^2 f_{\mathrm{out}} R_L^2 C} \tag{10}
$$

The frequency at which the inverter operates and capacitance influence the ripple loss. since larger operating frequencies and capacitance may lower the inverter's ripple loss. Overall inverter power loss is expressed as,

$$
P_T = P_{\mathrm{RL}} + P_{\mathrm{CL}} + P_{\mathrm{SL}} \tag{11}
$$

The efficiency of the configuration can be expressed as

$$
\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{RL}} + P_{\mathrm{CL}} + P_{\mathrm{SL}} + P_{\mathrm{out}}} \tag{12}
$$

where P out represents the power output.

According to Tables 2 and 3, the suggested MLI is more efficient than existing configurations owing to substantially lesser power losses. Table 3 indicates that the lower power loss associated with the suggested ESC9LI leads to a greater efficiency (98.89%). The power loss of the ESC9LI is measured through PLECS. The net losses were assessed at an output power of 550.9 W. In this case, the ESC9LI's effective switching loss is 0.11 % and its conduction loss is 1.0 %. Meanwhile, the % η and power loss are measured through

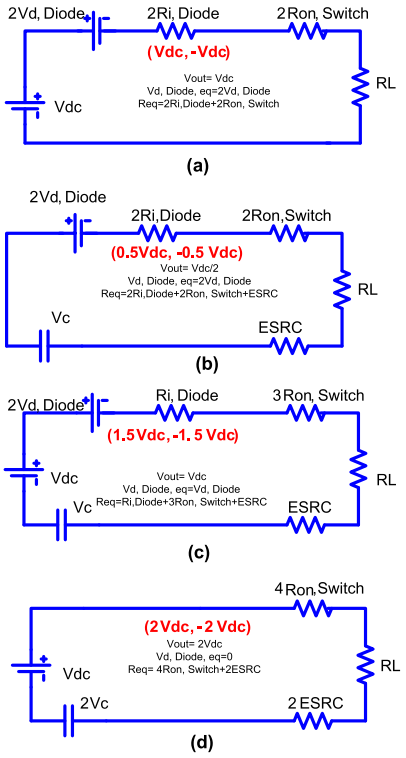

FIGURE 5. Equivalent circuits (a) 0.5Vdc &-0.5 Vdc (b) Vdc &-Vdc (c) 1.5Vdc &-1.5 Vdc (d) 2Vdc &-2Vdc.

simulation and experimental setup, and the findings are displayed in Table 3. The power loss of the ESC9LI experimental setup is measured through Yokogawa WT1800 power Analyzer. The net losses were assessed at an output power of 545.1W and efficiency is 98.86%.

The plot of the recommended ESC9LI % efficiency contrast with various power ratings is depicted in Fig. 5 (a), and the plot of the suggested ESC9LI 's loss comparison with various power ratings is displayed in Fig. 5 (b).

V. SIMULATION AND EXPERIMENTATION FINDINGS FROM THE STUDY

The results from the simulation were reported, which serves to substantiate the performance of the ESC9LI setup. MATLAB/Simulink is employed to simulate the ESC9LI. Assessing the viability of the presented ESC9LI, the experimental findings are further presented. Table 4 and 5 includes a list of experimental data. Featuring a peak voltage of 400V and 9 levels of output, the ESC9LI design is developed by incorporating 11 IGBT switches in combination with one DC supply (V=200V) and two Capacitor (C1, C2) of 2200 μF. There are nine distinct levels of output voltage, ranging from 0 to ±400V. The ESC9LI was evaluated in a diverse variety of loading scenarios, including dynamic load changes. Four different loading test cases are taken into account in the investigation: a R load value of 200Ω, a RL load value of 200 Ω −50 mH, and a sudden phase transition loading circumstance in which the load changes from R to L a. Finally

TABLE 3. Power Loss Comparison and Efficiency of the ESC9LI Different Output Power.

Load Rating	Simulation			Experimental		
	Output Power	%η	% Loss	Output Power	%η	% Loss
200 Ω	550.9	98.89	1.11	545.1	98.86	1.14
175Ω	675.4	98.85	1.15	667.2	98.82	1.18
150Ω	800.9	98.79	1.21	799.4	98.74	1.26
125Ω	1000.9	98.75	1.25	998.5	98.72	1.28
100Ω	1430	98.72	1.28	1380	98.71	1.29
75Ω	1689	98.70	1.3	1654	98.69	1.31
50Ω	2010	98.65	1.35	1999	98.62	1.38

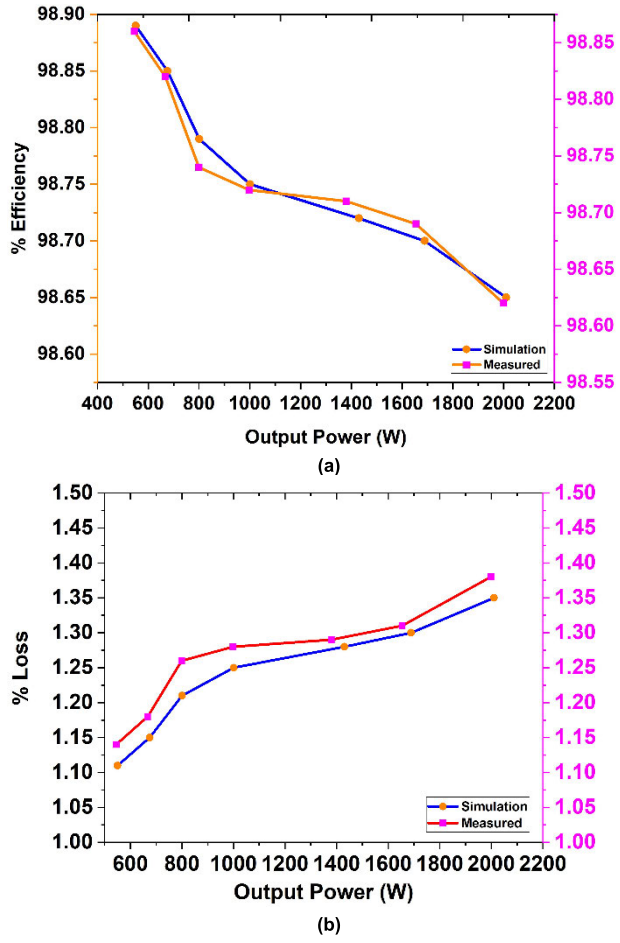

FIGURE 6. Comparison of (a) % Efficiency vs output power (b) % Loss vs output power.

tested with L-R-L (50 mH-200 Ω −50 mH) phase transition loading circumstance.

Fig. 7(a) and (b) display the voltage and current patterns produced by the ESC9LI as well as the harmonic bands for test scenario 1 (an R load value of 200 Ω). The harmonic distortion of both current and voltage is 12.90%, resulting in a peak fundamental voltage of 400V. The alternating voltage, current, and harmonic band waveforms for test scenario 2 are shown in Fig. 8(a) and (b). The fundamental peak of the

TABLE 4. Experimental Parameters.

Parameters	Value/Type
Switch	IGBT -FGA25N120
Driver	TLP250
Controller	dSpace 1104
Input supply/capacitors	V = 200V and (C1 and C2) 2200 µF
Load	R - 200Ω, L - 50 mH

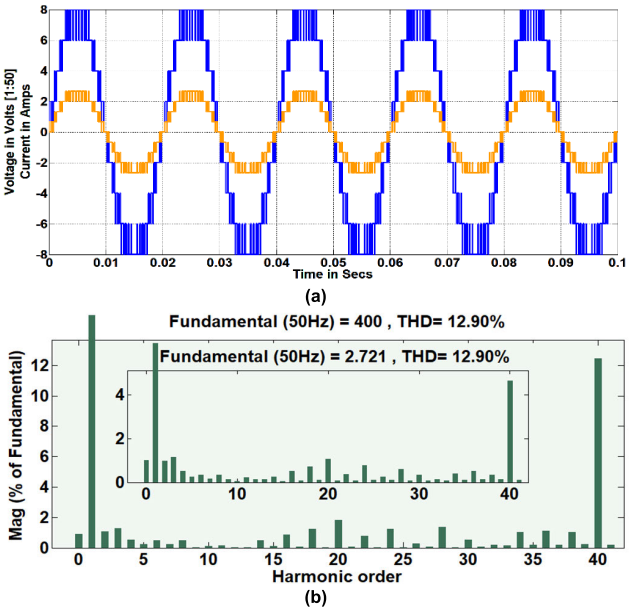

FIGURE 7. Simulation results: (a) Voltage and current waveforms (R-load 200Ω). (b) Harmonic spectrum.

voltage that exists is 400 V, and the distortion caused by harmonics is 12.90% and 0.63 % of harmonic content present in the resultant current. The ESC9LI setup has been successfully evaluated under sudden transition load, as witnessed by the third test scenario, using 200Ω R load to 50 mH L load.

Fig. 9(a) and (b) demonstrate the current waveforms and voltage for dynamic load shifts from 200Ω R load to 250 mH L load at t = 0.06 sec, together with associated harmonic spectra. The load voltage holds stable despite the major transformation in the load. Findings from analyzing the harmonic spectra of the voltage and current at the output indicate a THD level of 12.90% for the voltage and 10.80% for the current. The results presented above reveal that the ESC9LI setup is robust and able to explore a variety of loads and dynamic circumstances. Figures 10(a) and (b) show the harmonic spectra and waveforms of voltage and current for test scenario 4. The fundamental peak value of the voltage waveform is 400 V, with 12.90 % harmonic distortion. 3.83% of harmonic content present in the resultant current. Furthermore, the experimental test results are reported to evaluate the design's viability in practice. Two capacitors' voltage waveforms are exposed in Fig. 11. After the system achieves a steady state, as shown in Figure 11, the voltage of both capacitors remains stable at

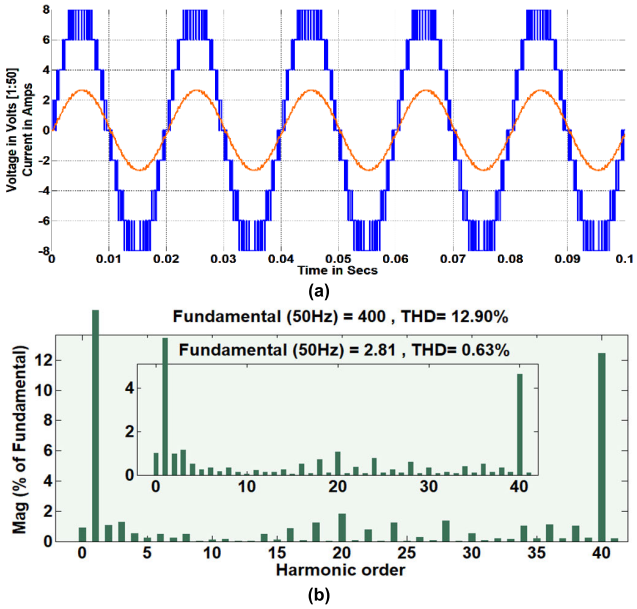

FIGURE 8. Simulation results: (a) Voltage and current waveforms produced by RL Load (200 Ω, 50 mH). (b) Harmonic spectrum.

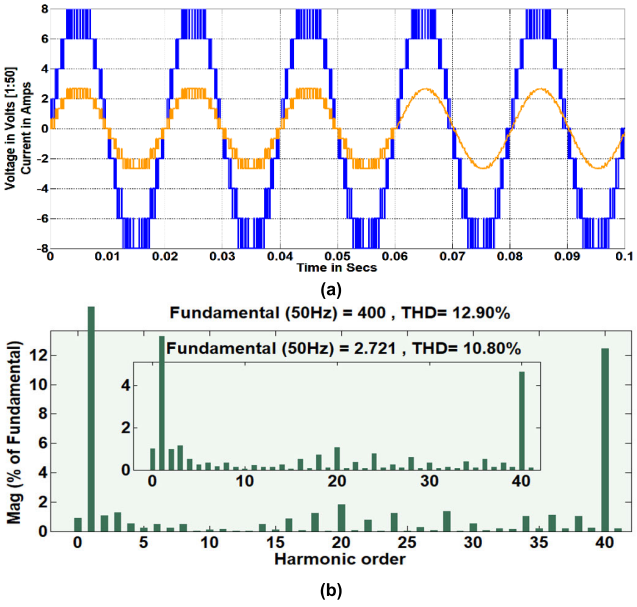

FIGURE 9. Simulation results: (a) Voltage and current waveforms by (R to L). (b) Harmonic spectrum.

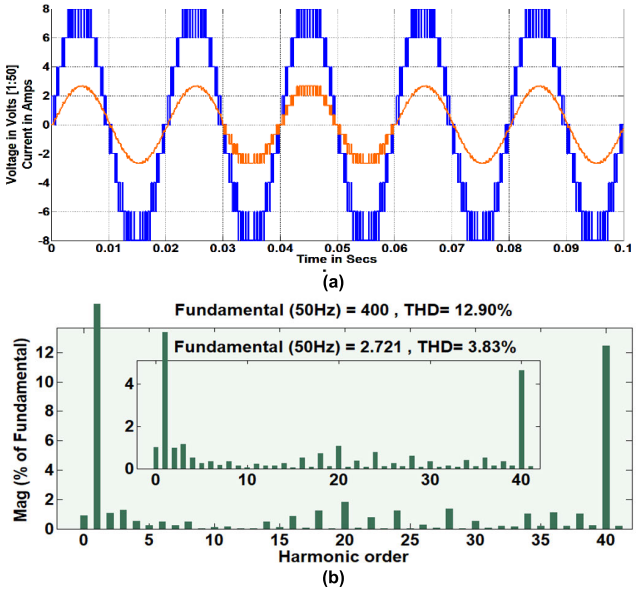

FIGURE 10. Simulation results: (a) Voltage and current waveforms by L-R-L Load (50mH, 200 Ω, 50 mH). (b) Harmonic spectrum.

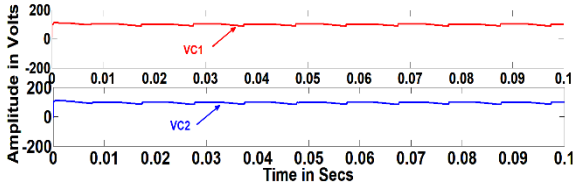

FIGURE 11. Capacitor voltage waveform.

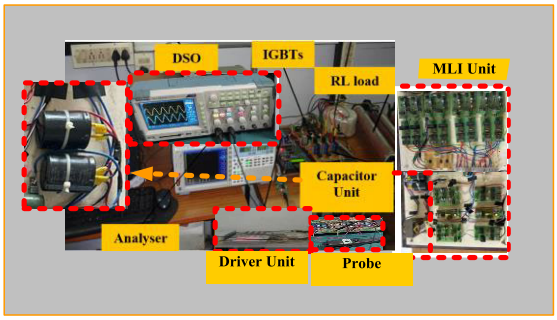

FIGURE 12. Practical setup for proposed ESC9LI.

or near their rated value, and indicating that capacitor voltage is balanced.

Fig. 12 depicts the experimental set-up used to test the ESC9LI configuration. Experimentally obtained voltage and current waveforms under test conditions 1 are exposed in Fig. 13(a). Spectra of the associated harmonics are revealed in Fig. 13(b). Figure 14 (a) shows the voltage and current waveforms that resulted from the second test scenario. Figure 14(b) shows the corresponding harmonic spectra. Additionally, Figures 15(a) and (b) shows the voltage, current, and harmonic bands for test Scenario 3 with the rapid phase shift load, respectively, confirming the effectiveness and impact on the effectiveness. Figure 16 (a) shows the voltage and current waveforms that resulted from the fourth test scenario. Figure 16(b) shows the corresponding harmonic spectra.

Figure 17 illustrates the grid-tied capabilities of the proposed configuration, showcasing the application of a closed-loop control technique outlined in [24].

$$P_{cal} = 1/2\left[v_{gr\alpha} i_{gr\alpha} + v_{gr\beta} i_{gr\beta}\right] \quad (13)$$

$$Q_{cal} = 1/2\left[v_{gr\beta} i_{gr\alpha} - v_{gr\alpha} i_{gr\beta}\right] \quad (14)$$

vgα, vgβ, igα, and igβ reveal the different components of grid voltage as well as current in the α and β orientations. Using equations (13) and (14), we can calculate the current

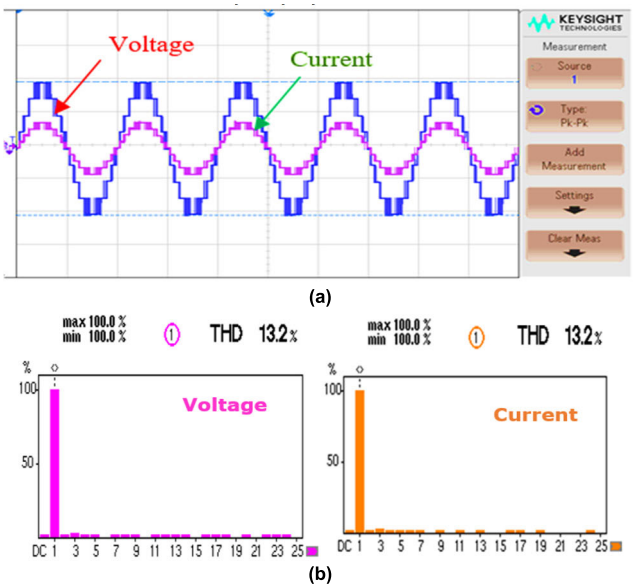

FIGURE 13. The outcomes from the experiment: (a) voltage, current (R- load200Ω). (b) Harmonic band.

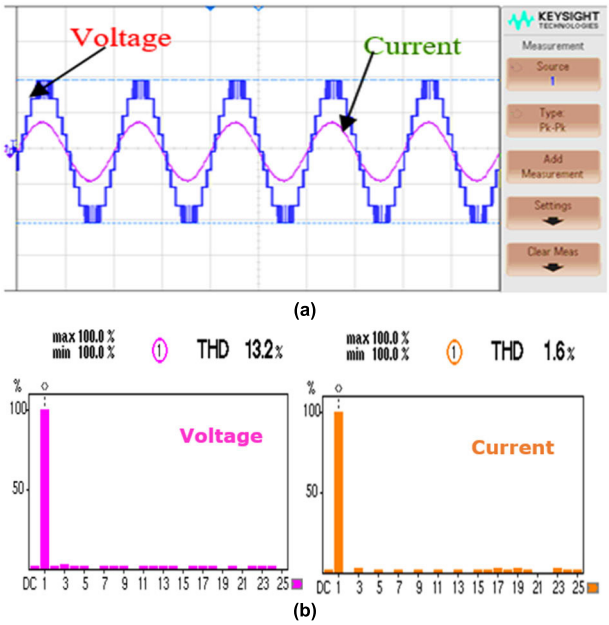

FIGURE 14. The outcomes from the experiment: (a) voltage, current produced (RL Load 200 Ω, 250 mH). (b) Harmonic band.

in the $\alpha\beta$-reference frame:

$$i_{gr\alpha} = \frac{2\left(P_{cal} * v_{gr\alpha} + Q_{cal} * v_{gr\beta}\right)}{v_{gr\alpha}^2 + v_{gr\beta}^2} \tag{15}$$

$$i_{gr\beta} = \frac{2\left(P_{cal} * v_{gr\beta} + Q_{cal} * v_{gr\alpha}\right)}{v_{g\alpha}^2 + v_{gr\beta}^2} \tag{16}$$

Following the single-phase P-Q theory, it is possible to generate the grid-in-current reference by controlling the average active and reactive power [24]. Two proportional-integral (PI) controllers have been employed, as seen in Figure 17, to regulate the active and reactive power, which remains

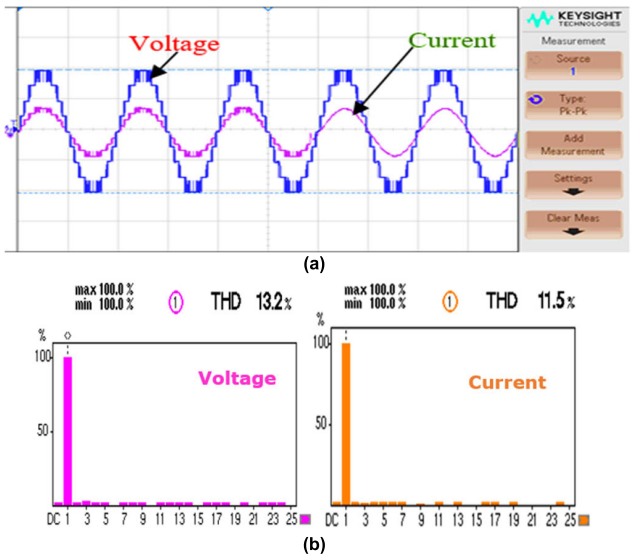

FIGURE 15. The outcomes from the experiment: (a) the voltage and current waveforms by (R to L). (b) Harmonic band. (Ch1: 200 V/div, Ch2: 4 A/div).

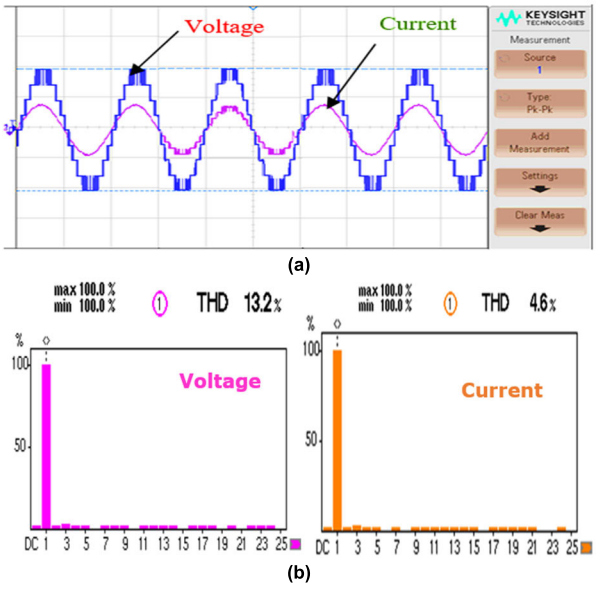

FIGURE 16. Harmonic spectrum. (load shifting from L load to R load and R load to L load). (b) Harmonic band.

constant in a steady state. The equation below shows how to use the OSG system to obtain the grid reference current (17), as shown at the bottom of the next page. When Prefe and Qrefe denote the power references, and the transfer functions of the PI-based controller are Gp(s) and Gq(s), which may be described in the following way:

$$G_p(s) = K_{pp} + K_{pi} * \frac{1}{s}$$

$$G_q(s) = K_{qp} + K_{qi} * \frac{1}{s} \tag{18}$$

The integral and proportional gains for the active and reactive power are expressed as Kpp, Kpi, Kqp, and Kqi.

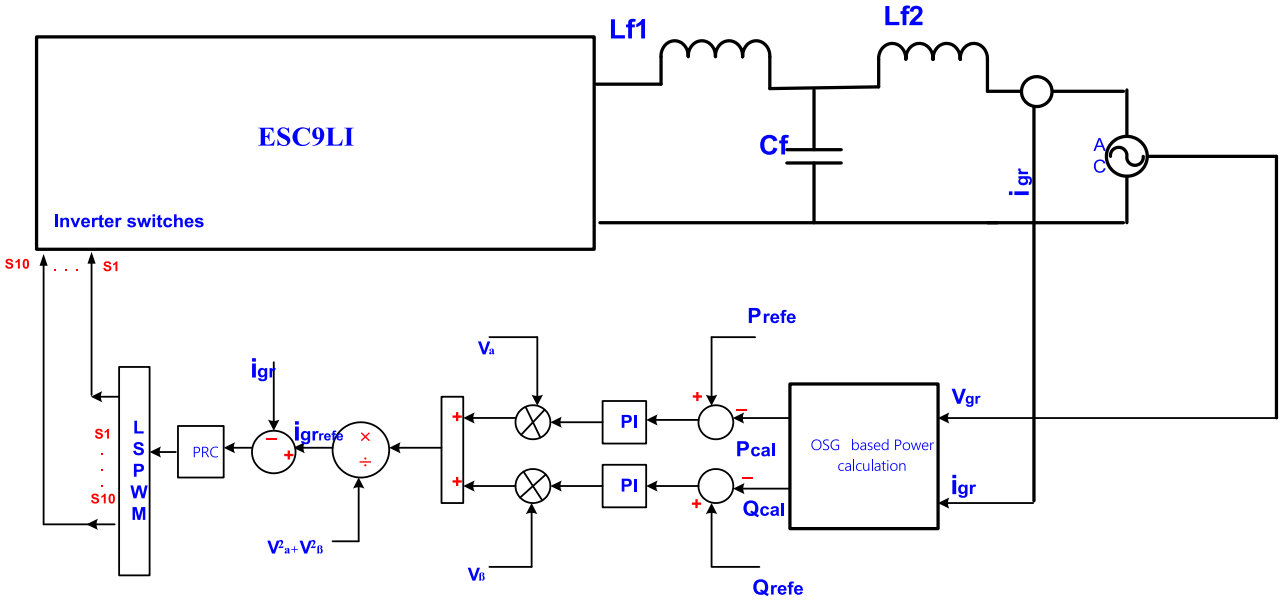

FIGURE 17. Closed loop control for inverter topology [24].

TABLE 5. Parameter and Specification Used Experimental Setup.

Input voltage	100 Vdc
Grid Voltage/Frequency	400V/50 Hz
Filter capacitor	2.2 μF
Filter inductors	1 mH, 0.5mH
Switch	FGA25N120 IGBT
Driver	TLP250
Real time controller	dSpace 1104

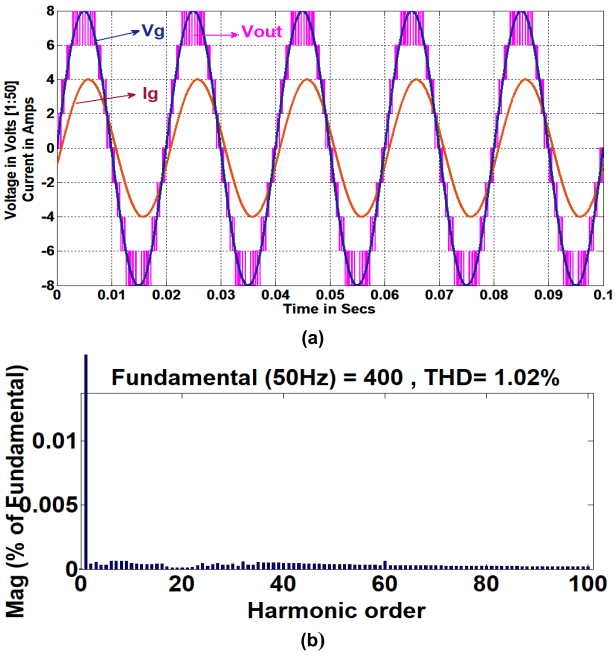

FIGURE 18. Simulation findings for Grid connected mode (a) MLI voltage, Grid Voltage and current wave forms (b) FFT plot of Grid voltage.

The control system, depicted in Figure 17, comprises an orthogonal signal generator (OSG) unit responsible for computing active and reactive power, two proportional-integral (PI) controllers, a grid current controller, and an LSPWM generation block that generates control pulses for the switching devices. The OSG system facilitates the calculation of active power (P) and reactive power (Q) for the proposed topology.

In adherence to the single-phase P-Q theory, the reference current for grid input can be generated by regulating the averaged active and reactive power. As these powers remain constant in a steady state, two PI controllers, as depicted in Figure 10, have been employed for their control. The OSG system plays a pivotal role in deriving the grid reference current. Various control methods, such as the conventional PI controller, repetitive controller (RC), proportional resonant controller (PRC), and deadbeat (DB) controller, can be adopted to control the grid current. These methods possess the capability to track reference signals without steady-state error. Given the superior performance of the PRC in tracking

$$i_{grrefe} = \frac{\left[(P_{\text{refe}} - P_{\text{cal}}) * G_p(s) * v_{gr\alpha} + (Q_{\text{refe}} - Q_{cal}) * G_q(s) * v_{gr\beta}\right]}{\left(v_\alpha^2 + v_\beta^2\right)} \tag{17}$$

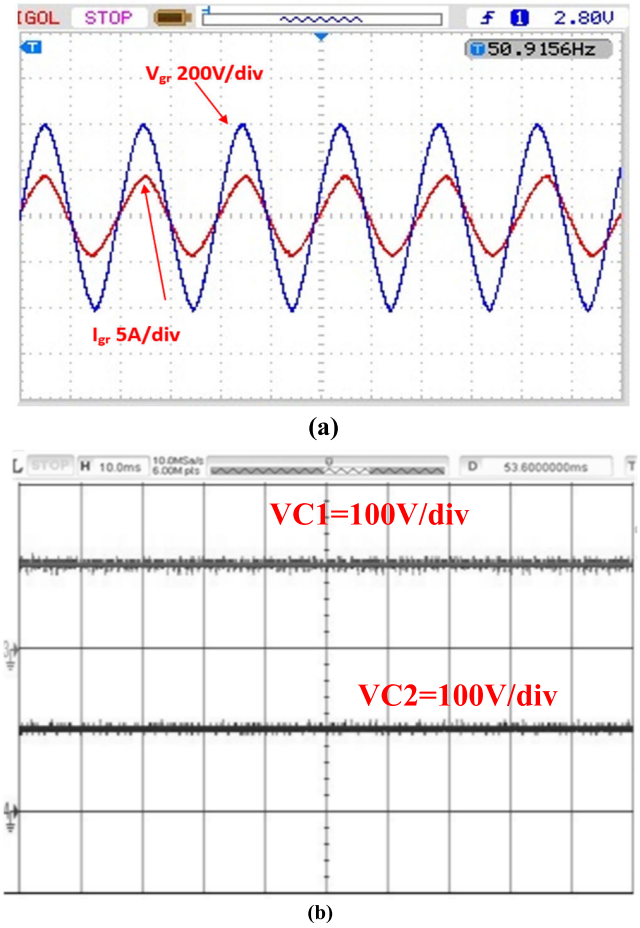

FIGURE 19. Experimental findings for Grid connected mode (a) Grid voltage and current wave forms (Ch1: 200 V/div, Ch2: 4 A/div). (b) Balanced Capacitor Voltages (VC1 and VC2) voltage.

reference signals, it has been chosen to govern the output current of the proposed topology. Consequently, the output of the PRC contributes to the design of an efficient PWM control system. Furthermore, the suggested system's performance under grid is tested and results of simulation and experimental conditions are presented in Figs. 18 and 19.

VI. CONCLUSION

In this work, an ESC9LI setup has been designed to generate the highest possible voltage with the fewest number of capacitors and switches and to mitigate the stress on the high-rated switches. A more efficient use of components allows the proposed design to provide more levels via a series-parallel conversion of the SC configuration. To accomplish capacitor voltage self-balancing, further circuitry is not required, and the control method is simple. The ESC9LI setup produces alternating current voltage by not employing polarity-generating H-bridges, that possess the largest BV. Additionally, switching shifts are kept to a minimum and there are only a maximum of four conducting switches allowed in each stage. Taking into account comparable topologies, comparative research is carried out, focusing on parameters such as component count, voltage gain, and voltage stress. Findings show that ESC9LI is superior to the other topologies considered. The proposed configuration uses fewer DC source and capacitors than the conventional inverter, enabling it to be expanded to higher voltage levels. Additionally, the ESC9LI configuration is a wise option for producing green power as well as high voltage. Several comparisons were done using various criteria to show that the suggested ESC9LI configuration is better than many of the other most newly reported configurations. The suggested ESC9LI setup surpassed the majority of existing configurations documented in the literature. Finally, simulation studies have shown the effectiveness of the suggested ESC9LI feature. In addition, the laboratory configuration proposed for ESC9LI was successfully implemented, and the outcomes computed using ESC9LI correspond to those estimated by simulation. The outcomes of the simulations and experiments confirm the system's applicability for real-time applications.

REFERENCES

[1] J. Liu, J. Wu, J. Zeng, and H. Guo, "A novel nine-level inverter employing one voltage source and reduced components as high-frequency AC power source," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2939–2947, Apr. 2017, doi: 10.1109/TPEL.2016.2582206.

[2] N. Sandeep and U. R. Yaragatti, "Operation and control of an improved hybrid nine-level inverter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5676–5686, Nov. 2017, doi: 10.1109/TIA.2017.2737406.

[3] S. S. Lee, "Single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8204–8207, Oct. 2018, doi: 10.1109/TPEL.2018.2805685.

[4] N. Sandeep, J. S. M. Ali, U. R. Yaragatti, and K. Vijayakumar, "Switched-capacitor-based quadruple-boost nine-level inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7147–7150, Aug. 2019, doi: 10.1109/TPEL.2019.2898225.

[5] M. D. Siddique, S. Mekhilef, N. M. Shah, N. Sandeep, J. S. Mohamed Ali, A. Iqbal, M. Ahmed, S. S. M. Ghoneim, M. M. Al-Harthi, B. Alamri, F. A. Salem, and M. Orabi, "A single DC source nine-level switched-capacitor boost inverter topology with reduced switch count," *IEEE Access*, vol. 8, pp. 5840–5851, 2020, doi: 10.1109/ACCESS.2019.2962706.

[6] Y. Nakagawa and H. Koizumi, "A boost-type nine-level switched capacitor inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6522–6532, Jul. 2019, doi: 10.1109/TPEL.2018.2876158.

[7] J. Liu, W. Lin, J. Wu, and J. Zeng, "A novel nine-level quadruple boost inverter with inductive-load ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4014–4018, May 2019, doi: 10.1109/TPEL.2018.2873188.

[8] J. S. Mohamed Ali and V. Krishnasamy, "Compact switched capacitor multilevel inverter (CSCMLI) with self-voltage balancing and boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4009–4013, May 2019, doi: 10.1109/TPEL.2018.2871378.

[9] M. D. Siddique, S. Mekhilef, N. M. Shah, J. S. M. Ali, M. Meraj, A. Iqbal, and M. A. Al-Hitmi, "A new single phase single switched-capacitor based nine-level boost inverter topology with reduced switch count and voltage stress," *IEEE Access*, vol. 7, pp. 174178–174188, 2019, doi: 10.1109/ACCESS.2019.2957180.

[10] M. J. Sathik, N. Sandeep, D. Almakhles, and F. Blaabjerg, "Cross connected compact switched-capacitor multilevel inverter (C^3-SCMLI) topology with reduced switch count," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 12, pp. 3287–3291, Dec. 2020, doi: 10.1109/TCSII.2020.2988155.

[11] Y. Zhang, Q. Wang, C. Hu, W. Shen, D. G. Holmes, and X. Yu, "A nine-level inverter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1659–1671, Feb. 2020, doi: 10.1109/TPEL.2019.2921015.

[12] S. A. Khan, D. Upadhyay, M. Ali, M. Tariq, A. Sarwar, R. K. Chakrabortty, M. J. Ryan, B. Alamri, and A. Alahmadi, "M-type and CD-type carrier based PWM methods and bat algorithm-based SHE and SHM for compact nine-level switched capacitor inverter," *IEEE Access*, vol. 9, pp. 87731–87748, 2021, doi: 10.1109/ACCESS.2021.3087825.

[13] S. Dhara and V. T. Somasekhar, "A nine-level transformerless boost inverter with leakage current reduction and fractional direct power transfer capability for PV applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7938–7949, Dec. 2022, doi: 10.1109/JESTPE.2021.3074701.

[14] S. Pal, M. G. Majumder, R. Rakesh, K. Gopakumar, L. Umanand, D. Zielinski, and A. R. Beig, "A cascaded nine-level inverter topology with T-type and H-bridge with increased DC-bus utilization," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 285–294, Jan. 2021, doi: 10.1109/TPEL.2020.3002918.

[15] A. Iqbal, M. D. Siddique, B. P. Reddy, and P. K. Maroti, "Quadruple boost multilevel inverter (QB-MLI) topology with reduced switch count," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7372–7377, Jul. 2021, doi: 10.1109/TPEL.2020.3044628.

[16] A. Srivastava and J. Seshadrinath, "A new nine level highly efficient boost inverter for transformerless grid connected PV application," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 1, no. 1, pp. 1–18, Dec. 2022, doi: 10.1109/JESTPE.2022.3210512.

[17] A. K. Singh, R. Raushan, R. K. Mandal, and Md. W. Ahmad, "A new single-source nine-level quadruple boost inverter (NQBI) for PV application," *IEEE Access*, vol. 10, pp. 36246–36253, 2022, doi: 10.1109/ACCESS.2022.3163262.

[18] K. Varesi, F. Esmaeili, S. Deliri, and H. Tarzamni, "Single-input quadruple-boosting switched-capacitor nine-level inverter with self-balanced capacitors," *IEEE Access*, vol. 10, pp. 70350–70361, 2022, doi: 10.1109/ACCESS.2022.3187005.

[19] M. Chen, Y. Yang, P. C. Loh, and F. Blaabjerg, "A single-source nine-level boost inverter with a low switch count," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2644–2658, Mar. 2022, doi: 10.1109/TIE.2021.3065609.

[20] R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera, Y. P. Siwakoti, and J. Pou, "Nine-level nine-switch common-ground switched-capacitor inverter suitable for high-frequency AC-microgrid applications," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 6132–6143, May 2022, doi: 10.1109/TPEL.2021.3131847.

[21] Z. Xun, H. Ding, Z. He, W. Zhou, and Y. Zheng, "A single-phase switched-capacitor nine-level inverter with reduced capacitance," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7410–7421, Dec. 2022, doi: 10.1109/JESTPE.2022.3186926.

[22] A. Hassan, X. Yang, and W. Chen, "Single and double input DC sources multilevel inverter topologies with reduced components counts and voltage boosting property for grid-connected photovoltaic converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7704–7720, Dec. 2022, doi: 10.1109/JESTPE.2022.3176810.

[23] M. Daula Siddique, M. Aslam Husain, A. Iqbal, S. Mekhilef, and A. Riyaz, "Single-phase 9L switched-capacitor boost multilevel inverter (9L-SC-BMLI) topology," *IEEE Trans. Ind. Appl.*, vol. 59, no. 1, pp. 994–1001, Jan. 2023, doi: 10.1109/TIA.2022.3208893.

[24] M. Islam, N. Afrin, and S. Mekhilef, "Efficient single phase transformerless inverter for grid-tied PVG system with reactive power control," *IEEE Trans. Sustain. Energy*, vol. 7, no. 3, pp. 1205–1215, Jul. 2016, doi: 10.1109/TSTE.2016.2537365.

[25] D. Kumar, R. Raushan, and S. Chakraborty, "A single source quadruple boost nine-level switched-capacitor inverter with reduced components and continuous input current," *IEEE Access*, vol. 12, pp. 52922–52933, 2024, doi: 10.1109/ACCESS.2024.3386747.

[26] G. Dhasharatha, M. H. Khan, and B. Mangu, "A novel nine-level quadruple boost inverter for electric vehicle applications," *IEEE Access*, vol. 12, pp. 60694–60704, 2024, doi: 10.1109/ACCESS.2024.3393846.

[27] S. A. Hosseini and K. Varesi, "Hybrid switched-capacitor 9-Level boost inverter," in *Proc. 12th Power Electron., Drive Syst., Technol. Conf. (PEDSTC)*, Tabriz, Iran, Feb. 2021, pp. 1–4, doi: 10.1109/PEDSTC52094.2021.9405886.

[28] R. Sreedhar, K. Karunanithi, P. Chandrasekar, and R. B. Teja, "Nearest space-vector control strategy for high-resolution multilevel inverters," in *Proc. 6th Int. Conf. Converg. Technol.*, 2021, pp. 1–26.

[29] R. B. Teja, S. Baskar, G. N. Rao, and R. Sreedhar, "Multi-level inverter with reduced switch count and DC source," in *Proc. 2nd Int. Conf. Intell. Technol.*, 2022, pp. 1–24.

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