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RESEARCH ARTICLE

X-Band Harmonic-Tuned High Power and Efficiency GaN HEMT Oscillator IC

YEONGMIN JANG[1], WONSEOK CHOE[2], (Member, IEEE), MINCHUL KIM[2], (Member, IEEE), AND JINHO JEONG[1], (Member, IEEE)

[1]Department of Electronic Engineering, Sogang University, Seoul 04107, South Korea

[2]MMII Laboratory, Seoul 05854, South Korea

Corresponding author: Jinho Jeong (jjeong@sogang.ac.kr)

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ABSTRACT An *X*-band harmonic-tuned oscillator integrated circuit (IC) with high power and efficiency is presented, utilizing gallium nitride (GaN) high electron mobility transistor (HEMT). It consists of a feedback and load network to provide optimal harmonic impedances while satisfying the oscillation condition at the fundamental frequency. The feedback network is synthesized from harmonic load-pull simulations and further simplified into a circuit comprising capacitors and transmission line, eliminating the inductors. This modification serves to reduce losses, which in turn improves output power and efficiency, while also reducing circuit area. The feedback network incorporates parallel resonant shunt stubs to enhance frequency selectivity and facilitate harmonic impedance matching, while also serving as a bias circuit. The oscillator, fabricated using a 250-nm GaN HEMT process, achieves a high output power of 35.0 dBm delivered to the load at 10.5 GHz, demonstrating a remarkable efficiency of 48.9% and excellent phase noise at −124.9 dBc/Hz with a 1 MHz offset. These results indicate a significant improvement in power and efficiency compared to previous *X*-band watt-level GaN oscillator ICs.

INDEX TERMS GaN HEMT, high efficiency, microwave oscillator, phase noise, power oscillator.

I. INTRODUCTION

An *X*-band (8-12 GHz) is an attractive frequency range for applications including satellite, optical communications, radars, and radio detection [1], [2]. High-power and high-efficiency oscillator is an essential circuit block for these applications converting DC to RF signal. Microwave oscillators are commonly designed using advanced transistor technologies such as gallium arsenide (GaAs), silicon germanium (SiGe), and indium phosphide (InP) heterojunction bipolar transistors (HBTs) [3], [4], [5], [6], [7]. This is because HBTs inherently have a lower flicker noise corner frequency compared to filed effect transistors (FETs), leading to better phase noise performance [8]. However, these technologies have a low breakdown voltage, making it difficult to achieve high output power. As a result, additional buffer amplifiers are needed, which increase the overall system cost and reduce reliability [9].

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Recently, gallium nitride (GaN) technology has attracted significant interest in microwave integrated circuits (MMICs) due to its high gain and high power. Especially, GaN on silicon carbide (SiC) offers an excellent thermal conductivity, making it an attractive choice for high-power applications. The high output power of GaN-based oscillators can directly enhance the signal-to-noise ratio according to Leeson's equation, thereby improving phase noise performance [10], [11]. Furthermore, high-power oscillators can eliminate the need for a power amplifier. Therefore, GaN transistors can be a good choice for high-power and high-efficiency microwave oscillator with good phase noise [12].

There have been numerous research efforts designing microwave high-power and high-efficiency oscillator using GaN transistors [12], [13], [14]. In [12] and [13], GaN power oscillators have been developed, employing a common-gate FET with inductive feedback to generate negative resistance. In [12], the oscillator produced an output power of 1.7 W with an efficiency of 16% at 9.556 GHz. A Colpitts oscillator using a GaN HEMT with a field plate achieved an efficiency

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of 21.5% and an output power of 1.9 W at 5 GHz [14]. In summary, many X-band watt-level GaN oscillator ICs have been developed; however, achieving high efficiency exceeding 40% has proven challenging at this frequency band.

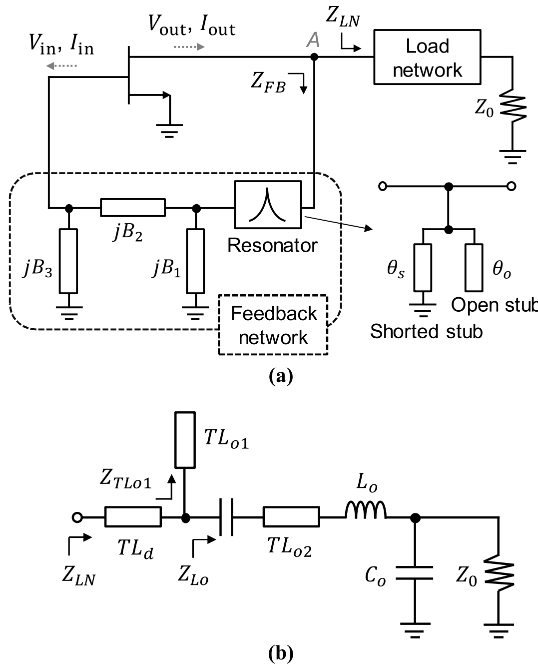


FIGURE 1. Design of a harmonic-tuned oscillator. (a) Block diagram of a harmonic-tuned oscillator. (b) Circuit schematic of a load network.

Switching-mode oscillators have been commonly adopted to achieve high efficiency [15], [16], [17]. In [15], a class-E load network with finite DC-feed inductance was utilized to achieve an efficiency of 53% and an output power of 0.3 W at 2.5 GHz. However, a class-E or switching oscillator is not suitable for high-efficiency operation at X-band or higher frequencies due to the increased switching losses, degrading output power or efficiency [18].

The harmonic-tuned oscillator has been reported to achieve high power and high efficiency [19], [20], [21]. In [21], a discrete GaN HEMT was employed in the design of a harmonic-tuned oscillator, achieving a high output power of 37.8 dBm and a high efficiency of 83% at 2.45 GHz. However, there is limited research on high-power and high-efficiency oscillators using harmonic tuning technique at higher frequencies like the X-band. This is due to the increased difficulty of simultaneously designing impedance matching circuits for both the fundamental and harmonic frequencies at these higher frequencies. The use of discrete transistors exacerbates these difficulties due to parasitic elements from packaging and circuit boards.

In this work, a harmonic tuning technique is applied to design an X-band oscillator integrated circuit (IC). The feedback-type oscillator is constructed by adding a feedback loop from the drain to the gate of the harmonic-tuned common-source amplifier to meet the oscillation condition. To achieve high-power and high-efficiency in IC, the feedback network is synthesized based on harmonic load-pull simulations, followed by network transformations to eliminate large and low-quality factor on-chip inductors. Additionally, a parallel resonant shunt stub (PRSS) is incorporated to enhance frequency selectivity of the feedback network and to facilitate harmonic impedance matching, also serving as a bias circuit. The designed feedback and load networks ensure optimal harmonic impedances for power and efficiency, while meeting an oscillation condition at the fundamental frequency. Section II discuss the design of harmonic-tuned oscillator, followed by the measurement results in section III.

II. DESIGN OF HARMONIC-TUNED OSCILLATOR

Harmonic-tuned oscillator IC with high-power and high-efficiency was designed using a 250-nm GaN HEMT process from WIN Semiconductors Corp., Taiwan [22]. This process offers high-performance transistors with transit and maximum oscillation frequency of 25 and 82 GHz, respectively. The drain-to-gate breakdown voltage is as high as 120 V. Additionally, it also provides a 100 μm-thick SiC substrate with high thermal conductivity which is highly beneficial for the operation of a high-power oscillator. The SiC substrate has a dielectric constant of 9.7 and a loss tangent of 0.003. To achieve high output power, we use a transistor with a total gate width of 800 μm (4 finger × 200 μm) including three individual source vias (ISVs), which reduces the impact of source degeneration. The transistor is biased in deep class AB to increase efficiency, with the drain voltage set to 25 V.

A. OPTIMAL HARMONIC IMPEDANCE OF TRANSISTOR

Fig. 1(a) shows the block diagram of the designed harmonic-tuned oscillator, consisting of a transistor, feedback, and load network. The input signal at the gate is amplified by the transistor and returns to the gate via a feedback network, so that the circuit can oscillate when the loop gain is greater than unity at the oscillation frequency $f_0 = 10$ GHz. In addition, the feedback network, together with load network, provides the optimal impedances to the drain at harmonic frequencies, enabling high power and efficiency.

At first, the optimum load impedances of the transistor for maximum power and efficiency are determined from the harmonic load-pull simulations as follows: $Z_{Lopt1} = 15 + j30\ \Omega$ at f_0, $Z_{Lopt2} = -j25\ \Omega$ at $2f_0$, and $Z_{Lopt3} = j5\ \Omega$ at $3f_0$, respectively. The source impedance at f_0 is determined to be $Z_{Sopt1} = 15 + j\ 5\ \Omega$ through source-pull simulation. The source impedances at $2f_0$ and $3f_0$ were not considered as they have a negligible impact on the power and efficiency. Then, a harmonic-tuned power amplifier is constructed by terminating the transistor with the optimal source and load impedances determined above. The simulation demonstrates that it can deliver an output power (P_{out}) of 36.3 dBm and power added efficiency (PAE) of 76.0% for an available source power (P_{avs}) of 27 dBm at f_0. The fundamental voltage and current at the gate and drain (V_{in}, I_{in}, V_{out}, and I_{out} in Fig. 1(a)) can be obtained at this P_{out} and utilized to construct

the feedback and load network at f_0 consisting of reactive (B_1, B_2, and B_3) and conductive (G_1) elements [21].

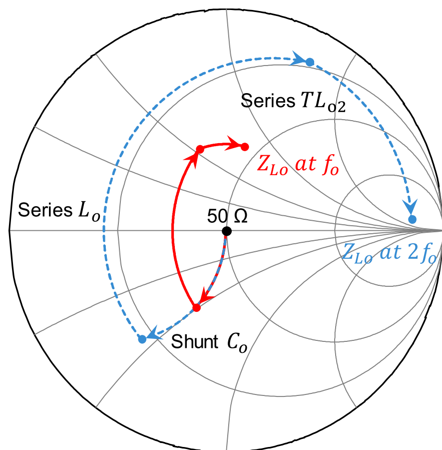


FIGURE 2. Load impedance trajectory at f_0 (solid) and $2f_0$ (slotted).

The calculated values are $B_1 = -7.9$ mS, $B_2 = -16.7$ mS, $B_3 = 18.1$ mS, and $1/G_1 = R_1 = 77\ \Omega$. In Fig. 1(a), the reactive elements (B_1, B_2, and B_3) are implemented with π-type feedback network and the conductive element (G_1) is reflected in the load network (Z_{LN}). In this way, the feedback and load network enable the impedance matching at both the gate and drain of the transistor at f_0 for high power and efficiency.

B. DESIGN OF LOAD NETWORK

Basically, the load network is designed to present the optimum impedances (R_1, Z_{Lopt2}, and Z_{Lopt3} at f_0, $2f_0$, and $3f_0$, respectively). For the impedance matching at $2f_0$ and $3f_0$, the $\lambda/12$-long open stub TL_{o1} is employed as shown in Fig. 1(b). Its input impedance Z_{TLo1} is $-j28.9\ \Omega$ at $2f_0$ and a short circuit at $3f_0$. Then, the open stub TL_{o1}, together with a very short 2°-transmission line TL_d, enables the optimum impedance matching at harmonic frequencies. Specifically, Z_{LN} equals $-j24.4\ \Omega$ at $2f_0$, assuming Z_{Lo} is infinite at $2f_0$, and $j5.3\ \Omega$ at $3f_0$. These values are very close to Z_{Lopt2} and Z_{Lopt3}, respectively.

The remaining load network (the Z_{Lo} part in Fig. 1(b)) is designed to provide the optimum impedance matching, satisfying $Z_{TLo1}||Z_{Lo} = R_1$, that is, $Z_{Lo} = 43.0 + j38.2\ \Omega$ at f_0. In addition, Z_{Lo} should be very high impedance at $2f_0$. To meet these impedance conditions for Z_{Lo}, it is designed using a series transmission line (TL_{o2}), series inductor (L_o), and a shunt capacitor (C_o), as shown in Fig. 1(b). Impedance matching is accomplished at f_0 by selecting the element values as $C_o = 255$ fF, $L_o = 810$ pH, and a 15° transmission line with characteristic impedance of $Z_o = 50\ \Omega$. Fig. 2 illustrates the Z_{Lo} trajectory from 50 Ω by C_o, L_o, and TL_{o2} at f_0 and $2f_0$. This matching network allows a considerably high impedance of $562.1 + j205.1\ \Omega$ at $2f_0$.

As a results, the designed load network provides the optimum impedances at f_0, $2f_0$, and $3f_0$ frequencies for maximum power and efficiency.

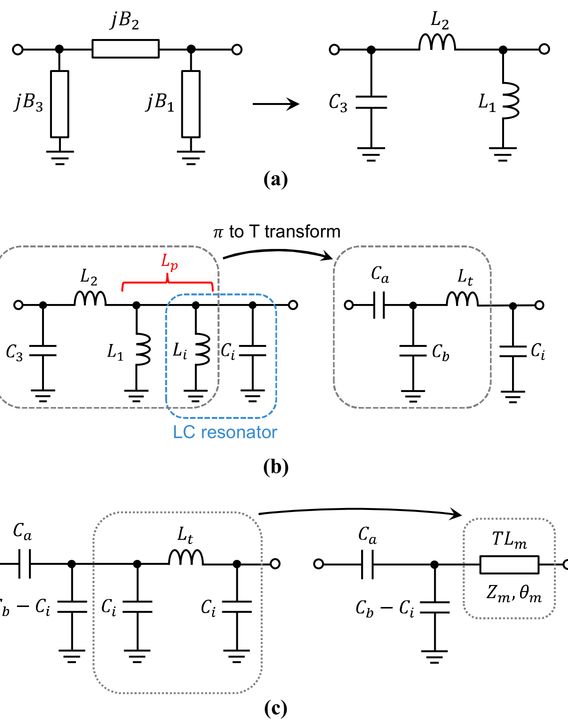


FIGURE 3. Design of feedback network. (a) Implementation of feedback network using lumped elements. (b) π-to-T transformation. (c) Transformation from π-network to transmission line. (d) Simulated inductance (L_t and L_e) and capacitance (C_e) as a function of characteristic impedance (Z_m).

C. DESIGN OF RESONATOR

A resonator is utilized within the feedback network to selectively pass the oscillation signal at f_0 while rejecting harmonic components, as illustrated in Fig. 1(a). The transmission line-based microstrip resonator facilitates a straightforward implementation of harmonic impedance matching, granting improved control over the desired harmonic attributes compared to on-chip LC resonators. In this study, parallel resonant shunt stubs (PRSS) are utilized for the resonator, where open- and shorted-stubs with electrical length of $\theta_s = \theta_o = 45°$ are connected in parallel, and they are shunt with the signal line, as depicted in Fig. 1(a). The two stubs present the same admittance with opposite sine, and thus zero admittance at f_0,

so that it functions as an open circuit [23]. They present short impedances at both DC due to shorted stub and $2f_0$ due to open stub. The PRSS exhibits a narrower passband and better frequency selectivity (a 42.9% higher Q-factor), compared to the conventional band-pass filtering stub such as the shunt 90°-long shorted stub with characteristic impedance of 50 Ω. It also offers a more flexible and compact layout. Finally, the PRSS can also serve as a bias circuit, which will be explained later.

D. DESIGN OF FEEDBACK NETWORK

The feedback network is designed to implement the reactive components (B_1, B_2, and B_3), which can be realized using lumped elements: $L_1 = 2028.3$ pH, $L_2 = 954.1$ pH, and $C_3 = 288.3$ fF, as shown in Fig. 3(a). However, the inductance L_1 is too large to be integrated on-chip, which also introduces significant parasitic resistance and capacitance. This leads to a decrease in output power and efficiency, and the Q-factor of the feedback network, degrading phase noise performance. Additionally, it will exhibit a low self-resonant frequency, which can be problematic in achieving the desired impedance at harmonic frequencies.

To alleviate this drawback, it is useful to reduce the value and number of the required inductors. For this purpose, the original π-type feedback network in Fig. 3(a) is converted to T-network. Initially, an LC parallel resonator, consisting of L_i and C_i, is connected in shunt with L_1, as shown in Fig. 3(b). Then, the shunt inductor, $L_i = 1/\omega_0^2 C_i$, is combined with L_1 to create a single inductor, $L_p = L_1 || L_i$.

The resultant π-network consisting of C_3, L_2, and L_p is converted into a T-network represented by C_a, C_b, and L_t which are given as follows:

$$C_a = C_3\left(1 + \frac{L_p}{L_2}\right) - \frac{1}{\omega_o^2 L_2}, \quad (1a)$$

$$C_b = C_3\left(1 + \frac{L_2}{L_p}\right) - \frac{1}{\omega_o^2 L_p}, \quad (1b)$$

$$L_t = \left(\frac{1}{L_2} + \frac{1}{L_p} + \frac{1}{\omega_o^2 C_3 L_2 L_p}\right)^{-1}. \quad (1c)$$

Note that these values are all dependent on C_i. Next, we decompose the shunt capacitor C_b into two capacitors of $C_b - C_i$ and C_i in parallel, as illustrated in Fig. 3(c). Then, the π-network, consisting of a series L_t and two shunt capacitors C_i's, can be transformed into a transmission line (TL_m) with a characteristic impedance Z_m and electrical length θ_m [24]. Therefore, the final T-type feedback network consists of two capacitors and a single transmission line, without an inductor.

In this study, θ_m, the electrical length of TL_m, is selected to be 50° and this line is divided into two segments, TL_{m1} of 5° and TL_{m2} of 45° line, as shown in Fig. 4. Then, the PRSS (TL_{op} and TL_{sh} with C_{B1}) is connected to the junction B between TL_{m1} and TL_{m2}. Recall that the feedback network should present an infinite impedance at $2f_0$ to the node A (Z_{FB}) for the harmonic impedance matching at the drain. This is achieved by this 45°-long TL_{m2} line which functions as a λ/4 long line at $2f_0$. Therefore, it presents infinite impedance to the node $A(Z_{FB})$ at $2f_0$, because the junction B is short-circuited due to the 45°-long open stub TL_{op} at f_0.

Finally, we determine the characteristic impedance Z_m of the transmission line TL_m under the condition of $\theta_m = 50°$. The equivalent inductance L_e and capacitance C_e of the transmission line TL_m are determined by the following equations [24].

$$L_e = \frac{Z_m}{\omega_o} \sin\theta_m, \quad (2a)$$

$$C_e = \frac{1}{\omega_o Z_m} \frac{1 - \cos\theta_m}{\sin\theta_m}. \quad (2b)$$

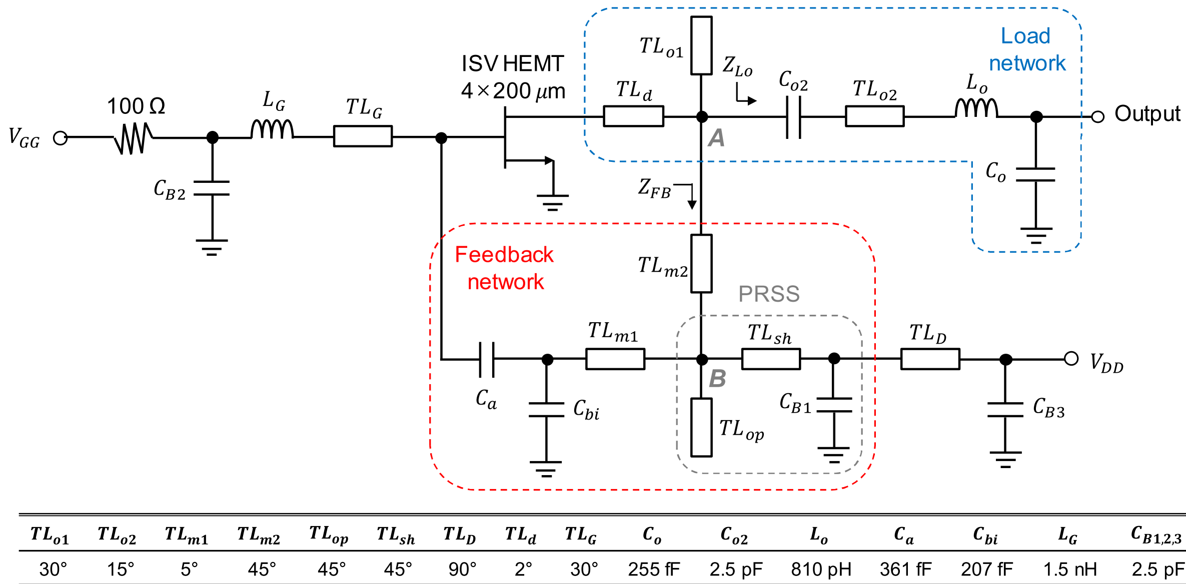
Fig. 3(d) shows the calculated L_e and C_e as a function of Z_m using (2). In this figure, L_t is also included which is calculated as follows: C_i is substituted with the computed C_e as a function of Z_m, and the resulting L_p is then used in (1c) to compute L_t. Therefore, we can determine Z_m to be 73.3 Ω in this figure, at which L_e equals L_t (marked by a dot), thus enabling the transformation of the π-network into the transmission line as shown in Fig. 3(c). L_e and C_i are determined to be 894.0 pH and 101.2 fF, respectively, at $f_o = 10$ GHz.

E. FINAL DESIGN OF HARMONIC-TUNED OSCILLATOR

Fig. 4 depicts the final design of the harmonic-tuned oscillator with the parameter values. The PRSS presents infinite impedance and thus does not impact the circuit operation at f_0. The shorted stub in the PRSS is realized using the transmission line (TL_{sh}) and the RF capacitor (C_{B1}), serving to apply the drain bias as well. Additional short-circuited λ/4 long line (TL_D and C_{B3}) is employed to minimize the effect of the bias line impedance. The RF choke in the gate bias line is established through a combination of a spiral inductor (L_G) and an additional line (TL_G) for compact circuit integration.

Fig. 5(a) presents the simulated voltage and current waveforms at the intrinsic drain of the transistor as shown in Fig. 4, operating a deep class AB bias condition with a drain voltage of 25 V and a quiescent current of 17.8 mA. It is worthwhile to emphasize that the voltage and current waveforms in class B mode, as illustrated by the load-line in Fig. 5(b), resemble a sine wave and half-sine waveforms, respectively, with minimal overlap. This results in a high efficiency of 77.3% with a high output power of 36.2 dBm delivered to the load. Ideal circuit components without any losses were used in the simulation. Note that this performance is very close to that obtained from the harmonic-tuned power amplifier, demonstrating that the feedback and load networks were properly designed to provide optimum load and source impedances to the transistor.

In the actual layout, the lines in Fig. 4 were implemented using microstrip lines with the signal strip consisting of two gold layers of a total thickness of 5.1 μm. The spiral inductor in the load network was designed with a narrow line width of 20 μm to achieve a sufficiently high self-resonance frequency, leading to increased losses. In addition, the length of



TL_{o1}	TL_{o2}	TL_{m1}	TL_{m2}	TL_{op}	TL_{sh}	TL_D	TL_d	TL_G	C_o	C_{o2}	L_o	C_a	C_{bi}	L_G	$C_{B1,2,3}$
30°	15°	5°	45°	45°	45°	90°	2°	30°	255 fF	2.5 pF	810 pH	361 fF	207 fF	1.5 nH	2.5 pF

FIGURE 4. Designed harmonic-tuned oscillator.

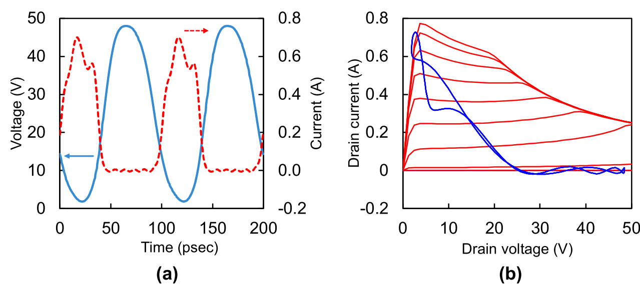


FIGURE 5. Simulated waveforms and load-line of the designed oscillator at 10 GHz. (a) Intrinsic drain voltage and current waveforms. (b) Intrinsic load-line trajectory.

TL_d should be slightly increased in the layout, because four components (TL_d, TL_{m2}, TL_{o1}, and C_{o2}) with finite size must be connected at a single node A. This results in an increase in the oscillation frequency by 0.2 GHz and a slight change in the impedance seen from the drain. Consequently, the electromagnetic (EM) simulation reveals a total reduction of 1.7 dB in the output power compared to the circuit simulation using ideal components, resulting in an output power of 34.5 dBm and a drain efficiency of 52.9%.

III. MEASUREMENT RESULTS

The designed oscillator was fabricated using a 250-nm GaN HEMT process. Fig. 6(a) shows the photograph of the fabricated IC with an overall size of 2.4 mm × 1.4 mm. The oscillator IC was mounted on a copper plate with a high thermal conductivity to ensure efficient heat dissipation. External bias circuits were implemented on an FR-4 PCB, including bypass capacitors and resistors for the regulation of DC biases and enhancement of circuit stability. Fig. 6(b) illustrates the on-wafer measurement setup. Output power and spectrum were measured using the power meter (Agilent's U8485A) and the spectrum analyzers (Keysight's E4407B and Anritsu's MS2830A), respectively.

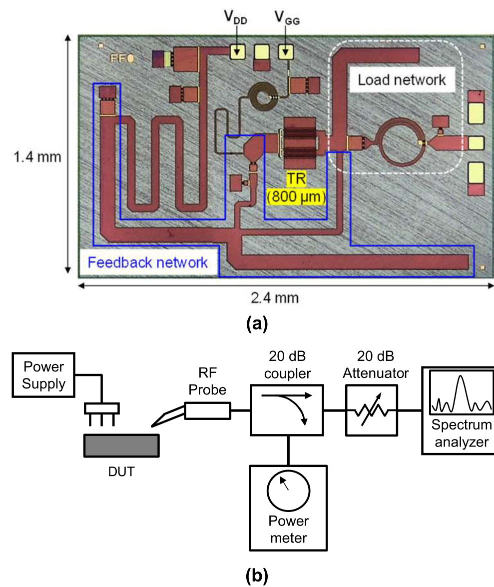


FIGURE 6. Fabricated harmonic-tuned oscillator IC. (a) Photograph of the fabricated oscillator IC. (b) On-wafer measurement setup.

Fig. 7 presents the measured results for output power, oscillation frequency, and drain efficiency of the oscillator across a drain voltage range from 21 V to 29 V. The oscillation frequency varies between 10.36 to 10.57 GHz, depending on the drain voltage, with high efficiency exceeding 46.2%. The measured oscillation frequency closely matches the EM simulation results, with an increase of ∼0.2 GHz. This difference can be predicted by slightly adjusting the parasitic inductance

TABLE 1. Comparison of published X-band GaN oscillators.

	Process	Topology	f_{osc} (GHz)	P_{out} (dBm)	DE (%)	Gate width (μm)	Chip size (mm×mm)	PN (dBc/Hz) 100 kHz	PN (dBc/Hz) 1 MHz	Power density (W/mm)	FoM (dBc/Hz)
[9]	250 nm GaN HEMT	Hartley	7.9	21	8.6	800	1.1×0.6	-112	-135	0.16	-223.30
[11]	250 nm GaN HEMT	Balanced colpitts	9.92	-6	0.14	800	N/A	N/A	-136	~0	-181.39
[12]	250 nm GaN HEMT	Common gate	9.556	32.3	16	1500	1.6 mm^2	-87	-115	1.13	-218.95
[16]	250 nm GaN HEMT	Class E	9.348-9.46	27.89	27.86	400	2×1.5	N/A	-121.62	1.54	-223.38
[26]	250 nm GaN HEMT	Feedback	7.26	1.06	7	N/A	2×1	N/A	-122.48	N/A	-189.21
[27]	AlGaN/GaN	Colpitts	9.11-9.55	*3.3	*7	100	1.2×1.05	-82	-110	0.03	-181.15
[28]	AlGaN/GaN	Inductive feedback	8.5-9.5	35	**~16	1500	1.6×1.6	*-77	*-101	2.11	-207.13
[29]	AlGaN/GaN	Balanced colpitts	9.1	6	0.66	320	1.8×1.5	-101	**~-130	0.01	-193.38
This work	250 nm GaN HEMT	Harmonic tuning	10.5	35	48.9	800	2.4×1.4	-91.7	-124.9	3.95	-237.22

* the mean value
**~ approximate value read from graphs

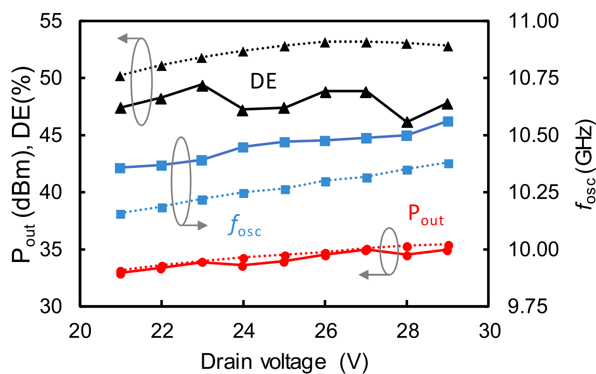
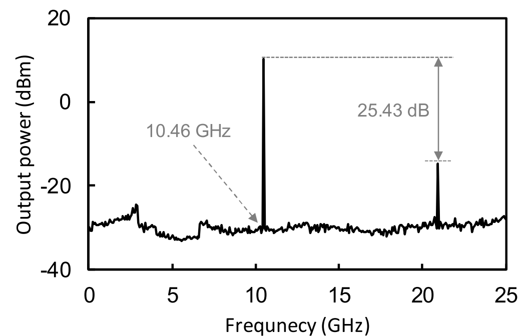


FIGURE 7. Measured (solid) and simulated (dotted) output power (P_{out}), drain efficiency (DE), and oscillation frequency (f_{osc}), according to drain voltage.

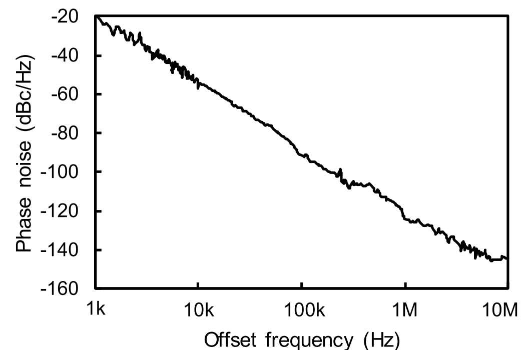
of the transistor in simulation. The average output power from 21 to 29 V was measured to be 34.1 dBm, corresponding to a 0.4 dB decrease compared to the EM simulation. This reduction in output power entails the reduction in efficiency from 52.3% in the EM simulation to 47.9%. The highest efficiency of 49.4% is achieved at a drain bias of 23 V, with an output power of 33.9 dBm at an oscillation frequency of 10.38 GHz. The maximum output power of 35.4 dBm is achieved at a drain voltage of 30 V, with an efficiency of 48.4%. At 27 V, output power is measured to be 35.0 dBm with an efficiency as high as 48.9%. The oscillation frequency was tuned from 10.465 to 10.490 GHz by varying the gate bias voltage from −2.6 to −1.4 V.

Fig. 8 shows the output spectrum of the oscillator measured at a drain voltage of 27 V. As shown in Fig. 8(a), the oscillator exhibits high 2nd harmonic suppression of 25.4 dB, compared to the fundamental power. Fig. 8(b) depicts the measured phase noise performance with a $1/f^3$ phase noise corner frequency of approximately 7 MHz. It shows −91.7 dBc/Hz and −124.9 dBc/Hz at 100 kHz and 1 MHz offsets, respectively. This phase noise performance is comparable to previously reported SiGe oscillators (−126 ∼ −120 dBc/Hz at 1 MHz offset) [3], [4], [5], while providing significantly higher output power.

Table 1 provides the performance comparison among various high-power and high-efficiency GaN oscillator ICs



(a)



(b)

FIGURE 8. Measured output spectrum of the oscillator IC at a drain voltage of 27 V. (a) Output spectrum. (b) Phase noise performance.

operating around 10 GHz. The oscillator IC developed in this work achieves high output power exceeding 35.0 dBm with a remarkable efficiency of 48.9%, representing a more than 20% improvement compared to previous works, as depicted in Fig. 9. Moreover, this output power is achieved from the transistor with an 800 μm gate width, resulting in a maximum power density of 3.95 W/mm, one of the highest power densities in the table. The performance of oscillator ICs can be compared using the figure of merit (FoM) according to the following equation:

$$\mathrm{FoM} = PN - 20\log\left(\frac{f_{osc}}{\Delta f}\right) - 10\log\eta - 10\log\left(\frac{P_{out}}{1mW}\right) \quad (3)$$

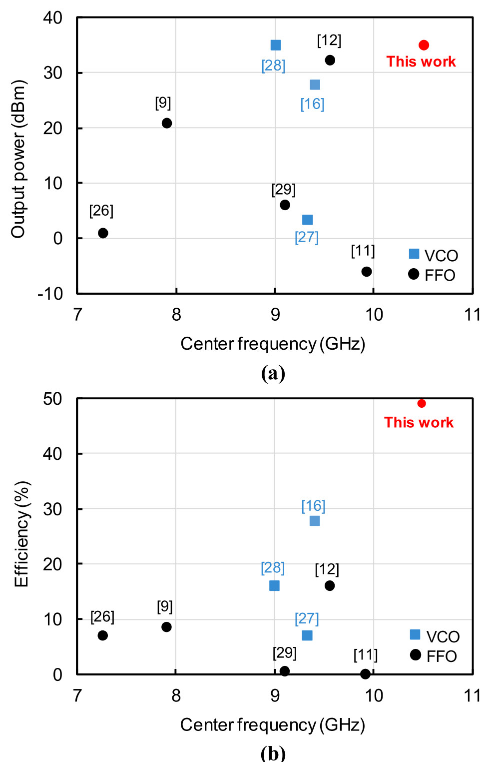


FIGURE 9. Comparison of published GaN oscillators operating around 10 GHz. (a) Output power versus frequency. (b) Efficiency versus frequency. Circle: fixed-frequency oscillator, square: voltage-controlled oscillator.

where PN is the measured phase noise at offset frequency Δf of 1 MHz, f_{osc} is the oscillation frequency, and η is the drain efficiency [25]. The FoM for the fabricated oscillator IC in this work is calculated to be −237.22 dBc/Hz, corresponding to the best performance among those listed in Table 1.

IV. CONCLUSION

In this paper, an X-band harmonic-tuned oscillator IC was designed for high-power and high-efficiency operation. The feedback and load network were designed to provide optimal harmonic impedances while satisfying the oscillation condition at the fundamental frequency. The synthesized feedback network was modified through a π-to-T transformation, followed by a conversion to a transmission line, resulting in a simplified network without inductors, reducing circuit area and enhancing power and efficiency. The fabricated oscillator IC in a 250-nm GaN HEMT process achieved excellent performance, including a high output power of 35.0 dBm and an efficiency of 48.9% at the X-band. It can be applied to on-off keying communications, pulsed radars, and wireless power transfer. To expand its applications, frequency-tuning elements can be included in the proposed oscillator to design a voltage-controlled oscillator (VCO). Future research will focus on designing a VCO by incorporating a varactor into the PRSS.

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YEONGMIN JANG received the B.S. degree in electrical engineering from Dong-A University, Busan, South Korea, in 2020. He is currently pursuing the Ph.D. degree in electronic engineering with Sogang University, Seoul. His research interests include monolithic microwave integrated circuits, THz integrated circuits, and wireless power amplifier.

WONSEOK CHOE (Member, IEEE) was born in Daegu, South Korea, in 1985. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from Sogang University, Seoul, South Korea, in 2012, 2014, and 2019, respectively. In 2019, he was a Co-Founder at the MMII Laboratory Corporation, an RF front-end IC design house, Seoul. The MMII Laboratory designs gallium arsenide (GaAs-), gallium nitride (GaN-), and silicon germanium (SiGe)-based RF front-end monolithic microwave integrated circuits (MMICs) and discrete circuits for sub-6GHz handset, low earth orbit (LEO) satellite, mm-wave, and 6G communication and radar.

MINCHUL KIM (Member, IEEE) was born in Seoul, South Korea, in 1987. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Hanyang University, Ansan, South Korea, in 2012, 2014, and 2019, respectively. In 2019, he was a Co-Founder with the MMII Laboratory Corporation, an RF front-end IC design house, South Korea. The MMII Laboratory designs GaAs-, GaN-, and SiGe-based RF front-end monolithic microwave integrated circuits (MMICs) and discrete circuits for sub-6GHz handset, LEO satellite, mm-wave, and 6G communication and radar.

JINHO JEONG (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1997, 1999, and 2004, respectively. From 2004 to 2007, he was with the University of California at San Diego, La Jolla, CA, USA, as a Postdoctoral Scholar, where he was involved with the design of high-efficiency and high-linearity RF power amplifiers. In 2007, he joined the Department of Electronics and Communications Engineering, Kwangwoon University, Seoul. Since 2010, he has been with the Department of Electronic Engineering, Sogang University, Seoul. His research interests include monolithic microwave integrated circuits (MMICs), THz integrated circuits and waveguide modules, microwave non-linear circuits (power amplifiers and oscillators), and wireless power transfer.