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RESEARCH ARTICLE

Ka-Band CMOS Stacked-FET Power Amplifier With Pre-Distorted Driver Stage for 5G Applications

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ABSTRACT In this study, we proposed a pre-distorted driver of a power amplifier in which the driver stage can serve as a pre-distorter of the power stage. In order to secure the linearity of the power amplifier, AM-PM distortions according to the input power of the common-source (CS) and two stacked-FET structures were analyzed and compared with the simulated results. Based on the analyzed AM-PM distortions of the two structure, it was verified that the driver stage with CS structure can act as a pre-distorter of the power stage with the two stacked-FET structure by optimizing the bias voltages of the two structures. The Ka-band power amplifier was designed with a 65-nm CMOS process to verify the feasibility of the proposed pre-distorted driver stage. At 28 GHz, the measured P_{1dB}, saturated output power (P_{SAT}), and peak power-added efficiency (PAE) were 18.6 dBm, 19.7 dBm, and 32.9%, respectively. The measured small signal gain was 24.1 dB. When 5G-NR modulation signals (64-QAM, 100-Msym/s, 9.7-dB PAPR) were used, under conditions where the EVM was less than –25 dB, the measured output power and ACLR were 13.3 dBm and –29.4 dBc, respectively.

INDEX TERMS AM-PM distortion, CMOS, driver stage, pre-distortion, stacked-FET.

I. INTRODUCTION

Power amplifiers are traditionally one of the most actively studied circuits in wireless communication systems. In particular, with the introduction of 5G mobile communication technology using beamforming systems, CMOS power amplifiers operating in the millimeter wave band have also been actively studied recently, considering the integration level of multi-channel RF transceiver [1], [2], [3]. However, the low breakdown voltage and lossy Silicon substrate of CMOS process are obstacles to securing the output power and efficiency of the CMOS power amplifier. These performance degradations worsen as the operating frequency increases, especially like Ka-band, which is mainly used by 5G mobile communications.

Accordingly, various studies on CMOS power amplifiers were introduced to overcome the disadvantages of the CMOS process and improve output power and efficiency [4], [5], [6]. In particular, the stacked-FET power amplifier is recognized as one of the useful structures that can overcome the low breakdown voltage of CMOS and improve output power [7]. Therefore, various studies have been conducted on the stacked-FET power amplifier, such as optimization technique of external capacitors connected to the gate node of stacked-FETs, capacitive neutralization technique, and internal matching technique [7], [8], [9], [10], [11], [12]. Consequently, the output power of the stacked-FET power amplifier is continuously and successfully improved.

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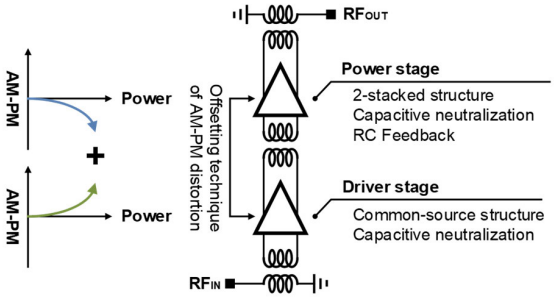

FIGURE 1. Conceptual diagram of the proposed power amplifier with pre-distorted driver.

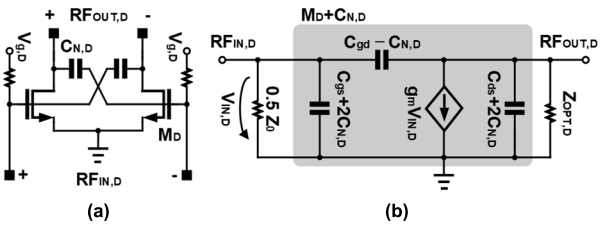

FIGURE 2. Designed driver stage: (a) schematic and (b) equivalent circuit.

Although there are relatively few studies to improve linearity compared to the research on the output power improvement technique of CMOS power amplifier, recently research on linearity improvement technique has also become active as the output power improvement technique has matured [13], [14], [15]. In general, there are various techniques such as RC-feedback, pre-distortion, anti-phase, and adaptive biasing techniques to improve the linearity of the power amplifier [16], [17], [18], [19]. However, in the millimeter wave power amplifier, the performance degradation due to parasitic components is deteriorated, so the application of linearization technique is limited compared to the power amplifier in the GHz band. Furthermore, the power amplifier for beamforming system applications consisting of multiple channels also has limitation on the allocation of additional chip area for linearization techniques.

In this study, we proposed a Ka-band CMOS power amplifier in which the driver stage with a common-source (CS) structure acts as a pre-distorter for the power stage with a two stacked-FET structure. With the pre-distorted driver stage, linearity was improved by suppressing AM-PM distortion of the power amplifier. Since the driver stage acts as a linearizer, there is no additionally required linearizer. Consequently, additional chip areas are unnecessary for linearity improvement. Fig. 1 depicts a conceptual diagram of the proposed linearity improvement technique of the CMOS amplifier structure. In this study, the AM-PM distortions of each driver and power stages were investigated, and the optimal bias condition was analyzed in which the distortion occurring in each stage offset each other. The proposed power amplifier was designed with a differential structure.

In section II, we proposed a structure of a power amplifier in which the driver stage acts as a pre-distorter by analyzing the AM-PM distortions of each of the two stacked-FET power stage and the CS driver stage. Other incidental design details were presented in section III. In Section IV, we verified the feasibility of the proposed power amplifier by presenting the measured results of the AM-PM distortion and output power using 5G modulation signals.

II. PROPOSED TWO STACKED-FET POWER AMPLIFIER WITH PRE-DISTORTED DRIVER STAGE

Here, we described the offset of AM-PM distortion through the cascade connection between the designed power stage and the driver stage acting as a pre-distorter. The power stage was designed in a two stacked-FET structure with a supply voltage of 2.0 V to ensure the required output power, whereas the driver stage was designed in a CS structure with a supply voltage of 1.0 V to minimize dc power consumption [20].

First, the AM-PM distortion of driver and power stages was investigated, and then a power amplifier structure was proposed in which the distortions of driver and power stages connected by cascade offset each other.

A. AM-PM DISTORTION OF COMMON-SOURCE STRUCTURE

Fig. 2 depicts the schematic of the designed driver stage and its equivalent circuit. In the driver stage, the capacitive neutralization technique was applied through $C_{N,D}$. In consideration of a differential structure, the source impedance of the input of the driver stage was defined as $0.5Z_0$, and $Z_{OPT,D}$ represents the load impedance of the driver stage. In Fig. 2(b), if the voltages of $RF_{IN,D}$ and $RF_{OUT,D}$ nodes and voltage gain are v_{out}, v_{in}, and A_v, respectively, the relationship between v_{out}, v_{in}, and A_v can be expressed as follows:

$$v_{out} = A_v\left(v_{in}\right), v_{in}, \quad \angle\Delta v_{out} = \angle A_v\left(v_{in}\right) \tag{1}$$

In order to analyze the AM-PM distortion of the driver stage, the phase relationship between v_{in} and v_{out} should be examined. Therefore, the phase variation of v_{out} based on the phase of v_{in} can be expressed as follows:

$$\angle\Delta v_{out} = \tan^{-1}\left(\frac{Im\left[A_v\left(v_{in}\right)\right]}{Re\left[A_v\left(v_{in}\right)\right]}\right) \tag{2}$$

Applying these to the designed diver shown in Fig. 2, the v_{out} and the phase variation of v_{out} according to the v_{in} can be calculated as follows:

$$v_{out} = \frac{\omega Z_0\left(C_{gd} + C_{gs} + C_{N,D}\right) + j2}{\omega Z_0\left(C_{gd} + C_{N,D}\right)} v_{in} \tag{3}$$

$$\angle\,\Delta v_{out}|_{CS} = \tan^{-1}\left(\frac{2}{\omega Z_0\left(C_{gs} + C_{gd} + C_{N,D}\right)}\right) \tag{4}$$

The phase variation of v_{out} is related to the parasitic components of M_D and $C_{N,D}$. As illustrated in Fig. 3(a), trans-conductance, g_m and C_{gs} showed a relatively large variation range depending on $V_{g,D}$. On the other hand, C_{gd} and C_{ds} showed relatively small variation according to the $V_{g,D}$. Eq. (4) shows that, when the driver stage is designed with CS

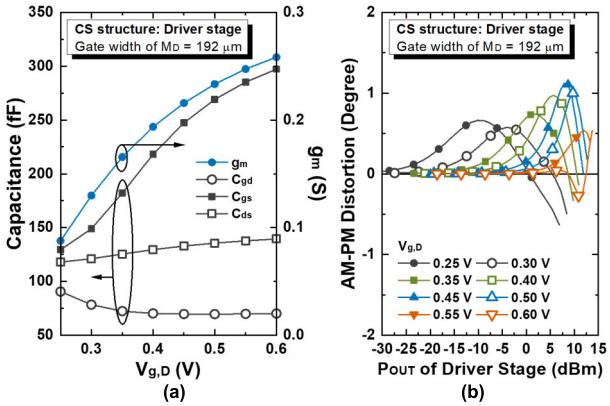

FIGURE 3. Simulated results of the driver stage with CS structure: (a) parasitic components and trans-conductance, g_m and (b) AM-PM distortion.

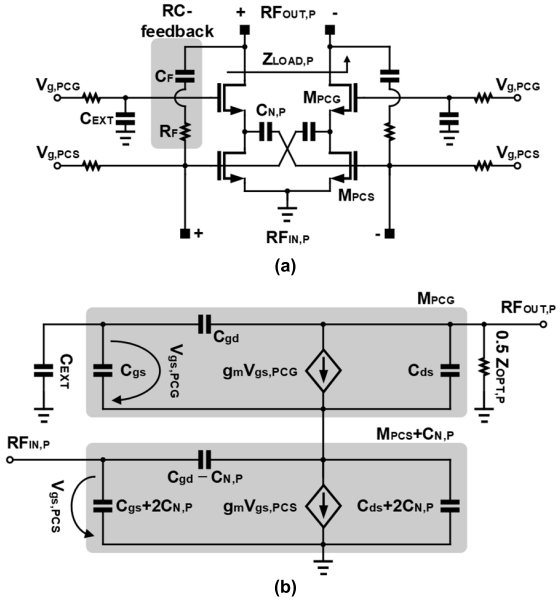

FIGURE 4. Designed power stage: (a) schematic and (b) equivalent circuit.

structure, the phase variation of the output voltage depending on the input voltage is always positive.

In order to confirm the feasibility of the derived numerical analysis results of the CS structure, a simulation of the designed driver stage was performed. For simulation the gate width of the transistor M_D constituting the driver stage was designed to be 192 μm. The $C_{N,D}$ was designed to be 43 fF.

Fig. 3(b) shows the simulation results of AM-PM distortion of the designed driver stage. In this simulation, the distortion according to output power was observed while varying the gate bias voltages $V_{g,D}$ and input power. As shown in Fig. 3(b), most of the distortion has positive values, as predicted by numerical analysis, except in areas where the gate voltage increases excessively.

B. AM-PM DISTORTION OF TWO STACKED-FET STRUCTURE

Fig. 4 depicts the schematic of the designed power stage and its equivalent circuit. The power stage was designed with

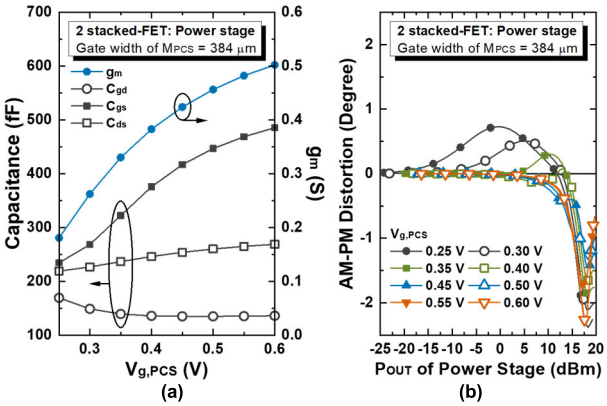

FIGURE 5. Simulated results of the power stage with two stacked-FET structure: (a) parasitic components and trans-conductance, g_m and (b) AM-PM distortion.

a two stacked-FET structure using capacitive neutralization technique in which various studies have already been introduced. The phase variation of v_{out} based on the phase of v_{in} can be expressed as follows:

$$\angle\, \Delta v_{out}|_{2-stack} = \tan^{-1}\left(\frac{\omega g_m \left(C_{gs}+C_{gd}+C_{EXT}\right)\left(C_{ds}+2C_{gd}\right)}{C_{gd}\left(\omega^2 C_{gs}^2+g_m^2\right)}\right) - \tan^{-1}\left(\frac{\omega C_{ds}\left(C_{gd}+C_{EXT}+C_{gs}\right)}{g_m C_{gd}}\right) \quad (5)$$

Here, for simplicity of the analysis, C_{gd} and $C_{N,P}$ were assumed to be same. In addition, it was assumed that the size of M_{PCS} and M_{PCG} were the same, so that the parasitic capacitances of both transistors were also the same. Fig. 5(a) shows g_m and parasitic capacitances according to the gate voltage of the M_{PCS}. As the voltage applied to the gate increases according to the increase of the input power, g_m and C_{gs} increase relatively steeply. Accordingly, when the input power increases, the decrease in the first term of Eq. (5) becomes greater than the decrease in the second term, resulting in a negative value of Eq. (5).

In order to confirm the feasibility of the derived numerical analysis results of the two stacked-FET structure, a simulation of the designed power stage was performed. For simulation, both the transistors M_{PCS} and M_{PCG} were designed to have a gate width of 384 μm. $C_{N,P}$ and C_{EXT} were designed at 110 fF and 1.11 pF, respectively. In addition, R_F and C_F constituting the RC-feedback were to 33 Ω and 22 fF, respectively. The detailed design process of the power stage with the two stacked-FET structure can be found in Appendix section.

Fig. 5(b) shows the simulated results of the AM-PM distortion of the designed power stage. As shown in Fig. 5(b), the tendency of numerical analysis results is also consistent with the simulated AM-PM distortion of the two stacked-FET structure. As the simulation results show, AM-PM distortion becomes negative under high input power condition.

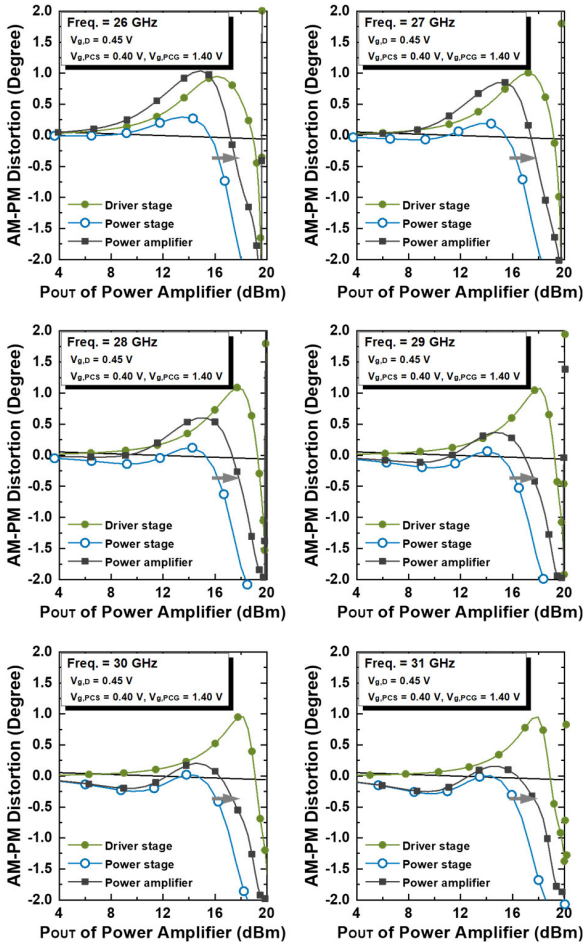

FIGURE 6. Simulated results of AM-PM distortion.

C. AM-PM DISTORTION OF POWER AMPLIFIER WITH PRE-DISTORTED DRIVER STAGE

In this study, a technique to improve the linearity of the power amplifier was proposed by utilizing AM-PM distortions of CS and stacked-FET structures. Given that the signs of the distortion of CS and stacked-FET structures are opposite under high input power conditions, the power stage is designed with the two stacked-FET structure, while the driver stage is designed with the CS structure. In this case, through optimization of the bias voltage of the driver stage and power stages, the driver stage with the CS structure may function as a pre-distorter of the power stage with the two stacked-FET structure.

Fig. 6 shows the results of optimizing the bias voltages so that the driver stage can function as a pre-distorter of the power stage. Using the gate bias voltages, the AM-PM distortion of the power stage according to the output power was offset by the AM-PM distortion of the driver stage. As shown in Fig. 6, the distortion of the power amplifier is more suppressed than that of the power stage.

III. DESIGN OF THE POWER AMPLIFIER

Fig. 7 depicts the block diagram and schematic of the designed power amplifier, respectively. The power amplifier

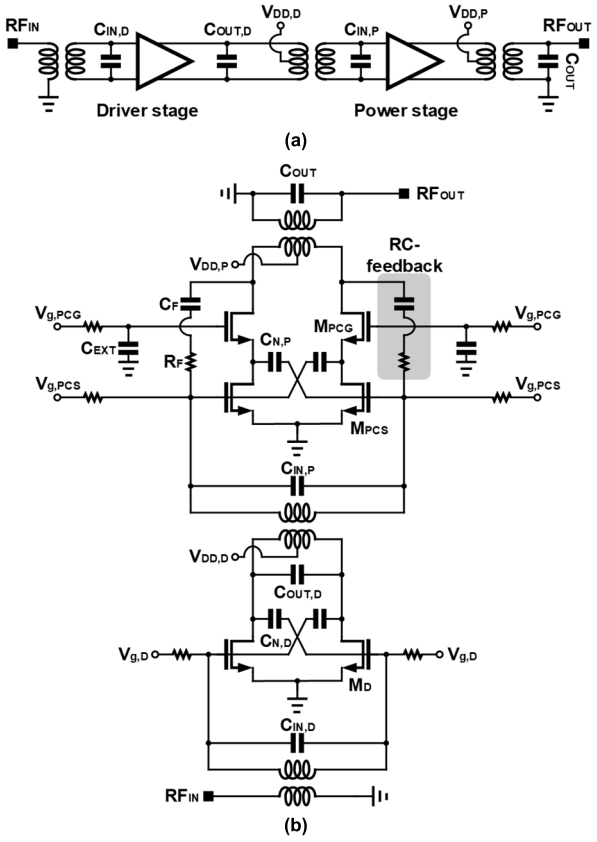

FIGURE 7. Designed power amplifier: (a) block diagram and (b) schematic.

was designed using 65-nm RFCMOS process, and the supply voltage of the driver and power stages were 1.0 V and 2.0 V, respectively. For impedance matching, $C_{IN,D}$, $C_{OUT,D}$, $C_{IN,P}$ and C_{OUT} were additionally used, and they were designed with 14 fF, 63 fF, 14 fF, and 43 fF, respectively.

In general, the layout of the power stage directly effects the performance of the power amplifier, so the power stage should be carefully laid out. Fig. 8 shows the layout of the designed two stacked-FET power stage. As shown in Fig. 8, the C_{EXT}, which is an external gate capacitor, was designed in a split layout structure so that the effect of the C_{EXT} is evenly applied to the unit-transistors constituting the power transistor [12].

Since the power stage is designed with a power matching technique, the deterioration phenomenon of S_{22} often occurs. Accordingly, it is required to improve the degraded S_{22}, and the stability should also be carefully observed. As can be seen from the simulated K-factor shown in Fig. 9(a), there is a frequency interval in which the K-factor of the power stage designed without RC-feedback becomes less than 1. In addition, as shown in Fig. 9(b), the S_{22} are also deteriorated. In this study, to improve the stability and S_{22}, RC-feedback technique was applied. With RC-feedback, the power stage become unconditionally stable. In addition, the S_{22} was also improved. The used values of R_F and C_F constituting the RC-feedback shown in Fig. 4 were 33 Ω and 22 fF.

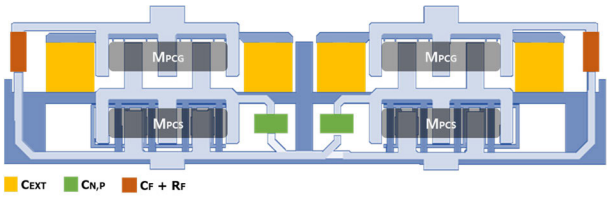

FIGURE 8. Layout of the two stacked-FET power stage.

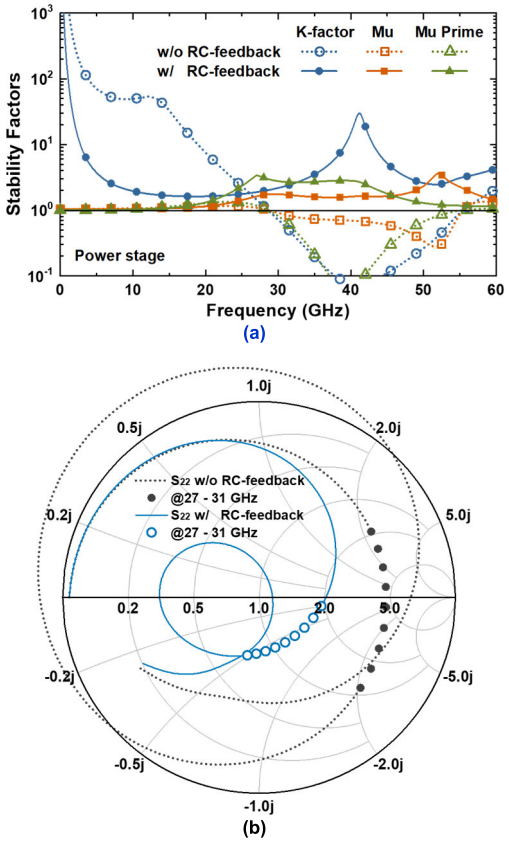

FIGURE 9. Simulated results with and without RC-feedback: (a) K-factor and (b) S_{22}.

Specific simulation results are presented together with measured results for convenience of comparison.

Fig. 10 shows the load-pull simulation results and output matching network of two stacked-FET power stage with the previously determined values of C_{EXT}, $C_{N,P}$, R_F, and C_F. Since two transistors are stacked, a power supply voltage of 2.0 V was used. The blue and red lines in Fig. 10(a) represent the contours of the output power and PAE, respectively. Simulated maximum output power and PAE of the power stage were 21.5 dBm and 42%, respectively. The output matching network for power matching was completed with a transformer and a C_{OUT} of 43 fF as shown in Fig. 10(b). The output transformer is designed with a 1:1 turn ratio, and the supply voltage of the power stage was supplied through the center-tap of the primary winding of the transformer. Fig. 10(c) shows the layout of the output matching network. The $Z_{LOAD,P}$, the input impedance of

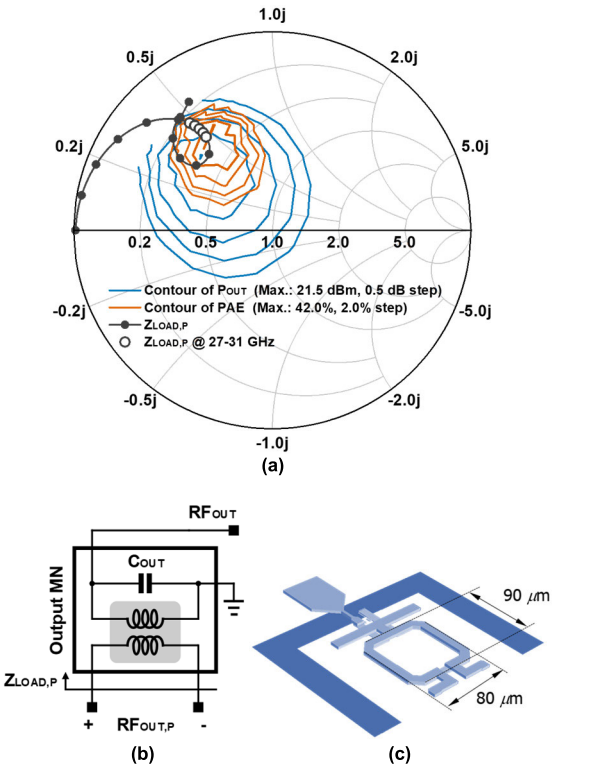

FIGURE 10. Output matching network of the power stage: (a) load-pull simulation results at 29.0 GHz and (b) schematic and (c) layout of the output matching network.

the designed output matching network, is shown as a black line in Fig. 10(a). As shown in Fig. 10(a), power matching was successfully completed at the operating frequency range of 27 – 31 GHz.

IV. MEASUREMENT RESULTS

The power amplifier to which the proposed pre-distorted driver stage was applied was fabricated using 65-nm RFCMOS process. Fig. 11 shows a chip photograph with a chip and core sizes of 0.68×0.52 mm^2 and 0.52×0.19 mm^2, respectively. Supply voltages and gate voltages were applied using bonder-wires, and input and output signals were measured by the on-wafer probing technique.

Fig. 12 shows the simulated and measured S-parameters and K-factors using small signal. In consideration of the downshift of the operating frequency that occurs routinely when developing a millimeter wave circuit, the design was carried out by raising the target frequency of the simulation by 1 GHz. The measurement results showed that the operating frequency was shifted down approximately 1 GHz compared to the simulation results. From the measured K-factors, it can be seen that the designed power amplifier is unconditionally stable.

Fig. 13 shows the simulated and measured results using large signal. The target frequencies of the simulation and measurement were 29 GHz and 28 GHz, respectively. The measured result was somewhat downshifted compared to the simulated result. For continuous wave signals, the designed

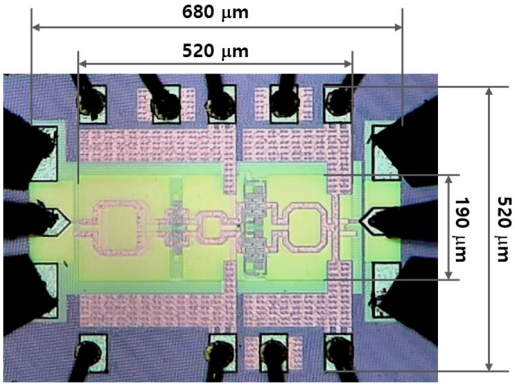

FIGURE 11. Chip photograph of the proposed power amplifier.

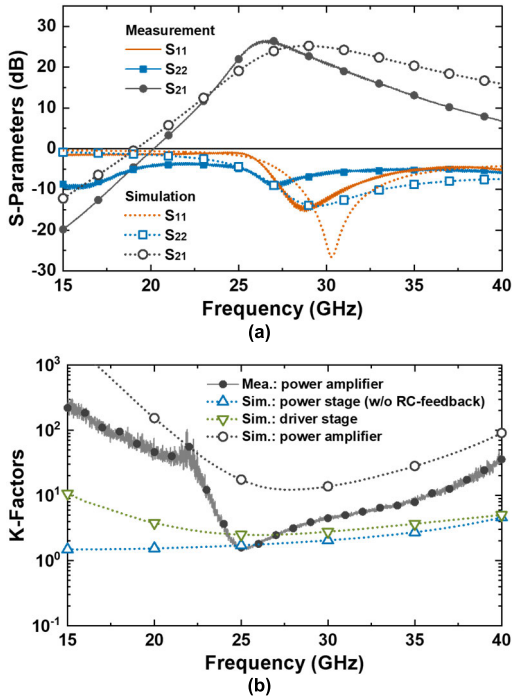

FIGURE 12. Simulated and measured results with small signal: (a) S-parameters and (b) stability factors.

power amplifier showed the best performance at 27 GHz. At an operating frequency of 27 GHz, P_{1dB} and peak PAE were 19.1 dBm and 38.0%, respectively. In the operating frequency range of 26 GHz to 30 GHz, the difference between the maximum and minimum output power was approximately 0.9 dB. The measured peak PAE was higher than 29.7%.

Fig. 14 shows the measured performances of the power amplifier using a 5G-NR modulated signal with 64-QAM, 100-Msym/s, and 9.7-dB PAPR. The P_{AVG} in Fig. 14 is the measured output power when the EVM is less than –25 dB. PAE and ACLR measured under the same conditions are also shown in Fig. 14. The power amplifier using the modulated signal showed the best performance at 28 GHz.

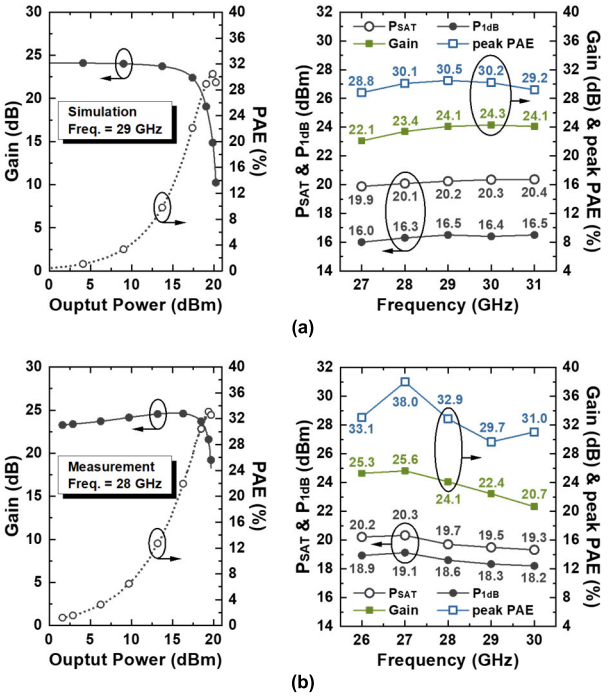

FIGURE 13. Large signal characteristics: (a) simulated and (b) measured results.

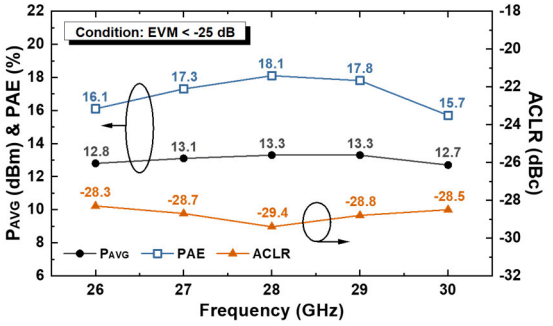

FIGURE 14. Measured results with 5G-NR modulation signal (64-QAM, 100-Msym/s, 9.7-dB PAPR).

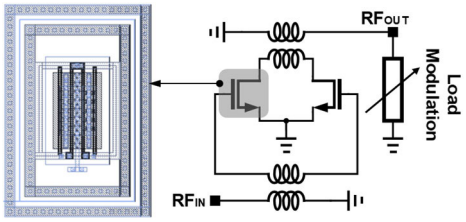

FIGURE 15. Differential schematic and transistor for the load-pull simulation of the power stage.

The summarized performances of the CMOS power amplifiers are compared in Table 1. The proposed power amplifier is designed to be relatively compact in size because the driver stage itself serves as pre-distorter, and there is no additional required linearizer. The proposed power amplifier showed reasonable performance in terms of output power and PAE. The power amplifier of Ref. 11 designed with

TABLE 1. Performance summary and comparison of K-/Ka-Band CMOS power amplifiers.

Ref.	TCAS-II'24 [11]	MWTL'23 [13]	TCAS-II'21 [21]	TMTT'21 [22]	MWCL'20 [23]	MWCL'18 [24]	TMTT'22 [25]	This work	
Tech. (nm)	65	65	65	65	40	65	28	65	
Structure	CS+ 3-stack	CS+CS+ 2-stack	Cascode + Doherty	CS+ Cascode	Cascode + Cascode	2-stack	CS+ Cascode	CS+2-stack	
Linearization Technique	N/A	T-shape linearizer	N/A	Cold-FET linearizer	Drain-body connection	N/A	N/A	Pre-distorted driver stage	
V_{DD} (V)	1.0 / 3.3	0.8 / 2.2	2.0	1.1 / 2.2	-	2.4	2.2	1.0 / 2.0	
Freq. (GHz)	29	28	28	31	28	34	37	28	26 – 30
Gain (dB)	25.2	33	20.4	18.9	20.1	13.8	19.9	24.1	> 20.7
OP_{1dB} (dBm)	22.4	19.2	17	15	18.3	17	17.8	18.6	> 18.2
P_{SAT} (dBm)	22.7	20.4	17.5	17.1	20.25	19.9	19.5	19.7	> 19.3
PAE_{PEAK} (%)	25.8	38.2	27	38.2	25 (34[$])	25.8	30.5	32.9	> 29.7
EVM[#] (dB)	–25	–25	-	–25	-	-	–25	–25	–25
P_{AVG}[#] (dBm)	15.6	14.2	-	9.6	-	-	12.3	13.3	> 12.7
PAE_{AVG}[#] (%)	-	17.1	-	-	-	-	12.7	18.1	> 15.7
Chip Area (mm^2)	0.381 (0.083†)	0.23†	0.35†	0.47 (0.16†)	0.214†	0.365	0.808 (0.165†)	0.354 (0.099†)	

[#]64-QAM 100-Msym/s, †Core size, [$]@ 26 GHz.

a three stacked-FET structure and the power amplifier of Ref. 13 using a higher supply voltage than the power amplifier of this study show somewhat higher output power performance. However, compared to other CMOS power amplifiers, the power amplifier of this study shows relatively high output power and PAE performance despite using the lowest supply voltage of the power stage.

V. CONCLUSION

In this study, we investigated the AM-PM distortion characteristics according to the input power of the common-source (CS) and two stacked-FET structures. Based on this, it was analyzed that distortions of the CS and the two stacked-FET structures can be offset by each other under high input power conditions. As a result, it was confirmed that the driver stage could serve as a pre-distorter of the power stage if the driver stage was configured with a CS structure and the power stage was configured with a two stacked-FET structure. Through this, we designed a Ka-band CMOS power amplifier with a pre-distorted driver stage. The power amplifier is measured with 5G NR modulation. At 28 GHz, the power amplifier achieves output power of 13.3 dBm with –25 dB EVM and the ACLR of –29.4 dBc, respectively.

APPENDIX

This Appendix provides the design information of the power stage of the proposed power amplifier. First, the design process of power stage was provided. Given that the process of determining the size of a transistor through load-pull simulation and capacitive neutralization applied to the power stage of this study are already well-known design techniques, the design process was briefly explained and key results were presented.

A. LOAD-PULL SIMULATION FOR DETERMINING TRANSISTOR SIZE

Fig. 15 shows the schematic for load-pull simulation and the layout of the used unit-transistor. The power stage was designed with a two stacked-FET structure, however, the size of the transistor was first determined through load-pull simulation of the CS structure with supply voltage of 1.0 V. In addition, although the required center frequency of the power amplifier is 28.0 GHz, the load-pull simulation was performed at an operating frequency of 29.0 GHz, considering the tendency of the operating frequency of the fabricated power amplifier to be down shifted.

As shown in Fig. 16, with the unit gate width of 3 μm and gate bias voltage of 0.3 V, the total gate width was determined to be 384 μm to obtain output power and power-added efficiency (PAE) higher than 20.0 dBm and 50.0%, respectively. Because the power stage was finally designed in a two stacked-FET structure, the output power would ideally increase by 3.0 dB. In addition, although the gate voltage of the CS amplifier was set to 0.3 V as an initial value in the load-pull simulation, the gate voltage was finally optimized and readjusted to improve linearity.

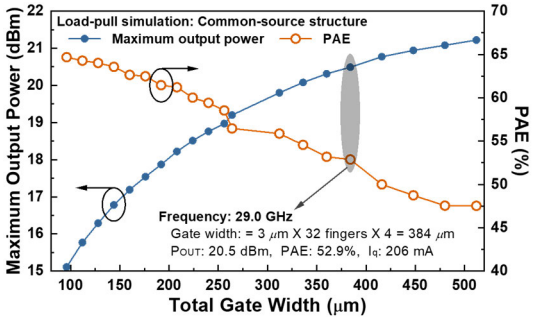

FIGURE 16. Simulation results of the load-pull according to the total gate width of the transistor.

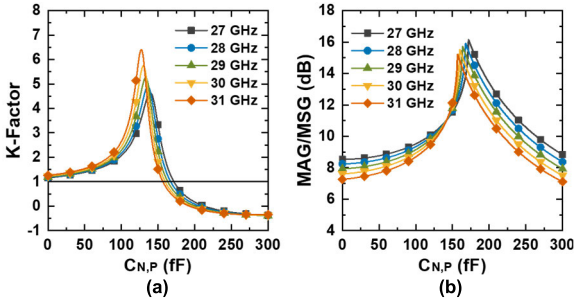

FIGURE 17. Simulation results of the load-pull according to the total gate width of the transistor.

In this study, all transistors constituting the two stacked-FET of the power stage have the same size.

B. DESIGN OF TWO STACKED-FET POWER STAGE

Fig. 4 shows the designed two stacked-FET power stage. To apply the stacked-FET structure, as shown in Fig. 4, C_{EXT}, which is an external gate capacitor, was used. The initial value of the C_{EXT} was determined based on theories that have already been studies in relation to the C_{EXT} effect. The final C_{EXT} value was determined to be 1.11 pF through the optimization and tuning process.

As the next step, the values of $C_{N,P}$, which are the neutralization capacitor, were investigated. Ideally, the performance of the power stage can be optimized when the value of $C_{N,P}$ is similar to the value of C_{gd}, which is the gate-drain parasitic capacitance of the power transistor, M_{PCS}. In this study, the C_{gd} value of M_{PCS} was simulated as 135 fF. Fig. 17 shows the simulation results of K-factor, maximum available gain (MAG), and maximum stable gain (MSG) according to $C_{N,P}$. Through the optimization and tuning process, the $C_{N,P}$ was finally determined to be110 fF.

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