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RESEARCH ARTICLE

Improvement of Thermal Characteristics and On-Current in Vertically Stacked Nanosheet FET by Parasitic Channel Height Engineering

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ABSTRACT For improving thermal characteristics and on-current (I_{ON}) in vertically stacked nanosheet field-effect transistor (NSFET), the effect of parasitic channel height ($H_{parasitic}$) on thermal and electrical characteristics has been investigated. By increasing $H_{parasitic}$, it has been demonstrated that the maximum lattice temperature (T_{max}) could be improved from 428 K to 416 K, and thermal resistance (R_{TH}) could be improved by 9.3 %. This thermal improvement has been achieved since the increased parasitic channel height could lead to the formation of effective heat sink. The relationship between $H_{parasitic}$ and the thermal characteristics of the device has rarely been addressed in previous studies, and we have explored this with a novel approach. In addition, regarding I_{ON}, it has been demonstrated that the proposed device structure could have 19.7 % higher I_{ON}, due to the increased fringing field effect. The origin and benefits of these thermal and electrical improvement have been thoroughly investigated through Synopsys Sentaurus three-dimensional (3D) technology computer-aided design (TCAD) simulation tool. The proposed NSFET structure is expected to be very strategic for the next-generation IC chip design with increased performance (from I_{ON} improvement) and enhanced reliability (from thermal improvement), at the same time.

INDEX TERMS Nanosheet field-effect transistor (NSFET), on-current (I_{ON}), maximum lattice temperature (T_{max}), thermal resistance (R_{TH}).

I. INTRODUCTION

Continuous downscaling of the semiconductor devices has steadily required the reduction in the dimensions of transistors such as gate length [1], [2], [3]. However, as gate length decreases, a couple of undesirable short-channel effects (SCEs) concomitantly arise, posing challenges in maintaining good electrostatics [4]. To address this issue, several three-dimension (3D) device structures such as fin field-effect transistor (FinFET), gate-all-around (GAA) MOSFET, and nanosheet field-effect transistor (NSFET) have been proposed to enhance gate controllability [5], [6], [7], [8], [9]. Among these 3D structures, since gate fully encompasses the sheet-shaped channel, NSFET shows excellent electrostatic

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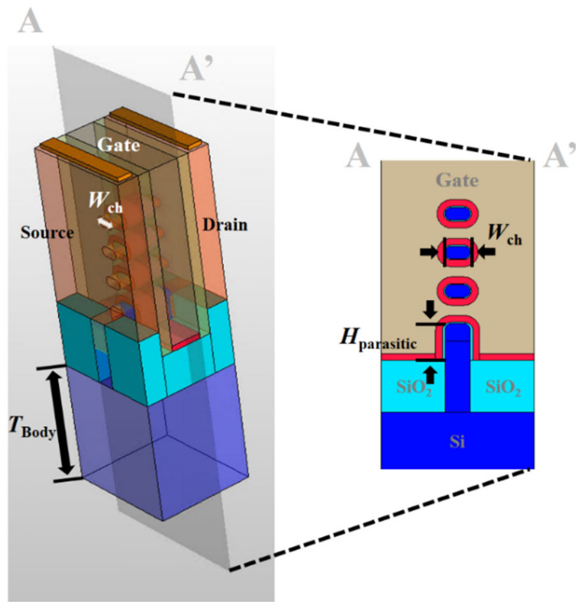

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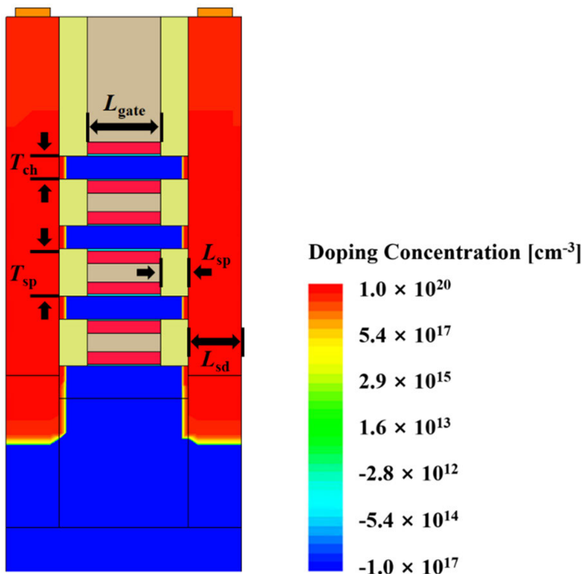

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FIGURE 1. (a) 3-D schematic diagram and cross-sectional view of the proposed vertically stacked NSFET with the explanation of the parameter $H_{parasitic}$, and (b) Another cross-sectional view of the proposed vertically stacked NSFET with various parameters.

characteristics, providing superior channel control, higher on-current (I_{ON}), and better circuit-design flexibility from flexible channel width design [10], [11], [12].

In addition to this structural development, NSFET has been steadily developed with the vertically stacked structure, since the vertically stacked NSFET enables an increased number of channels, consequently providing higher I_{ON}. Specifically, the vertically stacked NSFET could enable 2-3 times higher I_{ON}, compared to single channel NSFET [13], [14]. Due to this I_{ON} advantage, it has been widely accepted that the vertically stacked NSFET could be promising

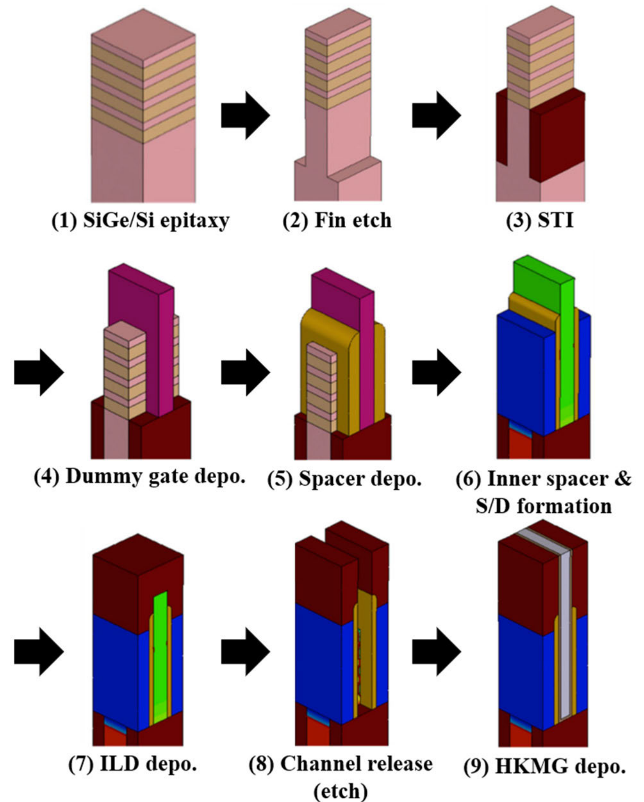


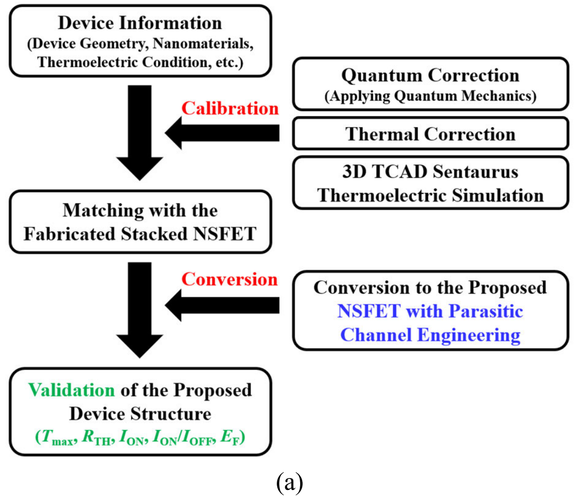
FIGURE 2. Illustration describing step-by-step fabrication flow of the proposed device [17]. The abbreviations of STI / depo. / ILD / HKMG stand for shallow trench isolation (STI) / deposition (depo.) / interlayer dielectric (ILD) / high-κ metal gate (HKMG), respectively.

candidate for next-generation high performance (HP) semiconductor applications with the improved device/circuit performance [13], [14].

However, even though the vertically stacked NSFET has better gate controllability and higher on-current, its thermal characteristics are inferior to those of FinFET and single channel NSFET [13]. This is because the gate dielectric with low thermal conductivity completely encases the silicon channels, thereby making it hard to dissipate the generated heat from the channels [13]. This issue is exacerbated by the use of hafnium oxide (HfO_2), which has a thermal conductivity 2–3 times lower than that of silicon dioxide (SiO_2) [7], [12].

In addition, in the vertically stacked NSFET, its vertically stacked structure even makes it difficult to dissipate the heat generated from multiple channels as well. Consequently, this heat issue, known as self-heating effects (SHEs), simultaneously degrades the performance and reliability of the vertically stacked NSFET [13], [14].

When it comes to performance degradation, I_{ON} decreases due to the increased temperature caused by SHE. I_{ON} degradation from SHE is particularly of great importance, since a decrease in I_{ON} directly impacts a couple of performances at the circuit level [13], [14], [15], [16]. For instance, I_{ON} decrease at the transistor level could worsen the delay



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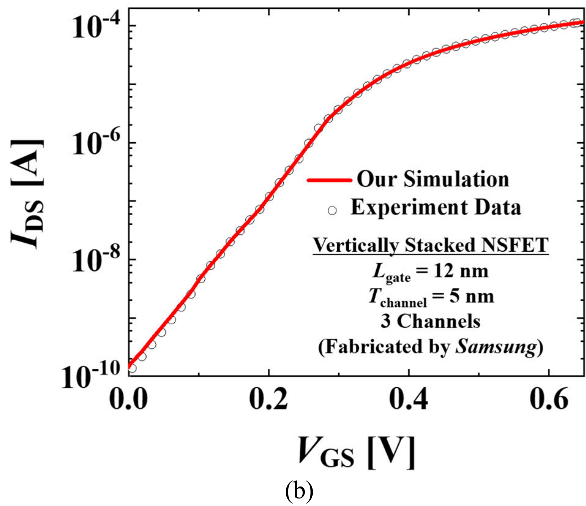

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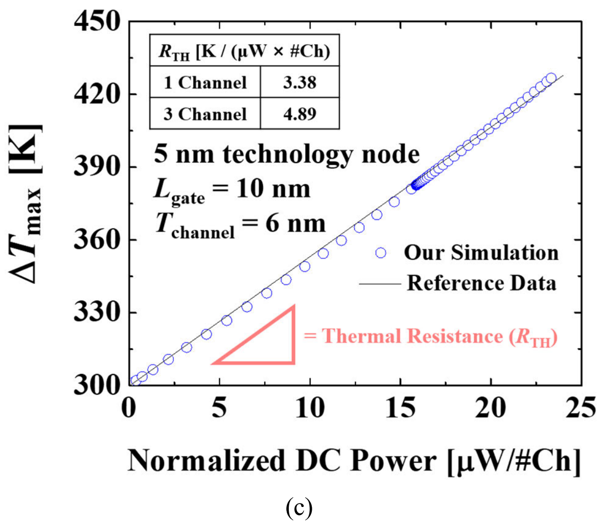

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FIGURE 3. (a) Illustration explaining the overall workflow of this research, (b) Calibration result with electrical characteristics [23], and (c) Calibration result with thermal characteristics [20].

in a three-stage ring oscillator (RO3), inverter delay, and resistance–capacitance (RC) delay, at the same time. For these reasons, addressing the SHE issue is crucial not only at the transistor level but also at the circuit level.

In order to improve the thermal characteristics of the vertically stacked NSFET, several approaches have been proposed by previous studies. For example, Tayal et al. have utilized titanium dioxide (TiO_2) as gate dielectric, instead of HfO_2 [13]. However, TiO_2 has lower bandgap (3.0-3.2 eV), compared to HfO_2 (5.3-5.7 eV). Therefore, the gate current (I_{gate}) might be significantly increased in the vertically stacked NSFET shown in previous research [13].

On the other hand, Kim et al. have utilized two different materials for spacer [9]. For example, they have utilized HfO_2 as inner spacer and SiO_2 as outer spacer. However, from these dual-κ spacer structure, the device dimension should be increased accordingly, which might be significantly undesirable for device integration.

In this regard, we have explored a novel approach to improve the thermal characteristics in vertically stacked NSFETs without increasing the device size as in previous approach [9], or increasing the gate current as in previous approach [13]. Specifically, we have focused on the fact that the fabrication of the vertically stacked NSFET has concomitantly led to the formation of parasitic channel at the bottom of the main channels [15], [16] and the parasitic channel height ($H_{parasitic}$) could affect the overall electrical characteristics and thermal characteristics of the transistor.

Therefore, we have investigated into the effect of $H_{parasitic}$ on the electrical and thermal characteristics of the vertically stacked NSFET, and consequently demonstrated that it is possible to design the vertically stacked NSFET with decreased maximum lattice temperature (T_{max}), decreased thermal resistance (R_{TH}), and increased I_{ON}, with the help of parasitic channel height engineering. Importantly, the connection between $H_{parasitic}$ and the thermal characteristics of the device has seldom been explored in earlier studies, and we have investigated this using a novel approach.

This paper is organized as follows. To begin with, careful calibration has been performed both electrically and thermally, so that more accurate and precise research could be conducted. Then, thermal characteristics such as T_{max} and R_{TH} have been investigated by analyzing the location of heat dissipation path. Thereafter, the improvement of electrical characteristics such as I_{ON} has been analyzed. Finally, potential benefits of the overall improvement of thermal and electrical characteristics in the proposed vertically stacked NSFET have been discussed.

II. DEVICE STRUCTURE AND CALIBRATION PROCESS

Fig. 1 shows the schematic structure of the vertically stacked NSFET. This vertically stacked NSFET structure could be fabricated through the gate-last fabrication process, and the detailed fabrication steps could be found in Fig. 2 [17]. For the detailed specification of this structure, device parameters at 3-nm technology node presented in the International Roadmap for Devices and Systems (IRDS, previously named as ITRS) have been utilized [18].

TABLE 1. Model parameters and the corresponding values.

Symbol	Description	Value	Unit[a]
L_{gate}	gate length	16	nm
L_{sp}	spacer length	6	nm
EOT	equivalent oxide thickness	1	nm
T_{HfO2}	hafnium oxide thickness	2.7	nm
T_{SiO2}	silicon dioxide thickness (interfacial layer)	0.5	nm
T_{Body}	body silicon thickness	800	nm
T_{ch}	channel thickness	5	nm
$H_{parasitic}$	parasitic channel height	5-19	nm
W_{ch}	channel width	10	nm
κ_{HfO2}	HfO_2 thermal conductivity	0.27	W/(K×m)
κ_{SiO2}	SiO_2 thermal conductivity	0.84	W/(K×m)
$\kappa_{channel}$	silicon thermal conductivity (channel)	8.9	W/(K×m)
κ_{sd}	silicon thermal conductivity (source/drain)	7.9	W/(K×m)
κ_{gate}	gate metal thermal conductivity	175	W/(K×m)

[a]The following units are the same as international system of units (SI) for electrical and material engineering [17]; nm = nanometer, W = Watt, K = Kelvin, m = meter.

A. STRUCTURE OF THE VERTICALLY STACKED NSFET

Fig. 1(a) and Fig. 1(b) illustrate the detailed structure of the vertically stacked NSFET. The gate length (L_{gate}) is designed with 16 nm [18]. Regarding silicon (Si) channel, channel width (W_{ch}) and channel thickness (T_{ch}) are set as 10 nm and 5 nm, respectively. In addition, the gate stack is composed of 2.8 nm-thick hafnium oxide (HfO_2) layer and 0.5 nm-thick interfacial silicon dioxide (SiO_2) layer, so that the equivalent oxide thickness (EOT) could be designed as 1 nm [18]. Moreover, doping concentration for source/channel/drain regions are set as 1×10^{20} / 1×10^{17} / 1×10^{20} cm^{-3}, respectively. The thermal conductivities of 0.27, 0.84, 8.9, 7.9, 175 W/(K×m) are applied for HfO_2 [19], SiO_2 [19], channel [20], source and drain [20], gate metal [21], respectively. This structure has been investigated using Synopsys Sentaurus three-dimensional (3D) technology computer-aided design (TCAD) simulation [22]. The detailed parameters could be found in Table 1.

B. WORKFLOW OF RESEARCH AND CALIBRATION PROCESS

Fig. 3(a) shows the overall workflow of this research. First, calibration of GAA MOSFET has been conducted, and then structure of the proposed vertically stacked NSFET has been validated through thermal characteristics and electrical characteristics.

In order to analyze the electrical and thermal characteristics of the vertically stacked NSFET, thermodynamics, Shockley-Read-Hall (SRH) recombination, and Fermi models are applied by Synopsys Sentaurus 3D TCAD simulation. In addition to these model physics, Trap-assisted-tunneling (TAT) and direct tunneling are applied to carefully investigate electrical characteristics of the vertically stacked NSFET.

During the calibration process, quantum correlations are performed through I_{DS}-V_{GS} calibration under Synopsys Sentaurus 3D TCAD simulation [22]. During this process, we have used mobility model (phumob / Enormal (Lombardi) / high field saturation) to apply Coulomb scattering and interfacial surface roughness scattering. Firstly, I_{DS}-V_{GS} calibration has been carefully conducted by applying the quantum model and velocity saturation model and gate metal work function (WF). Secondly, thermal conductivity, heat dissipation paths, and thermal boundary conduction (300 K) to each heat dissipation path have been adjusted to consider thermal characteristics of the vertically stacked NSFET. Fig. 3(b) and Fig. 3(c) show that our simulation fits electrically and thermally with the previous research [20], [23].

III. RESULT AND DISCUSSION

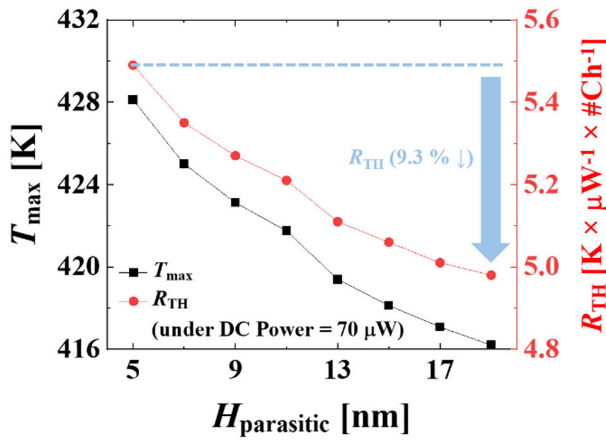
A. IMPROVEMENT OF THERMAL CHARACTERISTICS IN THE VERTICALLY STACKED NSFET

Fig. 4(a) and Fig. 4(b) illustrate how T_{max} and R_{TH} could be changed according to parasitic channel height ($H_{parasitic}$) [Fig. 1(a)]. Specifically, as $H_{parasitic}$ increases from 5 nm to 19 nm, T_{max} could be improved from 428 K to 416 K, and R_{TH} could be improved by 9.3 %. R_{TH} could be calculated from the gradient of Fig. 4(b), and the equation for R_{TH} could be found in the following [20], [21], [24], [25], and [26].

$$R_{TH} = \frac{\Delta T}{\Delta P} [K/\mu W] \quad (1)$$

This thermal improvement could be explained by the phenomenon that increased $H_{parasitic}$ leads to the formation of heat sink at the bottom of channel [Fig. 4(c)]. Specifically, when $H_{parasitic}$ is 5 nm, SiO_2 is located next to parasitic channel (as shown in the first cross-sectional view in Fig. 4(c)). Since insulator (SiO_2) has low thermal conductivity, heat generated by parasitic channel could not pass easily when $H_{parasitic}$ is 5 nm. On the other hand, when $H_{parasitic}$ is 17 nm, metal becomes located next to parasitic channel (as illustrated in the fourth cross-sectional view in Fig. 4(c)). Since metal has high thermal conductivity [Table 1], heat generated by parasitic channel could pass easily through metal when $H_{parasitic}$ is high. Namely, since the gate metal could act as an effective heat sink, heat could be easily dissipated as $H_{parasitic}$ increases.

Especially, R_{TH} continuously improves with increasing $\underline{H}_{parasitic}$. This might be explained by the structural difference between nanosheet-shaped channel and fin-shaped channel. When it comes to nanosheet-shaped channel, the heat generated by nanosheet-shaped channel is difficult to dissipate, because gate dielectric fully surrounds nanosheet-shaped channel. In contrast, when it comes to fin-shaped channel, the heat generated by fin-shaped channel could dissipate either through gate dielectric or the bottom substrate. For these reasons, it has been widely accepted that fin-shaped channel (like FinFET) is superior to thermal characteristics, compared to nanosheet-shaped channel. Therefore, as $H_{parasitic}$ increases, the effect of fin-shaped channel (parasitic channel) might be relatively increased, compared to the effect of



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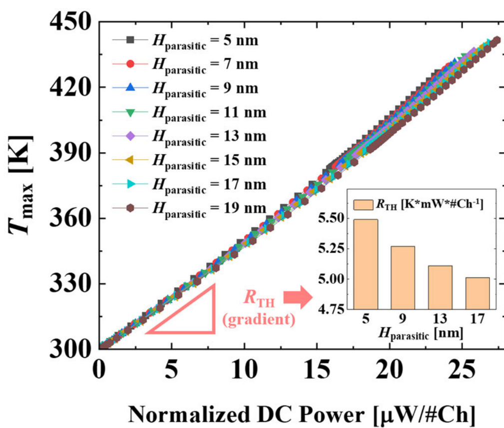

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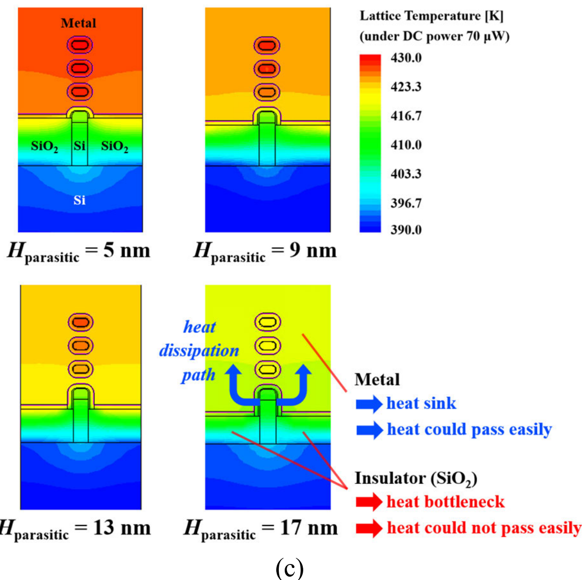

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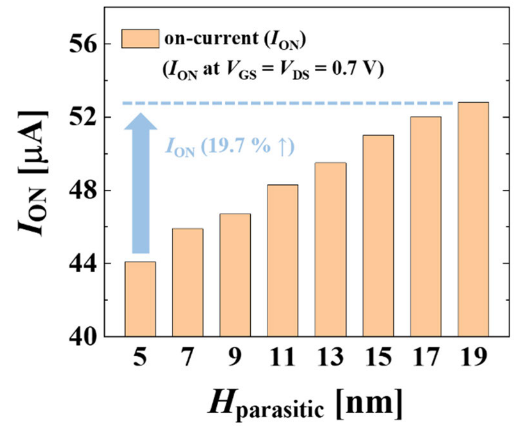
FIGURE 4. **(a) Effect of parasitic channel height on maximum lattice temperature and thermal resistance, (b) Change of maximum lattice temperature according to the normalized DC power, and (c) Cross-sectional view illustrating distribution of lattice temperature.**

nanosheet-shaped channel (main channels). Because of this, R_{TH} has been continuously improved.



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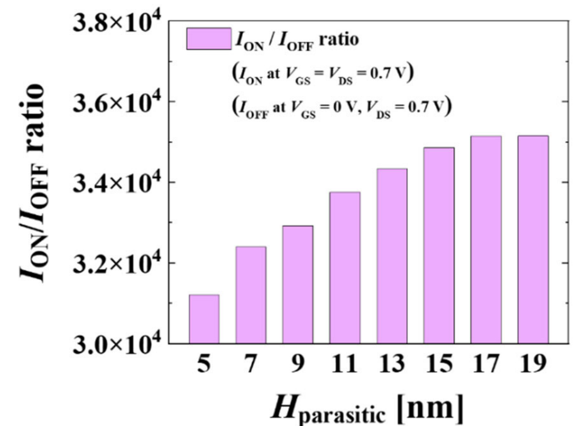

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FIGURE 5. **(a) Comparison of on-current according to parasitic channel height, and (b) Comparison of on-current/off-current ratio according to parasitic channel height.**

B. IMPROVEMENT OF ELECTRICAL CHARACTERISTICS IN THE VERTICALLY STACKED NSFET

In addition to the thermal improvement discussed in the previous section, improvement of electrical characteristics has been investigated as well. Fig. 5(a), Fig. 5(b), and Fig. 5(c) show I_{ON}, I_{ON}/I_{OFF} ratio, and transfer characteristics, respectively.

When it comes to I_{ON}, it has been demonstrated that I_{ON} could be improved by 19.7 %, as $H_{parasitic}$ changes from 5 nm to 19 nm [Fig. 5(a)]. This phenomenon could be explained by increased fringing field effect. For example, as shown in Fig. 6(a), as $H_{parasitic}$ increases, fringing field (E_F) at SiO_2 region gradually increases. This increased E_F leads to increase in electron current density [Fig. 6(b)]. For these reasons, as $H_{parasitic}$ increases, I_{ON} consequently increases [Fig. 5(a)]. In a similar context, regarding I_{ON}/I_{OFF} ratio, the increase in $H_{parasitic}$ improves I_{ON}/I_{OFF} ratio as well, as described in Fig. 5(b). Specifically, I_{ON}/I_{OFF} ratio becomes saturated as $H_{parasitic}$ increases, because I_{OFF} is increased as $H_{parasitic}$ increases. This phenomenon will be carefully explained in the next following section IV.

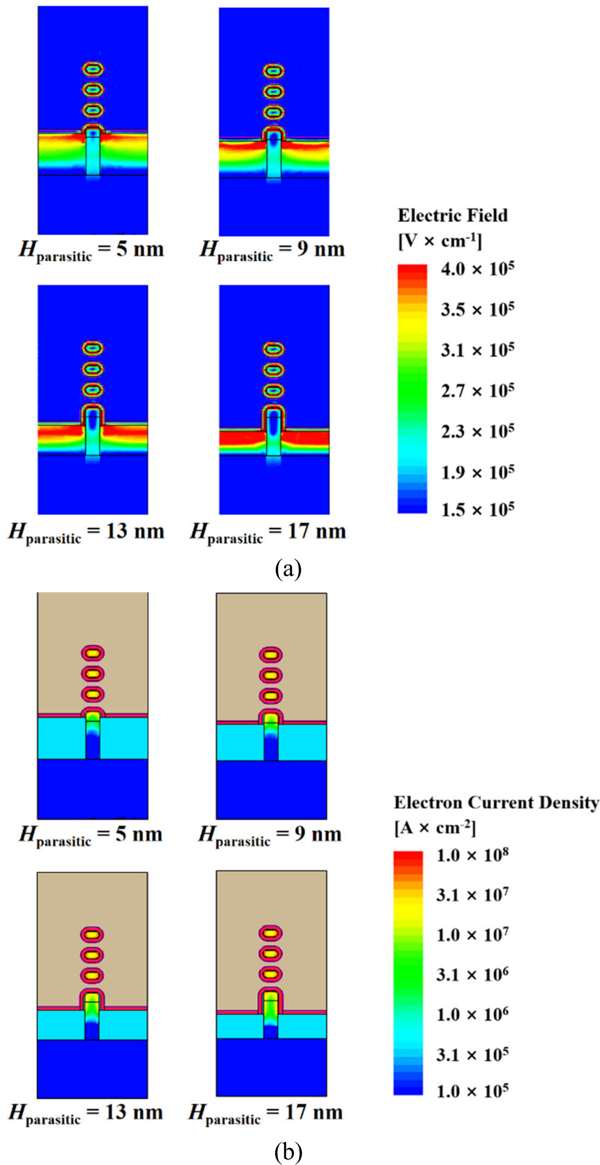


FIGURE 6. **(a) Cross-sectional view illustrating amount of electric field (under $V_{GS} = V_{DS} = 0.7$ V), and (b) Cross-sectional view describing electron current density (under $V_{GS} = V_{DS} = 0.7$ V). As $H_{parasitic}$ increases, the amount of electric field increases. This increased electric field leads to an increase in electron current density, thereby increasing on-current.**

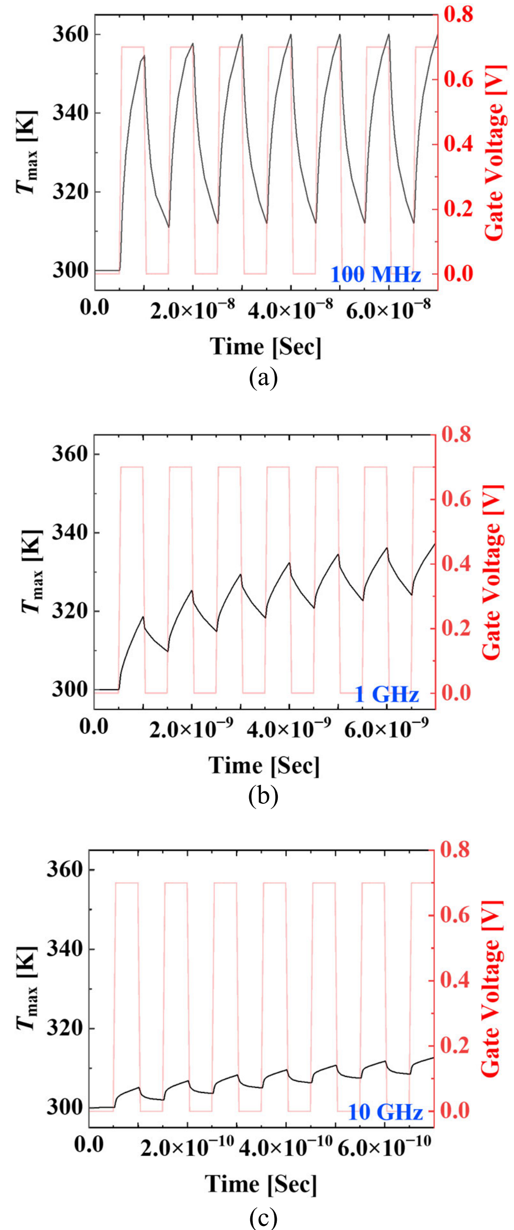


FIGURE 7. **Maximum temperature change under AC condition with (a) 100 MHz, (b) 1 GHz, and (c) 10 GHz.**

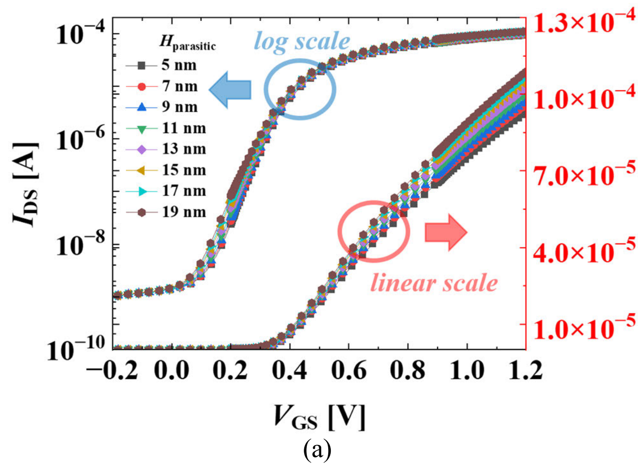
C. INVESTIGATION OF THERMAL CHARACTERISTICS UNDER AC CONDITION

Furthermore, the thermal characteristics of the proposed structure have been investigated under various alternating current (AC) conditions. Given the practical operating condition of modern IC chips, it is also important to analyze the thermal characteristics of transistor under AC conditions. It has demonstrated that the thermal characteristics under AC signals varies from thermal characteristics under direct current (DC) signals, since the heat accumulation / heat dissipation happens repeatedly in AC condition [Fig. 7].

Specifically, it has been demonstrated that heat accumulation phenomenon could be found during ON states, while heat dissipation phenomenon could be found during OFF states [Fig. 7].

In this analysis, a gate voltage of 0.7 V, an increasing time of 5 % of a period, a decreasing time of 5 % of a period, and a duty cycle of 50 % are applied to gate terminal [27]. Fig. 7(a), Fig. 7(b), and Fig. 7(c) show the thermal characteristics of the proposed structure ($H_{parasitic} = 19$ nm) under 100 megahertz (MHz) band, 1 gigahertz (GHz) band, and 10 GHz band, respectively. Specifically, in the 100 MHz band, as described in Fig. 7(a), heat accumulation and heat dissipation occur over and over again, however, the overall T_{max} rises as more cycles are applied.

This phenomenon could be explained by the phenomenon that each cycle of heat accumulation and heat dissipation



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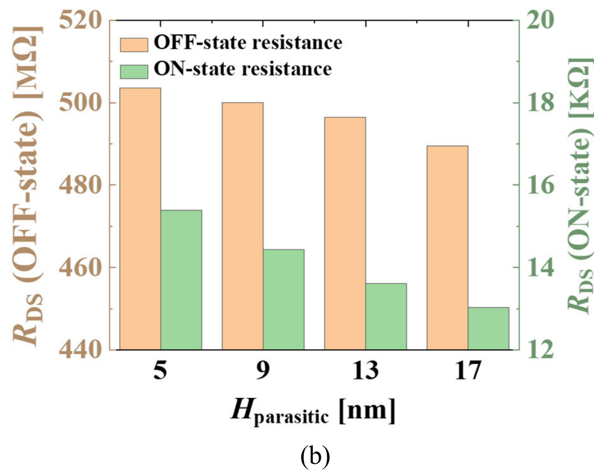

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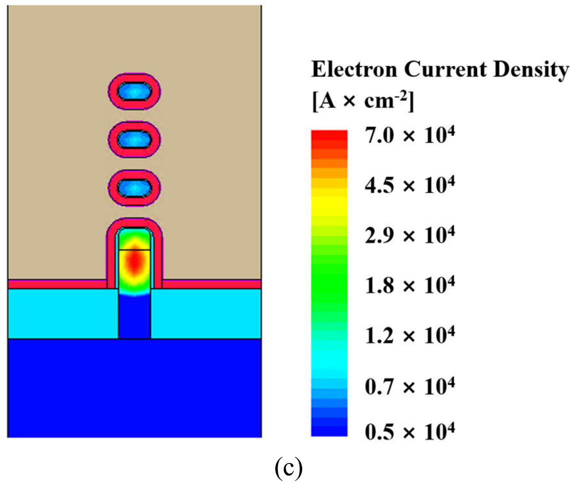

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FIGURE 8. (a) Transfer characteristics with log scale and linear scale (under bias condition $V_{DS} = 0.7$ V), (b) drain-source resistance (R_{DS}) according to $H_{parasitic}$, and (c) Cross-sectional view illustrating electron current density.

consequently leaves residual heat. The same pattern is also observed in 1 GHz band and 10 GHz band as well [Fig. 7(b) and Fig. 7(c)]. Importantly, as the frequency increases from 100 MHz to 10 GHz, lower T_{max} is observed [Fig. 7]. This is because, compared to 100 MHz, higher frequency band such as 10 GHz has shorter heat-accumulation time.

TABLE 2. Performance comparison with previous research.

	IEDM 2021 [35]	TED 2020 [36]	TED 2020 [37]	This Work
V_{DD} [V]	0.7	0.65	0.65	0.7
T_{ch} [nm]	5	6	6	5
W_{ch} [nm]	20	25	25	10
L_{gate} [nm]	15	14	11.5	16
# of stacks	4	3	2	3
I_{ON}/I_{OFF}	29,600	29,166	7,307	35,150
P_{OFF} [pW]	1,890	7,800	16,900	1,330

As a result, the lower frequency band, 100 MHz shows higher T_{max}, while the higher frequency band 10 GHz shows lower T_{max}.

The overall performance of the proposed structure has been summarized in Table 2. As shown in Table 2, our proposed structure could be expected to have improved electrical characteristics and thermal characteristics at the same time.

IV. LIMITATION OF THE RESEARCH AND FUTURE SCOPE OF THE RESEARCH

All in all, the proposed vertically stacked NSFET ($H_{parasitic}$ = 19 nm) could operate with increased I_{ON} and improved thermal characteristics (improved reliability) at the same time. Given these factors, it is expected that the proposed NSFET configuration will be very strategic for designing next-generation high performance (HP) IC chips with improved performance and enhanced reliability.

Nevertheless, our proposed device structure has some limitation as well. For example, even though it could be true that the increased $H_{parasitic}$ could lead to thermal and electrical improvement in the vertically stacked NSFET, it might be difficult to fabricate the vertically stacked NSFET as $H_{parasitic}$ increases.

Specifically, considering the fact that our simulation structure has $W_{channel}$ of 10 nm, it might be possible to fabricate the vertically stacked NSFET with 19 nm $H_{parasitic}$ (with the aspect ratio about 2:1) [28], [29], [30]. However, it might be difficult to fabricate with higher $H_{parasitic}$ (over the aspect ratio 3:1). Even though there was previous research showing aspect ratio of the fin-shaped silicon channel over 10:1, it might be difficult to fabricate this kind of fin-shaped channel with high yield rate [31]. In this regard, the authors would like to suggest the future research addressing the fabrication of vertically stacked NSFET with various $H_{parasitic}$ values, so that the parasitic channel height engineering could be understood not only from the modelling perspective but also from the fabrication perspective.

In addition, I_{ON}/I_{OFF} ratio becomes saturated as $H_{parasitic}$ reaches 19 nm, despite I_{ON} continuing to increase [Fig. 5(c)]. This is because the increased $H_{parasitic}$ leads to higher off-current (I_{OFF}) as well [Fig. 8(a) and Fig. 8(b)].

This phenomenon could be explained by illustration of electron current density during OFF-state. As shown in

Fig. 8(c), it can be interpreted that most of I_{OFF} is derived by the parasitic channel (also known as 'parasitic resistance'), which leads to increased I_{OFF} in the proposed device structure. Because of this phenomenon, drain-source resistance (R_{DS}) during OFF-state could be decreased as $H_{parasitic}$ increases, thereby leading to undesirable increased I_{OFF} [Fig. 8(b)]. Therefore, even though our proposed structure could be strategic for high performance (HP) IC chip design, for designing low power (LP) IC chip design, other strategies such as incorporation of low power devices such as tunnel field-effect transistor (TFET) will be needed [32], [33], [34].

V. CONCLUSION

In this paper, simultaneous improvement of thermal characteristics and electrical characteristics in the vertically stacked NSFET has been demonstrated. As the height of parasitic channel increases, maximum lattice temperature and thermal resistance have been improved, since the increase of parasitic channel height leads to formation of effective heat sink. In addition to this thermal improvement, it has been demonstrated that the parasitic channel height engineering could increase on-current by 19.7 % in the vertically stacked NSFET, since the increased fringing field leads to increase of electron current density, thereby increasing on-current. The connection between parasitic channel height and the thermal characteristics of the device has rarely been researched in earlier studies, and we have explored this with a novel approach. Our proposed structure with the increased parasitic channel height would be strategic for future scaling technology with enhanced thermal characteristics and improved electrical performance, at the same time.

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