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RESEARCH ARTICLE

An Integrated AC–DC Isolated Converter Electrolytic-Free With Intrinsic Active Low-Frequency Ripple Reduction

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ABSTRACT Capacitance reduction in single-phase rectifiers has been the focus of several works, allowing, in many cases, the replacement of short-lifetime electrolytic with film capacitors, prolonging the lifespan of the converter. Among the different techniques used to promote this capacitance reduction, the use of modulation and control strategy has the advantage of not adding extra elements to the circuit. Thus, this work proposes the application of a hybrid modulation in a converter derived from integrating an interleaved boost rectifier and a full-bridge Zero Voltage Switching (ZVS) DC-DC converter to reduce the output low-frequency ripple actively. Besides the active low-frequency voltage ripple reduction allowing employ only film capacitors, the proposed solution presents low DC bus voltage, reducing the voltage stress, low input current ripple, simple control strategy, and fast dynamic response. Experimental results of a prototype with a rated power of 300 W are presented to validate of the proposed solution, operating with an efficiency of 92.4%, a power factor of 0.9936, and a total harmonic distortion (THD) of 10%. The adopted hybrid modulation and control strategies allow for reducing the voltage output ripple with a capacitance/watts ratio of 0.18 μF/W, a 33 times capacitance reduction, avoiding electrolytic capacitors, and maintaining a fast dynamic response of output voltage.

INDEX TERMS Electrolytic capacitor-free, low frequency ripple reduction, power factor correction (PFC), power decoupling, hybrid modulation strategy, integrated converter.

NOMENCLATURE

CCM	Continuous Conduction Mode.
DCM	Discontinuous Conduction Mode.
MPPT	Maximum Power Point Tracking.
PF	Power Factor.
PI	Proportional Integral.
PFC	Power Factor Correction.
PSM	Phase-shift Modulation.
THD	Total Harmonic Distortion.
ZVS	Zero Voltage Switching.
ϕ	Phase-shift.
ϕ_{max_ef}	Maximum effective value.
ϕ_{max}	Maximum phase-shift.
ϕ_{min}	Minimum phase-shift.
ω_z	Zero controller frequency.
ω_p	Polo controller frequency.
C_{f1} e C_{f2}	Input filter capacitor.
C_{DC}	Bus capacitor.
C_o	Output capacitor.
$C_{S1}, \ldots, C_{S4}$	Intrinsic MOSFET capacitor.
D	Duty-cycle.
$D_1, \ldots, D_4$	Input diode.
$D_{o1}, \ldots, D_{o4}$	Output diode.
$D_{S1}, \ldots D_{S4}$	Intrinsic MOSFET diode.
f_r	Line frequency.
f_s	Switching frequency.

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i_{in}	Input current.
I_o	Output current.
L_{f1} e L_{f2}	Input filter inductor.
L_o	Output inductor.
L_r	Resonance inductor.
N_P	Primary winding.
N_S	Secondary winding.
P_o	Output power.
R_o	Nominal load.
R_d	Auxiliary variable.
$S_1, \ldots, S_4$	MOSFET.
T_S	Switching period.
T_r	Transformer.
V_{DC}	Bus voltage.
V_{DCmax}	Maximum bus voltage.
V_{DCmin}	Minimum bus voltage.
$V_{GS1}, \ldots, V_{GS4}$	MOSFET gate source voltage.
v_{in}	Input voltage.
v_{in_max}	Maximum input voltage.
V_o	Output voltage.

I. INTRODUCTION

A. MOTIVATION

Industrial and residential consumers widely use high-power factor rectifiers to convert alternating current into direct current. The instantaneous input power is pulsed in single-phase rectifiers due to the voltage supplying power being alternated [1], [2]. This pulsed power is twice the frequency of the input voltage and results in a second-order bus voltage (VDC) ripple on the system output [3]. The second-order or low-frequency ripple present in the converters interfaces of single-phase alternating systems, including inverters and rectifiers, can degrade performance in some applications. Some examples are the efficiency reduction of the maximum power point tracking (MPPT) in photovoltaic generation systems, flicker in lighting systems and reduction of lifespan in generation systems with fuel cells connected to the electrical grid [4]. Another important application of these rectifiers is battery charging systems, in which low-frequency oscillation in the recharging current can increase battery temperature, reducing it lifespan [5].

It is possible to reduce the voltage low-frequency ripple actively using a fast output voltage control loop. However, this control action increases the input current distortion, compromising the input power factor in conventional rectifiers.

The most common solution for solving the problem of power decoupling is to oversize the bus capacitor to absorb the instantaneous power demand. Therefore, it is common to use electrolytic capacitors in this type of solution that requires high capacitance. However, the life expectancy of large aluminum electrolytic capacitors is limited and very dependent on the operation temperature, becoming an obstacle to power supply for long-lifetime loads [6].

Using large bus capacitors to attenuate this low-frequency ripple also impairs the dynamic response of the rectifier stage. The high power factor operation is maintained in conventional systems with high energy stored in the bus capacitor, limiting the controller bandwidth to reject the low-frequency oscillation in the DC bus and output voltage. The usual result is a slow dynamic response with significant oscillations in the bus voltage, which characterizes this input stage as a pre-regulator [7].

Using active power-decoupling techniques effectively reduces the inherent double-line frequency ripple power in single-phase power systems by applying active circuits, control strategies, and specific modulations. Reduced capacitance is used in these solutions, allowing the development of converters without the use of electrolytic capacitors, which is an essential requirement for some applications where a high converter lifespan and high reliability are necessary. Some examples are military applications, converters installed in difficult-to-access places, and applications with high maintenance costs.

A new configuration with active low-frequency ripple reduction is proposed considering the following main operating requirements:

- High power factor operation, complying with the standard IEC 610000-3-2 Class D;
- Galvanic isolation;
- Soft-switching in all active switches, allowing the operation with high switching frequency;
- Eliminating electrolytic capacitors to expand the converter lifetime and reliability for applications with these requirements;
- Structure integration, reducing the number of components, circuit redundancy, and circuit complexity;
- Fast output response, eliminating an additional output processing stage to attend to the dynamic requirements. Some single-stage topologies proposed present a limited dynamic performance and low-frequency output ripple, operating as a pre-regulator and requiring a second stage to comply with the dynamic performance of some applications.

B. LITERATURE REVIEW

The single-phase isolated rectifiers are conventional structures composed of two conversion stages [8], [9], [10], [11], formed by a power factor correction (PFC) stage and an isolated DC-DC stage [1]. Other alternatives are the single-stage and quasi-single-stage converters, integrating the input and output sections into one [12], [13], [14], [15]. The integration of converters with sharing switches and passive components as the DC bus capacitor is an option to reduce complexity and cost and maintain similar features to the two-stage converters. This kind of structure has been studied in some works [16], [17], [18], [19]. However, additional development is necessary for these rectifiers for low-frequency ripple reduction and electrolytic capacitor elimination. A comprehensive review of the prior-art and state-of-the-art control strategies in active power decoupling

is presented in [3], and several circuit topologies for active power decoupling are reviewed in [4].

The active decoupling circuit topologies can be classified into different forms and are usually divided into independent and dependent [4]. In the independent structure, the active decoupling circuit operates independently of the original converter, and the circuit of the decoupling structure can be inserted in series or parallel with the load. In the case of dependent structures, the semiconductor and passive elements are shared partially and/or completely with the original converter. However, in both cases, including an additional circuit for active decoupling increases circuit complexity, cost, and losses, reducing system efficiency.

Therefore, many works aim to achieve power decoupling and, through different techniques, reduce the size of the required capacitance [2], [6], [11], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33].

Table 1 compares the proposed solution with other solutions in the literature concerning the strategy used for power decoupling, power factor, efficiency, power, transient response, non-use of electrolytic capacitor, and energy/power ratio.

The integration of a hard-switching flyback DC-DC converter with the input rectifier is proposed in [21], [22], and [23]. Among the power decoupling techniques, some solutions involve distortion of the input current up to the maximum allowed by the standard, but on the other hand, penalize the power factor [6], [21]. The duty-cycle control is used in [21] to deform the input current to allow a reduction of output voltage ripple. The duty-cycle is calculated by acquiring the input voltage, and due to current deformation, the power factor is only 0.9 at nominal power. However, the converter still uses relatively large electrolytic capacitors. An additional circuit for active ripple reduction is included in series with the output in [22] and in parallel with the output in [23]. However, including additional circuits increases the circuit complexity and includes additional losses. The hard-switching operation limits the switching frequency. The integration of a soft-switching active clamping flyback DC-DC converter with the input rectifier is proposed in [24] and [25], allowing the operation with high switching frequency. An additional full-bridge is included in series with the output as an active ripple reduction in [24], Fig. 1(a), increasing the complexity and cost. The active clamping circuit used for the soft-switching operation also implements an active ripple reduction circuit [25], making this structure presented in Fig. 1(b) more competitive. Although the solution using single-stage flyback-based converters [21], [22], [23], [24], [25], usually utilizes the lowest count of power semiconductor devices, this solution is generally restricted in low-power applications (P_o<100 W), such as LED drivers [26]. Despite the power decoupling, some solutions still use a bulky electrolytic capacitor, such as [21], [22], and [25].

A bridgeless half-bridge full-bridge bidirectional converter for battery charge is proposed in [27] operating with

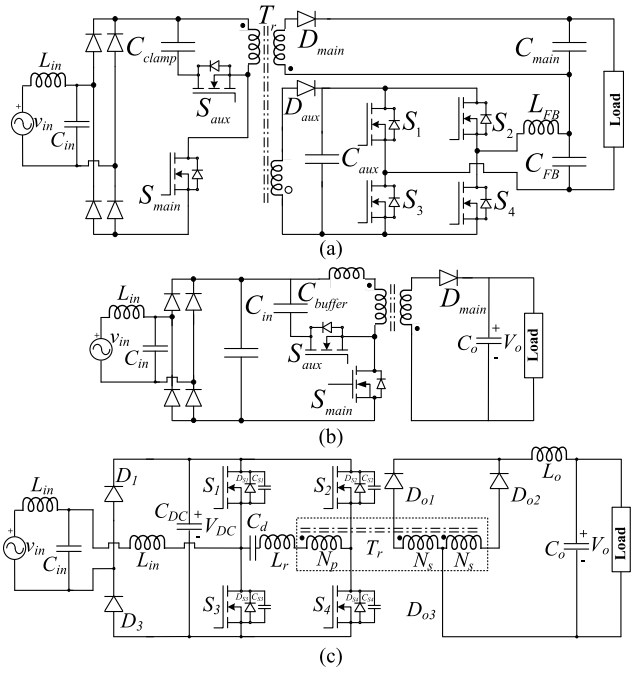


FIGURE 1. Decoupling circuit topologies: (a) [24], (b) [25] and (c) [26].

soft-switching. This solution includes an active filter at the battery side for active low-frequency reduction. The bidirectional power flow requires a solution with a higher number of active semiconductors.

A solution for the low-frequency output voltage ripple reduction in systems with a DC bus, as the conventional two-stage and quasi-single-stage topologies, is the increment of the DC bus voltage, allowing a high DC bus voltage ripple. This configuration reduces the DC bus capacitance, eliminating the electrolytic capacitor. However, the high voltage operation maintains a high stored energy at the DC bus and significantly increases the voltage stress at the system's primary side. High-voltage DC bus capacitors also increase the system volume and cost. As an example of this implementation, shown in Fig. 1(c), an asymmetric modulation is used in a bridgeless single-stage full-bridge to control power factor correction (PFC) and obtain the power decoupling for capacitance reduction [26]. The topology presents a very slow dynamic response (2 seconds) and operates with a high DC bus voltage reaching 800 V at the load transient, requiring high-voltage capacitors and switches.

C. CONTRIBUTION AND PAPER ORGANIZATION

Compliance with all specified requirements, such as high power factor, soft-switching operation, electrolytic capacitor elimination, and fast output transient response, is obtained using a new integrated structure. The definition of the new structure includes the choice of the AC-DC configuration topologies, the specific modulation strategies for high power factor operation with intrinsic low-frequency ripple

TABLE 1. Comparison with other structures.

Topologies	Strategic power decoupling	PF	Efficiency at full load(%)	Power (W)	Step response	Electrolytic Capacitor-Free	Capacitance/ Power	Energy/Power $(C.V^2/2)$/W
[21]	Control/Modulation	0.9	84	100	*	No	140 μF/W	25.27 mJ/W
[22]	Buck ripple suppressor	0.996	89.5	50	**	No	14.94 μF/W	12.36 mJ/W
[23]	Ripple current compensation	0.99	85.1	28	*	Yes	0.83 μF/W	4.77 mJ/W
[24]	Parallel ripple cancellation	0.97	92.5	100	*	Yes	1.68 μF/W	5.685 mJ/W
[25]	Buffer capacitor	*	94	100	**	No	7.07 μF/W	14.69 mJ/W
[26]	Control/Modulation	0.997	93	2000	2s	Yes	0.15 μF/W	21 mJ/W
[27]	Decoupling circuit	*	94	1000	*	Yes	0.3522 μF/W	2.13 mJ/W
Proposed	Control/Modulation	0.9936	92.4	300	1ms	Yes	0.18 μF/W	7.5 mJ/W

*not informed ** almost constant output voltage due to the use of high capacitance

reduction, and the control system structure and design for the fast transient response.

The proposed solution is the integration of a low voltage stress interleaved boost rectifier and a full-bridge Zero Voltage Switching (ZVS) DC-DC converter using a hybrid modulation.

Different from the conventional independent or dependent active power decoupling circuits that include additional components, increasing the circuit complexity and losses, no additional components are necessary for the proposed circuit. The operation of the active power decoupling does not change the converter losses, maintaining the same efficiency without the power decoupling. The modulation used also allows the active power decoupling without change in the input power factor. The active low-frequency ripple reduction and fast output control are obtained using a hybrid asymmetric pulse width modulation (APWM) and phase-shift modulation (PSM) developed for the proposed converter. The modulation restrictions, which are usual in integrated structures with hybrid modulations and limit their operation, are solved in the proposed structure.

Reducing the capacitance and the converter stored energy, allowed by the active power decoupling, requires an efficient control system to ensure stability and fast response to load transient. A simple and effective control system is proposed, allowing a very fast output response (1 ms) with low overshoot/undershoot. Therefore, including an output stage or post-regulation to comply with the dynamic response requirements is unnecessary in the proposed structure. The phase-shift controls the output voltage and the fast output voltage control loop can reduce the low-frequency output voltage ripple without compromising the input power factor without using additional circuits. The control structure allows simultaneous control of the output and bus voltage. The input section stage with the proposed control system structure also allows the operation with reduced voltage at the DC bus converter, reducing the semiconductor voltage stress and reducing the conduction losses. This operating characteristic differs from previous works as [26], which use high bus voltage to reduce the converter capacitance. The high bus voltage increases the converter cost and losses using high voltage components.

The interleaved boost rectifier used in the system input presents low voltage stress operating with a DC bus voltage close to the peak of the AC input voltage, operating with high power factor. The interleaved operation reduces the high-frequency input current ripple, allowing the reduction or elimination of the high-frequency input filter usual in the input of the Discontinuous Conduction Mode (DCM) boost rectifiers. The high-frequency input filter is necessary for all converters presented in Table 1 except for the proposed structure.

As seen in Table 1, the proposed structure is competitive compared with the other solutions. It presents a high power factor (0.9936), fast transient response (1 ms) with very low overshoot, and a low capacitance/power ratio (0.18 μF/W).

The distinctive features of the proposed converter are summarized as follows:

- The integrated structure allows for keeping the bus voltage controlled and close to the input peak voltage;
- Switch sharing allows the input stage to switch ZVS commutation;
- Unlike other solutions, the control is simple, without needing a current sensor;
- Fast control of output voltage reduces the low frequency ripple and provides fast dynamics response;
- Active power decoupling is achieved and eliminates the bulk electrolytic capacitors;
- Fast transient regulation of the bus voltage with the control strategy used.

As a disadvantage, the input rectifier stage operates in DCM, which can limit the use of this converter in high-power applications.

Other sections in the paper are organized as follows. The proposed converter is presented in section II, indicating the origin of the structure and details of the hybrid modulation. An analysis of the topology is given in section III, with the system operation. The design and component sizing methodology is described in section IV. The converter control strategy is demonstrated in section V. The experimental results that confirm the functioning of the strategy and the integrated structure are presented in section VI. Finally, a conclusion is carried out in section VII.

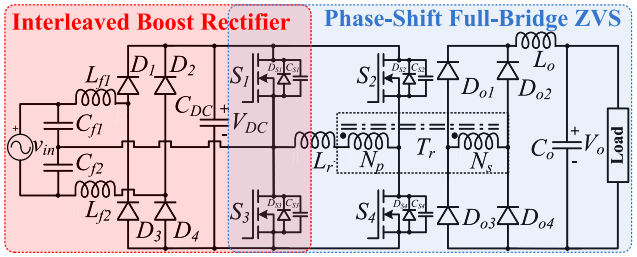


FIGURE 2. Proposed ZVS PS-PWM integrated AC-DC converter.

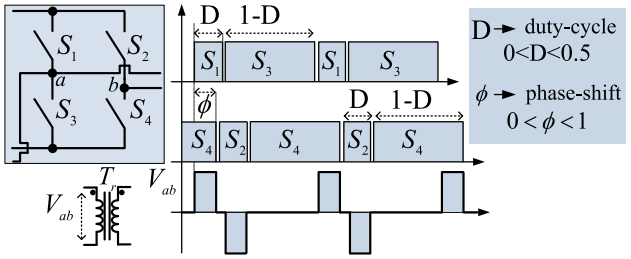


FIGURE 3. Hybrid modulation (Asymmetric PWM plus phase-shift).

II. INTEGRATED CONVERTER

Figure 2 shows the topology composed of the integration of an interleaved boost rectifier and a phase-shift full-bridge ZVS DC-DC converter, in which switches S_1 and S_3 and the DC bus are shared between the interleaved boost rectifier and the full-bridge ZVS converter. The interleaved boost rectifier [34] used at the system input presents a high power factor and low input current distortion without current sensors operating in DCM. The interleaved operation with low input current ripple eliminates the high frequency input filter usual in DCM boost rectifiers. This structure also presents reduced voltage and current stress compared with the conventional DCM boost rectifier.

This topology's lowest current and voltage stress is obtained, operating close at the boundary of the continuous conduction mode (CCM) and DCM at the nominal output power with the maximum duty-cycle (D=0.5). With this operation condition, the voltage across the input capacitors (C_{f1} - C_{f2}) is close to half of the AC input voltage, and the rectifier output voltage is close to the double of the peak of the input capacitor voltage. Therefore, the DC bus voltage is close to the peak of the AC input voltage, which is a low value compared with the conventional step-up rectifiers. The control and modulation strategy maintains reduced voltage stress in low power operation, which is a problem for some structures operating in DCM. The full-bridge stage operates in CCM with ZVS soft-switching using a hybrid modulation.

A. MODULATION

The hybrid modulation strategy used in this paper consists of phase-shift modulation (PSM) and asymmetric PWM modulation working together. The simultaneous modulation as PWM and frequency modulation or PWM and phase-shift have been studied in different applications. When a simultaneous modulation is applied in an integrated converter, some restriction problems can occur depending on the converters used in the integration. The limits of the hybrid modulation applied in the proposed structure are identified, and a solution for the simultaneous modulation restriction is presented, overcoming its limits.

The hybrid modulation is shown in Fig. 3. In phase-shift modulation, one of the inverter arms is kept fixed, and the second arm is phased concerning the first. Regarding angle, it can be understood as a variation from 0° to 180°. However, for simplicity, the variation of the phase-shift adopted in this work is from zero to one, where the zero corresponds to the minimum output power and one the maximum output power. In conventional asymmetric PWM modulation, the maximum phase-shift is kept fixed, and only the duty-cycle varies from 0 to 0.5.

In this way, hybrid modulation is obtained by using the two modulations simultaneously, in which both the duty-cycle (D) and the phase-shift (ϕ) are used as control variables. The phase-shift modulation does not change the input current and the converter power factor. Therefore, the phase-shift modulation can control the system output voltage with a very fast control loop without changing the input current distortion.

The fast output voltage control with the phase-shift modulation reduces the output low-frequency ripple, and a fast load transient response is obtained operating with low-value capacitors.

The control of the DC bus voltage is accomplished by the asymmetric PWM modulation. The duty-cycle variation also changes the system output. However, the duty-cycle variation must be relatively slow, as one semi-cycle of the AC input voltage, to maintain the high power factor operation. Therefore, any change in the converter duty-cycle is compensated by the fast phase-shift control, maintaining the output constant.

It is important to emphasize that considering the maximum duty-cycle (D=0.5), the phase-shift (ϕ) can vary from zero to one and control the power transfer throughout the entire range. The operational condition illustrated in Fig. 4(a) demonstrates a limit when the duty-cycle is less than 0.5, and the phase-shift (ϕ) is at the maximum effective value

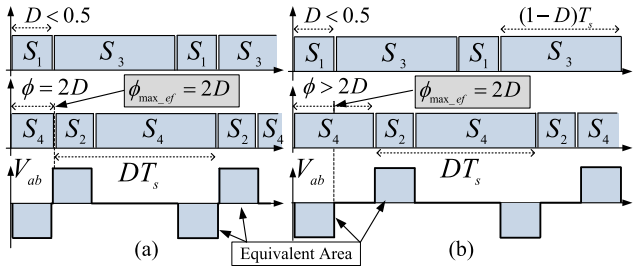


FIGURE 4. Limit of the output power transfer by hybrid modulation in D<0.5: (a) maximum effective value ϕ=2D and (b) limit exceeded ϕ>2D.

(ϕ_{max_ef}) equal to $\phi = 2D$. If this limit is exceeded, as shown in Fig. 4(b), it is impossible to increase the power supplied to the output, as the area of the voltage applied to the transformer remains the same. Therefore, a phase-shift (ϕ) greater than 2D does not affect controlling the output power. This limit does not interfere with the steady-state operation with the proper design procedure. However, considering the transients as the load rejection, this limit can be achieved. The control design considerations section presents a simple solution for this problem, allowing the correct system operation with the hybrid modulation for any system transient.

III. CONVERTER ANALYSIS

The converter operation is presented considering the alternated input voltage at the positive semi-cycle and half of the operation stages are shown due to the symmetry of the circuit operation.

A. OPERATION STAGES AT STEADY STATED

The system operation is presented, operating close to the boundary of the CCM and DCM, and with the maximum duty-cycle (D=0.5), which is the recommended operation point for the nominal specification. There are sixteen operation stages of the proposed structure. Due to the symmetry, Fig.5 shows the equivalent circuit diagram of the first eight operation stages.

Stage 1 [$t_0 < t < t_1$]: At the first operation stage, S_3 is switched off in the previous stage (Stage 16), and the junction capacitor C_{S3} begins to charge. Meanwhile, the secondary of the transformer has zero voltage, and the output diodes D_{o1} and D_{o4} start to conduct. The current in D_{o2} and D_{o3} decreases. The junction capacitor C_{S1} discharges until the voltage reaches zero, when this stage ends, at t_1. The equivalent circuit of stage 1 is presented in Fig. 5(a).

Stage 2 [$t_1 < t < t_2$]: This stage starts at t_1 when the body diode D_{S1} starts to conduct. At the same time, the input rectifier diode D_1 starts to conduct, and the current in L_{f1} increases. The voltage across S_3 and S_2 is equal to the bus voltage. This stage ends at t_2, when S_1 is commanded to conduct. The equivalent circuit of stage 2 is presented in Fig. 5(b).

Stage 3 [$t_2 < t < t_3$]: At t_2, S_1 is commanded to conduct at zero voltage. (The direction of the S_4 current changes, after the inductor L_r is fully discharged). This stage finishes at t_3 when the output diodes D_{o2} and D_{o3} are reverse biased. The equivalent circuit of stage 3 is presented in Fig. 5(c).

Stage 4 [$t_3 < t < t_4$]: This stage starts at t_3 when the output diodes D_{o2} and D_{o3} are blocked. This stage ends at t_4. The equivalent circuit of stage 4 is in Fig. 5(d).

Stage 5 [$t_4 < t < t_5$]: This stage starts at t_4, when the direction of the S_1 current changes. This stage ends at t_5. The equivalent circuit of stage 5 is presented in Fig. 5(e).

Stage 6 [$t_5 < t < t_6$]: At t_5, the current of L_{f2} reaches zero and D_4 is blocked. This stage finishes at t_6 when S_4 is switched off. The equivalent circuit of stage 6 is presented in Fig. 5(f).

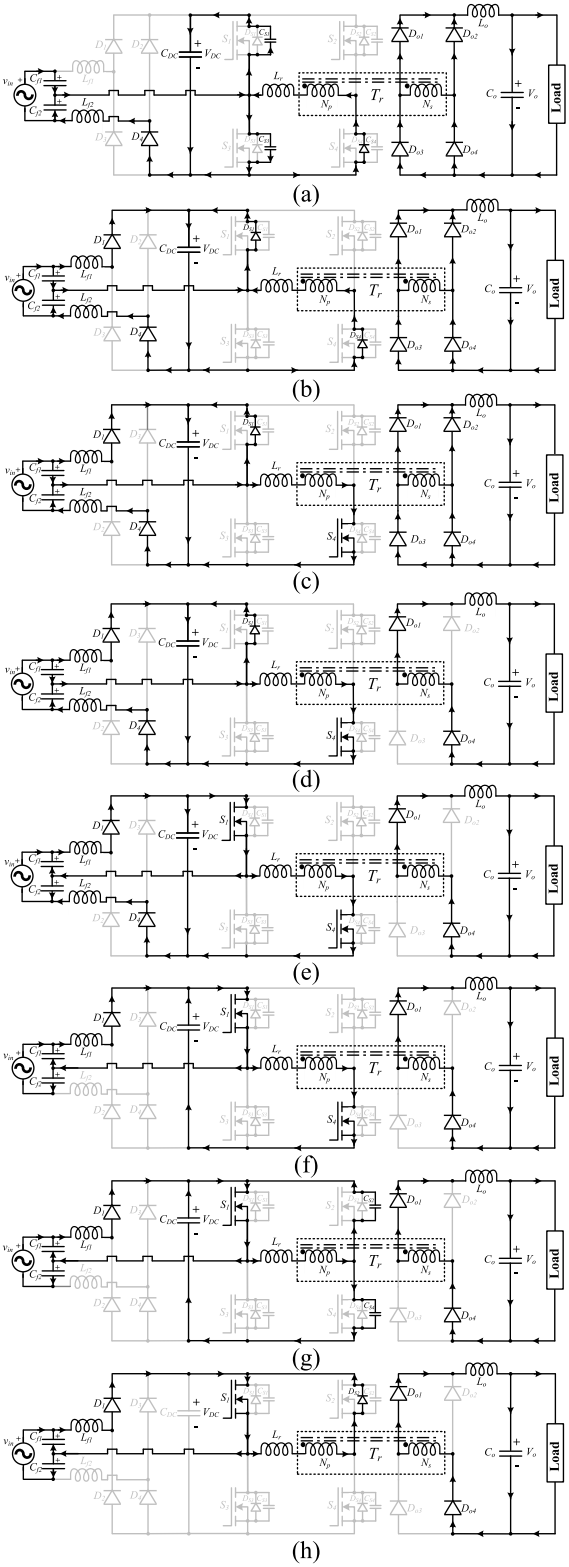


FIGURE 5. Operation stages: (a) Stage 1 [t_0 - t_1]. (b) Stage 2 [t_1 - t_2]. (c) Stage 3 [t_2 - t_3]. (d) Stage 4 [t_3 - t_4]. (e) Stage 5 [t_4 - t_5]. (f) Stage 6 [t_5 - t_6]. (g) Stage 7 [t_6 - t_7]. (h) Stage 8 [t_7 - t_8].

Stage 7 [$t_6 < t < t_7$]: At t_6, S_4 is switched off. In this stage, the junction capacitor C_{S2} starts to discharge until it reaches zero. The junction capacitor C_{S4} begins to charge until it reaches the bus voltage at t_7. The equivalent circuit of stage 7 is presented in Fig. 5(g).

Stage 8 [$t_7 < t < t_8$]: At t_7, after the intrinsic capacitor C_{S2} discharges, the body diode D_{S2} starts to conduct, and just after this, S_2 is turned on at zero voltage. At the end of this stage, S_1 is switched off. The equivalent circuit of stage 8 is presented in Fig. 5(h).

From the eighth stage of operation onwards, there is symmetry, in which the intrinsic capacitors on the left arm of the inverter exchange energy, similar to what occurs in the first stage, and so the stages follow. The key operation waveforms of the converter with D=0.5 are shown in Fig. 6. The interleaving effect can be seen in Fig. 6, where the input current is in CCM, even though the current through each inductor is in DCM [34].

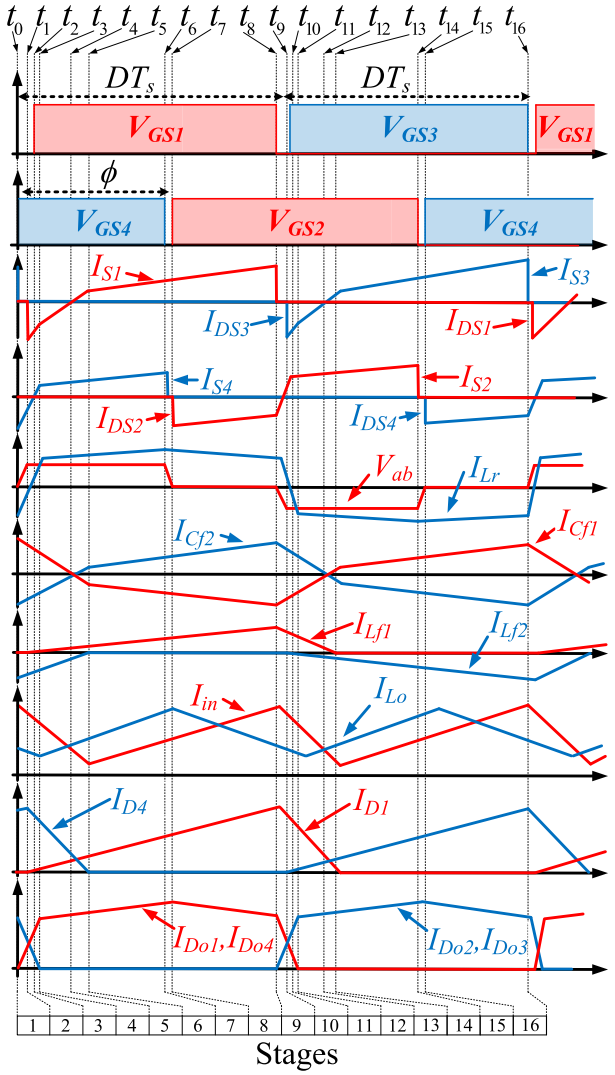


FIGURE 6. Main theoretical waveforms at steady state operation.

All power switches operate with ZVS commutation. The input current presents reduced ripple due to the interleaved operation of the input inductors.

The soft switching of the integrated converter can be analyzed by the traditional phase-shift full-bridge ZVS switching. The ZVS of the switches can be achieved through the exchange of energy between the resonance inductor and the parasitic capacitors of the switches [35]. In this way, critical switching occurs in the arm composed of switches S_1 and S_3. It depends on the exchange of energy between the parasitic capacitance (C_{S1} and C_{S3}) of the switches and the resonance inductance.

IV. DESIGN PROCEDURE

This section presents the design procedure for the proposed converter with active ripple reduction control.

A. DESIGN CONSIDERATIONS

Table 2 presents the main specifications of the converter.

To simplify the design of the converter, it can be carried out initially considering the traditional design of the full-bridge converter, just defining the basic ripple parameters, as shown in Fig. 7. In this way, some already well-known equations are not presented. As can see in Fig. 7, during the steady state, the function of the phase-shift (ϕ) is to keep the reduced output voltage ripple. Therefore, it must vary from a minimum value ϕ_{min} to a maximum value ϕ_{max}. When the

TABLE 2. Specifications of the prototype.

Symbol	Description	Value
v_{in}	Input voltage	127 Vrms
P_o	Output power	300 W
V_o	Output voltage	250 V
f_r	Line frequency	60 Hz
f_s	Switching frequency	50 kHz
R_o	Nominal load	208.33 Ω
ΔI_{Lo}	Current ripple of L_o	50%
ΔV_{DC}	Voltage ripple of C_{DC}*	30%
ΔV_o	Voltage ripple of C_o**	0.05 V(0.02%)
V_{DC}	Bus voltage	270 V

*low frequency($2f_r$) **switching frequency

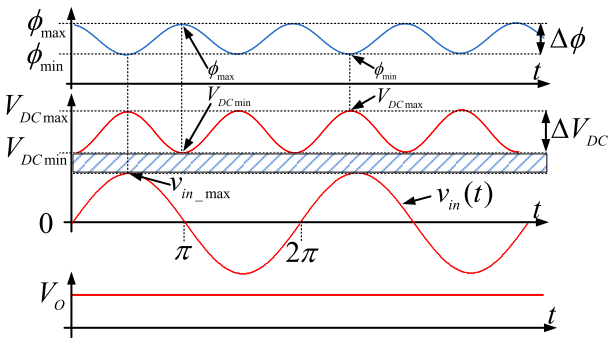


FIGURE 7. Limits of the ripple of the phase-shift variation at nominal power.

bus voltage is minimum (V_{DCmin}), it must be sufficient to maintain the output voltage at the desired level. Therefore, the ϕ_{max} must be slightly below 1, allowing certain operating flexibility. At the instant in which the bus voltage is maximum (V_{DCmax}), the phase-shift (ϕ) will be lower. Another detail is the choice of the minimum bus voltage. Due to the operating characteristic of the rectifier, this voltage must be above the peak voltage of the input voltage to avoid distortion of the input current. The minimum bus voltage can be close to the peak of the AC input voltage in the proposed structure.

Based on these maximum and minimum voltage limits, the DC bus capacitor ripple can be specified, implying the maximum voltage on the converter components. Therefore, a low-frequency ($2f_r$) ripple of approximately 30% of the bus voltage was chosen. The required bus capacitance value for the desired ripple is found by (1)

$$C_{DC} = \frac{2P_o}{2\pi f_r (V_{DCmax}^2 - V_{DCmin}^2)} \cong 40\,\mu F. \tag{1}$$

Considering (2), the value of the auxiliary variable R_d is obtained, which will be used to obtain the maximum and minimum values of phase-shift (ϕ) by (3) and (4). Using a transformer with a transformation ratio of 1.36 (N_S/N_P), it is possible to find the value of the maximum and the minimum phase-shift (ϕ).

$$R_d = 4\left(\frac{N_S}{N_P}\right)^2 L_r \cdot f_s = 31.4 \tag{2}$$

$$\phi_{max} = \frac{V_o}{\frac{N_S}{N_P} V_{DCmin} / \frac{R_d}{R_o} + 1} \cong 0.91 \tag{3}$$

$$\phi_{min} = \frac{V_o}{\frac{N_S}{N_P} V_{DCmax} / \frac{R_d}{R_o} + 1} \cong 0.67 \tag{4}$$

The output capacitor is designed according to the (5) considering the high-frequency ripple, as the control will be responsible for attenuating the low-frequency ripple (120 Hz). Output inductor can be designed by (6) to operate in continuous conduction mode (CCM).

$$C_o = \frac{\Delta I_o \cdot I_o}{16 \cdot f_s \cdot \Delta V_o \cdot V_o} = 15\,\mu F \tag{5}$$

$$L_o = \frac{V_o(1-\phi_{min})}{2 \cdot f_s \cdot \Delta I_o \cdot I_o} = 1.4\,mH \tag{6}$$

The input rectifier elements are designed according to [34], where the value of input inductors can be determined (7). Where v_{in_max} correspond to $v_{in}\sqrt{2}$.

$$L_{f1}, L_{f2} = \frac{v_{in\_max}^2}{8 \cdot P_o \cdot f_s} 0.329 = 88.3\,\mu H \tag{7}$$

The input capacitors are designed by (8)

$$C_{f1}, C_{f2} = \frac{1}{4 \cdot \pi^2 \cdot f_s^2 \cdot 0.22^2} = 2.2\,\mu F. \tag{8}$$

The main designed converter parameters are shown in Table 3.

TABLE 3. Designed converter parameters.

Symbol	Description	Value
$L_{f1} = L_{f2}$	Input filter inductor	88.3 μH
$C_{f1} = C_{f2}$	Input filter capacitor	2.2 μF
L_r	Resonance inductor	88 μH
f_s	Switching frequency	50 kHz
L_o	Output inductor	1.4 mH
T_r	Transformer	N_S/N_P=103/76
C_{DC}	Bus capacitor	40 μF
C_o	Output capacitor	15 μF

The primary function of the resonant inductor (L_r) in series with the transformer is to assist in ZVS switching when the output current level is reduced. Furthermore, a large resonance inductance increases the converter stability. However, a high inductor value implies a more significant loss of effective power transfer to output. This way, an intermediate inductor allowing around 10% loss of effective power transfer was chosen.

Following the methodology presented in [36], it is possible determine the minimum output current at which it still occurs soft switching is approximately 0.44 A, which is equivalent to 35% of output power.

V. CONTROL SYSTEM

The proposed control system is relatively simple and can be divided into output voltage control and DC bus voltage control, as can be seen in the block diagram presented in Fig. 8. The phase-shift represents the phase difference between the inverter arms and controls the output voltage. The output voltage controller is designed to be fast enough to actively reduce the low-frequency ripple and also regulate the output voltage. Using a controller that provides zero error at steady state is essential, as the output voltage is also kept constant through this control. A proportional-integral (PI) with a lag controller was chosen for the fast output voltage control.

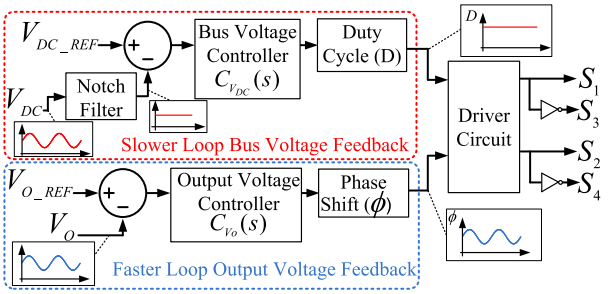


FIGURE 8. Control block diagram circuit of the integrated converter.

It is characteristic of the boost rectifier to increase the DC bus voltage by reducing the load supplied to the output. Therefore, the bus voltage tends to rise for power lower than nominal. The second control variable, the duty-cycle (D), can control this voltage. Consequently, these two controls (ϕ, D) act in parallel to control the bus and output voltage

simultaneously. The PFC of the converter is compromised if the duty-cycle has a significant periodic variation. It is desired that the duty-cycle is as constant as possible in a semi-cycle of the input voltage. The bus voltage control loop must not respond to the frequency of the DC bus voltage ripple. Therefore, the bus voltage measurement inserts a selective notch filter tuned to 120 Hz ($2f_r$). This second-order filter allows a more significant rejection of the DC bus low-frequency ripple and does not limit the controller design at a low crossover frequency.

The DC bus voltage should have a certain freedom within the limits established by design. Therefore, it is recommended to use a controller that allows a small error in a steady state. Therefore, a lag controller is used to control the DC bus voltage. Furthermore, as the duty-cycle is used to keep the DC bus voltage controlled, the controller is designed so that at rated power, the duty-cycle is kept fixed at D=0.5.

A. CONTROL DESIGN CONSIDERATIONS

The output voltage transfer function full-bridge converter is used for the control design. By substituting the values, it is possible to find (10) that represents the output voltage as a function of the phase-shift variable control.

$$\frac{V_o(s)}{\phi(s)} = \frac{\frac{N_S}{N_P} V_{DC}}{s^2 \cdot L_o \cdot C_o + s\left(\frac{L_o}{R_o} + R_d \cdot C_o\right) + \frac{R_d}{R_o} + 1} \tag{9}$$

$$\frac{V_o(s)}{\phi(s)} = \frac{365.921}{2.0999 \times 10^{-8} s^2 + 0.000669 s + 1.2145} \tag{10}$$

As discussed previously, this controller must have a fast enough response to attenuate the 120 Hz ripple present at the output. The design of this controller is classical and carried out in the s-plane, using Bode diagrams. It is considered a system crossover frequency of 1200 Hz, prioritizing a high gain close to 120 Hz to reduce the steady-state error in this frequency and the low-frequency ripple. A simple proportional-integral (PI) controller was used together with a lag controller, as shown in (11). The PI controller provides zero error in a steady state and helps with stability, while the lag Controller improves system response at this frequency of 120 Hz.

$$C_{Vo}(s) = K_p \frac{(s + \omega_{z\_PI})(s + \omega_{z\_lag})}{s(s + \omega_{p\_lag})} \tag{11}$$

Also, adding the voltage sensor gain in (10) the (12) represents the controller designed in the frequency domain.

$$C_{Vo}(s) = \frac{1.04 \times 10^{30} s^2 + 1.67 \times 10^{33} s + 1.57 \times 10^{35}}{2.5 \times 10^{29} s^2 + 9.424 \times 10^{31} s} \tag{12}$$

The Bode plot of the V_o transfer function is presented in Fig. 9, where it is possible to observe that after the compensation, the gain is high at low frequency, especially at 120 Hz.

Bus voltage control can be designed with the help of the equation of a traditional boost rectifier operating in discontinuous conduction mode (DCM). Equation (13) represents the DC bus voltage in relation to the duty-cycle.

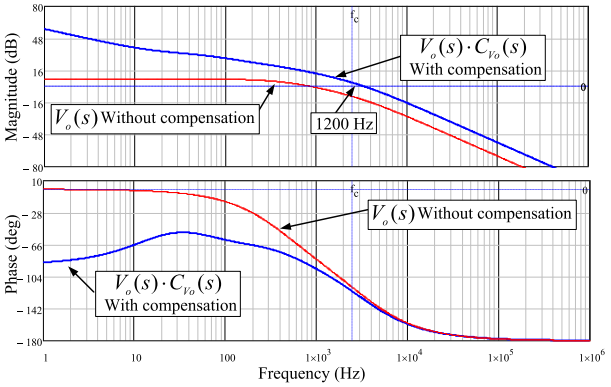


FIGURE 9. Transfer function Bode plot of V_o.

$$\frac{V_{DC}(s)}{D(s)} = \frac{270}{0.00243 s + 1} \tag{13}$$

The Bode plot of the transfer function of second order notch filter is presented in Fig. 10 where it is possible to observe that the attenuation is centering at 120 Hz. That prevents the controller $C_{V_{DC}}(s)$ from being affected by the low-frequency ripple in the DC bus voltage.

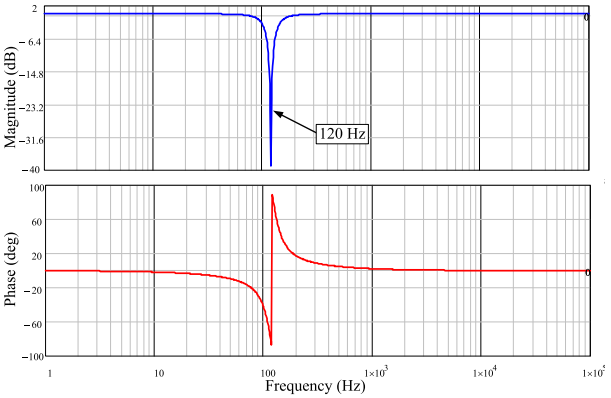


FIGURE 10. Transfer function Bode plot of notch filter.

The most suitable DC bus voltage controller $C_{V_{DC}}(s)$ is a lag compensator since, as mentioned before, zero error at bus voltage is not necessary at steady state. Equation (14) shows a lag compensator, in which, $\omega_p < \omega_z$.

$$C_{V_{DC}}(s) = K_p \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \tag{14}$$

In this case, the system crossover frequency selection is around 40 Hz, and the controller is represented by (15)

$$C_{V_{DC}}(s) = \frac{4.0042 \times 10^{20} s + 1.6478 \times 10^{23}}{1.2149 \times 10^{21} s + 5 \times 10^{21}} \tag{15}$$

The Bode plot of the V_{DC} transfer function is presented in Fig. 11, where it is possible to observe that after the compensation, with the crossover frequency around 40 Hz.

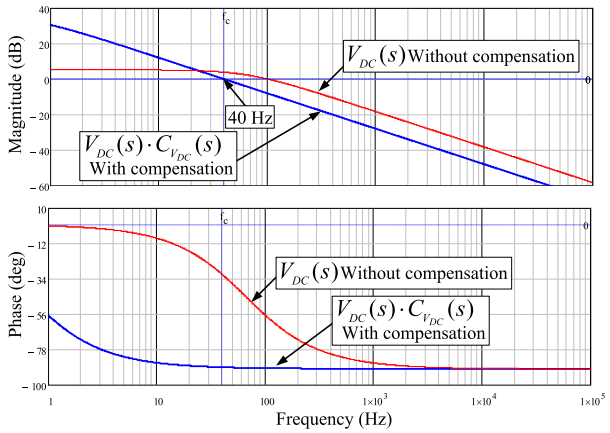


FIGURE 11. Transfer function Bode plot of V_{DC}.

The design of the two compensators was made on a continuous (plan s), making it necessary to discretize the converters for digital application. The Tustin discretization method was used, in which the processor sampling frequency is equal to the switching frequency of the switches. Output voltage and DC bus voltage compensator are shown as (16) and (17), respectively.

$$C_{Vo}(z) = \frac{4.851 - 9.549z^{-1} + 4.697z^{-2}}{1 - 1.992z^{-1} + 0.992z^{-2}} \quad (16)$$

$$C_{V_{DC}}(z) = \frac{0.3309 - 0.3282z^{-1}}{1 - 0.9999z^{-1}} \quad (17)$$

Due to the DC bus response being slowest compared to the output voltage loop, for load variations, the ϕ variable may quickly assume a high value to maintain the power drained by the load. However, the duty-cycle may take longer to stabilize and reach the required value. In these transient situations, the $\phi = 2D$ limit presented in Fig. 4 may be exceeded. As a solution to this condition, it is adopted that the minimum value at the compensator output of the duty-cycle is equal to $\phi/2$. This ensures control flexibility and a fast duty-cycle response during the transient period.

Limiting the duty-cycle at a minimum value $\phi/2$ in a transient presents a DC bus voltage increment. The instantaneous ϕ imposed by the voltage control loop will be reduced when the DC bus increase, changing the limit for other point. This instantaneous and dynamic adjustment of the minimum duty-cycle ensure the maximum power transfer to the output at the transients and the DC bus voltage variation occurs in a limited range, as presented in the experimental results.

VI. EXPERIMENTAL VERIFICATION

The experimental results are obtained from a 300 W prototype, presented in Fig. 12. The equipment used to acquire the waveforms was an oscilloscope Tektronix DPO 3014 and power values wattmeter: Yokogawa WT500. Digital control was implemented using the Launchpad F28379D. The main converter components are shown in Table 4.

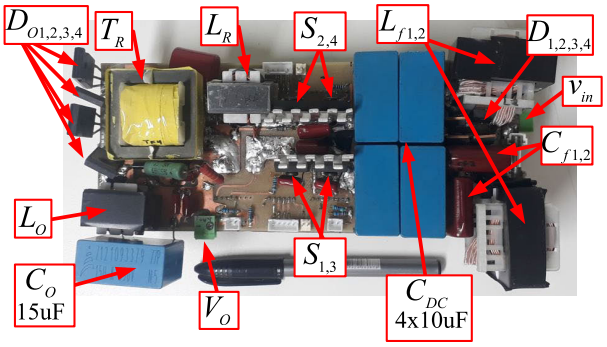
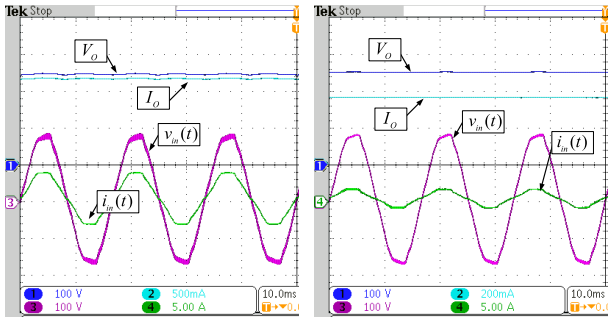


FIGURE 12. Photograph of the experimental prototype.

TABLE 4. Converter components.

Symbol	Description	Part Number/Value
$S_1, ..., S_4$	MOSFET	IPW65R019C7
$D_1, ..., D_4$	Input diode	MUR 1560
$D_{o1}, ..., D_{o4}$	Output diode	CSD10120D
C_{f1} e C_{f2}	Input filter capacitor	2.2 μF, 250V
C_{DC}	Bus capacitor	4x10 μF*, 450 V
C_o	Output capacitor	15 μF*, 450 V
T_r	Transformer	Epcos E42/21/15 N87(103:76)
L_o	Output inductor	Thornton, E30/14 (1.2 mH)
L_{f1} e L_{f2}	Input filter inductor	Epcos E42/21/15 N87 (88µH)
L_r	Resonance inductor	Thornton, E42/15 (88 µH)
	Controller	F28379D

*Polypropylene capacitor



(a) (b)

FIGURE 13. Waveform of the v_{in}, i_{in}, V_O and I_O (a) in 100% of load and (b) 30% of load condition.

Figure 13(a) shows the main waveforms of the converter operating at nominal load and Fig.13(b) at 30% load. With active ripple reduction on, the output voltage V_o, in both situations, has a small ripple. The waveforms of the output current, input voltage, and input current are also displayed. It is important to note that the input current follows the input voltage waveform, maintaining a high power factor. The harmonic spectrum of the input current is present in Fig. 14 operating at nominal load and is compared with the limits imposed by the IEC 61000-3-2 Class D [37] standard. It is possible to observe that the standard is met, and voltage ripple reduction does not significantly influence the input current. The total harmonic distortion rate obtained is 10 %.

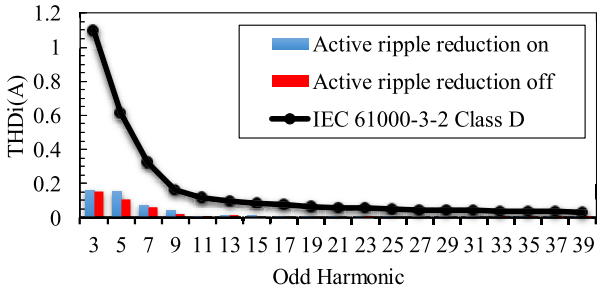


FIGURE 14. Comparison of IEC 610000-3-2 Class D current harmonic limits to the proposed converter with v_{in} = 127 Vrms and P_o = 300W.

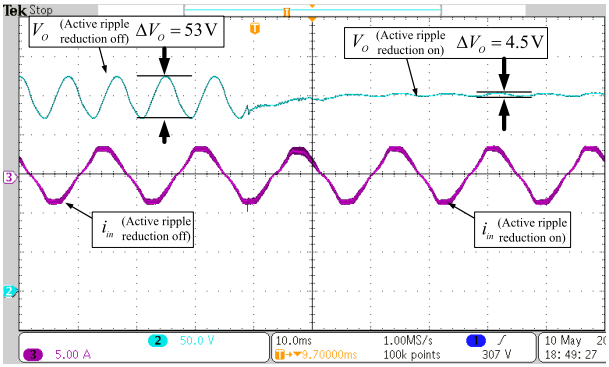


FIGURE 15. Output voltage with active decoupling on and with active decoupling off.

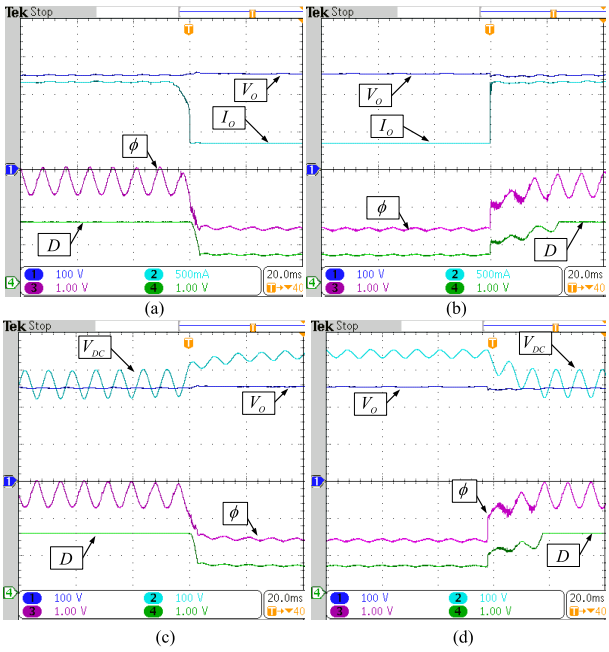


FIGURE 16. Transient waveforms with a load change (a) V_o, I_o from 100% to 30%, (b) V_o, I_o from 30% to 100%, (c) V_o, V_{DC} from 100% to 30%, (d) V_o, V_{DC} from 30% to 100%.

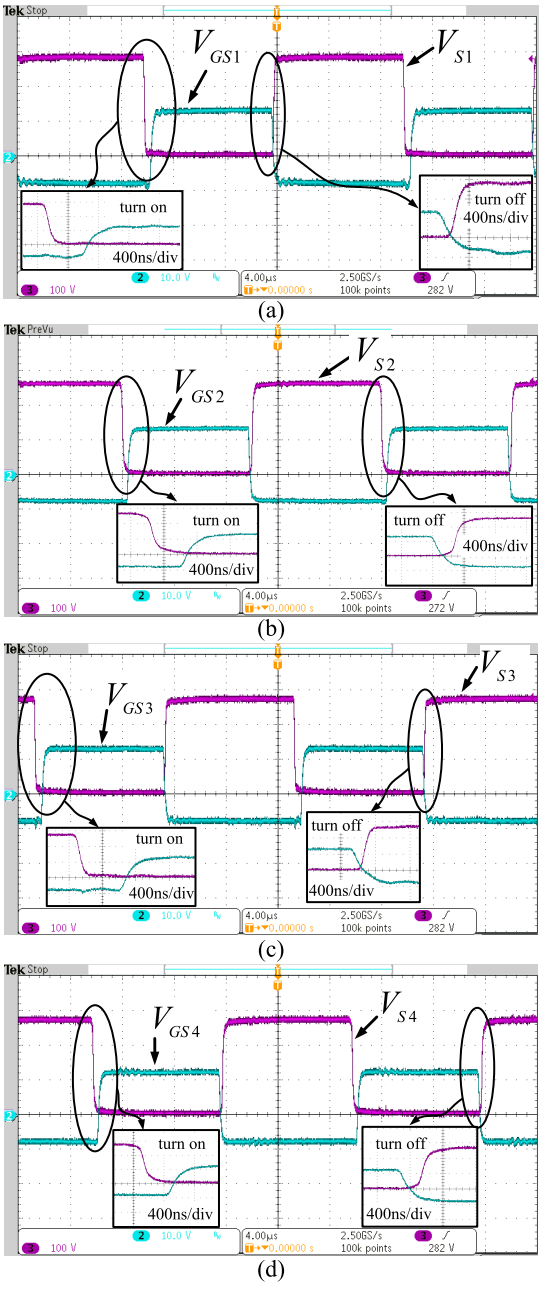


FIGURE 17. Experimental waveforms V_{GS} (gate signal) and V_S (Voltage Drain to Source) of MOSFET (a) S_1, (b) S_2, (c) S_3 and (d) S_4.

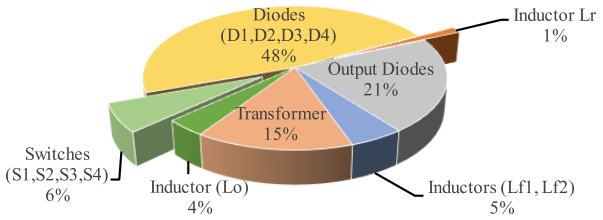


FIGURE 18. Converter losses distribution.

Figure 15 presents the output voltage waveform with the control on and off. It is possible to observe in detail that the significant variation of the 53 V in the output voltage is reduced to 4.5 V after the control is active without changing any capacitor in the circuit. It is important to observe that the input current waveform and the converter efficiency are unchanged even with the intrinsic active low-frequency ripple

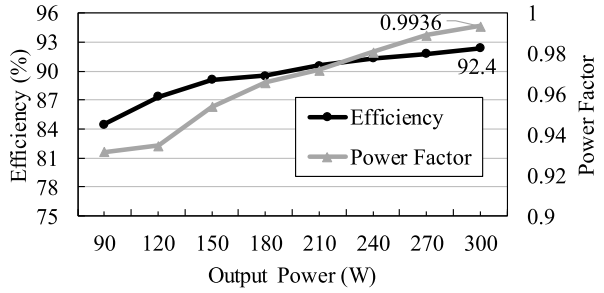


FIGURE 19. Efficiency and Power Factor curve of the proposed converter under different power output (30% to 100%).

reduction is turned on. For comparison purposes, without the active ripple reduction control, it is necessary to use a capacitor of approximately 500 μF to obtain the same voltage ripple of the 5 V at the output. Thus, using the proposed modulation, it is possible to reduce the capacitance of the output capacitor by approximately 33 times. This makes it possible to avoid the use of electrolytic capacitors.

The dynamic performance of the converter to load step is presented in Fig. 16. It is possible to observe in Fig. 16(a) and Fig. 16(b) that the output control is fast and stable, and the waveform of V_o does not present a significant change even with a reduced capacitor in the output. As shown in Fig. 16(c), the bus remains controlled even with a considerable load reduction limiting the DC bus voltage variation. During the return to nominal load (Fig. 16(d)), the duty-cycle returns to a nominal value and enters a steady state. As seen in Fig. 16, the duty-cycle responds quickly despite the bus controller being slower than the output. Figure 17(a), Fig. 17(b), Fig. 17(c) and Fig.17(d) show the ZVS in switches S_1, S_2, S_3 and S_4 under nominal load conditions. The trigger is set to acquire at instantaneous peak input voltage ($\pi/2$). The estimated loss distribution for the converter is shown in Fig. 18. As can be seen, the input diodes are responsible for the most significant losses followed by the output diodes. Figure 19 shows the efficiency and Power Factor measured for different output power values. Under nominal load conditions, the PF is 0.9936, and the efficiency was 92.4%. The efficiency obtained with the converter with active ripple control at the output voltage on and off had no significant difference, demonstrating that ripple reduction has minimal influence on losses.

VII. CONCLUSION

This paper aims to propose an application of a hybrid modulation in an integrated converter that can significantly reduce the storage capacitance, allowing the elimination of the electrolytic capacitor to achieve a long lifetime of the converter. The converter input rectifier stage works in DCM and does not need a current sensor to achieve PFC. However, in high-power applications, the DCM is not indicated. The ZVS operation in all switches is obtained by integrating the interleaved boost rectifier and a full-bridge ZVS DC-DC converter. A simple and robust control scheme is also proposed, which allows to get a fast transient control of the output and DC bus voltage. This paper also presents a methodology to project the limits that can be used to select the value for the bus capacitor. In order to validate, a prototype with 300 W was implemented, and it was demonstrated that when activating the active output voltage ripple reduction control, a reduction of approximately 33 times in capacitance was obtained. The converter has a power factor of 0.9936 and an efficiency of 92.4% when operated at full load. The results also demonstrated that the converter used with harmonic distortion within the limits imposed by the IEC 610000-3-2 Class D standard.

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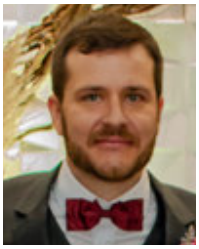

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