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RESEARCH ARTICLE

Influence of Reverse Conduction on Dead Time Selection in GaN-Based Inverters for AC Motor Drives

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ABSTRACT Although Gallium Nitride (GaN) Field Effect Transistor (FET) devices have found extensive application in DC-DC converters, their utilization in inverter motor drives remains an evolving area of study. In particular, the intricacies of reverse conduction operation during the dead time, specific to GaN FETs, require in-depth exploration for inverters supplying AC currents to electrical motors. Therefore, this paper undertakes an assessment of reverse conduction during the dead time intervals in low-voltage GaN FETs employed in motor drives applications. This analysis provides correlations between device technology attributes and the variations in AC phase current. To facilitate this investigation, a dedicated numerical tool is developed to evaluate the reverse conduction characteristics of GaN FET and associated power losses. Furthermore, this study includes a comparative analysis of the reverse conduction behavior of GaN FET devices with their low-voltage MOSFET counterparts, taking into account their differing static and dynamic characteristics. As a result, the main contribution of this work is to provide to the inverter designers a comprehensive understanding of dead-time effects in GaN-based inverters, along with guidance on selecting and optimizing dead time intervals within inverter legs for motor control applications employing the latest generation of GaN FET devices.

INDEX TERMS GaN FET, MOSFET, dead time, reverse conduction, body diode, inverter drive.

I. NOMENCLATURE

GaN FET	Gallium Nitride Field Effect Transistor.
HEMT	High Electron Mobility Transistor.
2DEG	Two-Dimensional Electron Gas.
MOSFET	Metal Oxide Silicon Field Effect Transistor.
IMMD	Integrated Modular Motor Drive.
BLDC	BrushLess Direct Current motor.
PMAC	Permanent Magnet AC motor.
FOC	Field-Oriented Control Algorithms.
THD	Total Harmonic Distortion.
DFT	Direct Fourier Transform.
ZVS	Zero Voltage Switching.
PHS	partial hard switching.
HS, LS	High-Side, Low-Side.
Q_{HS}, Q_{LS}	Half-Bridge high-side and low-side device.
V_{gHS}, V_{gLS}	Gate signal commands for HS and LS Devices (V).
V_{GS}	Gate-Source Voltage (V).
V_{SD}	Source-Drain voltage drop (V).
Q_{rr}	reverse recovery charge (C).
V_{GSth}	Threshold Gate-Source Voltage (V).
R_{DSon}	Direct resistance of the switches (Ω).
C_{oss}	Parasitic output devices capacitances (F).
C_{load}	Parasitic capacitance introduced by the motor (F).
V_{DC}	Bus Voltage (V).
V_{DS}	Drain-Source Voltage (V).

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dV_S/dt	Half Bridge node voltage slew rate (V/s).
v_{tr}	Triangular carrier signal (V).
v_{mod}	Modulation control voltage (V).
t_{dt}	Dead time (s).
t_{rc}	Reverse conduction time (s).
t_f	fall time at maximum dV_S/dt (V/s).
t_{zvs}	Zero Volt Switching time (s).
$I_{a,b,c}$	Inverter current for phases a, b and c (A)
f_{load}	Fundamental motor current frequency (Hz).
I_{load}	Half-Bridge output load current (A).
I_{MAX}, I_{min}	The threshold currents in the t_{rc} range (A).
E_{rc}	Reverse conduction Energy Losses(J).
E_{hs}	Hard switching losses.
P_{rc}	Reverse conduction Power Losses (W).
P_{Grc}, P_{Mrc}	Reverse conduction Power Losses for GaN FET and MOSFET (W).
q_E	Charge injection into the depletion region of a body diode (C).
q_M	Stored charge in the depletion region of a body diode (C).
T_M	Charge diffusion time in a body diode (s).
τ	Recombination time constant of the depletion region of a body diode (sec).
$I_{S,LM}$	Saturation current of the body diode used in the SPICE model (A).
V_{Diode}	Voltage drop of the diode without considering the voltage drop due to the series resistor (V).
T_J	Junction temperature (K).
k	Boltzmann's coefficient.

II. INTRODUCTION

Nowadays, wide bandgap devices are increasingly used in power electronics systems. In low-voltage systems, GaN technology-based switches gradually replace Silicon (Si) MOSFETs in applications such as DC-DC power converters due to their favorable thermal characteristics, small device size and high dynamic performance. In DC-AC converters, GaN technology is much more attractive because the High Electron Mobility Transistors (HEMTs) can operate at higher switching frequencies compared with Si MOSFET, improving motor efficiency [1].

The increase in the switching frequency minimizes the current ripple in the motor. Furthermore, a higher switching frequency enables a reduction of the overall capacitance value of the DC link, allowing the replacement of electrolytic capacitors with smaller non-polarized capacitors [2].

The high-power density of GaN FETs facilitates the creation of compact AC drive systems that seamlessly integrate the motor and drive components into a single unit. This design approach enables the development of Integrated Modular Motor Drives (IMMDs) suitable for both three-phase and multi-phase solutions [3]. In an inverter system, a critical parameter is the dead time that influences the quality of the voltage's output waveforms. A large dead time increases the number of harmonics, thus worsening the total harmonic distortion (THD) [4]. Minimizing the dead time interval not only has a positive impact on improving the quality of the output phase current waveforms but also serves to significantly reduce the torque ripple in motor drive applications along with enhanced motor performance, reduced electromagnetic interference, and improved overall efficiency in motor control systems. Therefore, optimizing the dead time is a crucial consideration for achieving superior performance and minimizing undesirable effects in motor drive applications [5].

TABLE 1. Literature summary and contributions of this paper.

Reference	Contributions
[5]	Advantages of GaN-enabled dead-time reduction in motor drives
[6]	Dead-time optimization in GaN DC/DCs
[7-9]	Dead-time phenomena in GaN devices
[10-11]	Dead-time in Silicon MOSFETs
This work	Comprehensive analysis of reverse conduction during dead-time. Analysis of losses dependance on the load when supplying motor drives.

Given the switching frequency and the input dc voltage, the phase voltage distortion produced by dead time is affected by its time length. The correct dead time selection is of paramount importance in GaN FET devices. Reducing both the rise time and the fall time substantially reduces the dead time in the leg-switching circuits [6]. During the dead time interval, the GaN FET operates in a reverse conduction mode [7]. In this reverse conduction state, the GaN FET exhibits characteristics akin to an equivalent diode, albeit with a higher voltage drop. Unlike Si MOSFETs, GaN FETs do not experience the reverse recovery phenomena typically associated with the body diode [8]. This unique behavior of GaN FETs during reverse conduction has significant implications for their performance in power electronics applications.

In AC motor control applications, the amplitude and direction of the sinusoidal current waveform significantly impact the rate of voltage change (dv/dt) across the devices within the inverter legs during switching operations [9]. These dv/dt characteristics, along with the current level, play a crucial role in determining reverse conduction power losses.

The dead time effect is explored deeply in the literature, especially in the case of DC-DC converters and Si MOSFET devices [10], [11], however low-voltage GaN FET in a DC-AC converter for motor drives application requires additional studies. In Table 1 a summary of the main literature contributions is reported, highlighting the article target.

The recent HEMT technology dynamic characteristics allow us to regulate the dead time more strictly, obtaining significant advantages that merit better understanding and exploration. Furthermore, the differences between the GaN FET and Si MOSFET in reverse conduction during the dead time need a deep investigation to consider advantages and drawbacks, giving guidelines to the inverter designers on the

use of HEMT switches in DC-AC converters in the proper way.

The contribution of this article is a detailed analysis of the reverse conduction during the dead time of the last generation of the GaN FET in low voltage (<100V) motor applications, currently widespread in both industrial applications (automation and robotics) and in light traction (e-bikes, scooters, drones, etc.) [8], [13].

Furthermore, the reverse conduction investigation is applied to a low-voltage Si MOSFET to compare the advantages and drawbacks in the dead time selection using the two different technologies.

This article is an extension of [14] and brings in the following added value:

1) A complete analysis of the reverse conduction of GaN FETs along with the impact on the dead-time that is adopted for inverters supplying three-phase motors.
2) A novel numerical methodology based on the deeper analysis of the switching waveforms in reverse conduction to study the dead time effect and losses in the case of motor load with sinusoidal variable waveforms. The investigation considers the variation from zero voltage switching (ZVS) to hard switching operative conditions depending on the half-bridge switching node voltage slope (dv/dt) and the variable phase-leg current sign and amplitude.
3) An experimental comparison between two Half-Bridge boards with similar layouts, one with GaN FETs and one with equivalent nominal current and voltage Si MOSFETs, demonstrating the different dead time requirements between the two technologies and to provide an energy losses estimation during the dead time length.

The article is organized as follows. Section III presents an analysis of the impact produced by the inverter dead-time in motor drive applications, while Section IV focuses on the GaN FET reverse conduction. Sections V and VI present an evaluation of additional reverse conduction losses according to the chosen dead time for GaN FET and MOSFET, respectively. Finally, the experimental comparison between two boards employing MOSFET and GaN FET is provided in Section VII.

III. DEAD TIME IMPACT IN INVERTER FOR MOTOR DRIVES APPLICATION

In the context of an inverter leg, the implementation of dead time serves a crucial purpose: preventing shoot-through scenarios during switching transients. However, it's essential to strike a balance by selecting the dead time length as small as possible. This minimization helps mitigate the non-linear effects stemming from an equivalent voltage drop within the inverter output waveforms. Consequently, this reduction in power loss attributed to dead-time effects translates into improved converter efficiency. Fig. 1 depicts a two-level inverter, which is used as a basic hardware platform for

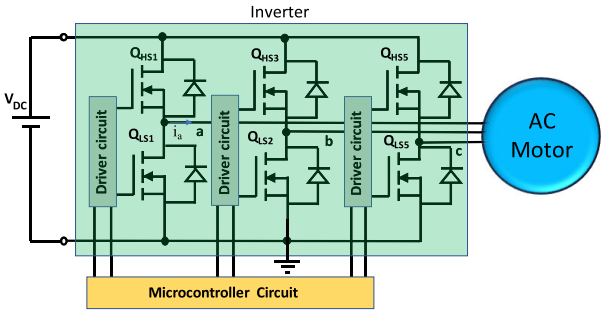

FIGURE 1. Considered inverter system architecture diagram.

evaluating dead time issues in dc-ac converter applications. The dead time analysis can be carried out by considering mainly a single phase of the inverter (see Fig.2a, being them decoupled during the switching events. The gate signal commands, V_{gHS} and V_{gLS}, are generated by comparing the triangular carrier signal v_{tr} v_{tr} with the modulation control voltage $v_{mod}v_{mod}$, as illustrated in Fig. 2b.

The impact of dead time t_{dt} on the output phase voltage, error $\Delta v\Delta v$, can be expressed as [5]:

$$\Delta v = \frac{4}{3} \cdot f_{sw} \cdot V_{DC} \cdot t_{dt} \cdot sign\,(I_a) \tag{1}$$

Consequently, the waveform of the average output voltage will display a discontinuity represented by ΔV when the current changes its sign, as shown in Fig. 2c.

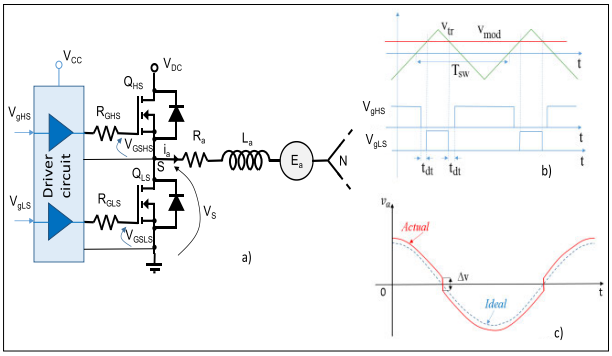

FIGURE 2. a) Inverter phase a. b) PWM command generation with dead time. c) Dead time effect on the average of the output voltage generated by phase a.

A three-phase inverter experimental board (EPC9145 [8]) driving a BLDC motor is used as a case study. The inverter is operated with a dc-link voltage of 48V at a switching frequency of 40 kHz, while the maximum motor load current is equal to 10 A_{peak} (typical switching frequency choice of the latest generation of low-voltage Silicon MOSFET-based inverters).

The application field is related to light vehicle electrification (e-bike, e-scooter) [8]. Two dead times t_{dt} lengths have been selected, as described below:

1. t_{dt1} = 500 ns, which is typical of the Silicon (Si) MOSFETs
2. t_{dt2} = 14 ns, for the GaN FETs.

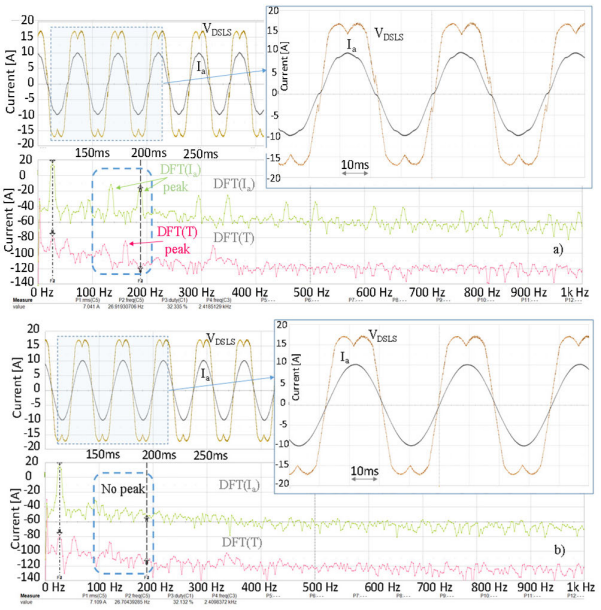

FIGURE 3. Motor phase current (5A/div), phase current DFT, motor torque (500 mV/Nm), DFT of motor torque. Case a) $t_{dt1} = 500$ ns, Case b) $t_{dt2} = 14$ ns. Motor phase current $I_a = 5$ A/div. reconstructed inverter voltage $V_{DSLS} = 5$ V/div. DFT of the mechanical torque 500 mV/Nm. DFT of the inverter phase current, t = 50 ms/div, zoom view t = 10ms.

Fig. 2a shows the phase of a motor current, its Direct Fourier Transform (DFT), and the motor torque for the case $t_{dt} = 500$ ns and an output fundamental frequency of 27 Hz.

As demonstrated by the experimental waveforms for the case $t_{dt} = 500$ ns, the dead time causes significant distortion of the motor phase currents. The distortion effect becomes evident through a spectral analysis of the phase current and mechanical torque T. As depicted in Fig. 3a, the dead time distortion leads to pronounced 5th and 7th harmonics in the phase current, consequently resulting in a significant 6th harmonic component in the mechanical torque at 161 Hz. If the dead-time is reduced to $t_{dt2} = 14$ ns thanks to the use of the GaN devices, the waveforms significantly improve, as shown in Fig. 3b. Indeed, the phase current for a dead-time of 14 ns is almost sinusoidal. As demonstrated in Fig. 2b, the low-order harmonics in the phase current and motor torque are almost eliminated.

The additional power losses due to the inverter dead-time effects need further and specific considerations, as reported in the following sections.

IV. INVESTIGATION OF GAN FET REVERSE CONDUCTION APPLIED TO AC MOTOR DRIVE

During the dead time the equivalent body diode of the power switches is brought into conduction. In this operational state, the technology of GaN FET devices significantly differs in terms of static and dynamic behavior when compared to Si technology.

A. GAN FET: REVERSE CONDUCTION OPERATION

The GaN structure is a prominent representative of High Electron Mobility Transistor (HEMT) technology, distinguished as a versatile bidirectional switching device, as highlighted in reference [15]. Its symmetric bidirectional operation is a notable feature, realized when the gate-source voltage (V_{GS}) surpasses the threshold voltage (V_{GSth}), a pivotal point at which the two-dimensional electron gas (2DEG) phenomenon manifests. The presence of this 2DEG phenomenon is instrumental, as it empowers the device with notably high electron mobility, as elucidated in reference [16]. In the context of reverse conduction, when V_{GS} exceeds V_{GSth}, the GaN FET seamlessly operates within an ohmic region, characterized by a reverse-source-drain resistance (R_{DSon}) that closely resembles the resistance observed during direct conduction, a graphical representation of which can be seen in Fig 3. Conversely, when the gate-source voltage falls below the threshold ($V_{GS} < V_{GSth}$), the dynamics of reverse conduction diverge, particularly in the context of third-quadrant operation, a detailed illustration of which is provided in Fig 4.

In a Silicon (Si) MOSFET, its physical structure incorporates a p-n junction, which plays a crucial role in facilitating reverse conduction. This specific junction structure is commonly referred to as the 'body diode,' as detailed in reference [17].

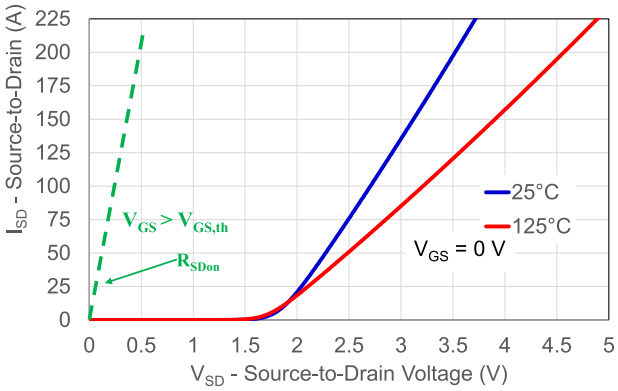

FIGURE 4. The third quadrant static operation with $V_{GS} > V_{GSth}$ (reverse on-state curve - dashed line) and the equivalent diode static curve at $V_{GS} = 0$ at two different temperatures. The direct and reverse curves are reported in the same operation quadrant for easy comparison.

However, in an enhancement-mode High Electron Mobility Transistor (HEMT) Gallium Nitride (GaN) FET, the absence of minority carrier conduction results in the absence of a body diode. Instead, an equivalent diode operation is considered, characterized by a source-drain voltage drop (V_{SD}) that exceeds that of a Si MOSFET when operating in reverse conduction. The comparison between the equivalent diode curve, depicted in Fig. 4 during third-quadrant operation at $V_{GS} = 0$ V, and the reverse conduction curve at $V_{GS} > V_{GSth}$, is illuminating. Notably, the static curve of the equivalent body diode of the GaN FET exhibits a positive temperature coefficient, as pointed out in reference [16]. Furthermore, the GaN FET equivalent diode does not exhibit any reverse

recovery charge (Q_{rr}), being this a major advantage when compared to Si devices counterpart. Consequently, during third-quadrant operation with $V_{GS} = 0$, power losses primarily stem from the conduction voltage drop of the equivalent diode, a value considerably higher than that of the body diode in an equivalent Si MOSFET. In contrast, these losses are unaffected by the Q_{rr} contribution, a notable distinction from MOSFET devices.

B. IMPACT ON THE REVERSE CONDUCTION TIME IN INVERTER LEGS

Several experimental tests are carried out to describe the impact of the load current on the reverse conduction time. The tests are performed on an inverter board set-up driving a permanent magnet (PMAC) AC motor with conventional field-oriented control algorithms (FOC) [18]. The power ratings of the inverter and AC motor used for the experimental tests are reported in Table 2. The block schematic of the electrical drive system based on EPC9145 is depicted in Fig. 5. Observing the experimental waveforms of an inverter driving an AC motor, four different switching behaviors can be distinguished. The reverse conduction is affected by four parameters:

- the output current direction,
- the current amplitude,
- the equivalent switching leg output capacitance,
- dead-time length, as imposed by the motor controller.

TABLE 2. Motor drive main characteristics.

Quantity	Symbol	value
	PMAC Motor	
Motor voltage range	V_m (V)	24-75
Nominal RMS current	I_m (A)	20
	Inverter	
Bus Voltage	V_{DC} (V)	48
Max Phase current peak	$I_{a,b,c}$ (A)	25
Switching frequency	f_{sw} (kHz)	100
Dead time	t_{dt} (ns)	50'

The application field considered for the current and voltage rate are light vehicles such as e-scooter. The main switching events for the inverter phase a are reported in Fig. 6.

In Fig. 6a is highlighted the case with positive I_a (i.e. the current is considered positive when it exits from the switching leg), while in Fig. 6b is highlighted the case with negative I_a [19]. In Fig. 6a, when the high-side device turns ON, it generates a hard switching event during the positive dv/dt. Therefore, when the current flows to the motor before the positive dv/dt, the equivalent diode of the low-side switch remains in conduction for the whole dead-time interval.

A similar condition of reverse conduction appears on the high-side device for negative dv/dt when the current is in the direction from the motor to the inverter, as shown in Fig. 6b. At low positive phase current during negative dv/dt; no reverse conduction appears (see Fig. 6a). Similarly, with the low and negative current flow, a zero reverse conduction occurs with positive dv/dt (Fig. 6b) To better analyze

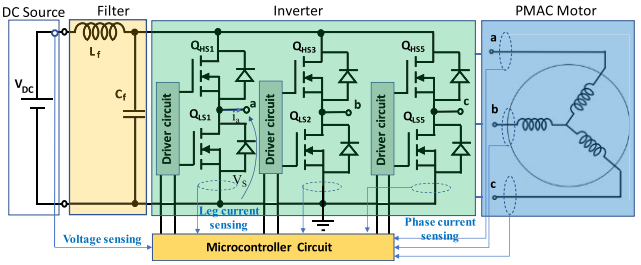

FIGURE 5. Three phases electrical drive system block schematic for the experimental tests.

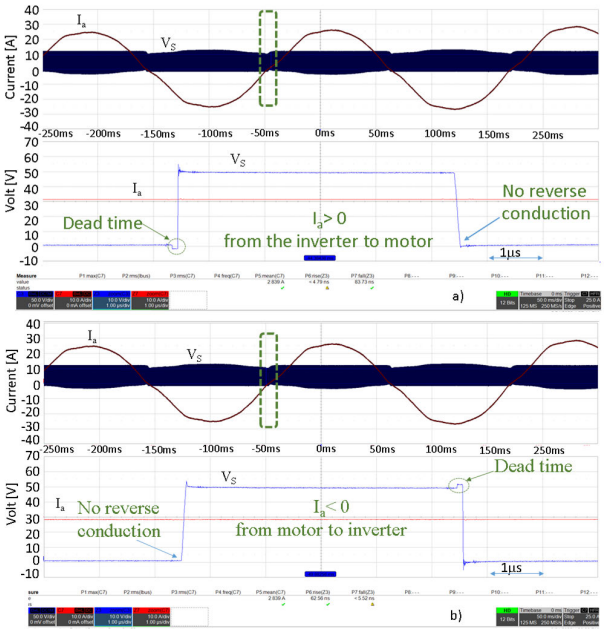

FIGURE 6. a) Positive current experimental test at low Ia. b) Negative current experimental test at low Ia. Low-frequency Figure scales $V_S = 50$ V/div, $I_a = 10$ A/div, t = 50 ms/div. Zoomed view VS = 10V/div, Ia = 10 A/div, t = 1 μs/div.

the transient behavior of the reverse conduction voltage (V_{SD}), an in-depth analysis is performed, by examining additional switching waveforms for two distinct positive load current values. Specifically, the turn-off (LS) and turn-on (LS) switching events under conditions of low positive leg current are examined, as presented in Fig. 7a and Fig. 7b, respectively.

In contrast, Fig. 7c and Fig. 7d illustrate the turn-on (LS) and turn-off (LS) transients under conditions of high positive leg current.

In the experimental results depicted in Fig. 7, it's important to note that the delay time denoted as t_{dt} between V_S and the command signals V_{gHS} and V_{gLS} is attributed to the inherent delay in the driver circuit. When the low-side switch is commanded in off state as shown in Fig. 7a and Fig. 7c, the current flows in the body equivalent diode of the low side device throughout the entire dead time duration, t_{dt}. Subsequently, after the conclusion of the dead time period, the high-side device HS is activated, redirecting the current

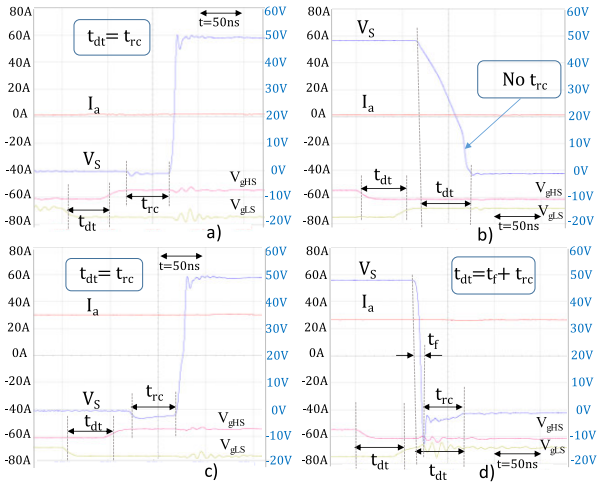

FIGURE 7. Switching waveforms illustrating LS device V_S transitions at two distinct positive load current levels: a) turn-off at low positive current, b) turn-on at low positive current. c) turn-off at a high positive current, d) turn-on at a high positive current. Notably, the dead time duration (t_{dt}) is set to 50 ns. The voltage scale (V_S) is 20 V/div, the current scale (I_a) is 10 A/div, and the gate-source voltage scales (V_{gHS} and V_{gLS}) are both 10 V/div. The time scale (t) is 50 ns/div.

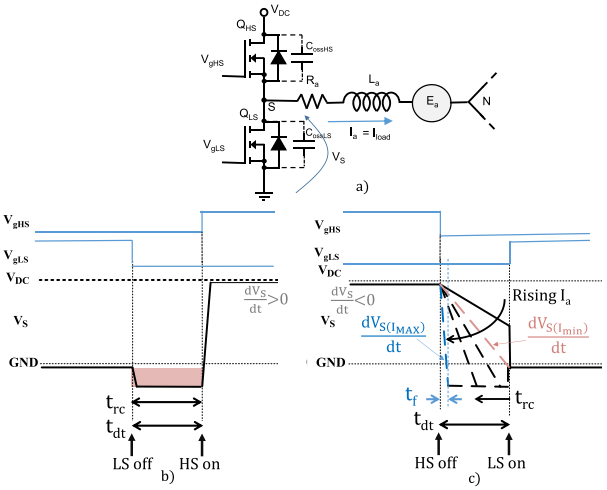

FIGURE 8. Theoretical leg output voltage V_S waveforms at load current $I_{load} = I_a$ positive (from the inverter to the motor). a) Inverter switching leg with output devices parasitic capacitances, b) positive dV_S/dt where voltage transition is not affected by the load current, c) negative dV_S/dt where the voltage transition is a function of the load current.

flow towards it. By looking at the experimental waveforms of Fig. 7a and Fig. 7c, it is evident that the duration of reverse conduction, denoted as t_{rc}, remains consistent and equal to t_{dt}, regardless of the instantaneous load current (I_{load}) value. Consequently, in scenarios featuring a positive voltage slope and varying load currents, t_{rc} is equal to

$$t_{rc} = t_{dt} \text{ if } \frac{dV_S}{dt} > 0 \; and \; I_{load} > 0 \tag{2}$$

When a negative variation occurs in the drain-source voltage (with $dV_S/dt<0$), as demonstrated in Fig. 7b and Fig. 7d, the voltage variation slope is influenced by both the load current value and the total capacitance at the switching node, namely C_{oss}. C_{oss} is determined by the parallel combination of parasitic capacitances, C_{ossHS} and C_{ossLS}, which, in turn, are connected in parallel (as depicted in Fig.8a) with the parasitic capacitance introduced by the AC motor, known as C_{load}. In case of low current values, as illustrated in Fig. 7b, the voltage slew rate (dV_S/dt) during commutation is determined by the time the load current takes to discharge C_{oss}. During this period, V_S gradually decreases until the LS device is driven to the on state at the end of the dead time duration t_{dt} [19], and V_S is immediately forced to zero. In this case, the equivalent body diode does not enter conduction mode, thereby preventing associated conduction losses. In contrast, at high current values, as evident in Fig. 7d, the voltage descent rate dV_S/dt is notably steeper. In this case, the equivalent diode of LS conducts during part of the dead time. This conduction time (denoted as t_{rc}), is always shorter than the total dead time duration. The t_{rc} increases with the load current until dV_S/dt reach its maximum value and the voltage fall time t_f became constant

$$t_f = \frac{V_{DC}}{\left(\frac{dV_S}{dt}\right)_{max}} \tag{3}$$

For positive load current variation, (Fig. 8a), the Fig. 8b. and Fig. 8c. depict the theoretical voltage V_S switching transients, distinguishing between positive dV_S/dt and negative dV_S/dt conditions. For positive dV_S/dt (Fig. 8b), t_{rc} duration matches the dead time duration t_{dt}. Per contrary, in the case of negative dV_S/dt as shown in Fig. 8c, it is possible to identify two different levels of current, I_{MAX} and I_{min}. When the load current magnitude falls below the I_{min} threshold, the dv/dt is insufficient to drive the phase voltage to complete commutation (i.e., fall below GND) and activate the equivalent diode. This results in partial-ZVS switching. In contrast, when the switching leg output current ($I_{load} = I_a$) lies within the range defined by $I_{MAX} > I_{load} > I_{min}$, the load facilitates the phase voltage's complete commutation, leading to reverse conduction for only a portion of the dead time as dictated by the controller. When the load current exceeds I_{MAX}, the equivalent body diode conducts for a segment of the designated dead time, resulting in the voltage V_S reaching its peak rate of change, referred to as $(dV_S/dt)_{MAX}$. Consequently, the fall time t_f (also observed in Fig. 7d) represents the minimum duration for V_S to decrease to its ground value (GND). The qualitative variation in reverse conduction time versus load current is summarized in the plot presented in Fig. 9. The value of the two current thresholds can be expressed as follows

$$\begin{cases} I_{min} = C_{oss} \cdot \left(\frac{V_{DC}}{t_{dt}}\right) \\ I_{Max} = C_{oss} \cdot \left(\frac{V_{DC}}{t_f}\right) \end{cases} \tag{4}$$

To summarize, in the case of positive load current and negative dV_S/dt, the reverse conduction time t_{rc} can be expressed

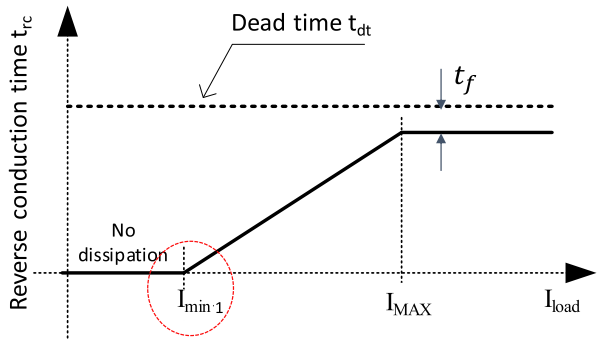

FIGURE 9. Reverse conduction time versus load current.

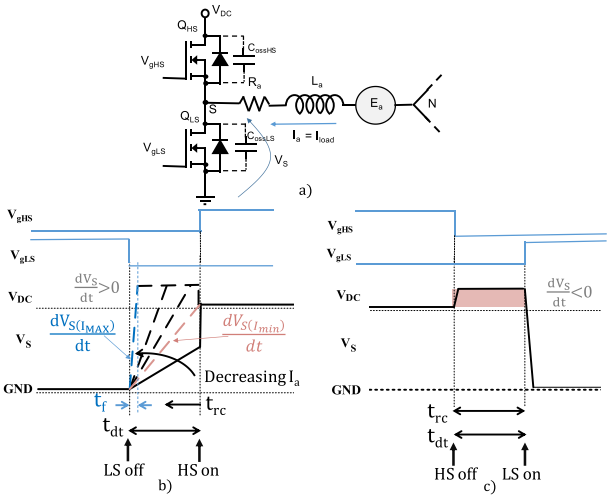

FIGURE 10. Theoretical leg output voltage V_S waveforms at load current $I_{load} = I_a$ negative (from the motor to the inverter). a) Inverter switching leg with output devices parasitic capacitances, b) positive dV_S/dt where the voltage transition is a function of the load current, c) negative dV_S/dt where voltage transition is not affected by the load current.

as follows

$$\begin{cases} t_{rc} = 0 & \text{if } \dfrac{dV_S}{dt} < 0 \text{ and } 0 < I_{load} < I_{min} \\ t_{rc} = t_{dt} - C_{oss} \cdot \dfrac{V_{DC}}{I_a(t)} & \text{if } \dfrac{dV_S}{dt} < 0 \text{ and } I_{min} < I_{load} < I_{Max} \\ t_{rc} = t_{dt} - t_f & \text{if } \dfrac{dV_S}{dt} < 0 \text{ and } I_{Max} < I_{load} \end{cases} \tag{5}$$

In contrast, when dealing with negative phase current values (Fig. 10a), an opposing behavior comes into play. During a commutation characterized by negative dV_S/dt, the equivalent body diode of the LS device conducts for the entire dead time duration t_{dt}. Conversely, when encountering a transient featuring positive dV_S/dt, the switching transient is affected by the load current value. To visualize these dynamics, the theoretical V_S waveforms under negative load current are shown for positive and negative dV_S/dt, respectively in Fig. 10b and in Fig. 10c.

TABLE 3. EPC2206 GaN FET parameters.

Quantity	Symbol	value
Breakdown Voltage	BV_{DSS} (V)	80
Direct Resistance	$R_{DSon,max}(\Omega)$	2.2m @ T_J=25°C
Reverse Voltage	V_{SD} (V)	2.25 @ I_{SD}=80 A, T_j=25°C, V_{GS}=0V
Inner output Capacitance	C_{oss} (pF)	2700 @V_{DS}=0 V 1025 @V_{DS}=48 V 920 @V_{DS}=80 V

V. DEAD TIME DURATION IMPACT ON GAN FET REVERSE CONDUCTION LOSSES

In this section, the power losses of GaN FETs in reverse conduction conditions are evaluated for different dead times. The experimental validation if performed using a three-phase inverter consisting of six GaN FET EPC2206 manufactured by EPC whose power ratings are reported Table 3. The three-phase inverter is commanded so to impose a sinusoidal current to load, featuring an amplitude of $I_a = 25$ A. The DC bus voltage (V_{DC}) is maintained to 48 V by an external dc power supply, while the inverter is operated at a switching frequency of 100 kHz. The inter-winding capacitance of the load motor has been experimentally measured and found to be $C_{load} = 820$ pF. A numerical computational approach is employed to analyze power losses during reverse conduction through the equivalent body diode. The study considers a sinusoidal load current characterized by a fundamental frequency denoted as f_{load}.

A numerical computational approach is employed to analyze power losses during reverse conduction through the equivalent body diode. The study considers a sinusoidal load current characterized by a fundamental frequency denoted as f_{load}. This sinusoidal waveform is discretized into N = 10,000 equal-length discrete time intervals, each referred to as n. During each of these intervals, it is assumed that the current remains constant, as indicated by equations (5) and (2). The duration of reverse conduction within each discrete interval, referred to as t_{rcn}, depends on both the magnitude of the load current and the polarity of the switching node voltage slope.

To determine the variation of reverse conduction time, t_{rc}, during the current phase period (assuming $I_a = I_{load}$), the contributions from all n intervals in the discretization process are sum up. Fig. 11 provides a visual representation of the numerical computation of the t_{rc} curve shape concerning the discrete N intervals, corresponding to the discretized sinusoidal current I_a.

Two dead time values are considered: $t_{dt} = 100$ ns and $t_{dt} = 20$ ns. In Fig. 11a. the case with $t_{dt} = 100$ ns is shown. The upper plots depict the reverse conduction curve under positive dV_S/dt conditions, while the lower plot considers the scenario with negative dV_S/dt.

Whereas in Fig. 11b, the same curves with $t_{dt} = 20$ ns are shown. Upon examining the curves in Fig. 11, it is possible

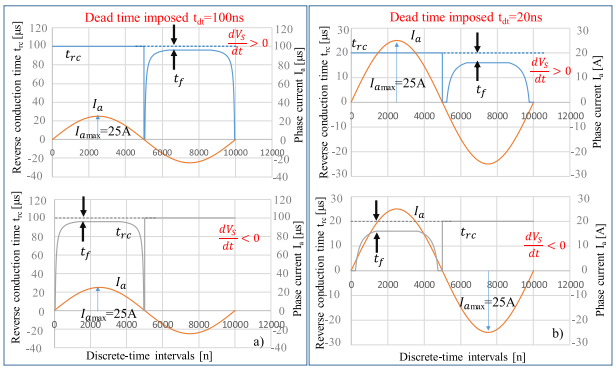

FIGURE 11. Discretized sinusoidal load current with a peak current of I_{amax} = 25 A, alongside the reverse conduction time, t_{rc}, spanning an entire period for both positive and negative node voltage slopes (dV_S/dt) at specified dead times. a) t_{dt} = 100 ns. b) tdt = 20 ns.

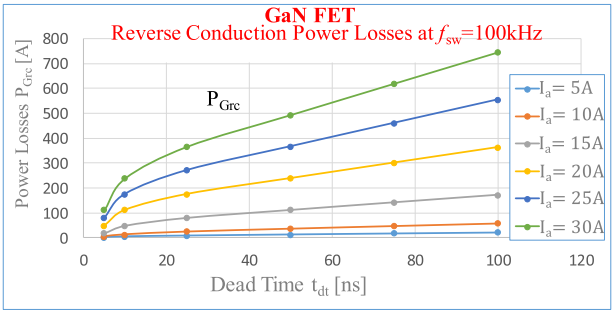

FIGURE 12. Reverse conduction power losses for different load current levels as a function of dead time duration.

to observe that for both t_{dt} = 100 ns and 20 ns, in the case of positive voltage slope ($dV_S/dt>0$) and positive load current (top plot first half of the period), the reverse conduction duration, t_{rc}, reaches its maximum value, equal to t_{dt}(t_{dt} = t_{rc}). Otherwise said, the equivalent body diode conduction time trc equals the imposed dead time t_{dt}. However, during the half period with negative load current (top plot second half period), t_{rc} varies in proportion to the amplitude of the load current.

Notably, the values of the current threshold I_{MAX} and t_f remain unaffected by the t_{dt} duration. Notably, the values of the current threshold I_{MAX} and t_f remain unaffected by the tdt duration. When the load current is greater than I_{MAX}, the reverse conduction time becomes constant and independent from the load current t_{rc} = t_{dt} − t_f. Instead, I_{min} exhibits an inverse relationship with t_{dt}, as demonstrated by equation (4). Additionally, as t_{dt} decreases, the interval in which t_{rc} = 0 expands, resulting in reduced associated power losses. The same analysis applies to the scenario of negative voltage slope ($dV_S/dt<0$) in the lower plots of Fig. 11. The numerical approach presented can be used to effectively compute the power loss estimation during reverse conduction through the use of data obtained from the datasheets of the devices and the calculation of t_{rc} described and represented in Fig. 11.

A. REVERSE CONDUCTION POWER LOSSES ESTIMATION

The computation of energy losses attributed to reverse conduction during a typical commutation event, denoted as 'i', can be performed as outlined in reference [14]

$$E_{rci} = \int_0^{t_{rcn}} V_{rc} \cdot i_a(t) \cdot dt \tag{6}$$

Utilizing the discretization method devised for the sinusoidal load current, along with the $t_{rc,n}$ values, the instantaneous power dissipation can be computed using a discrete formula. This computation focuses on the scenario of reverse conduction exclusively. This approach factors in I_a as the phase current and V_{rc} = V_{SD} as the voltage of the equivalent body diode during reverse conduction.

$$P_{rci} = \left(\sum_{n=1}^{N} V_{rc} \cdot \left(I_a \cdot \sin\left(2 \cdot \pi \cdot \frac{n}{N} \right) \right) \cdot t_{rcn} \right) \cdot f_{sw} \tag{7}$$

In the first approximation, the V_{rc} value can be assumed as constant and equal to V_{SD} (value reported in Table 3) thus enabling to simplification of the computation process. The losses are computed across varying dead time durations while maintaining a constant load current amplitude, thus facilitating the analysis of how dead time duration impacts reverse conduction losses. Fig. 12 reports the variation of reverse conduction losses as a function of dead time length for several load current amplitudes, considering a switching frequency (f_{sw}) of 100 kHz.

Fig. 12 shows that there is a direct correlation between power losses (P_{Grc}) due to the GaN FET equivalent body diode's reverse conduction and both the duration of dead time and current magnitude. Notably, power losses exhibit an almost linear trend, especially during extended dead times. In this linear correlation, the reverse conduction time (t_{rc}) approximates to t_{dt} and t_{dt}-t_f for a substantial portion of the dead time range. Moreover, under conditions of heightened load currents, these curves indicate increased losses, resulting from an extended t_{rc} and amplified load currents. In this scenario, the maximum current threshold (I_{MAX}) rises, while the minimum threshold (I_{min}) consistently holds across all scenarios. Fig. 11a, with a dead time of 100 ns, exemplifies this reverse conduction behavior.

Per contrary in Fig. 11b, where the dead time is shorter (i.e. 20 ns), the contribution of t_{rc} = 0, becomes more pronounced. This effect leads to a reduction in associated power losses, resulting in the parabolic shape shown in Fig. 12 for short dead time values. The parabolic path is characterized by a higher current threshold, I_{min}, where the reverse conduction time becomes negligible across a broader range of current amplitudes.

VI. REVERSE CONDUCTION IN SI MOSFET

In case of Si MOSFET inverters for low-voltage (e.g., 48 V) AC motor drive applications, it's common to set the dead time duration in the order of 100 ns or even more. Hence, it is of particular interest to investigate the differences in reverse

TABLE 4. BSC026N08NS5 Si MOSFET parameters.

Quantity	Symbol	value
Breakdown Voltage	BV_{DSS} (V)	80
Direct Resistance	$R_{DSon,max}(\Omega)$	2.6m @ T_J=25°C
Reverse Voltage	V_{SD} (V)	0.9 @ I_{SD}=80 A, T_j=25°C, V_{GS}=0V
Inner output Capacitance	C_{oss} (pF)	5500 @V_{DS}=0 V 750 @V_{DS}=48 V 600 @V_{DS}=80 V

conduction behavior in comparison to GaN FETs, with a particular focus on understanding the dynamic characteristics of the body diode and its impact on power losses [20]. SPICE simulations are used to perform a direct comparison between the two technologies. A half-bridge configuration is simulated to evaluate the body diode's behavior during reverse conduction. The analyzed switching leg circuit is shown in Fig. 13a. The bus voltage, denoted as V_{DC}, is kept constant at 48 V, while a current generator is used to impose the load current. In this analysis, the BSC026N08NS5 Si MOSFET is chosen, exhibiting equivalent characteristics to the previously exemplified EPC2206 GaN FET. The main characteristics of the Si MOSFET are reported in Table 4.

Additionally, an equivalent model for the body diode to replicate the reverse recovery process is used [21]. The body diode model employs Lauritzen and Ma's physical-based diode modeling approach [22]. A simplified schematic of the model of the body diode is depicted in Figure 13b, where R_S represents the series resistor, I_{Diode} denotes the diode current, and a current source supplies it.

The diode's current value is determined as follows

$$I_{Diode} = (q_E - q_M)/T_M \tag{8}$$

Here, q_E represents the charge injection into the depletion region, q_M represents the stored charge in the depletion region, and T_M is the charge diffusion time between the edge and inside the depletion region.

The expressions describing the dynamic behavior of q_E and q_M charges are as follows

$$\frac{d}{dt}q_M = i_{Diode} - \frac{q_M}{\tau} \tag{9}$$

$$q_E = I_{S,LM} \cdot \tau \cdot (e^{\frac{q \cdot v_{Diode,ak}}{nd \cdot k \cdot T_J}} - 1) \tag{10}$$

where:

- τ is the recombination time constant of the depletion region
- n_d represents the emission coefficient. It is equal to 2 to indicate that half of the diode voltage drops across the p+-i junction (considering a p-i-n structure with high injection). When n equals 1, the model function becomes a low-voltage p-n junction diode.
- $I_{S,LM}$ is the saturation current of the body diode used in the SPICE model;
- V_{Diode} is the voltage drop of the diode without considering the voltage drop due to the series resistor R_S;
- T_J is the junction temperature expressed in K [22].
- q is a fundamental physical constant known as the electronic charge and k is the Boltzmann's coefficient that represents the average kinetic energy of particles in a system [22].

The dynamics of electrical variables during a reverse recovery event of the body diode are meticulously analyzed through simulations conducted using the half-bridge configuration depicted in Fig. 13 a).

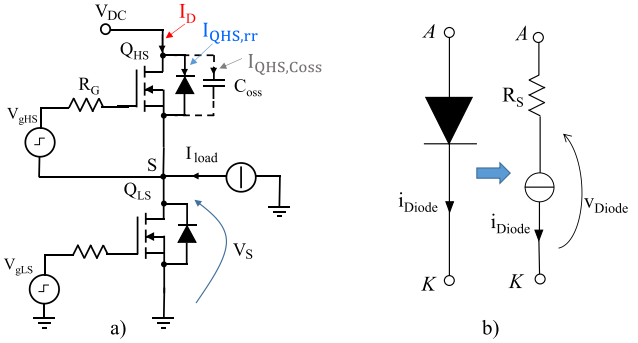

FIGURE 13. a) Switching leg schematic for investigating the MOSFET body diode behaviour in reverse conduction. b) simplified model schematic of the body diode.

The transient behavior of the high-side switch Q_{HS} is analyzed, specifically during the moment when the low-side MOSFET Q_{LS} switches on after a designated dead-time interval. This analysis takes into account the load current entering the switching node S. Multiple simulations are carried out, varying load current values and dead-time interval lengths within a range from t = 0 ns to t = 100 ns. Two key parameters under scrutiny are the charge injection into the depletion region, denoted as q_E, and the stored charge, q_M, of the high-side MOSFET, particularly with respect to I_{load} values of 25 A at different dead times (10 ns, 50 ns, 100 ns). It's worth noting that in all simulations, a junction temperature of 125 °C is assumed to be one of the worst case scenario for the reverse recovery charge (as shown in Fig. 14a, with a specific highlight on q_M for $t_{dt} = 10$ ns).

In Fig. 14b, the reverse recovery current $I_{QHS,rr}$ is presented alongside the capacitive current $I_{QHS,Coss}$ (as seen in Fig. 13a), both at $V_{DC} = 48$ V. The MOSFET drain current I_D, which operates in reverse conduction, results from the summation of these two currents, $I_{QHS,Coss}$ and $I_{QHS,rr}$. Following the reverse recovery transient, a constant V_{rc} is considered as the voltage drop during the remaining duration of the dead time. Similar to the approach employed with the GaN FET, the power losses in reverse conduction for the MOSFET devices are determined by incorporating the contribution of the body diode. In Fig. 15, the MOSFET power dissipation denoted as P_{Mrc}, is depicted as a function of the dead time value.

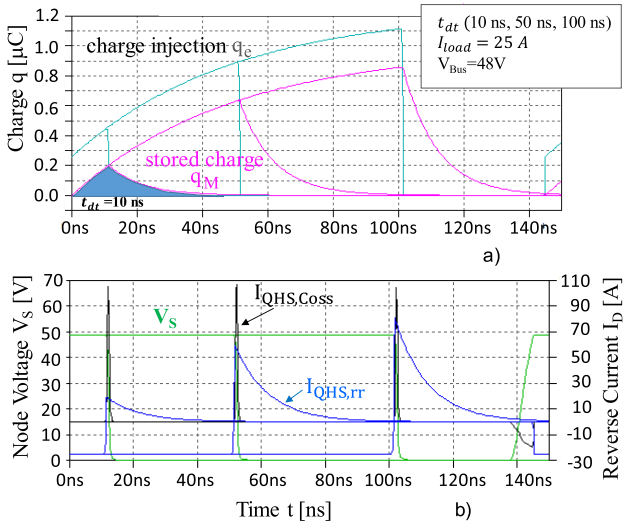

FIGURE 14. a) Variation of charge injection into the depletion region (q_E) and the stored charge (q_M) within the high-side MOSFET body diode, considering I_{load} at 25 A, for different dead time intervals (10 ns, 50 ns, 100 ns). b) Reverse recovery current ($I_{QHS,rr}$), capacitive current ($I_{QHS,Coss}$), and voltage at the switching node (V_S).

It's important to note that the magnitude of power loss attributed to the reverse recovery of the body diode escalates with increasing dead-time duration, t_{dt}, and current levels [23]. The losses associated with dead time due to reverse recovery (Q_{rr}) are negligible when the dead time interval (t_{dt}) approaches zero.

However, as t_{dt} increases, these losses exhibit a rapid escalation, ultimately becoming directly proportional to the duration of t_{dt} counterparts, particularly in scenarios with short dead times. Notably, the MOSFET has additional losses due to diode reverse recovery (Q_{rr}), which become more pronounced when dealing with shorter dead times. It's essential to emphasize that the Q_{rr} diode losses do not impact GaN FETs, setting them apart. However, it's worth noting that the reverse conduction voltage drop in GaN FETs is comparatively higher than that observed in MOSFETs.

Consequently, this leads to a steeper slope in GaN FETs' loss curve. As a result, for longer dead times, the MOSFET proves to be the more efficient device in terms of power dissipation. This insightful comparison sheds light on the performance characteristics of these semiconductor devices in real-world applications.

VII. REVERSE CONDUCTION POWER LOSSES COMPARISON IN GAN FETS AND SI MOSFETS

In this section, the reverse conduction losses of the GaN FET and Si MOSFET are compared using the data obtained in the previous analysis. Fig. 16 provides a comparison of power dissipation curves between GaN FETs and MOSFETs, taking into account variations in the dead time parameter. These graphs were generated under consistent switching conditions with $V_{DC} = 48$ V, and a fixed frequency of $f_{sw} = 100$ kHz

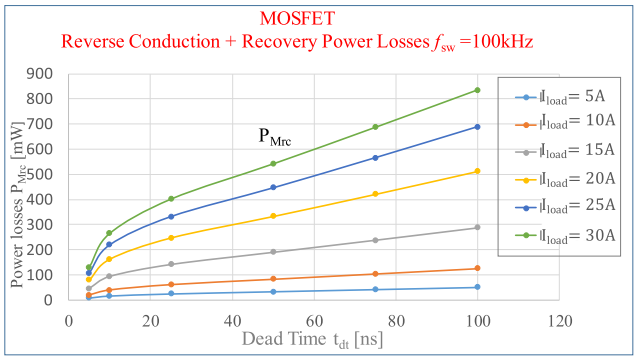

FIGURE 15. MOSFET power losses during full reverse conduction for various load current values (I_a) within a dead time duration (t_{dt}) range of 5-100 ns.

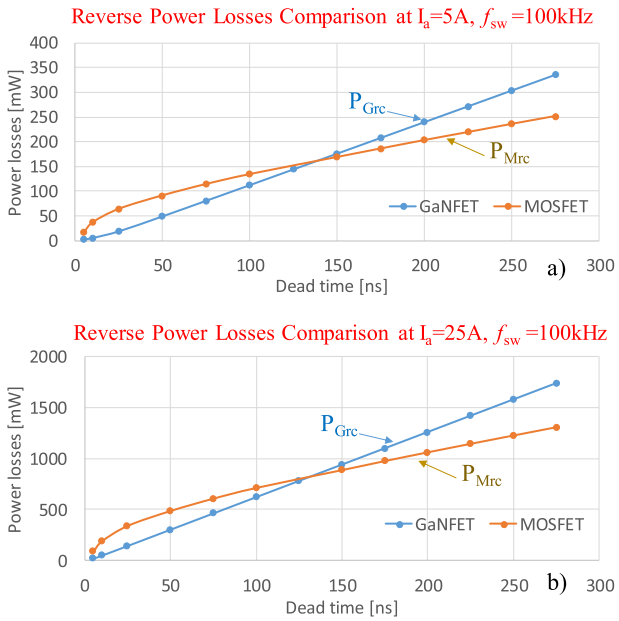

FIGURE 16. Reverse conduction power losses numerical calculation at two current I_{load} values versus the dead time duration. Dead time range 5-275 ns. a) I_{load} = 5 A. b) I_{load} = 25 A.

was applied to both devices. In Fig. 16a, the load current is set at $I_a = 5$ A, while in Fig. 16b, the load current is set at a notably higher value of $I_a = 25$ A.

Upon a closer examination of the graphical results, it becomes evident that GaN FETs exhibit markedly lower losses compared to their Si MOSFET counterparts, particularly in scenarios with short dead times. Notably, the MOSFET has additional losses due to diode reverse recovery (Q_{rr}), which become more pronounced when dealing with shorter dead times. It's essential to emphasize that the Q_{rr} diode losses do not impact GaN FETs, setting them apart. However, it's worth noting that the reverse conduction voltage drop in GaN FETs is comparatively higher than that observed in MOSFETs. Consequently, this leads to a steeper slope in GaN FETs' loss curve. As a result, for longer dead times, the MOSFET proves to be the more efficient device in terms

of power dissipation. This insightful comparison sheds light on the performance characteristics of these semiconductor devices in real-world applications.

The presence of the body diode in the MOSFET switching features an additional reverse recovery time compared to the switching time of the GAN FET. For this reason, the dead time of the GaN FET can be chosen to be shorter (20 ns) than the MOSFET one (100 ns). The figures show that the GaN FET is significantly more efficient than the MOSFET as the chosen dead time was short. The graphic comparison results show that the GaN FET is considerably more efficient than the MOSFET when the dead time selected is short. In addition, as the load increases, the range in which the GaN FET is advantageous compared to the MOSFET extends over a wider range of losses (from 0 mW to 160 mW in the case of $I_{load} = 5$ A; from 0 mW to 820 mW in the case of $I_{load} = 25$ A). The point of intersection between the loss curves of the MOSFET and GaN FET shifts for higher loss values the higher the load current.

A. MOSFET VS GAN FET EXPERIMENTAL EVALUATION IN INVERTER SWITCHING LEG

Two similar circuit boards using a half-bridge configuration, one using GaN FETs and one with MOSFETs, are used to investigate experimentally the differences between the two technologies during the dead time. In this test, $V_{DC} = 48$ V is used. The circuit schematic of the switching leg board is depicted in Fig. 17a. The left side of Fig. 17b shows the board mounting the EPC2065 GaN FETs (featuring a breakdown voltage of 80 V and a conduction resistance, R_{DSON}, of 3.6 mΩ). The right side of Fig. 17b shows the board mounting the Onsemi FDMS2D5N08C MOSFETs (featuring a breakdown voltage of 80 V and a conduction resistance, R_{DSON}, of 2.7 mΩ).

The two boards have a similar layout, thus enabling the comparison of the two technologies while having, in first approximation, the same PCB parasitics. The devices to compare have been chosen with similar conduction properties, so the main difference is due only to the technology itself.

The board under test operates in buck mode at a constant duty cycle of duty = 0.025 (it is low thus to operate the buck in the low ripple region but big enough not to have interferences between the switching transients) at a switching frequency of $f_{SW} = 20$ kHz. A second switching converter interfaced via an LCL filter is connected to the switching node of the Half-Bridge leg imposing a controlled load current. The same dead time of 150 ns is set for both boards (i.e., GaN and MOSFET).

The 150 ns dead time is selected thus to have a zero-voltage switching in the MOSFET when the load current is 1.5 A.

Two trade-off items lead to the choice of these values. The first one (150 ns) depends on the current distortion desired due to the dead time length. The second one (1.5 A) is chosen to achieve low hard switching losses. The same hard switching losses (at 1.5 A) for GaN FET can be achieved at lower dead time but using 150 ns of t_{DT} allows a valuable comparison with the MOSFET device. The tests are conducted at room temperature (Ambient temperature $T_A = 25$ °C). The experimental waveforms showing VS (blue for the GaN FET and purple for the MOSFET), V_{GSH} (black for the GaN FET and red for the MOSFET), V_{GSL} (green for the GaN FET and yellow for the MOSFET) are reported in Fig. 17 for the case with a load current $I_a = 1.5$ A (the current is assumed positive when exiting from the switching node).

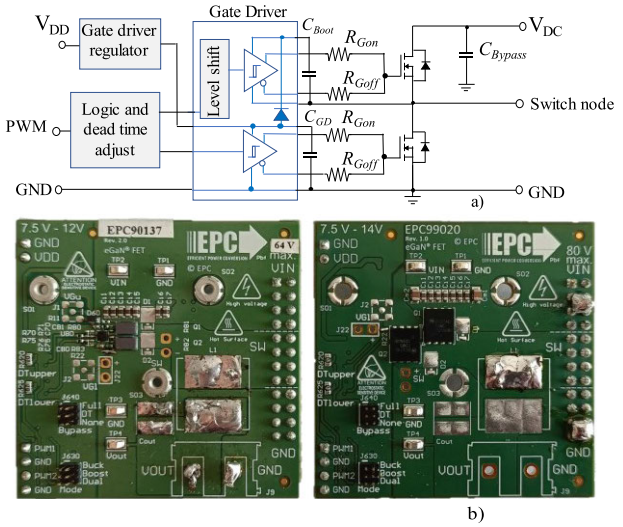

FIGURE 17. a) schematic of the H-Bridge. b) H-Bridge boards were used for the experimental test. GaN FET-based board on the left. MOSFET-based board on the right.

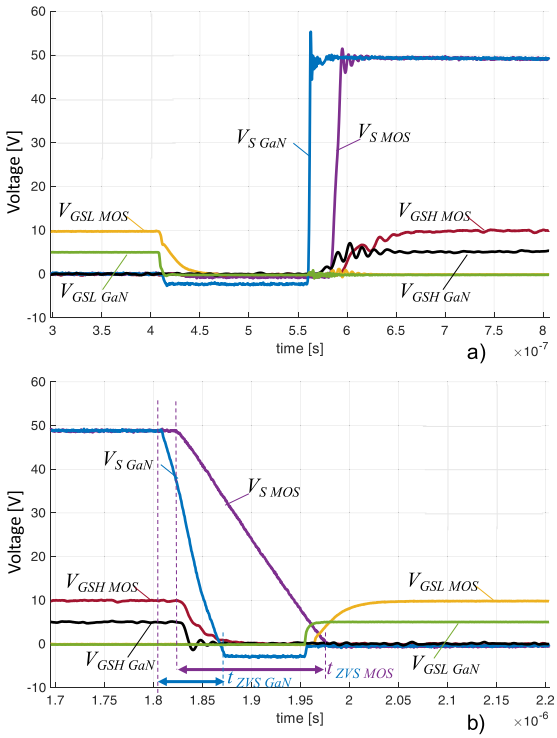

FIGURE 18. Comparison of the V_S, V_{GSH}, and V_{GSL} waveforms obtained with the MOSFET-based Half Bridge and the GaN FET-based one. 1.5 A load current. a) Q_{LS} turn-off and Q_{HS} turn-on. b) Q_{HS} turn-off and Q_{LS} turn-on.

The Q_{LS} turn-off and Q_{HS} turn-on transients are shown in Fig. 18a, while the Q_{HS} turn-off and Q_{LS} turn-on transients are shown in Fig. 18b.

In Fig. 18, GaN FET V_S differs from the MOSFET one for the reverse conduction time (RCT) duration and its voltage drop amplitude, which is bigger in the GaN FET. GaN FET V_S variation is steeper, and this causes V_S to rise to 48 V (see Fig. 18a) and to fall to 0 V (see Fig. 18b) earlier than the MOSFET. This is due to the smaller output parasitic capacitance of the GaN FET technology. When switching with a positive V_S slope (Fig. 18a, Q_{LS} turn-off and Q_{HS} turn-on), there is immediate reverse conduction without a C_{OSS} COSS charge/discharge transient. This occurs for both the GaN FET and the MOSFET. In Fig. 18b, MOSFET V_S reaches 0 V exactly when the 150 ns dead time has elapsed; thus, no reverse conduction happens. GaN FET in the same condition reaches 0 V before, from which reverse conduction appears. RCT always ends when the turning-on device (Q_{LS}) V_{GS} reaches the threshold value and starts conducting.

The test is repeated for I_a = 0.5 A, 1 A, 1.5 A, 2 A, 5 A, 10 A. The resulting V_S waveforms for different I_a values are reported in Fig. 19 (rising V_S) and in Fig. 20 (falling V_S).

The MOSFET plots are labeled with a), while the GaN FET ones are with b). Comparing Fig. 19a and Fig. 19b, waveforms are the same for all the I_a values. However, the GaN FET voltage rise is faster than the MOSFET. At 150 ns the reverse conduction time is wider than the voltage rise, especially for GaN FET. At $dV_S/dt>0$, the reverse conduction time can be reduced by a choice of a lower dead time duration than the one at $dV_S/dt<0$ (asymmetric dead time selection [24]). On the other hand, Fig. 20 shows that a higher current I_a makes the switching dynamic faster.

With a dead time of 150 ns, the MOSFET performs hard switching for I_a <1.5 A, while the GaN FET performs it only for the I_a = 0.5 A. For the other I_a cases, GaN FET shows reverse conduction for current over 0.75A until 10A. MOSFET features the reverse conduction for current above 1.5A.

From Fig. 20 the Zero Volt Switching (ZVS) time t_{zvs} is the time that goes from when V_S is 48 V to when V_S reaches 0 V, in Table 5 reports the t_{zvs} values for the GaN FET (t_{zvsGaN}), and the MOSFET (t_{zvsMOS}), for different positive I_a values in the commutation with falling V_S. ZVS coincides with the optimum dead time that must be set to achieve neither reverse conduction nor hard switching conditions.

The values presented in Table 5 serve to underscore the advantage of employing GaN FET technology in allowing for smaller dead time values compared to MOSFETs in terms of zero voltage transition time.

LTSpice simulations have been performed to estimate the energy losses for various dead-time and current I_a amplitude values, comparing the GaN FET and the MOSFET used in the experimental tests achieved from the setup of Fig. 17. The experimental waveforms at both positive and negative dV_S/dt (Fig.19 and Fig. 20) are used to validate the simulation runs.

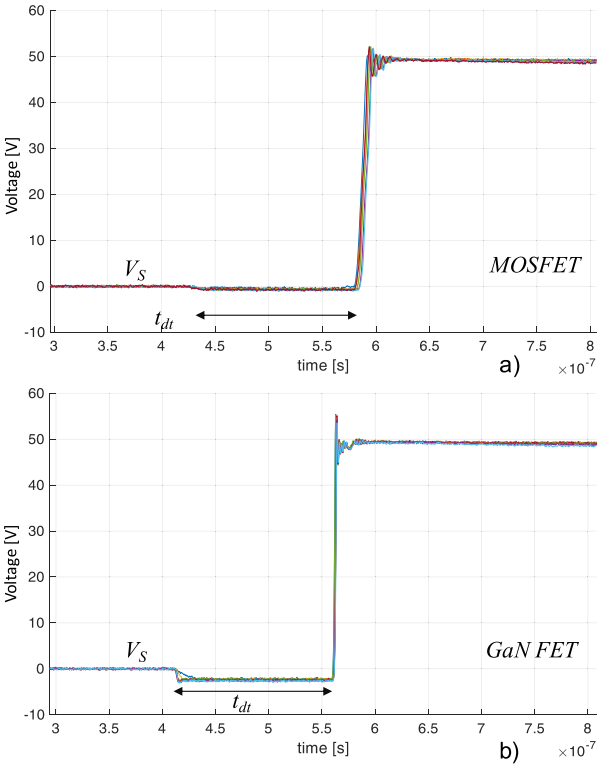

FIGURE 19. Rising V_S waveform for I_a = 0.5 A, 1 A, 1.5 A, 2 A, 5 A, 10 A. a) MOSFET-based Half-Bridge. b) GaN FET-based Half-Bridge.

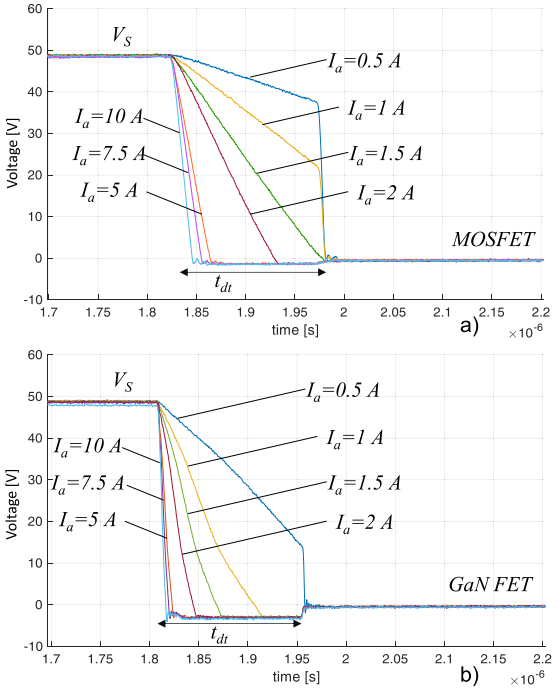

FIGURE 20. Falling V_S waveform for Ia = 0.5 A, 1 A, 1.5 A, 2 A, 5 A, 10 A. a) MOSFET-based Half-Bridge. b) GaN FET-based Half-Bridge.

The MOSFET model is extracted from the Onsemi manufacturer catalogue for the FDMS2D5N08C device. The MOSFET modelization is mature and effective for the

TABLE 5. Zero volt switching time versus phase current at node voltage fall.

Quantity	Phase Current	Zero voltage transition time MOSFET	Zero voltage transition time GaN
Symbol	I_a [A]	$t_{ZVS\ MOS}$ [ns]	$t_{ZVS\ GaN}$ [ns]
Values	0.5	>150	>150
	1	>150	102
	1.5	150	62
	2	112	38
	5	43	17
	7.5	36	13
	10	26	10

simulation analysis [25]. The model used for the simulation results of the GaN FET has been presented and validated in [26]. The simulation results allow the evaluation of the energy losses by the computation of voltage and current cross-conduction area during the various dV_S/dt transients. Instead, the device's current measurement in the experimental board of Fig. 17 is not attainable for the layout optimization to reduce the stray inductances in the switching leg power loop.

At $dV_S/dt>0$, looking at Fig. 19, two intervals of time can be distinguished. The first one starts from the low side (Q_{LS}) turn-off, when its gate-source voltage falls under the threshold level, until the high side (Q_{HS}) gate-source voltage rises to the threshold level. During this time interval, the reverse conduction appears, and the energy losses E_{rc} can be achieved. The second one is related to the hard switching transient. During this time interval hard switching losses E_{hs} losses can be evaluated.

The overall energy losses of MOSFET and GaN FET ($E_{rc} + E_{hs}$) versus phase current amplitude at two different dead times of 20 ns and 150 ns are plotted in Fig. 21a and Fig. 21b respectively.

The total energy losses comparison shows a better performance for the GaN FET in the overall current range. Moreover, the GaN FET curve is more linear than the MOSFET one. The increasing MOSFET Energy losses are due both to the higher parasitic capacitance (lower dV_S/dt rise) and the contribution of the body diode charge Q_{rr} as shown in Section VI (see Fig. 14). The curve trend of the MOSFET energy losses in Fig. 21a and Fig. 21b is not linear versus the current amplitude because of the body diode reverse recovery. The contribution of reverse conduction energy losses E_{rc} is lower in the MOSFET. However, the impact of these losses becomes minor in case the dead time is short, such as it is enabled in GaN FETs.

At $dV_S/dt<0$ with variable phase current amplitude three kinds of operative conditions appear in Fig. 20:

- zero voltage switching;
- reverse conduction time;
- partial hard switching (PHS).

The switching node voltage V_S starts falling when the high side (Q_{HS}) device turns off (its gate-source voltage drop under the threshold voltage level). ZVS happens if the low side

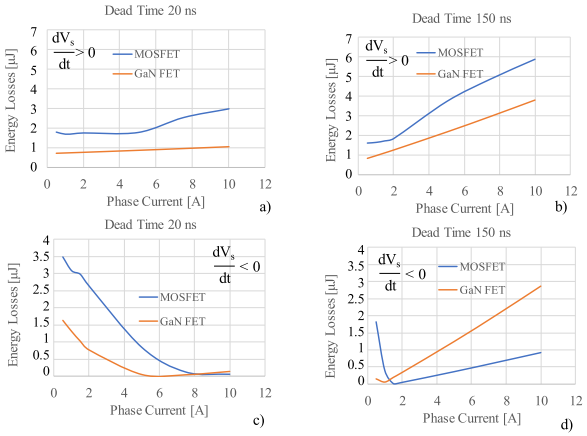

FIGURE 21. Overall energy losses of MOSFET and GaN FET versus positive phase current amplitude at two different dead times. At dVs/dt>0 a) 20 ns b) 150 ns. At dVs/dt<0 c) 20 ns. d) 150 ns.

device (Q_{LS}) turns on exactly when the falling V_S has reached the value of 0V. V_S falls to 0V at the end of t_{dt}. Instead, if the V_S falls to 0V earlier than the Q_{LS} turn on (before the end of t_{dt}), RCT appears. When the t_{dt} is short for the V_S slew rate (due to the low current amplitude) the low side (Q_{LS}) turns on with PHS (V_S >0V at the end of t_{dt}).

The comparison of the total energy losses of the RCT and PHS interval for MOSFET and GaN FET is depicted in Fig. 21c for the dead time of 20 ns and in Fig.21d for the dead time of 150 ns. The comparison of the curves in Fig. 21c and Fig.21d shows that the GaN FET is more advantageous than MOSFET for a wider current range and reduced dead time. At the same dead time, the GaN FET shows a ZVS condition at lower currents compared to the MOSFET.

Losses are due to PHS conditions for I_a less than the ZVS conditions. For higher current than ZVS condition V_S falls to 0V before the end of t_{dt}, and the RCT condition appears.

The energy losses depend on the duration of the dead time over the ZVS.

Furthermore, in the case of PHS, the GaN FET features lower energy losses compared with MOSFET, whatever the dead time used. On the other hand, in the case of reverse conduction, MOSFETs show lower energy losses than the GaN FETs. If dead time ends exactly when V_S falls to 0 V (ZVS), switching losses can be reduced by avoiding the reverse conduction interval.

An adaptive dead time selection can be adopted to minimize energy losses as shown in [24].

If the dead time is kept constant, to minimize the losses, it is crucial to use small values (i.e., 20 ns) when using GaN FETs.

VIII. DISCUSSION

This study investigates the effects of dead time impact on the reverse conduction phenomenon during the GaN FET and MOSFET commutation in inverter applications for motor control. This paper investigated the critical aspect of dead

time in an inverter leg within a motor drive system, focusing on utilizing GaN FET technology, including an extensive comparison between the reverse conduction characteristics of GaN FET-based and MOSFET-based switching legs. In the pulse-width modulation (PWM) cycle context, two distinct switching scenarios arise in each phase. One scenario entails continuous reverse conduction throughout the entirety of the dead time, regardless of the load current. In contrast, the reverse conduction dynamics of the other scenario are intricately linked to the magnitude of the phase current, exhibiting variability and occasionally even the absence of reverse conduction states (ZVS). These dynamic switching events are closely intertwined with the voltage slope at the switching leg node. In motor control, the hard switching condition during the current variation at dead time cannot be eliminated; it can occur at the lowest possible currents to reduce losses during hard switching transients. MOSFET and GaN FET differ in the duration of the ZVS condition for the same current depending on the equivalent switching node capacitance, and in GaN FET being smaller, there are shorter times compared to the equivalent MOSFET. The switching transients during reverse conduction in the dead time were evaluated with LTSpice simulations and experimental measurements using circuit boards specifically developed to make the tests for GaN FET and MOSFET as equivalent as possible. One of the more significant findings from this investigation is that the GaN FET features lower losses at short dead time duration (e.g. 20 ns) compared with the MOSFET. In the case of reduced dead time, despite the higher reverse conduction voltage drop of GaN FET, it features lower losses than MOSFET because of a lower output parasitic capacitance that implies a faster commutation and lower loss energy.

This investigation approach establishes a quantitative framework for detecting the optimal dead time for GaN FET-based low-voltage inverters in motor drive applications. This paper lays the groundwork for demonstrating that losses can be minimized by choosing a proper short dead time duration depending on the load.

Furthermore, the increasing of switching frequency in GaN-based inverter allows an output ripple current reduction and the dead time decrease acts on the quality of the waveforms with a benefit on the torque ripple diminishing reducing the vibration and increasing the motor drive reliability [5].

The application of GaN FETs leads to some opportunities to develop reliable, efficient, and size-compact solutions in motor drives. GaN transistors offer superior figures of merit compared to their silicon counterparts, facilitating size and weight reduction, and potentially lowering the bill-of-material cost [27], despite of the higher cost of the GaN transistors compared to silicon MOSFETs. Specifically, the hard-switching figure of merit for 80∼100 V GaN provides a fourfold improvement compared to silicon MOSFETs [28]. Additionally, GaN's high operating frequency enables a reduction in the quantities of passive components required for input and output filters. This reduction further allows for minimizing the overall size and weight of the application power converter boards, thereby decreasing the conductive area and the amount of copper in the PCBs. In particular, the switching frequency increasing reduces the dc link capacitors value and size. Instead, of electrolytic capacitors, non-polarized ceramic capacitors can be used with noticeable space and cost savings [8].

IX. CONCLUSION

This study has contributed valuable insights into the role of dead time in motor drive applications, shedding light on the performance disparities between GaN FETs and MOSFETs in the realm of reverse conduction and hard-switching transients, through simulation runs and experimental tests.

The paper has undertaken a comprehensive qualitative and quantitative exploration of reverse conduction losses, spanning various load current and dead time configurations for both GaN FETs and MOSFETs. To facilitate this analysis, a straightforward yet highly effective numerical tool was developed, based on real-world device characteristics and inverter drive electrical parameters. Furthermore, this study introduced a novel approach to gauging GaN FET losses during variable reverse conduction, defined by two threshold current values. The reverse recovery losses inherent to MOSFETs were estimated utilizing Lauritzen and Ma's physically-grounded diode model. A compelling comparison of reverse conduction losses between the two devices emerges, underscoring that GaN FETs exhibit superior performance when the dead time is relatively short. Conversely, MOSFETs emerge as more advantageous when dealing with long dead time intervals, thanks to their lower reverse conduction voltage.

Additionally, for switching leg GaN FETs and MOSFETs featuring equivalent conduction resistance properties and identical breakdown voltage ratings two experimental boards with equivalent layouts are developed to carry out several switching dead time tests. Furthermore, the switching tests are used to implement simulation run in LTSpice to compare the energy losses during the dead time at variable current values. The test results show that adopting shorter dead times (i.e., 20 ns) brings clear advantages in terms of energy dissipated during switching for GaN FETs, while it is even counterproductive for MOSFETs.

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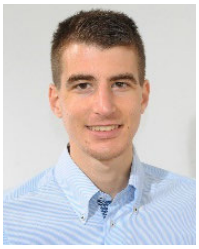

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