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RESEARCH ARTICLE

An Interleaved Buck-Boost-Zeta Converter With Coupled Inductor Multiplier Cell and Zero Input Current Ripple for High Step-Up Applications

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ABSTRACT An interleaved Buck-Boost-Zeta converter with the coupled inductor multiplier cell and zero input current ripple is proposed in this paper, which is suitable for high step-up applications such as the photovoltaic generation system. By integrating the Buck-Boost converter with the Zeta converter and adding the coupling inductor voltage multiplier cell and the auxiliary input inductor, the proposed converter achieves very high voltage gain and very low switch voltage stress. At the same time, very low input current ripple and continuous output current can be achieved, which is friendly to photovoltaic arrays and DC-bus. The leakage inductance energy is absorbed by the passive clamp circuit, the zero-current-switching (ZCS) turn-on of the switch is achieved and the reverse recovery problem of the diode is alleviated. The operation principles and performances of the proposed converter are analyzed in detail. The proposed converter can further improve the voltage gain by adding different voltage multiplier cells and their general structures are given. A prototype with 32V input and 400V output was built to verify the theoretical analysis.

INDEX TERMS Coupled inductor, high step-up, Buck-Boost-Zeta converter, zero input current ripple, ZCS turn-on, passive clamp.

I. INTRODUCTION

In recent years, in response to the energy crisis and environmental pollution, new energy technologies such as green and clean photovoltaic power generation have developed rapidly [1], [2]. The DC signal output by the photovoltaic array often needs to go through the front-end boost link [3], [4], [5] before subsequent operations such as grid connection or inversion, which requires the development of high step-up DC-DC converters with better performance. In recent years, many relevant researchers have proposed numerous converters to cope with the boosting process at the front end of the system. References [6], [7], and [8] provide reviews of recent research results and conduct comparative reviews of different topology types. It is not difficult to find that to meet the power transmission and distribution conditions of modern energy networks, it is necessary to increase the voltage gain of the converter while ensuring that it can operate more efficiently and stably.

To improve the converter, we can start with the common voltage multiplying structure, in which [9], the switched inductor is applied to boost, buck-boost, Cuk, Zeta, and Sepic converters, but it only improves the voltage gain of the converter without improving other performance. Further proposed the high-boost converter with active switching inductance cells, which can reduce the voltage stress of the switch, but has a hard switching problem [10], [11]. The switched capacitor structure can also be used, and the converter can achieve a voltage boost and reduce the voltage stress of the switching device [12], [13]. switched capacitor–inductor network [14], [15], [16] can be further proposed to integrate the two structures into a new cell, but excessive loss of components and cost issues must be considered. Moreover, active switched-inductor and passive switched-capacitor networks [17], [18], ensure continuous input current, but the ripple is large, and soft switching is

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not implemented. Coupled inductors can increase the voltage gain by adjusting the turn ratio without increasing the number of components [19], [20]. Due to the existence of leakage inductance, resonance is easy to occur, and the occurrence of peak voltages affects the stability of the equipment. A clamping branch is usually required to absorb leakage inductance energy [21], [22], [23]. It can be combined with a switched capacitor structure to increase the gain while using its branch as a passive clamping circuit to achieve ZCS turn-on [24], [25], and [26]. On this basis, the DC-DC converter [27] uses auxiliary switches to achieve zero-voltage-switching (ZVS) with the input current continuous. Converter with three-winding coupled inductors can achieve further voltage gain [28], [29], and the impedance network selects appropriate node locations that can develop different Three-winding types, such as Y-source [30]. To achieve high step-up, coupled inductors are integrated into different topologies, such as quadratic boost converters [27], [31], which achieve input continuously, and can also use interleaved parallel input to boost the voltage [32], [33], and can reduce current ripple. The double coupling structure was further introduced and combined with switched capacitors to form the voltage multiplier cell [34], [35], [36], both of which achieved ZCS. In [34], a symmetrical topology was proposed based on dual boost concepts, but its input current ripple was large. Interleaved DC-DC converter [35], [36], both of which reduce the input current ripple of the device, converter [36] proposed an interleaved series voltage-doubling module to reduce the voltage stress of the device further.

This paper proposes a novel interleaved Buck-Boost-Zeta converter with the coupled inductor multiplier cell and zero input current ripple. By differentially connecting the Buck-Boost converter and the Zeta converter, and integrating the coupled inductor voltage multiplier unit and the zero-ripple unit into a new structure, this unit cleverly uses the original devices to form a new multi-functional multiplexing structure. The converter achieves very high voltage gain, very low input current ripple, and continuous output current. At the same time, the passive clamp circuit is used to absorb the leakage inductance energy, which effectively suppresses the voltage spike generated by the parasitic capacitance and leakage inductance resonance and reduces the maximum voltage stress of the switches. Furthermore, the ZCS turn-on of the switches is achieved and the reverse recovery problem of the diode is alleviated by using leakage inductance. Meanwhile, the proposed converter can further improve the voltage gain by adding different voltage multiplier cells, and the general rules of topology variations are given.

The rest of the paper is organized as follows. The operation principles of the proposed converter are analyzed in Section II. The performance analysis is described in Section III. Design considerations are given in Section IV. Experimental results are provided in Section V. Conclusions are given in Section VI.

II. PROPOSED CONVERTER AND OPERATION PRINCIPLES

A. THE TOPOLOGY OF THE PROPOSED CONVERTER

The Buck-Boost converter and the Zeta converter are differentially connected on the input side to generate a differentially integrated Buck-Boost-Zeta converter (DI-BBZ) as shown in Fig. 1(a). The voltage gain of DI-BBZ is the sum of the voltage gains of Buck-Boost converter and Zeta converter. The switches S_1 and S_2 can be driven in a synchronous manner or an interleaved manner.

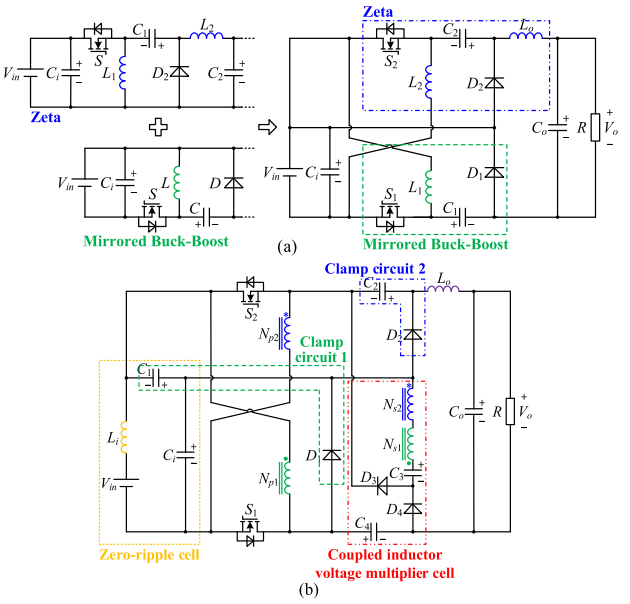

FIGURE 1. The topology of the proposed converter. (a) DI-BBZ, and (b) The proposed converter.

The coupled inductor voltage multiplier cell (N_{p1}-N_{s1}, N_{p2}-N_{s2}, C_3, D_3), passive clamp circuit (C_1-D_1), and auxiliary inductor (L_i) are integrated into the DI-BBZ to generate the proposed converter as shown in Fig. 1(b). The switches S_1 and S_2 are driven in an interleaved manner. The coupled inductance voltage multiplier cell is used to improve the voltage gain. The auxiliary inductor L_i and capacitors C_i and C_1 generate a zero-ripple unit, which achieves very low input current ripple. At the same time, the diode-capacitor branch (D_2-C_2) in the Zeta structure is multiplexed as a passive clamp circuit of the switch S_2. The output side has an inductance L_o, which realizes a continuous output current.

B. ANALYSIS OF OPERATION MODES

The equivalent circuit of the proposed converter is shown in Fig. 2. The coupled inductance is modeled as an ideal transformer with magnetizing inductance $L_{m1(2)}$ and leakage inductance $L_{k1(2)}$, which has a turns ratio of $n_{1(2)}$. In order to facilitate the steady-state analysis, the following assumptions are made: 1) All switches and diodes are ideal and their parasitic parameters can be ignored; 2) All capacitors are large enough that their ripple voltage can be ignored; 3) The currents of the magnetizing inductances $L_{m1(2)}$ and the

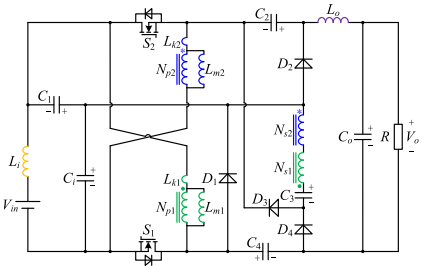

FIGURE 2. Equivalent circuit.

output inductance L_o are continuous, the proposed converter is operated in continuous conduction mode (CCM).

In general, the duty cycle of high gain converters is larger than 0.5 during steady state. Eight modes are present during one switching period T. The key waveforms of the proposed converter are shown in Fig. 3. The equivalent circuits of each mode are shown in Fig. 4.

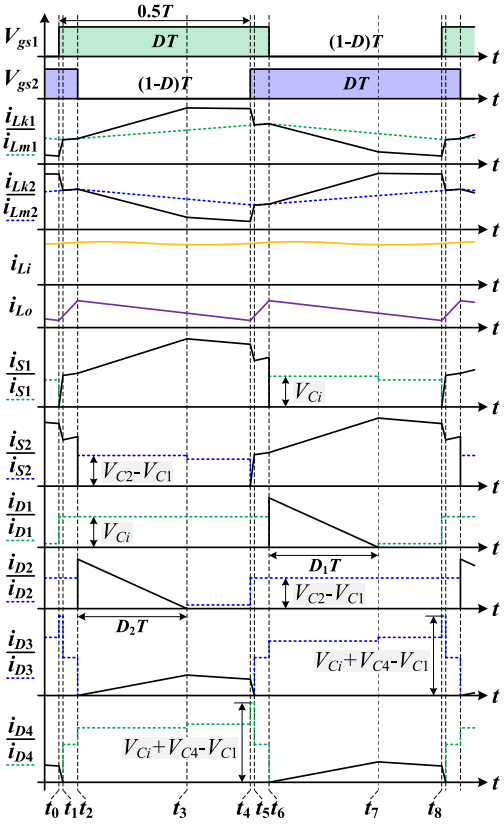

FIGURE 3. Key waveforms.

Mode I [t_0~t_1]: The switch S_2 and the diode D_3 are turned on, and other diodes are turned off. At time t_0, the current i_{S1} is increased from zero, and the ZCS turn-on of the switch S_1 is achieved. The coupled inductor 1 is charged by the input source V_{in}, the current i_{Lk1} is rapidly increased and the current i_{D4} is rapidly decreased. The output inductor L_o starts to be charged and the current i_{Lo} is increased linearly. At time t_1,

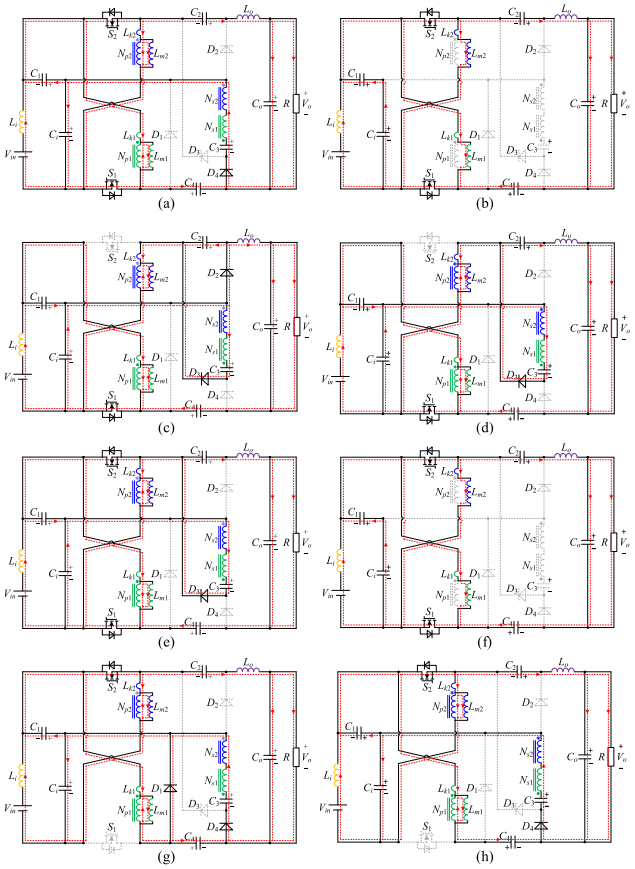

FIGURE 4. The equivalent circuit of YSCI-BBS converter in (a) mode I. (b) mode II. (c) mode III. (d) mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII. (h) Mode VIII.

the current i_{D4} decreases to zero, and the diode D_4 is turned off naturally. The current i_{D4} can be expressed as:

$$i_{D4}(t) = i_{D4}(t_0) + \frac{(n_2 - n_1)(V_{Ci} - V_{C1}) + V_{C3} - V_{C4} - V_{Ci}}{n_1^2 L_{k1} + n_2^2 L_{k2}}(t - t_0) \tag{1}$$

Mode II [t_1~t_2]: At time t_1, all diodes are turned off. Both coupled inductors are charged by the input source V_{in}, and the currents i_{Lm1} and i_{Lm2} are increased linearly. The current i_{Lo} continues to be increased linearly. The currents i_{Lm1} and i_{Lm2} can be expressed as:

$$\begin{cases} i_{Lm1}(t) = i_{Lm1}(t_1) + \dfrac{V_{in}}{L_{k1} + L_{m1}}(t - t_1) \\ i_{Lm2}(t) = i_{Lm2}(t_1) + \dfrac{V_{in} + V_{C1}}{L_{k2} + L_{m2}}(t - t_1) \end{cases} \tag{2}$$

Mode III [t_2~t_3]: At time t_2, the switch S_2 is turned off, and the diodes D_2 and D_3 are turned on. The energy of the leakage inductance L_{k2} is absorbed by the capacitor C_2 through the diode D_2 and the current i_{D2} is decreased linearly. The capacitor C_3 is charged by the secondary windings N_{s1} and N_{s2} through the diode D_3, the current i_{D3} is increased

from zero, and the ZCS turn-on of the diode D_3 is achieved. The output inductor L_o starts to discharge and the current i_{Lo} is decreased linearly. At time t_3, the current i_{D2} decreases to zero, and the ZCS turn-off of the diode D_2 is achieved. The currents of i_{Lk1} and i_{Lk2} can be expressed as:

$$\begin{cases} i_{Lk1}(t) = i_{Lm1}(t) + n_1 i_{D3},\ i_{Lk2}(t) = i_{Lm2}(t) - n_2 i_{D3} \\ i_{D3}(t) = \dfrac{(n_1 - n_2) V_{in} + (1+n_2) V_{C2} - n_1 V_{C1} - V_{C3}}{n_1^2 L_{k1} + n_2^2 L_{k2}} (t - t_2) \end{cases} \tag{3}$$

Mode IV [$t_3 \sim t_4$]: At time t_3, the current i_{D3} starts to decrease linearly, and the capacitor C_3 continues to be charged by the secondary windings N_{s1} and N_{s2} through the diode D_3. The current i_{Lo} is decreased linearly.

Mode V [$t_4 \sim t_5$]: At time t_4, the current i_{S2} is increased from zero, and the ZCS turn-on of the switch S_2 is achieved. The coupled inductor 2 is charged by the input source V_{in}, the current i_{Lk2} is rapidly increased and the current i_{D3} is rapidly decreased. The output inductor L_o starts to be charged and the current i_{Lo} is increased linearly. At time t_5, the current i_{D3} decreases to zero and the diode D_3 is turned off naturally. The current i_{D3} can be expressed as:

$$\begin{aligned} i_{D3}(t) &= i_{D3}(t_4) \\ &+ \frac{(n_1 - n_2)(V_{Ci} - V_{C1}) + V_{C1} - V_{C3}}{n_1^2 L_{k1} + n_2^2 L_{k2}} (t - t_4) \end{aligned} \tag{4}$$

Mode VI [$t_5 \sim t_6$]: This mode is the same as Mode II.

Mode VII [$t_6 \sim t_7$]: At time t_2, the switch S_1 is turned off, and the diodes D_1 and D_4 are turned on. The energy of the leakage inductance L_{k1} is absorbed by the capacitor C_1 through the diode D_1 and the current i_{D1} is decreased linearly. The capacitor C_4 is charged by the secondary side N_{s1}, N_{s2}, and capacitor C_3 in series through the diode D_4, the current i_{D4} is increased from zero, and the ZCS turn-on of the diode D_4 is achieved. The output inductor L_o starts to discharge and the current i_{Lo} is decreased linearly. At time t_7, the current i_{D1} decreases to zero, and the ZCS turn-off of the diode D_1 is achieved. The currents of i_{Lk1} and i_{Lk2} can be expressed as:

$$\begin{cases} i_{Lk1}(t) = i_{Lm1}(t) - n_1 i_{D4},\ i_{Lk2}(t) = i_{Lm2}(t) + n_2 i_{D4} \\ i_{D4}(t) = \dfrac{n_2 V_{Ci} + V_{C3} - (n_2 - n_1) V_{Ci} - V_{C4}}{n_1^2 L_{k1} + n_2^2 L_{k2}} (t - t_6) \end{cases} \tag{5}$$

Mode VIII [$t_7 \sim t_8$]: At time t_7, the current i_{D4} starts to decrease linearly, and the capacitor C_4 continues to be charged by the secondary windings N_{s1}, N_{s2} and capacitor C_3 through the diode D_4. The current i_{Lo} is decreased linearly.

III. PERFORMANCE ANALYSIS OF THE PROPOSED CONVERTER

A. TURNS RATIO SELECTION

According to the ampere-second balance principle of capacitors $C_1 \sim C_4$ and C_o, the average current of diodes $D_1 \sim D_4$ and output inductor L_o is equal to output current I_o, which can be expressed as:

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_o = L_o \tag{6}$$

According to the analysis of the operating mode, the average currents of the magnetizing inductances L_{m1} and L_{m2} can be expressed as:

$$\begin{cases} I_{Lm1} = \dfrac{1 + D + n_1}{1 - D} \\ I_{Lm2} = \dfrac{1 + D + n_2}{1 - D} \end{cases} \tag{7}$$

When $n_1 = n_2$, the average currents of the magnetizing inductors L_{m1} and L_{m2} are equal. The processing power of both coupled inductors is the same. Therefore, it can be assumed that $n_1 = n_2 = n$ in the following analysis.

B. VOLTAGE GAIN

According to Fig. 3, combined with (6) to (7), the time period $D_1 T$ (t_4 to t_5) and the time period $D_2 T$ (t_1 to t_2) can be expressed as:

$$D_1 T = D_2 T = \frac{2(1 - D)}{2 + n} T \tag{8}$$

During time period $D_2 T$, the current of diode D_3 is increasing, the voltage equation can be expressed as:

$$\frac{(1 + n) V_{C2} - n V_{C1} - V_{C3}}{n^2 (L_{k1} + L_{k2})} = \frac{(2 + n)^2 I_o}{2(1 + n)(1 - D)^2 T} \tag{9}$$

During time period $D_1 T$, the current of diode D_4 is increasing, the voltage equation can be expressed as:

$$\frac{n V_{Ci} + V_{C3} - V_{C4}}{n^2 (L_{k1} + L_{k2})} = \frac{(2 + n)^2 I_o}{2(1 + n)(1 - D)^2 T} \tag{10}$$

According to the volt-second balance principle of the input inductance L_i, the magnetizing inductances L_{m1}, L_{m2}, and the output inductance L_o in a switching period T, the following equations are given:

$$\begin{cases} V_{in} + V_{C1} - V_{Ci} = 0 \\ (V_{Ci} - V_{C1}) DT - V_{C1} D_1 T \\ \quad + \dfrac{V_{C3} + n(V_{Ci} - V_{C1}) - V_{C1} - V_{C4}}{1 + n} (1 - D - D_1) T = 0 \\ (V_{Ci} - V_{C1}) DT + (V_{Ci} - V_{C2}) D_2 \\ \quad + \dfrac{V_{Ci} + n(V_{Ci} - V_{C1}) - V_{C3}}{1 + n} (1 - D - D_2) T = 0 \\ (V_{C2} + V_{C4} - V_{C1} - V_o) D_1 T + (V_{Ci} + V_{C4} - V_o) D_2 T \\ \quad + \left(V_{C4} + V_{C2} - V_o + \dfrac{V_{C3} + n(V_{Ci} - V_{C1}) - V_{C1} - V_{C4}}{1 + n} \right) \\ \quad (1 - D - D_1) \\ \quad + \left(V_{C4} + V_{C2} - V_o + \dfrac{V_{Ci} + n(V_{Ci} - V_{C1}) - V_{C3}}{1 + n} \right) \\ \quad (1 - D - D_2) + (V_{Ci} + V_{C2} + V_{C4} - V_{C1} - V_o) \\ \quad (2D - 1) T = 0 \end{cases} \tag{11}$$

By combining (10)∼(11), the voltage gain considering the leakage inductance can be expressed as:

$$G = \frac{V_o}{V_{in}} = \frac{1 + 3D + 2n}{1 - D + \frac{n^2(2+n)^2}{(1+n)^2(1-D)}Q} \tag{12}$$

where, $Q = \frac{L_{k1}+L_{k2}}{RT}$ is the leakage inductance constant.

Fig. 5 shows the relationship between the voltage gain and the duty cycle under different leakage inductances. It can be seen that the leakage inductance affects the voltage gain. The voltage gain decreases with increasing leakage inductance and duty cycle. Therefore, the proposed converter should not work under the limited duty cycle in practical applications.

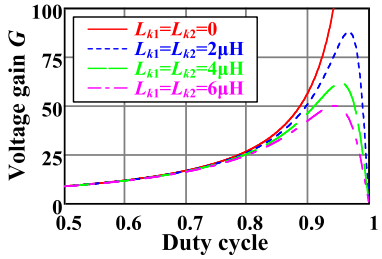

FIGURE 5. Voltage gain considering the effect of the leakage inductance (n = 1, CR = 400, CT = 1/50000).

If $L_{k1} = L_{k2} = 0$, the ideal voltage gain of the proposed converter can be expressed as:

$$G = \frac{V_o}{V_{in}} = \frac{1 + 3D + 2n}{1 - D} \tag{13}$$

C. VOLTAGE STRESS

According to the performance analysis, the voltage stresses of the capacitors are given by:

$$V_{vs-Ci} = \frac{1}{1-D}V_{in} = \frac{1}{1+3D+2n}V_o \tag{14}$$

$$V_{vs-C1} = \frac{D}{1-D}V_{in} = \frac{D}{1+3D+2n}V_o \tag{15}$$

$$V_{vs-C2} = \frac{1+D}{1-D}V_{in} = \frac{1+D}{1+3D+2n}V_o \tag{16}$$

$$V_{vs-C3} = \frac{1+D+n}{1-D}V_{in} = \frac{1+D+n}{1+3D+2n}V_o \tag{17}$$

$$V_{vs-C4} = \frac{1+D+2n}{1-D}V_{in} = \frac{1+D+2n}{1+3D+2n}V_o \tag{18}$$

The voltage stress of switches S_1 and S_2 is given by:

$$V_{vs-S1} = V_{vs-S2} = \frac{1}{1-D}V_{in} = \frac{1}{1+3D+2n}V_o \tag{19}$$

The voltage stresses of diodes are given by:

$$V_{vs-D1} = V_{vs-D2} = \frac{1}{1-D}V_{in} = \frac{1}{1+3D+2n}V_o \tag{20}$$

$$V_{vs-D3} = V_{vs-D4} = \frac{1+2n}{1-D}V_{in} = \frac{1+2n}{1+3D+2n}V_o \tag{21}$$

D. CURRENT STRESS

Assuming that Δi_{Lm1}, Δi_{Lm2}, and Δi_{Lo} are the current ripples of the magnetizing inductors L_{m1}, L_{m2}, and the output inductor L_o, which are expressed as:

$$\begin{cases} \Delta i_{Lm1} = \dfrac{V_{in}DT}{L_{m1}} \\ \Delta i_{Lm2} = \dfrac{V_{in}DT}{L_{m2}} \\ \Delta i_{Lo} = \dfrac{V_{in}\,(2D-1)\,T}{L_o} \end{cases} \tag{22}$$

The peak currents of diodes $D_1 \sim D_4$ can be expressed as:

$$i_{D1\_peak} = \frac{2+n}{1-D}I_o + \frac{1}{2}\left(\Delta i_{Lm1} + \Delta i_{Lo}\right) \tag{23}$$

$$i_{D2\_peak} = \frac{2+n}{1-D}I_o + \frac{1}{2}\left(\Delta i_{Lm2} + \Delta i_{Lo}\right) \tag{24}$$

$$i_{D3\_peak} = \frac{2+n}{(1-D)\,(1+n)}I_o + \frac{\Delta i_{Lm2} + \Delta i_{Lo}}{2\,(1+n)} - \frac{4I_o\,(\Delta i_{Lm2} + \Delta i_{Lo})}{(1+n)\,[2\,(2+n)\,I_o + (1-D)\,(\Delta i_{Lm2} + \Delta i_{Lo})]} \tag{25}$$

$$i_{D4\_peak} = \frac{2+n}{(1-D)\,(1+n)}I_o + \frac{\Delta i_{Lm1} + \Delta i_{Lo}}{2\,(1+n)} - \frac{4I_o\,(\Delta i_{Lm1} + \Delta i_{Lo})}{(1+n)\,[2\,(2+n)\,I_o + (1-D)\,(\Delta i_{Lm1} + \Delta i_{Lo})]} \tag{26}$$

The peak currents of switches S_1 and S_2 can be expressed as:

$$\begin{aligned} i_{S1\_peak} &= \frac{2+n}{1-D}I_o + \frac{\Delta i_{Lo}}{2} - \frac{4I_o\Delta i_{Lo}}{2\,(2+n)\,I_o + (1-D)\,\Delta i_{Lo}} \\ &\quad + \frac{[2\,(2-4D-n)\,I_o - (1-D)\,(\Delta i_{Lm2} + \Delta i_{Lo})]\,\Delta i_{Lm1}}{2D\,[2\,(2+n)\,I_o + (1-D)\,(\Delta i_{Lm2} + \Delta i_{Lo})]} \\ &\quad + n i_{D3\_peak} \end{aligned} \tag{27}$$

$$\begin{aligned} i_{S2\_peak} &= \frac{2+n}{1-D}I_o + \frac{\Delta i_{Lo}}{2} - \frac{4I_o\Delta i_{Lo}}{2\,(2+n)\,I_o + (1-D)\,\Delta i_{Lo}} \\ &\quad + \frac{[2\,(2-4D-n)\,I_o - (1-D)\,(\Delta i_{Lm1} + \Delta i_{Lo})]\,\Delta i_{Lm2}}{2D\,[2\,(2+n)\,I_o + (1-D)\,(\Delta i_{Lm1} + \Delta i_{Lo})]} \\ &\quad + n i_{D4\_peak} \end{aligned} \tag{28}$$

According to (22)∼(28), if $L_{m1} = L_{m2}$, the equations $i_{S1\_peak} = i_{S2\_peak}$, $i_{D1\_peak} = i_{D2\_peak}$ and $i_{D3\_peak} = i_{D4\_peak}$ are obtained. Therefore, the operating mode of the proposed converter is symmetrical.

E. BOUNDARY CONDITION ANALYSIS

When the proposed converter is operated in discontinuous conduction mode (DCM), assuming $L_{m1} = L_{m2} = L_m$, the key current waveform of DCM mode is shown in Fig. 6. Among them, D_xT and D_yT are the conduction time of diodes $D_{1(2)}$ and $D_{3(4)}$, respectively.

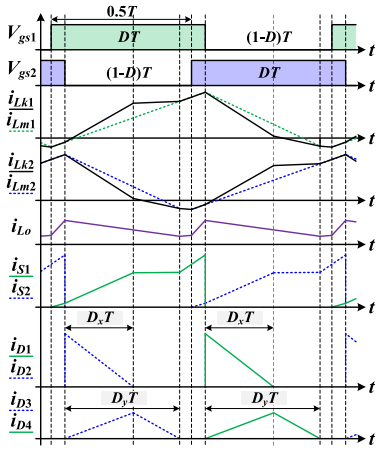

FIGURE 6. Key waveforms (DCM).

Assuming that the sum of the peak current of the magnetizing inductance L_m and the output inductance L_o is i_{Lep}, which can be expressed as:

$$i_{Lep} = \frac{V_{in}DT}{L_m} + \frac{V_{in}(2D-1)T}{L_o} = \frac{V_{in}DT}{\frac{DL_mL_o}{DL_o+(2D-1)L_m}} = \frac{V_{in}DT}{L_e} \tag{29}$$

where, $L_e = \frac{DL_mL_o}{DL_o+(2D-1)L_m}$ is defined as the equivalent inductance of the proposed converter.

According to Fig. 6, the average currents of diodes $D_{1(2)}$ and $D_{3(4)}$ are expressed as:

$$I_{D1(2)} = \frac{i_{Lep}D_xT}{2T} = I_o \tag{30}$$

$$I_{D3(4)} = \frac{\frac{D_y-D_x}{(1+n)D_y}i_{Lep}D_yT}{2T} = I_o \tag{31}$$

Solving (30) and (31), the duty cycles D_x and D_y can be obtained as:

$$D_x = \frac{2I_o}{i_{Lep}} \tag{32}$$

$$D_y = \frac{2(2+n)I_o}{i_{Lep}} \tag{33}$$

When the duty cycle D_y is equal to 1-D, the proposed converter is operated in boundary conduction mode (BCM). The time constant of the equivalent inductance can be defined as:

$$\tau_{Le} = \frac{L_e}{RT} \tag{34}$$

Combining (32) and (33), the boundary time constant of the equivalent inductance can be calculated as:

$$\tau_{LeB} = \frac{D(1-D)^2}{2(2+n)(1+3D+2n)} \tag{35}$$

According to (35), the boundary conditions of the proposed converter under different turn ratios are shown in Fig. 7. If $\tau_{Le} > \tau_{LeB}$, the proposed converter is operated at CCM

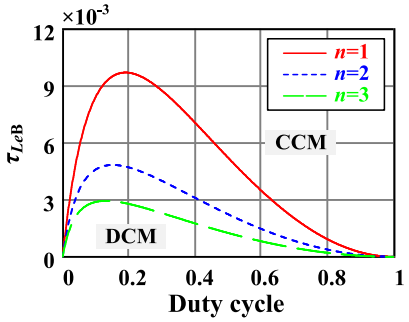

FIGURE 7. Boundary condition of the proposed converter.

and the region of CCM becomes wider as the turns ratio n increases.

F. TOPOLOGY VARIATION

The voltage gain of the proposed converter can be increased by adding different voltage multiplier cells. The general topology of the proposed converter with capacitor voltage multiplier cells (C-VMC) and coupled inductor voltage multiplier cells (CI-VMC) are shown in Fig. 8.

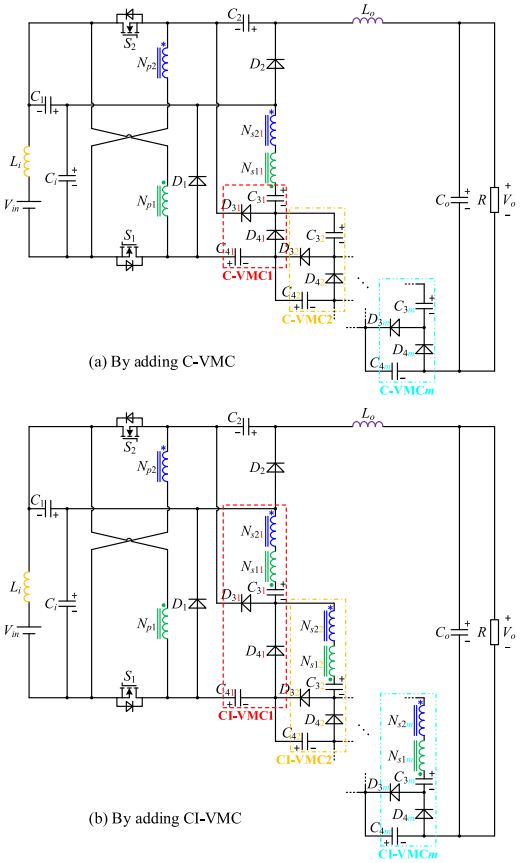

FIGURE 8. The general structure of the proposed converter. (a) By adding C-VMC. (b) By adding CI-VMC.

If m C-VMCs and m CI-VMCs are added, the general voltage gain and switch voltage stress of the converter can

TABLE 1. Performance comparison of the proposed converter with other literatures.

Topologies	[18]	[34]	[35]	[36]	Proposed
Voltage gain	$\frac{3+D}{1-D}$ (Lower)	$\frac{1+D+2n}{1-D}$ (Lower)	$\frac{2+2n}{1-D}$ (Higher when D<0.5)	$\frac{2+2n}{1-D}$ (Higher when D<0.5)	$\frac{1+3D+2n}{1-D}$ (Higher when D>0.5)
Switches voltage stress	$\frac{1}{3+D}V_o$	$\frac{1}{1+D+2n}V_o$	$\frac{1}{2+2n}V_o$	$\frac{1}{2+2n}V_o$	$\frac{1}{1+3D+2n}V_o$
Max. diodes voltage stress	$\frac{2}{3+D}V_o$	$\frac{1+n}{1+D+2n}V_o$	V_o	$\frac{1}{2}V_o$	$\frac{1+2n}{1+3D+2n}V_o$
No. of switches	2	2	4	2	2
No. of diodes	4	4	2	6	4
Switching type	Hard	ZCS	ZVS	ZCS	ZCS
Input current ripple	Large	Large	Low	Low	Very low
Output current	Pulsating	Pulsating	Pulsating	Pulsating	Continuous

be expressed as:

$$\begin{cases} G = \dfrac{3D + m\,(1+2m)}{1-D} \\ V_{vs-S} = \dfrac{1}{3D + m\,(1+2m)} \end{cases} \quad \text{(C-VMC)} \tag{36}$$

$$\begin{cases} G = \dfrac{3D + m\,[1+(1+m)\,n]}{1-D} \\ V_{vs-S} = \dfrac{1}{3D + m\,[1+(1+m)\,n]} \end{cases} \quad \text{(CI-VMC)} \tag{37}$$

It can be seen that the proposed converter achieves higher voltage gain and lower switch voltage stress by adding different voltage multiplier cells. These variations are more suitable for ultra-high step-up applications. Corresponding to the target output voltage levels of different applications, the corresponding number of unit cascades can be obtained according to the gain formula. However, the cost increase and loss issues caused by the multi-unit expansion structure must be considered.

G. COMPARISON

The proposed converter is compared with other high step-up converters proposed in the literature. The performance comparisons are shown in Table 1. In general, the step-up converter operates at $D > 0.5$, the proposed converter achieves higher voltage gain and lower switch voltage stress with two switches and four diodes. Compared to the converter proposed in [36], the proposed converter has a slightly higher maximum voltage stress of the diode but it is still lower than the output voltage. At the same time, the proposed converter achieves the lowest input current ripple and continuous output current, which is more suitable for high step-up applications.

IV. DESIGN CONSIDERATIONS

In order to verify the correctness of the theoretical analysis, a 32V input, 400V output, and 400W full-load prototype is designed. The switching frequency is selected as 50kHz.

A. DESIGN OF COUPLED INDUCTORS

The turns ratio n of the coupled inductors can be determined by the voltage gain and the maximum steady-state duty cycle. According to (13), the turns ratio n of the coupled inductors can be calculated as:

$$n = \frac{1}{2}\left[\frac{(1-D_{\max})\,V_o}{V_{in}} - 1 - 3D_{\max}\right] \tag{38}$$

Assuming that the maximum steady-state duty cycle $D_{\max}$ is 0.75. According to (38), the turns ratio $n = 1$ is selected.

The magnetizing inductances of the coupled inductors can be designed based on their current ripple. Assuming that the current ripple coefficient is designed as $\alpha = 0.6$, the magnetizing inductance can be calculated as:

$$\begin{aligned} L_m = L_{m1} = L_{m2} &= \frac{V_{in}D}{\alpha I_{Lm} f_s} = \frac{V_{in}D\,(1-D)}{\alpha\,(1+D+n)\,I_\alpha f_s} \\ &\geq 96.85\mu\text{H} \end{aligned} \tag{39}$$

therefore, the magnetizing inductances are designed as $L_{m1} = L_{m2} = 100\mu$H.

The leakage inductance of the coupled inductors can alleviate the diode reverse recovery problem. The leakage inductance can be designed based on the current falling rate of diodes, which can be calculated as:

$$L_k = L_{k1} = L_{k2} = \frac{(1+n)\,V_o}{2n^2\,(1+3D+2n)\,\frac{di_{D3(4)}}{dt}} \tag{40}$$

In general, the reverse recovery of the diode is alleviated when the current falling rate is less than 30A/us. According to (40), $L_k > 2.76\mu$H is designed.

In order to improve the integration of the prototype, two coupled inductors can be integrated into one magnetic core. The coupled inductors are decoupled and integrated into an EE core. The magnetic model is shown in Fig. 9. The coupled inductors are wound around the outer legs and the middle leg is used as a low-resistance magnetic circuit to realize their decoupling.

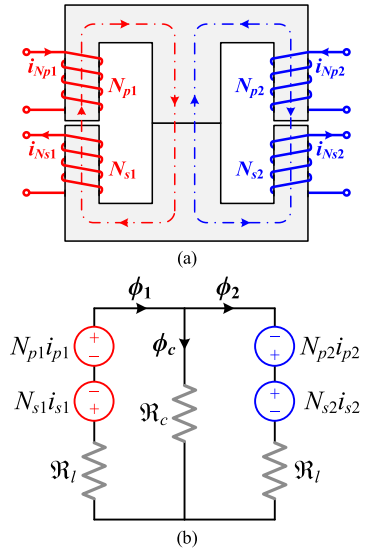

FIGURE 9. Magnetic model of EE core. (a) Flux flow path. (b) Equivalent circuit of the coupled-inductors.

The flux values flowing through the outer and central legs can be calculated as:

$$\begin{cases} \phi_1 = \dfrac{N_{p1}I_{Np1} - N_{s1}I_{Ns1} + \alpha\left(N_{p2}I_{Np2} - N_{s2}I_{Ns2}\right)}{(1+\alpha)\,\Re_l} \\ \phi_2 = \dfrac{N_{p2}I_{Np2} - N_{s2}I_{Ns2} + \alpha\left(N_{p1}I_{Np1} - N_{s1}I_{Ns1}\right)}{(1+\alpha)\,\Re_l} \\ \phi_c = \dfrac{N_{p1}I_{Np1} - N_{s1}I_{Ns1} - \left(N_{p2}I_{Np2} - N_{s2}I_{Ns2}\right)}{(1+\alpha)\,\Re_l} \end{cases} \tag{41}$$

where $\alpha = \Re_c/(\Re_c + \Re_l)$. When $N_{p1} = N_{p2} = N_p$, the dc fluxes in outer leg and center legs can be calculated by:

$$\begin{cases} \phi_{1-dc} = \dfrac{N_p I_{Lm}}{\Re_l} \\ \phi_{2-dc} = \dfrac{N_p I_{Lm}}{\Re_l} \\ \phi_{c-dc} = \phi_{1-dc} - \phi_{2-dc} = 0 \end{cases} \tag{42}$$

The ac fluxes in outer leg and center leg can be calculated by:

$$\begin{cases} \Delta\phi_{1-ac} = \Delta\phi_{2-ac} = \dfrac{V_{in}DT}{N_p} \\ \Delta\phi_{c-dc} = \dfrac{V_{in}\,(2D-1)\,T}{N_p} \end{cases} \tag{43}$$

Based on the above analysis and magnetic design theory, the core area A_c of the outer leg can be expressed as:

$$A_c = \frac{L_{m1(2)}\left(I_{Lm} + \frac{\Delta i_{Lm}}{2}\right)}{nB_{\max}} \tag{44}$$

where $B_{\max}$ is the maximum flux density.

According to (42)-(44), the EE55B magnetic core (PC40) is selected, the air gap of both outer legs is 0.8 mm and the number of primary turns of both coupled inductors is 17.

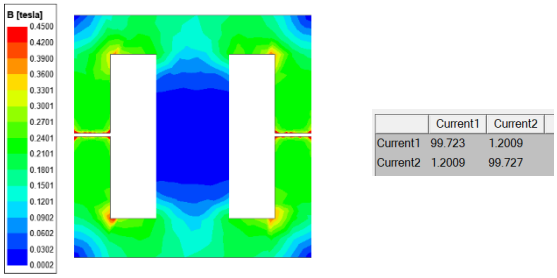

FIGURE 10. The general structure of the proposed converter.

The simulation of the magnetic flux density is shown in Fig. 10. It can be seen that the fluxes generated by the two coupled inductors are canceled in the center leg resulting in a lower flux density.

B. DESIGN OF INPUT AND OUTPUT INDUCTORS

The input inductor L_i and capacitors C_1 and C_i form a voltage loop, and its current ripple can be expressed as:

$$\Delta i_{Li} = \frac{V_{in} + V_{C1} - V_{Ci}}{L_i}\Delta T \tag{45}$$

Assuming that the voltage ripple of capacitors C_i and C_1 is 1%, the ripple of the input current is less than 10%. According to (45), the input inductance is designed as $L_i = 2.2\mu$H, which can effectively achieve a very low input current ripple.

The output inductor can be designed based on its equivalent average current, which can be expressed as:

$$I_{Loeq} = \frac{1}{2}\Delta i_{Lo} = \frac{2\,(2+n)\,I_o}{1-D} - \frac{1}{2}\Delta i_{Lm1(2)} \tag{46}$$

Assuming that the current ripple coefficient is designed as 0.2, the output inductance can be calculated as:

$$L_o = \frac{V_{in}\,(2D-1)}{0.2 I_{Loeq}\,f_s} > 53.4\mu\text{H} \tag{47}$$

In order to obtain a smaller output current ripple, the output inductor is designed as $L_o = 220\mu$H.

C. DESIGN OF CAPACITORS

The capacitors can be designed based on their voltage ripple and the output power P_o. Assuming that the voltage ripple of capacitors C_i and $C_1 \sim C_4$ is 1%, the voltage ripple of output capacitor C_o is 0.5%. The capacitors can be calculated as:

$$\begin{cases} C_i = \dfrac{P_o\,(1+3D+2n)}{1\%V_o^2 f_s} \geq 24.2\mu\text{H} \\ C_1 = \dfrac{P_o\,(1+3D+2n)}{1\%DV_o^2 f_s} \geq 39.5\mu\text{H} \\ C_2 = \dfrac{P_o\,(1+3D+2n)}{1\%\,(1+D)\,V_o^2 f_s} \geq 15.0\mu\text{H} \\ C_3 = \dfrac{P_o\,(1+3D+2n)}{1\%\,(1+D+n)\,V_o^2 f_s} \geq 9.3\mu\text{H} \\ C_4 = \dfrac{P_o\,(1+3D+2n)}{1\%\,(1+D+2n)\,V_o^2 f_s} \geq 6.7\mu\text{H} \\ C_o = \dfrac{P_o}{0.5\%V_o^2 f_s} \geq 10.0\mu\text{H} \end{cases} \tag{48}$$

Therefore, the capacitors are designed as $C_i = 100\mu$F, $C_1 = C_2 = 22\mu$F, $C_3 = C_4 = 20\mu$F, $C_o = 47\mu$F.

D. EFFICIENCY AND LOSS

Calculate the losses:

$$\begin{cases} P_{\mathrm{S}} = \sum\limits_{k=1,2} \left[I_{\mathrm{Sk\,rms}}^2 r_{\mathrm{Sk}} + \dfrac{f_s}{2}(V_{DS} I_{Lmk} t_{off} + V_{DSk}^2 C_{ossk}) \right] \\ P_L = \sum\limits_{k=1,2} I_{Lk\mathrm{rms}}^2 r_{Lmk} + I_{Ns\mathrm{rms}}^2 r_{Ns} \\ P_D = \sum\limits_{k=1,2,3,4} (I_0 V_{Fk} + I_{Dk\mathrm{rms}}^2 r_{Dk}) \\ P_C = \sum\limits_{k=1,2,3,o} I_{Ck\mathrm{rms}}^2 r_{Ck} \end{cases} \tag{49}$$

where V_{DS} is the turn-off voltage, t_{off} is the fall time, and C_{oss} is the output capacitance. V_F is the forward voltage drop, and r is the equivalent series resistance.

Therefore, the total loss and efficiency of the proposed converter can be estimated by:

$$P_{loss} = P_{\mathrm{S}} + P_L + P_D + P_C \tag{50}$$

$$\eta = \frac{P_o}{P_o + P_{loss}} \tag{51}$$

where, the parasitic parameters of the components can be obtained from the manufacturer datasheet and the rms currents of each component can be obtained from experimental tests.

V. EXPERIMENTAL RESULTS

According to the design parameters in Section IV, a prototype with 32V input, 400V output, and 400W full-load was built. Based on the calculation formula in Section IV as the basis for device selection, determine the specific parameters while ensuring the normal operation of the converter, and select switching devices with high-cost performance, low loss, and high efficiency. The key parameters of the prototype are shown in Table 2. A picture of the prototype is shown in Fig. 11. To facilitate testing, the current test terminal is on the prototype's top, and the switching device is on the bottom.

TABLE 2. The key parameter of the prototype.

Parameters	Proposed
Switches S_1, S_2	IPP075N15N3G
Diodes D_1, D_2	MBR20100CT
Diodes D_3, D_4	MUR1540CT
Input inductor L_i	2.2μH
Coupled inductors	L_{m1}=101.64μH, L_{k1}=3.95μH L_{m2}=100.98μH, L_{k2}=6.87μH n=1
Output inductor L_o	220μH
Capacitors C_i	100μF/100V electrolytic capacitor
Capacitors C_1, C_2	4×5.6μF/100V film capacitor
Capacitors C_3, C_4	2×10μF/400V film capacitor
Capacitors C_o	47μF/450V electrolytic capacitor
Switching frequency	50kHz

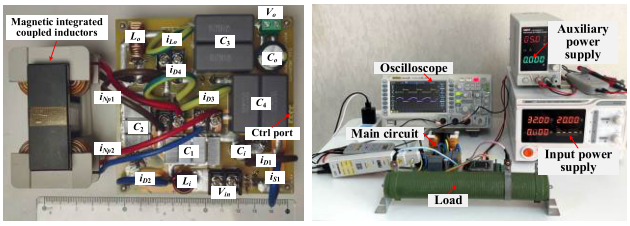

FIGURE 11. Picture of the prototype. (a) The prototype. (b) Experiment testing platform.

Photovoltaic arrays often use simple boost cascades. Fig. 12(a), and (b) show the experimental waveform of the boost converter. Under the same 400v output conditions, the duty cycle must be about 0.75. The gain effect is poor, and the input current ripple is large. Affect the stability of equipment operation. It is not difficult to see that the voltage impact of the switch is large, almost 200% its stress, and its voltage stress is the same as the output voltage. At the same time, there are serious reverse recovery phenomena and hard switching problems, and large losses can easily cause failures. The subsequent waveforms are the experimental results of the converter proposed in this article.

Fig. 12(c) shows the current waveforms of the primary windings L_{k1} and L_{k2} of the coupled inductor. Fig. 12(d) shows the current waveforms of the input current and output inductor L_o. It can be seen that the very low input current ripple and continuous output current of the prototype are achieved. Fig. 12(e)∼ (g) shows the voltage and current waveforms of the switches S_1 and S_2. It can be seen that the voltage stress of the switches S_1 and S_2 are both about 85V, which achieves a lower voltage stress. At the same time, the ZCS turn-on of both switches is achieved. Fig. 12(h)∼(i) shows the voltage and current waveforms of diodes. It can be seen that the diodes D_1, D_2 and the switches S_1, S_2 have the same voltage stress, and the ZCS turn-off of the diodes D_1 and D_2 are achieved. The maximum voltage stress of the diodes D_3 and D_4 is around 325V. The ZCS turn-on of diodes D_3 and D_4 are achieved and their reverse recovery problems are alleviated. Fig. 12(j) shows the dynamic effect waveform, with small fluctuations. The converter works stably and efficiently.

The measured efficiency of the prototype at 400V output is shown in Fig. 13(a). It can be seen that the peak efficiency is 96.2% and the full load efficiency is 95.9%. The efficiency of the prototype at full load is calculated as 97.25%. The measurement efficiency is lower than the calculated efficiency because of the large line losses caused by the leads at the current test terminals in the prototype. Therefore, a more compact layout and thicker copper can further reduce losses.

The loss breakdown of the prototype at full load is shown in Fig. 13(b). The power loss of the prototype is mainly generated in switches, diodes, and coupled inductors. The selection of better performing components can further improve the efficiency of the prototype.

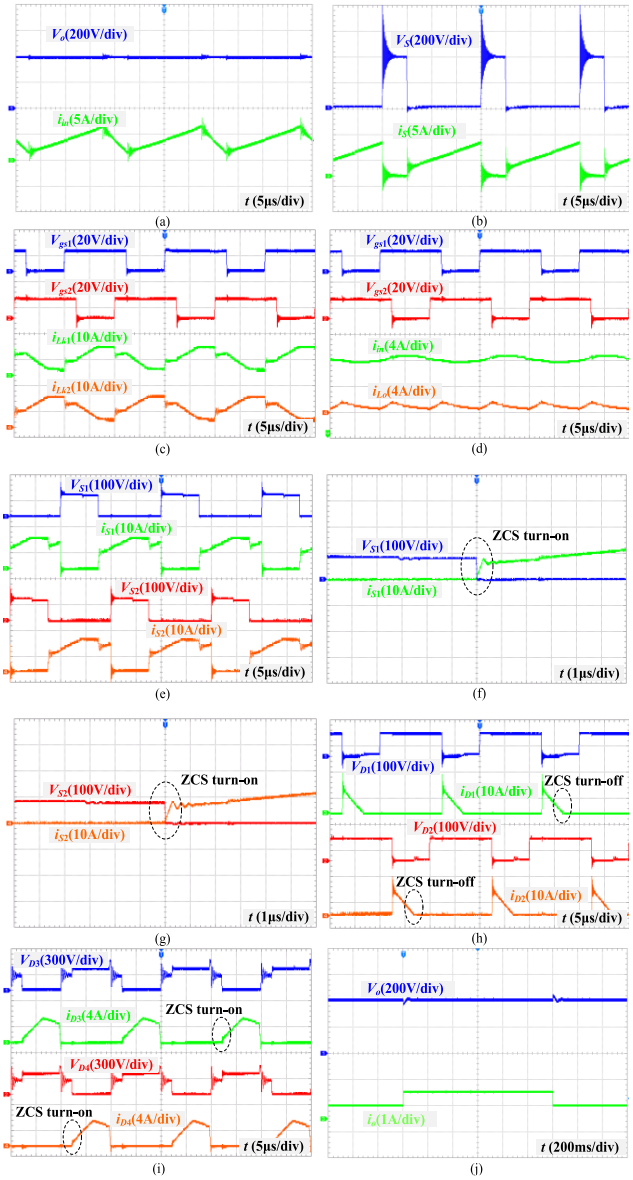

FIGURE 12. Experimental waveforms. (a) Boost- V_o& i_{in} (b) Boost- V_S& i_S. (c) V_{gs1}, V_{gs2}, i_{Lk1} & i_{Lk2}. (d) V_{gs1}, V_{gs2}, i_{in} & i_{Lo}. (e) V_{S1}, i_{S1} & V_{S2}, i_{S2}. (f) $S_{1ZCS\text{-}on}$. (g) $S_{2ZCS\text{-}on}$. (h) V_{D1}, i_{D1} & V_{D2}, i_{D2}. (i) V_{D3}, i_{D3} & V_{D4}, i_{D4}. (j) dynamic waveform.

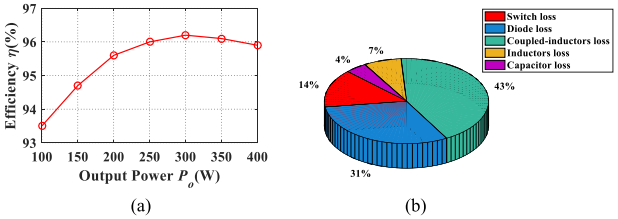

FIGURE 13. Efficiency analysis. (a) Test efficiency. (b) Power loss proportion.

VI. CONCLUSION

In this paper, an interleaved Buck-Boost-Zeta converter with the coupled inductor multiplier cell and zero input current ripple was proposed. A higher voltage gain of the proposed converter is achieved by integrating the coupled inductor voltage multiplier cell. The leakage inductance energy is absorbed by the passive clamping circuit, which suppresses the voltage spike generated by the switch parasitic capacitance and leakage inductance resonance. Therefore, very low voltage stress of the switch is achieved. At the same time, the ZCS turn-on of the switches is achieved and the reverse recovery problem of the diodes is alleviated. Moreover, the proposed converter has a very low input current ripple and continuous output current, which is very friendly to photovoltaic arrays and DC-bus. A 32V input, 400V output, and 400W prototype was built to verify the correctness of the theoretical analysis. The proposed converter is more suitable for high step-up applications such as the photovoltaic power generation system.

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