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RESEARCH ARTICLE

Fully Soft-Switched Single-Switch High Gain DC–DC Topology Based on Coupled Inductor

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ABSTRACT High-gain DC/DC converters play critical roles in most renewable-energy applications such as wind and solar power. A significant number of the high-gain converters are utilized to boost voltage gain by employing an excessive duty cycle and low turn ratio. However, the operation in high duty cycle raises losses and costs, lowers system effectiveness, and results in a low efficiency. This paper proposes a novel solution for a high-gain DC/DC boost converter. The proposed converter can be utilized in low input voltage scenarios that require a large voltage gain, such as solar photovoltaic panels and fuel cells. The novel topology is characterized by a simple operation, high voltage gain, improved efficiency by utilizing two resonance circuits, and continuous input current. An experimental high-gain boost converter with a power output of 300 watts and a voltage ranging from 20 volts to 160 volts is utilized to demonstrate the efficiency of the proposed converter topology.

INDEX TERMS High gain converter, DC to DC converter, two windings coupled-inductor, zero current switching.

I. INTRODUCTION

Solar energy infrastructure has become more decentralized, allowing individuals and communities to generate and store their own solar power, reducing reliance on traditional energy sources [1], [2]. One of the main challenges in such a production is the variations in the produced power due to continuously varying weather conditions and loads. High step-up voltage DC/DC converter topologies with higher efficiency are often employed to correct tracking of the output and raise the low photovoltaic (PV) voltage level to appropriate DC level required for inverters when connecting PV supplies to the electrical grid and obtaining the maximum energy potential from such sources under various operating environments [3]. Typically, a voltage ranging from 200 V to 400 V or even higher is supplied through the ac network or inverters. PV or batteries with cells can be linked in series or, ideally, in parallel to avoid voltage imbalance between the cells. However, the voltage levels using such links are often insufficient thus necessitating the use of DC/DC converters [17], [18], [19], [20], [21], [22], [23].

Recent studies have widely applied DC/DC boost converters to obtain an additional voltage gain in high-voltage applications [4]. An interleaved DC/DC boost converter was implemented in [5] by connecting two conventional boost converters in parallel to obtain high voltage gain with low current stresses. Notably, this approach posed challenges related to control complexity, efficiency trade-offs, and component sizing. Voltage-multiplier modules of capacitors, inductors and diodes with a voltage-raise circuit were applied in [6] to enhance the converter voltage gain. However, the method was not cost effective because the solution consisted of three

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independent topologies and cores. The work in [7] applied single-switch three-diode converters operating at constant frequency and constant duty cycle. The presented topology provided a high voltage gain, but the method resulted in discontinuous input current due to the series connection of the primary switch with the input DC supply. A coupled-inductor (CI) flyback converter was introduced in [8], and two coupled-inductor-based Z-source networks were presented in [9] to substantially increase the voltage gains. The drawbacks of these methods included a complexity in CI design and significant winding losses, respectively.

The work in [10] presented a high-gain converter topology based on a CI with three-windings. While this topology had a common-ground feature the input current was discontinues. The modified topology in [11] had a continuous input current while the voltage gain for renewable sources was not sufficient. The converters in [12] and [13] had an appropriate voltage gain and the input current was continuing, but there was no soft-switching operation, and the switching losses were high. The converters in [14] and [15] had a soft switching operation only for the output diode and the input current was discontinues. In the topologies presented in [16], not only these issues were solved, but also a fully soft switching for the single switch of the converter was considered. In order to achieve fully soft switching, the input current was damaged and made discontinuous, which required bulky capacitors at the input side.

This paper proposes a novel converter topology designed to address several critical issues in high step-up voltage DC/DC converters. The topology is characterized by its exceptional capability to ensure continuous input current, significantly improved efficiency, and higher voltage gain. This design enables seamless integration with renewable energy sources, such as solar panels, making it an ideal solution for clean energy applications.

The rest of the paper is organized as follow. The proposed converter topology and its operation principles are presented in Section II. Section III characterizes the proposed converter in terms of the semiconductors and other parameters. Section IV compares the proposed topology to other high-gain converter topologies. Performance analysis and component design are presented in Section V, followed by experimental results of the proposed converter configuration in Section VI. Finally, Section VII draws conclusion.

II. PROPOSED HIGH GAIN TOPOLOGY AND OPERATION PRINCIPLES

The suggested high step-up topology is an enhanced topology with some specific features. Fig. 1 (a) shows a high gain single switch topology in [25]. Unfortunately, there is no soft switching process at turning off the switch in this configuration and the switching losses are high. Fig. 1 (b) is a novelty for decreasing the switching loss and we can use it for zero voltage switching (ZVS) operation in some

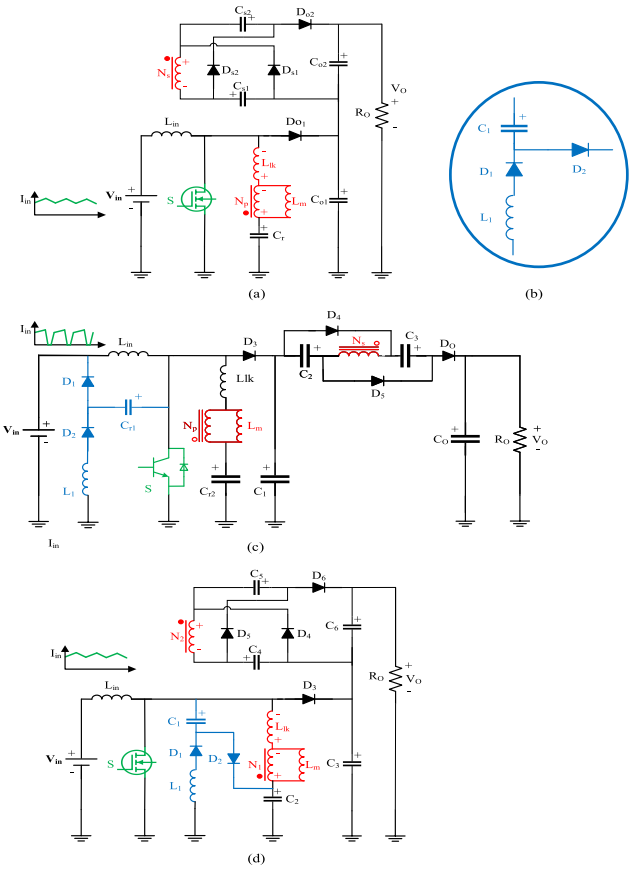


FIGURE 1. Topology derivation. (a). Topology in [24], (b). Circuit for achieving soft-switch operation (c). Topology in [1], (d)Suggested step up DC to DC topology.

specific configurations like topology in [1] which is shown in Fig. 1 (c).

The topology in [1] has an outstanding operation with minimum switching loss but the input current of this configuration is not continuous. A novel single MOSFET common ground topology having enhanced voltage gain is originally presented in order to get a high gain DC/DC topology for renewable sources, as depicted in Fig. 1 (d). Two resonance circuits are used that cause fully soft switching of the switch and decrease the voltage spikes of the components. Single CI with two windings, Single MOSFET (S), six diodes (D_{1-6}), six capacitors C_{1-6}, are used in the proposed topology. The CI in this converter is represented by an idealized transformer (N_p and N_s), with a magnetizing inductance L_m and a leakage inductance L_{lk}.

Equivalent circuit of the Suggested topology during six modes are depicted in Fig. 2 (a)-(f). Fig. 3 shows the main waveforms of the recommended topology.

Mode 1. Figure 2 (a) shows the equivalent circuit during mode one. At the beginning of this mode the MOSFET is turned on in zero current switching (ZCS) condition. The reason for this soft switching operation is related to input inductor and leakage inductance. In this mode the output

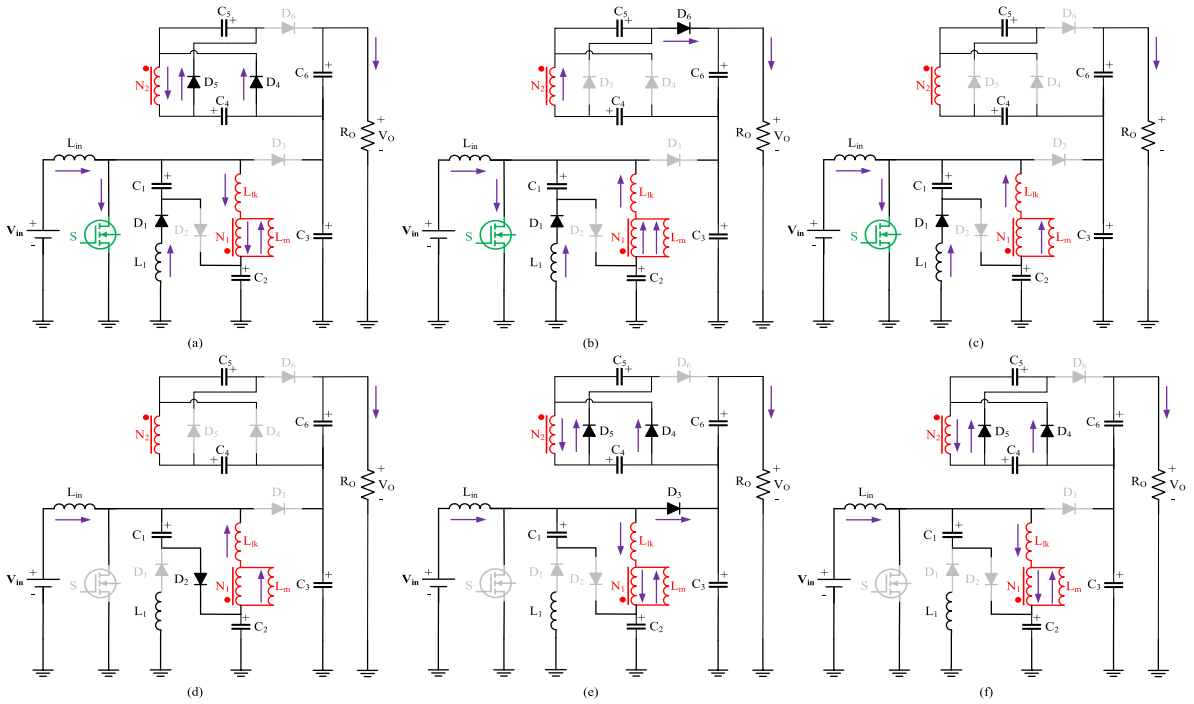


FIGURE 2. Equivalent circuit of the suggested topology during (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, and (f) Mode 6.

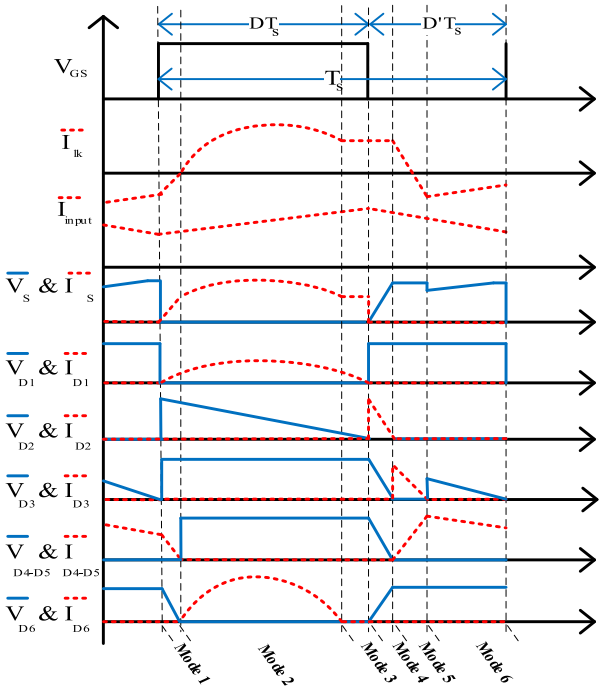


FIGURE 3. Essential waveforms of suggested High gain topology.

diodes D_3 and D_6 are reversed bias and diodes D_1, D_4, and D_5 are in forward bias state. As it can be found from Fig. 3, diode D_1 is turned on in ZCS due to inductor L_1.

Mode 2. This mode begins when output diode D_6 is in forward bias state. This diode turns on in ZCS condition due to resonance of the leakage inductance and C_2. The following equation can be obtained from this mode:

$$V_O = V_{C3} + V_{C6} \tag{1}$$

$$I_S = I_{in} + I_{lm} + I_{N1} + I_{L1} \tag{2}$$

$$V_{Lm}^D = \left[\frac{L_m}{L_m + L_k}\right] V_{C2} = kV_{C2} \tag{3}$$

$$V_{Lk}^D = \left[\frac{L_k}{L_m + L_k}\right] V_{C2} = (1-k)V_{C2} \tag{4}$$

$$V_{Lin}^D = V_{in} \tag{5}$$

$$V_{N2}^D = nV_{Lm}^D = knV_{C2} \tag{6}$$

$$V_{C4} + V_{C5} + V_{N2}^D = V_{C6} \tag{7}$$

Mode 3. In this mode, the resonant of the leakage inductance and C_2 is finished and D_6 turns off in ZCS. This mode lasts until the resonance of the L_1 and C_1 is finished and the switched turns off.

Mode 4. In this mode, most of the leakage inductance energy is stored in C_1 and it causes the switch voltage is increased slightly. On the other hand, switch turns off in zero voltage switching condition. It should be mentioned that C_1 and L_1 are not bulky passive components and they just utilized to absorb the leakage inductance energy which is caused high voltage spike on the switch and other components. The following equations can be obtained from this mode.

$$V_{C1} + V_{C2} + nV_{Lm}^D = V_{in} \tag{8}$$

$$V_{C1} = -V_{Lm}^{D'} - V_{Lk}^{D'} \tag{9}$$

Mode 5. By turning off D_2, D_3 turns on and the energy of L_{in} and the rest of the leakage inductance energy stored in C_3 through this diode. All the L_{lk} energy recycled in this mode and previous mode and the voltage spike of semiconductors are omitted completely. Also in this mode, C_4 and C_5 are charged through D_4, D_5, and N_s.

$$V_{Lin}^{D'} = V_{in} - V_{C3} \tag{10}$$
$$V_{Lm}^{D'} + V_{Lk}^{D'} = V_{Lin}^{D'} + V_{C1} - V_{in} \tag{11}$$
$$V_{Lm}^{D'} = V_{C2} - V_{C3} \tag{12}$$
$$V_{Lk}^{D'} = k\,(V_{C2} - V_{C3}) \tag{13}$$

Mode 6. By turning off *D3*, this mode is started and like as previous mode *C4* and *C5* are continued to charge. This mode ends when the switch turns on.

$$V_{Lin}^{D'} - V_{Lm}^{D'} - V_{Lk}^{D'} = V_{in} - V_{C2} \tag{14}$$
$$V_{C4} = V_{C5} = -V_{N2}^{D'} = -nV_{Lm}^{D'} \tag{15}$$
$$V_{N2}^{D'} = -V_{C1} + V_{C2} + V_{C3} - V_{C4} \tag{16}$$

III. VOLTAGE GAIN AND VOLTAGE STRESSES OVER THE MOSFET, DIODE(S), AND CAPACITOR(S)

A. G_m CALCULATION

By utilizing the volt-second equilibrium axiom for both input inductor and magnetizing inductance ((5) and (10)) V_{C3} is obtained:

$$\int_0^D V_{Lin}^{D} + \int_D^1 V_{Lin}^{D'} = 0 \rightarrow V_{C3} = \frac{V_{in}}{D'} \tag{17}$$

According to (16) and by utilizing the volt-second equilibrium axiom for magnetizing inductance and leakage inductance from (3), (4), (12), and (13) V_{C2} is obtained as follow:

$$\int_0^D (V_{Lm}^{D} + V_{Lk}^{D}) + \int_D^1 (V_{Lm}^{D'} + V_{Lk}^{D'}) = 0 \rightarrow V_{C2} = V_{in} \tag{18}$$

By substituting (18) into (6) this equation is obtained:

$$V_{N2}^{D} = nkV_{in} \tag{19}$$

By substituting (17) and (18) into (12) this equation is obtained:

$$V_{Lm}^{D'} = -k\frac{D}{D'}V_{in} \tag{20}$$

According to (15) and (20) V_{C4} and V_{C5} are obtained:

$$V_{C4} = V_{C5} = -V_{N2}^{D'} = nk\frac{D}{D'}V_{in} \tag{21}$$

By substituting (19) and (21) into (7) V_{C6} is obtained:

$$V_{C6} = nk\frac{1+D}{D'}V_{in} \tag{22}$$

By substituting (17) and (22) into (1) V_O is obtained:

$$V_O = \frac{V_{in}}{D'} + nk\frac{1+D}{D'}V_{in} \rightarrow V_O = \frac{1+nk+nkD}{D'}V_{in} \tag{23}$$

The nominal voltage gain of proposed converter in continuous conduction mode (CCM) is obtained:

$$G_{mCCM} = \frac{V_o}{V_{in}} = \frac{1+nk+nkD}{D'} \tag{24}$$

Hence, if the coupled inductor leakage inductance is not considered, it means the coupling coefficient k is equal to 1.

$$G_{mCCM} = \frac{V_o}{V_{in}} = \frac{1+n(1+D)}{D'} \tag{25}$$

Also, the V_{C1} is calculated from (9), and (20):

$$V_{C1} = \frac{D}{D'}V_{in} \tag{26}$$

B. VOLTAGE STRESS OF SEMICONDUCTORS

As indicated by past calculations, the MOSFET and diodes voltage stress is obtained from these following equations (27)-(31).

$$V_S = V_{D3} = V_{C3} = \frac{V_{in}}{D'} \tag{27}$$
$$V_{D1} \approx V_{C3} - V_{C1} = \frac{D}{D'}V_{in} \tag{28}$$
$$V_{D2} = V_{C2} + V_{C1} = \frac{V_{in}}{D'} \tag{29}$$
$$V_{D4} = V_{D5} = V_{C4} + V_{N2}^{D} = \frac{n}{D'}V_{in} \tag{30}$$
$$V_{D6} = V_{C6} - V_{C4} - V_{C5} - V_{N2}^{D'} = \frac{n}{D'}V_{in} \tag{31}$$

C. CURRENT STRESS OF SEMICONDUCTORS

To obtain conducting current of the MOSFET, assume Lin and L_m are adequate to ignore the current ripple. Ignoring the converter losses results in the following relationships:

$$I_{in} \approx I_{in(avg)} = G_m I_O \tag{32}$$
$$I_{lm} \approx I_{lm(avg)} = nI_O \tag{33}$$

The currents of the topology diodes are as follows:

$$I_{D1(peak)} \approx \frac{V_{C1}}{Z_{r1}} = \frac{DV_{in}}{D'\sqrt{\frac{L_1}{C_1}}} \tag{34}$$

$$I_{D2(peak)} \approx I_{in} + I_{lm} + \frac{V_{C1}}{Z_{r1}} = (G_m + n)\,I_O + \frac{DV_{in}}{D'\sqrt{\frac{L_1}{C_1}}} \tag{35}$$

$$I_{D3(peak)} \approx I_{in} + I_{lm} = (M+n)I_O \tag{36}$$

$$I_{D4(peak)} = I_{D5(peak)} \approx \frac{(M+n)I_O}{2n} \tag{37}$$

According to [25] it can be assumed $0.5^*T_{r2} = D^*T_s$ and for calculating I_{D6}:

$$I_{D6(peak)} \approx \frac{\pi T_s I_O}{T_{r2}} = \frac{\pi I_O}{2D} \tag{38}$$

Also, the switch current is approximately equal to:

$$I_S \approx I_{in} + I_{lm} + \frac{DV_{in}}{D'Z_{r1}}\sin(\omega_{r1}t) + \frac{\pi T_s I_O}{T_{r2}}\sin(\omega_{r2}t) \tag{39}$$

Thus, the MOSFET maximum current is:

$$I_{S(peak)} \approx (M+n)I_o + \frac{DV_{in}}{D'Z_{r1}} + \frac{N\pi T_s I_O}{T_{r2}} \tag{40}$$

D. DISCONTINUOUS CONDUCTING MODE (DCM) ANALYSE

According to (16) and by utilizing the volt-second equilibrium axiom for magnetizing inductance and leakage inductance from (3), (12)V_{C2} is obtained as follow:

$$\int_0^D V_{Lm}^D + \int_D^{D_1} V_{Lm}^{D'} = 0 \rightarrow V_{C2} = \frac{D_1 - D}{D_1 D'} V_{in} \tag{41}$$

By substituting (41) into (6) obtains:

$$V_{N2}^D = nk \frac{D_1 - D}{D_1 D'} V_{in} \tag{42}$$

By substituting (17) and (41) into (12) result in:

$$V_{Lm}^{D'} = k\left(\frac{D_1 - D}{D_1 D'} V_{in} - \frac{V_{in}}{D'}\right) \tag{43}$$

According to (15) and (43) V_{C4} and V_{C5} are obtained:

$$V_{C4} = V_{C5} = -V_{N2}^{D'} = nk\left(\frac{V_{in}}{D'} - \frac{D_1 - D}{D_1 D'} V_{in}\right) \tag{44}$$

By substituting (42) and (44) into (7) V_{C6} gives:

$$V_{C6} = nk\left(\frac{D_1 + D}{D_1 D'}\right) V_{in} \tag{45}$$

By substituting (17) and (45) into (1) V_O obtains:

$$V_O = \frac{V_{in}}{D'} + nk\left(\frac{D_1 + D}{D_1 D'}\right) V_{in} \tag{46}$$

The nominal voltage gain of proposed converter is given as:

$$G_{mDCM} = \frac{V_o}{V_{in}} = \frac{D_1 + nkD_1 + nkD}{D_1 D'} \tag{47}$$

Hence, if the coupled inductor leakage inductance is not considered, it means the coupling coefficient k is equal to 1.

$$G_{mDCM} = \frac{V_o}{V_{in}} = \frac{D_1 + n(D_1 + D)}{D_1 D'} \tag{48}$$

Also, the V_{C1} is calculated from (9), and (43):

$$V_{C1} = \frac{V_{in}}{D'} - \frac{D_1 - D}{D_1 D'} V_{in} \tag{49}$$

According to (37) the peak current of D_5 is equal as

$$I_{D5(peak)} \approx \frac{I_O}{2D_1} \tag{50}$$

On the other hand, the peak current of the I_{Lm} can given as

$$I_{Lm(peak)} = \int_0^{DT_s} \frac{1}{L_m} V_{Lm}^D dt = \frac{DV_{in}}{L_m f_s} \tag{51}$$

Also, the peak current of D_5 can be derived as

$$I_{D5(peak)} = \frac{I_{Lm(peak)}}{2n} = \frac{DV_{in}}{2nL_m f_s} \tag{52}$$

By substituting (50) in (52), D_1 is given by

$$D_1 = \frac{nL_m f_s I_O}{V_{in} D} \tag{53}$$

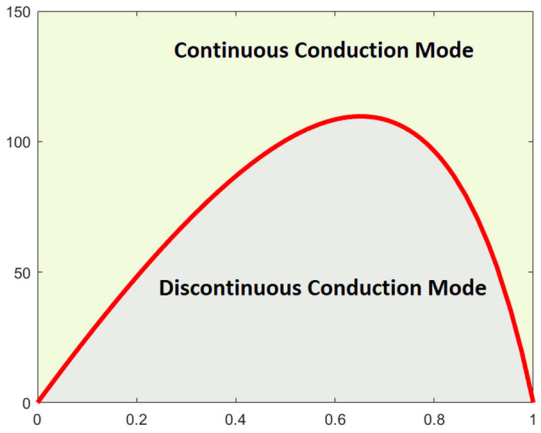


FIGURE 4. The boundary between DCM and CCM of Lm.

By substituting (53) in (48), G_{mDCM} is obtained as

$$G_{mDCM} = \frac{V_o}{V_{in}} = \frac{\frac{nL_m f_s I_O}{V_{in} D} + n\left(\frac{nL_m f_s I_O}{V_{in} D} + D\right)}{\frac{nL_m f_s I_O}{V_{in} D} D'} \tag{54}$$

Also, according to (33) the following is obtained:

$$I_{Lm} = nI_O = n\frac{V_O}{R} \tag{55}$$

Based on the inductor voltage equation, we have the following equation:

$$\Delta I_{Lm} = \frac{V_{Lm}}{L_m} DT_s = \frac{D}{L_m * f_s} V_{in} \tag{56}$$

The magnetic inductance current I_{Lm} respectively should be higher than ΔI_{Lm} since the magnetic parts were developed for CCM. According to (55) and (56) the following is obtained.

$$\Delta I_{Lm} < I_{Lm} \rightarrow \frac{D}{L_m * f_s} V_{in} < n\frac{V_O}{R} \tag{57}$$

According to above equations and (25) it can be written:

$$L_m > \frac{RDD'}{n \times (1 + n(1+D)) \times f_s} \tag{58}$$

Fig. 4. shows boundary conditions for magnetizing inductance.

IV. COMPARISON

While employing power converters, it is nearly impossible to attain the best outcomes for all construction and operational conditions. As a consequence, a trade-off should be made between the number of passive and active components, voltage gain, device stresses, and so on. The goal of this section is to provide a fair assessment of the suggested and other state-of-the-art high step-up DC-DC designs using CI. Table 1 compares the major characteristics of the recommended converter to those of existing converters provided in [14], [15], [19], [20], [21], [22], [23], and [24]. It is important to note that there are some components in the suggested topology with very low voltage and current ratings. For instance, as we

TABLE 1. Comparison of suggested topology with other topologies.

Ref.	Soft switch operation	Voltage Gain	Normalized Maximum voltage Stress on switches	Normalized Maximum voltage Stress on diode	Numbers of			
					CI + I	S	D	C
[14]	ZCS	$\frac{4}{1-D}$	$\frac{1}{4}$	$\frac{D}{1+n}$	2+0	4	4	4
[15]	Hard switching	$\frac{1+2n-nD}{1-D}$	$\frac{1}{1+2n+nD}$	$\frac{n}{1+2n+nD}$	1+0	1	4	4
[19]	ZCS	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	$\frac{n}{1+n}$	1+1	1	3	4
[20]	ZCS	$\frac{n+2}{1-D}$	$\frac{1}{2+n}$	$\frac{1+n}{2+n}$	1+1	1	3	4
[21]	ZCS	$\frac{(2n-1)+nD(n-1)}{(1-D)(n-1)}$	$\frac{(n-1)}{(2n-1)+nD(n-1)}$	$\frac{n(n-1)}{(2n-1)+nD(n-1)}$	2+0	2	2	4
[22]	Hard switching	$\frac{1+5D}{1-D}$	$\frac{2D}{2-2D}$	$\frac{2D}{1-D}$	0+6	2	13	1
[23]	ZCS	$\frac{2n-1}{(n-1)(1-D)}$	$\frac{1}{1+nD+D}$	$\frac{n+1}{1+nD+D}$	1+1	2	2	4
[24]	Hard switching	$\frac{2+n}{1-D}$	$\frac{2n}{1+2n}$	×	1+0	2	4	3
Conventional Boost converter	Hard switching	$\frac{1}{1-D}$	1	1	0+1	1	1	1
Proposed Topology	Fully soft switch	$\frac{1+n(1+D)}{D'}$	$\frac{1}{1+n(1+D)}$	$\frac{n}{1+n(1+D)}$	1+2	1	6	6

can found from Fig.6 the size of L_1 and C_1 are very low, and these components are ignorable in terms of power rating. As a consequence, it is essential to consider this point when we want to compare topologies together.

Additional voltage gain, voltage stress on switches, and output diode evaluations are shown in Fig. 5. In Fig. 5 (a), in terms of duty cycle, the proposed architecture offers the highest voltage gain between competitors especially in higher duty cycles. While the conventional boost converter has a lower number of components, but its voltage gain is also much lower than other topologies in this comparison. Fig. 5 (b) depicts the standardized voltage stress across the MOSFET (V_S/V_o) vs. the duty cycle of the MOSFET. The standardized voltage stress of the primary switch of the proposed converter is less than 0.33 for all duty cycle levels, as indicated in the figure.

Fig. 5 (c) depicts the standardized voltage stress across the output diodes (V_{Do}/V_o). This figure demonstrates that the voltage stress over the power diodes of the suggested converter is inside an acceptable range (lower than 0.7 for any duty cycles). Moreover, the normalized diode stress of suggested topology is less than conventional boost converter for any duty cycle value.

Table 2 shows a comparison in terms of cost between the suggested topology and similar converters. As the table shows, the total cost of suggested converter is not higher than similar topologies and the main reason of this is related to low size components in suggested topology.

TABLE 2. Comparison cost of suggested topology with other topologies.

Ref.	Cost of			
	CI + I	S	D	C
[14]	$11.4	$25.72	$40.96	$7.1
[15]	$9.24	$1.85	$12.1	$20.1
[19]	$4.22	$1.48	$6.39	$12
[20]	$31.93	$4.07	$4.44	$4.4
[21]	$11	$4.04	$44.56	$7.7
[22]	$114	$7.46	$22.03	$0.5
[23]	$13.5	$13.46	$2.5	$3.94
[24]	$14.4	$8.44	$4.5	$6.72
Proposed Topology	$12	$1.106	$8.76	$4.8

V. DETAILED ANALYSIS

A. EFFICIENCY ESTIMATION

In the earlier sections, the assessment of voltage and current stresses on the elements were carried out by selecting appropriate duty cycles and turn ratios to reduce these stresses. In this section, the examination of how energy is naturally dissipated in the provided topology is undertaken to validate the efficient operation of the converter. The proposed topology will operate according to the details provided in Table 2 .Please note that the prices listed in Table 2 are sourced from reputable suppliers such as Mouser Electronics, Digi-Key, and AliExpress.

The active power MOSFET experiences two types of dissipation: switching losses and conduction losses. Thanks to the soft switching operation, which smoothly increases the current from zero to its rated value when turning ON and gradually decreases the voltage from zero to its rated value when turning off, the switching losses for the MOSFET are minimal. The conduction loss can be calculated as:

The conduction loss can be determined by considering the switch on-resistance ($R_{DS(on)}$) during the conduction mode, as specified in the datasheet. Notably, in the experimental prototype, the conduction losses were found to be 1.63 W as

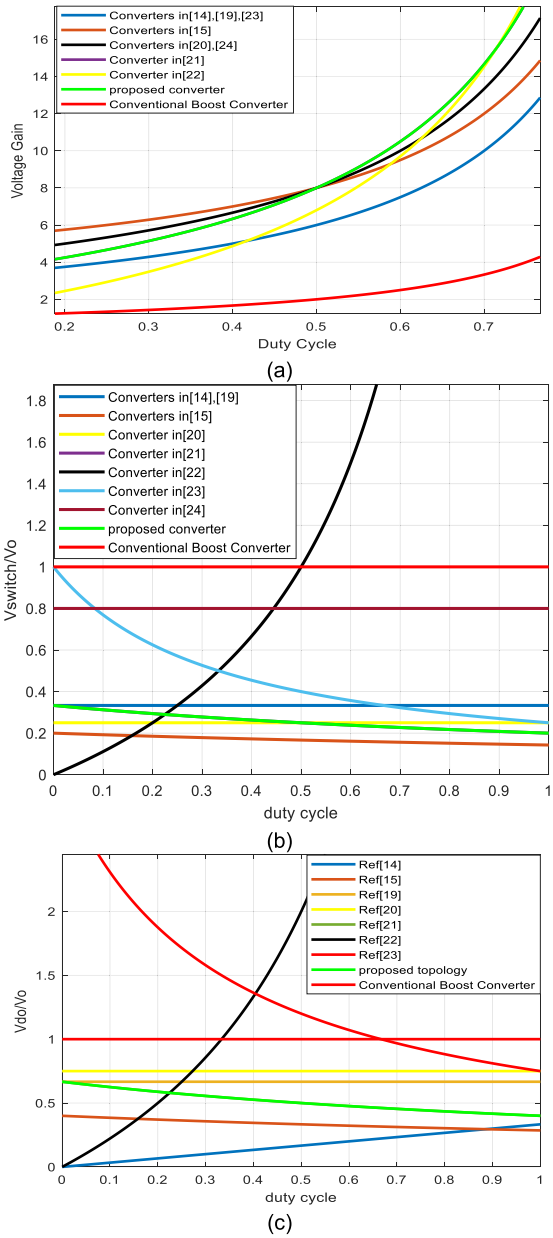


FIGURE 5. a) Comparison of voltage gain changes of various topologies vs duty ratio D. b) comparison normalized voltage stress of switch vs duty cycle in some converters. c) normalized voltage stress of output diode.

calculated using Equation (59) because $R_{ds}(on) = 6.3\ m\Omega$, $I_{switch} = 14.7$ A.

$$P_{Switch-conduction} = R_{DS(On)} * I^2_{D(RMS)} \tag{59}$$

The conduction dissipation of diodes can be summarized as follows:

$$P_{Diode} = V_{Forward} * I_{D(RMS)} \tag{60}$$

This conduction dissipation of diodes can be calculated using the diode's threshold voltage ($V_{Forward}$) as specified in the datasheet and the Root Mean Square current ($I_{D(RMS)}$). In the experimental prototype, the diode conduction losses

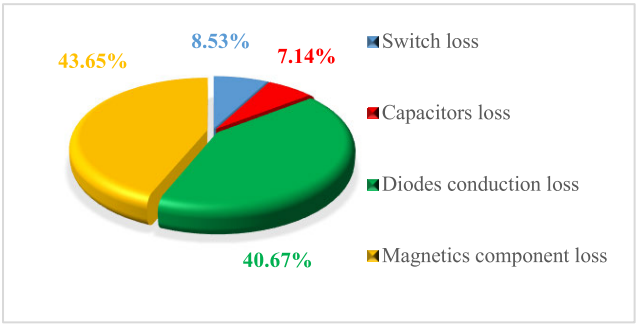


FIGURE 6. Power losses of different elements within the presented topology shown by a pie-chart.

were found to be 7.78W as calculated using Equation (60) because all diodes current are equal as output current 1.63 A and the V_F these diodes D_1, D_2, D_3 are equal 0.72 V and V_F these diodes D_4, D_5, D_6 are equal 0.87 V. To calculate the losses in the capacitors, we considered an equivalent series resistor (ESR) of 100 mΩ for the Aluminum Electrolytic Capacitors and disregarded the MKT capacitors because (ESRs are near zero in high frequancy). The total losses in the capacitors are as follows

$$P_{Capacitors} = ESR * I^2_{C(RMS)} \tag{61}$$

With $I_{C(RMS)}$ representing the RMS current of the capacitor, the practical ESR losses have been determined to be 1.36 W using Equation (61) because (24 is L_m core volume in cm^3 and power loss of this inductor in frequency of 50 kHz is 257 mW/cm^3 according to datasheet). Moreover, it is imperative to acknowledge that the cores of both transformers are subject to hysteresis and eddy current losses. When operating at a switching frequency of 50 kHz, the ETD49 (coupled inductor) experiences a dissipation of 6.16 W, while the T131-52 iron powder core (L_{in}) at the same frequency incurs a dissipation of approximately 2.18W because 6.84 × 2 is L_{in} core volume in cm^3 and power loss of this inductor in frequency of 50 kHz is 160 mW/ cm^3 according to datasheet. Hence, to determine the total magnetic loss (with wiring loss neglected due to its litz wire characteristics, and L_1 excluded due to its small size and current) is equal 8.34 W.

The overall losses are depicted in a pie chart in Fig. 6 for the implemented converter, with an input voltage (V_{in}) of 20 V and an output load of 300 W.

At the end of this part, it is important to note that there are indeed gate driver losses even when the operation of the MOSFET is fully soft-switched and our estimation in this section aimed to highlight the significant reduction in switching losses due to zero voltage switching. Moreover, it is important to note that gate driver loss of suggested converter is lower than topologies with more than one active switch.

B. COMPONENTS DESIGNS

1) INPUT FILTER DESIGN

By presupposing a 15% fluctuation in input current, we can determine the required dimensions of the input inductor using

TABLE 3. Converter parameters.

Parameters	Description/ Value
Switch: S	HY3912 MOSFET, 6.3 mΩ on-resistance
Diodes: D_1, D_2, D_3 D_4, D_5, D_6	MBR20100CT Schottky diode MBR20200CT Schottky diode
Magnetic coupled Inductor: L_m	Turns ratio: 2 (N_1:N_2=20:40) Core: ETD 49/25/16 ferrite core Magnetizing inductance: 130 μH With PSPS winding Leakage inductance :1 μH
Inductors: L_{in} L_1	220 μH, 23 turns wrapped on double T131-52 iron powder core 100 μH, 40 turns wrapped on T68-26 iron powder core
Capacitors: C_1 C_2, C_4, C_5 C_3 C_6	270 nF, 50 V (MKT) 10 μF, 100 V (MKT) 220 μF, 180 V 220 μF, 400 V
Switching Frequency	50 KHz
Output Power	300 W
Input Voltage	20 V

the following equation:

$$L_{Lin} = \frac{V_{in}D}{\Delta I_{in} f_s} \rightarrow L_{Lin} > 167\ \mu\text{H} \tag{62}$$

2) CAPACITORS DESIGN

To determine the capacitor sizes, the following equations are employed under the assumptions of 0.5% voltage ripple for C_3, 5% voltage ripple for C_4 and C_5, 0.1% voltage ripple for C_6, and an assumed average current matching the output current:

$$C_3 = \frac{P_O}{V_O \Delta V_{c3} f_s} \rightarrow C_3 > 93.75\ \mu\text{F} \tag{63}$$

$$C_{4,5} = \frac{P_O}{V_O \Delta V_{c4} f_s} \rightarrow C_4 > 9.375\ \mu\text{F} \tag{64}$$

$$C_6 = \frac{P_O}{V_O \Delta V_{CO} f_s} \rightarrow C_6 > 117.18\ \mu\text{F} \tag{65}$$

3) COUPLED INDUCTOR MAGNETIZING INDUCTANCE DESIGN

By considering a 50% current fluctuation, we can calculate the value of magnetic inductance using the following equation:

$$I_{Lm} = \frac{V_{in}D}{\Delta I_{Lm} f_s} \rightarrow L_{Lm} > 213.33\ \mu\text{H} \tag{66}$$

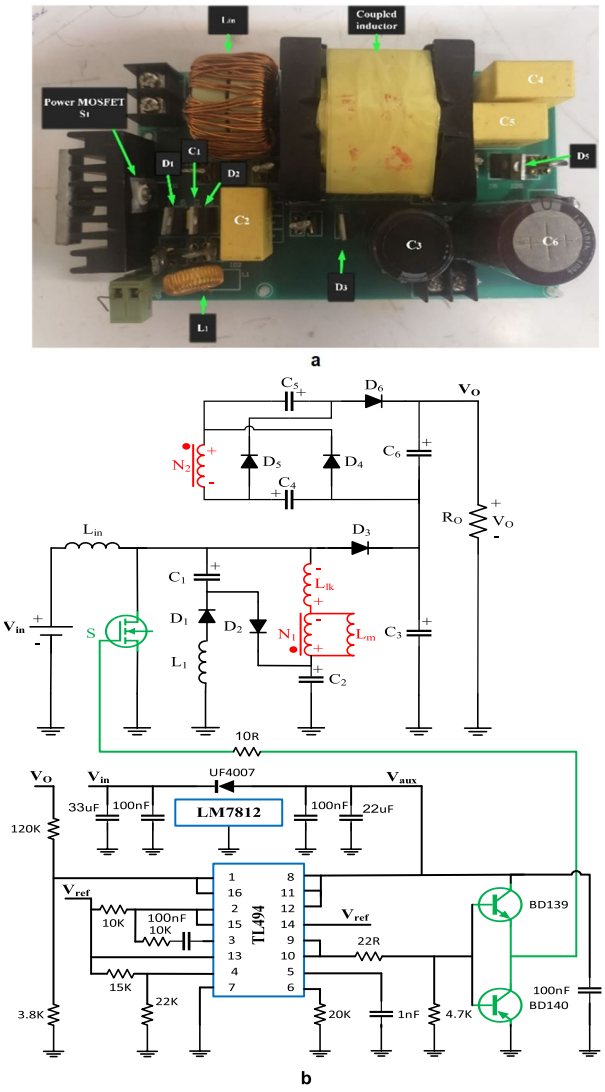


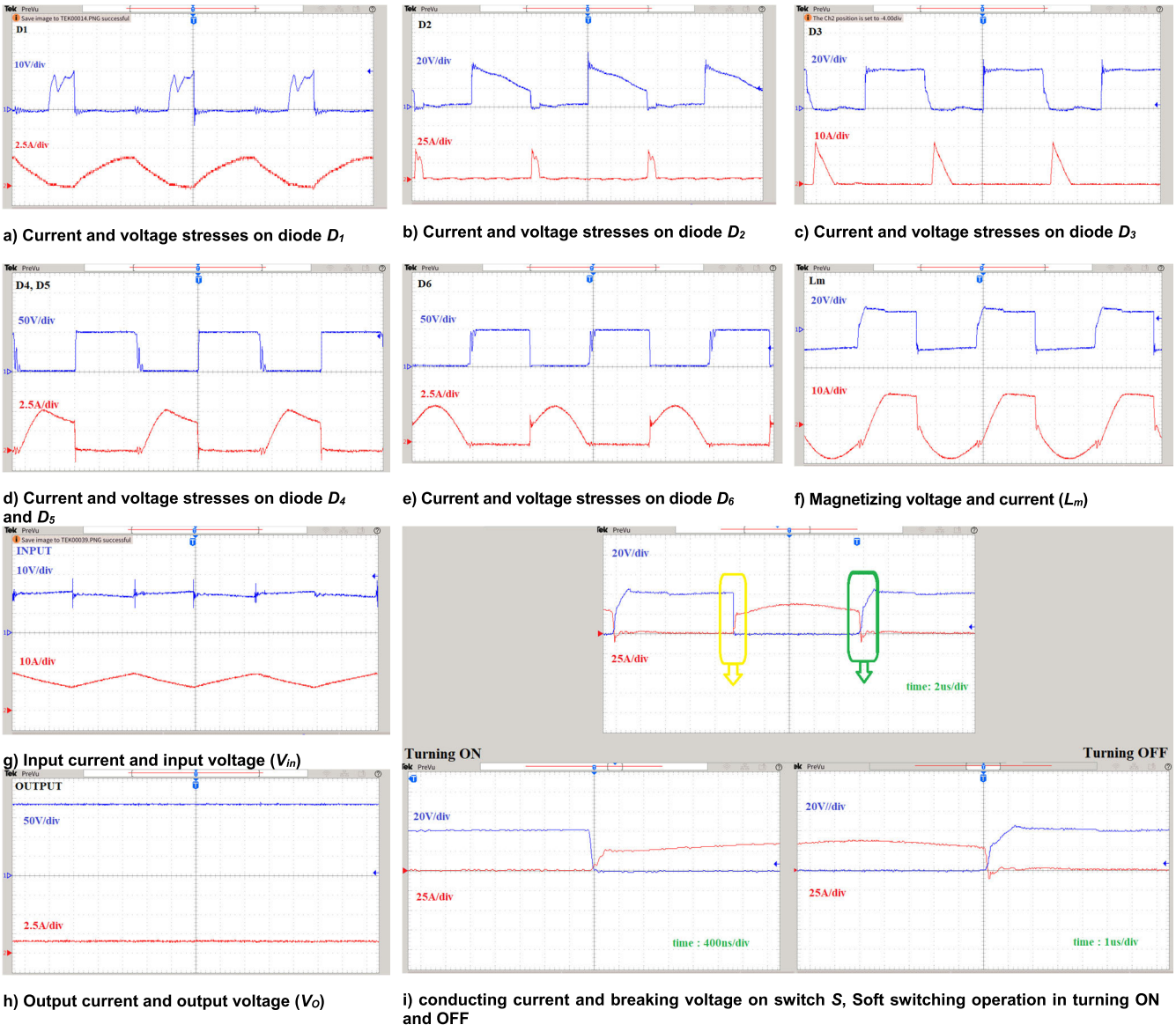
FIGURE 7. a) Experimental prototype of suggested topology. b) The control circuit of the suggested topology.

4) DESIGN OF RESONANCE COMPONENTS

Considering C_1, the resonance capacitor, it plays a key role in a method called zero voltage switching. When you increase the capacitance of C_1, the switch turns off more slowly, which is good because it reduces losses when turning off. However, when you add more capacitance, it also makes the switch carry more resonance current, which can lead to significant losses for the switch. To deal with this, you can increase the inductance L_1, which helps decrease the resonance current. But keep in mind, there is a specific equation you need to think about when doing this [1]:

$$2\pi\sqrt{L_1 C_1} < T_s \tag{67}$$

To calculate the values of C_2 (the second resonance capacitor) and the leakage inductance of the coupled inductor (L_{lk}), according to [1], these components are configured to



a) Current and voltage stresses on diode D_1

b) Current and voltage stresses on diode D_2

c) Current and voltage stresses on diode D_3

d) Current and voltage stresses on diode D_4 and D_5

e) Current and voltage stresses on diode D_6

f) Magnetizing voltage and current (L_m)

g) Input current and input voltage (V_{in})

h) Output current and output voltage (V_o)

i) conducting current and breaking voltage on switch S, Soft switching operation in turning ON and OFF

FIGURE 8. Experimental result, time division: 4μs/div.

operate in Boundary-resonance mode, a strategy aimed at reducing switching losses in the output diode and improving its ability to handle reverse recovery issues. Furthermore, the magnitude of L_{lk} is contingent on how the winding of the coupled inductor is arranged, as described by the following equation:

$$\pi\sqrt{L_{lk}C_2} = DT_s \rightarrow C_2 = \frac{D^2}{\pi^2 L_{lk} f_s^2} \tag{68}$$

VI. EXPERIMENTAL RESULTS

A. STEADY-STATE PERFORMANCE

In order to validate the operation of suggested topology, the results of experimental prototype system are considered in this section with system parameters indicated in Table 3. A 150 W laboratory prototype has been built for confirming the operation of the proposed converter depicted in Fig. 7 (a). As the figure shows, C_1, L_1 have a very low size compared to coupled-inductor and other capacitors that are in the power path. As a consequence, these parts have a very low cost. Fig. 7 (b) shows the control circuit of the suggested topology. TL494 (IC) is a constant-frequency PWM controller with a pair error amplifier, a waveform with a sawtooth shape generator, and a 5 V reference (V_{REF}). The IC has two distinct modes of functioning, allowing pulses to be captured from pins 9 and 10. The pulse frequency is created by a capacitor C_T(1 nF) and resistor R_T (20 kΩ), which may be attached outside at pins 5 and 6. These integrated circuits may operate in either single-ended or push-pull modes. The single-ended mode generates pulses with an identical phase

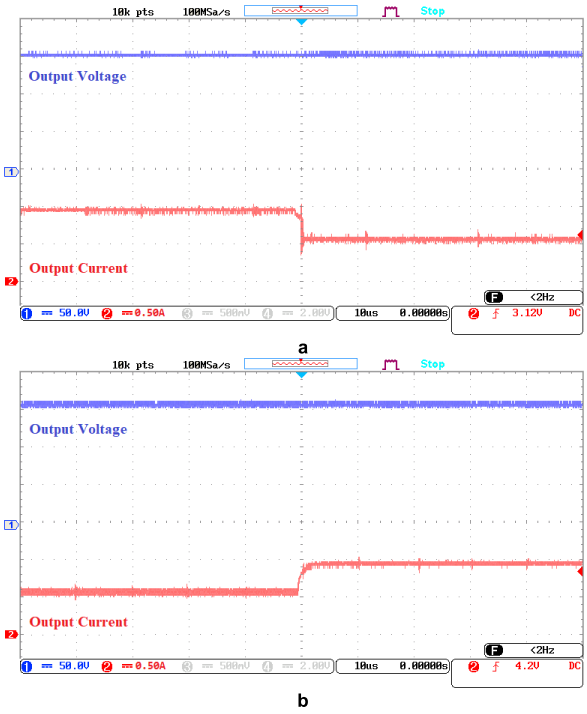


FIGURE 9. Transient response of suggested topology.

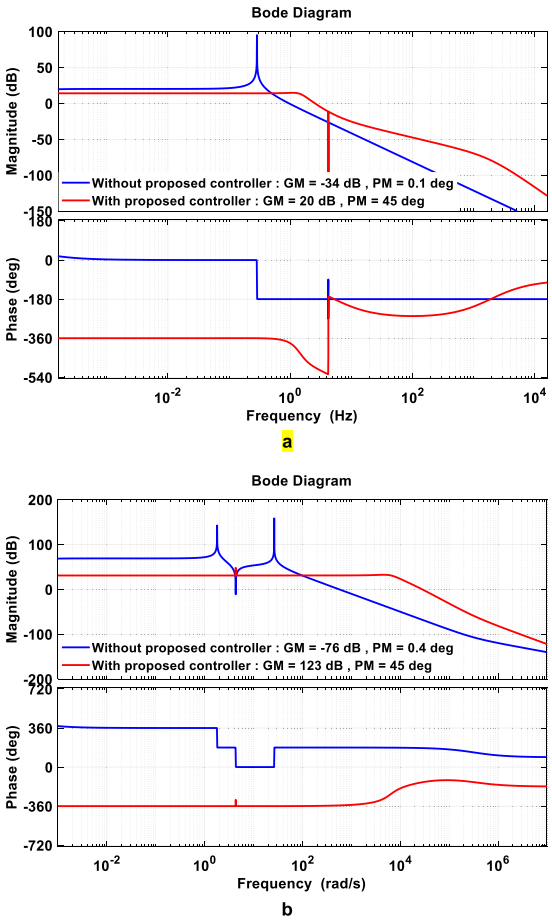


FIGURE 10. Frequency response (a) from input voltage to output voltage (b) from duty cycle to output voltage.

variation (zero degree). The push-pull mode generates pulses with a 180 degrees phase shift.

Fig. 8 (a) and (b) show D_1 and D_2 voltage and current respectively. These diodes are used to create the ZVS state of the switch at turning off. Moreover, the diode D_1 has a soft switching operation in turning on and off.

Fig. 8 (c) and (e) indicate D_3 and D_6 voltage and current. The current of D_6 turns on and off in ZCS condition. This is happened because of the resonance of the leakage inductance and C_2 which is occurred in the mode two.

Fig. 8 (d) shows $D_{4,5}$ voltage and current. As we can found from these figures, the current of $D_{4,5}$ turns on in ZCS condition and its turning on loss is very low.

Fig. 8 (f) shows the voltage and current of magnetizing of CI. As we can see from this figure, the operation of suggested converter is based on theoretical analysis in section II. Furthermore, Fig. 8 (g) shows the input current of suggested topology as we can see the input current is continues with minimized ripple and this is a good point for solar application. Also, the output current and voltage is shown in Fig. 8 (h).

The soft switching of the single switch of the converter is depicted in the Fig. 8 (i). Switch turns on in ZCS due to leakage and input inductance and it turns off in ZVS because of existing of capacitor C_1 and diode D_1. Also, because of this auxiliary circuit (C_1, L_1, D_1, D_2), the voltage increase caused by leakage inductance (Llk) did not happen on the switch. In addition, in Fig. 8 (i) the zero voltage switching is shown with zoomed-in figure, where the voltage off switch is increased slowly despite the 2.2 μH leakage inductance. It is important to note that, the soft switching operation in MOSFET of suggested topology is dependent on the input voltage. Choosing the components C_1, L_1 based on the input voltage can reduce switching losses in turning off effectively.

B. TRANSIENT RESPONSE

Figure 9 (a) illustrates the changing behavior of the output voltage with a step load adjustment from 300W to 150W. Under closed loop regulation, the output voltage remains insensitive to load change. Moreover, figure 9(b) depicts the suggested converter's dynamic reaction to a rapid load adjustment from 150W to 300W. As we can see, increasing the load from 150 to 300W causes no discernible output voltage decreases; hence, by selecting a suitable closed-loop controller, the converter's output voltage could be resilient and unaffected by load diversifications.

C. VOLTAGE MODE CONTROL OF THE PROPOSED CONVERTER

To effectively manage the output voltage across the load and input voltage fluctuations, it is essential to design an

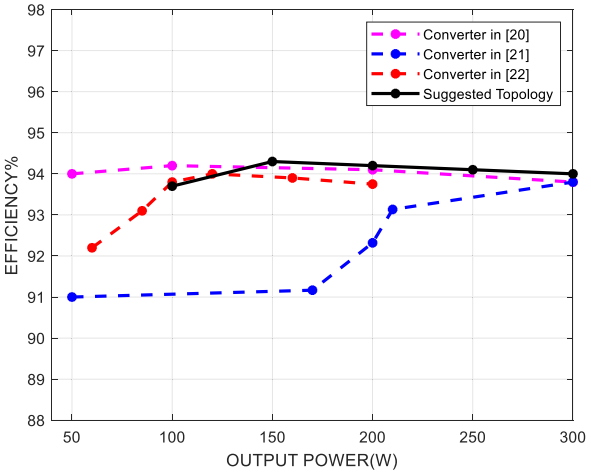


FIGURE 11. Experimental efficiency comparison.

appropriate controller. This study employs the state-space average model and small-signal model to handle the open-loop transfer function of the topology by adjusting the duty ratio. The state-space variables considered are:

$$X = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \\ x_9 \\ x_{10} \end{bmatrix} \Rightarrow \begin{bmatrix} I_{Lin} \\ I_{L1} \\ I_{LN1} \\ I_{LN2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \\ V_{C6} \end{bmatrix} \tag{69}$$

A Type-III controller is utilized to fine-tune the phase and gain margins of the transfer function. The transfer function of the proposed topology from the input voltage to the output voltage is given in equation (70), as shown at the bottom of the page, and from the duty ratio to the output voltage in equation (71), as shown at the bottom of the page. Figure 10 illustrates the stability margins achieved with the proposed controller. It compares the transfer functions from equations (70) and (71) to those of a system without a controller (only feedback). Before applying the controller, the phase and gain margins for equation (70) were 0.7 degrees and 6.6 decibels. After applying the controller, they improved to 53.3 degrees and 20 decibels, respectively. Figure 10 (b) shows the transfer function of the suggested topology before and after the controller application for equation (71). Initially, the phase and gain margins were −37.1 degrees and −70.1 decibels; post-application, they were 48.3 degrees and infinity decibels, respectively.

Fig. 10. shows the Bode diagram of suggested topology in open and closed loop condition. As the figure shows figure, the Bode plot of the closed loop system shows that the phase angle remains below −180 degrees at higher frequencies and in open loop bode diagram of topology, the phase angle does not reach −180 degrees, indicating that we can stabilize this topology in the closed loop state.

Figure 11 compares the efficiency of the proposed converter to other comparable topologies while maintaining output voltage control. The simulated findings in this figure use the identical specs, switching components, and circumstances ($f_S = 50$ kHz, $V_{in} = 20$ V, $n = 2$). The suggested converter is more efficient than others due to its high voltage gain during optimal duty cycles, resulting in minimal power losses (see figure).

VII. CONCLUSION

This paper has presented an innovative design for a fully soft-switched single-switch high gain CI boost converter. The proposed topology has several notable advantages, including the implementation of a low pass filter on the input side of the converter to ensure a continuous input current. Furthermore, the design eliminates switching losses on the switch, significantly improving the overall converter efficiency. By leveraging the resonant circuit and the leakage inductance, the energy stored in the inductors can be effectively recycled, reducing energy wastage.

The suggested topology has practical applications possibilities in various fields. For instance, in Electric Vehicle Systems, it can bridge the voltage gap between a 20V battery module and a 160V drive motor, optimizing power transfer. In R&D settings, its wide voltage conversion range facilitates testing and development of components across diverse voltage spectrums, crucial for integrating new technologies with existing systems. Additionally, in Solar Power Storage, it can efficiently step up 20V generated by solar panels to 160V for charging higher voltage battery banks or grid-tied inverters. This adaptability makes the topology valuable in diverse applications.

The utilization of a low-voltage-rating MOSFET with fixed reverse recovery diodes in the proposed configuration results in reduced conduction losses and enhanced efficiency.

$$G_{vg} = \frac{1.222e07s^7 + 3.048e-05s^6 + 2.264e14s^5 - 48.32s^4 - 1.551e21s^3 - 3.795e08s^2 + 2.099e27s - 1.574e13}{s^9 + 32.2\,s^8 + 1.987e07s^7 + 7.265e08s^6 - 1.101e14s^5 - 4.479e15s^4 - 1.645e20s^3 + 1.896e21s^2 + 9.234e26s + 1.205e28} \tag{70}$$

$$G_{vd} = \frac{-8.326e04s^8 + 1.521e10s^7 - 1.582e12s^6 - 6.361e16s^5 + 1.016e19s^4 - 1.72e23s^3 - 1.253e25s^2 + 7.324e29s + 6.177e29}{s^9 + 32.2\,s^8 + 1.987e07s^7 + 7.265e08s^6 - 1.101e14s^5 - 4.479e15s^4 - 1.645e20s^3 + 1.896e21s^2 + 9.234e26s + 1.205e28} \tag{71}$$

The elimination of voltage spikes on the MOSFET, which are typically caused by leakage inductance in traditional CI-based converters, is a distinct advantage of the proposed topology. Lastly, the lower breakdown voltage requirement for the output diode allows for the cost-effective use of diodes. In summary, this innovative design offers multiple benefits, enhancing the performance and cost-efficiency of the converter.

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