IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

IEEE Vehicular Technology Society Section

Received 7 July 2024, accepted 19 July 2024, date of publication 29 July 2024, date of current version 6 August 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3434602

RESEARCH ARTICLE

Design Approach of Planar Transformer-Based 2-TR Phase-Shift Full-Bridge Converter for High Efficiency and High Power Density in LDC

SANG-GYUN RYU[1], SEONG-YONG HONG[1], CHAN-BAE PARK[2], HYUNG-WOO LEE[3], AND JAE-BUM LEE[4]

[1]Department of AI Transportation Convergence, Korea National University of Transportation, Uiwang-si, Gyeonggi-do 16106, South Korea
[2]Department of Railroad Operation Systems Engineering, Korea National University of Transportation, Uiwang-si, Gyeonggi-do 16106, South Korea
[3]Department of Railway Vehicle System Engineering, Korea National University of Transportation, Uiwang-si, Gyeonggi-do 16106, South Korea
[4]Department of Railroad Electrical and Electronic Engineering, Korea National University of Transportation, Uiwang-si, Gyeonggi-do 16106, South Korea

Corresponding author: Jae-Bum Lee (leejb@ut.ac.kr)

This work was supported by the Technology Innovation Program, Development of Power Module and Integrated Circuit Technology for High Power Density of Electric Components for Hydrogen Electric Commercial Vehicles through the Ministry of Trade, Industry, and Energy (MOTIE), South Korea, under Grant 20018971 and Grant 1415185855.

ABSTRACT The recent focus on greenhouse gas emissions from fossil fuel usage has led to strengthened regulations on carbon emissions. Consequently, research on electric vehicles (EV), which have higher energy efficiency compared to internal combustion engine vehicles, is actively being pursued. With advancements in the technology of electronic components in electric vehicles, there is a growing trend in the demand for higher-rated capacities of Low DC-DC Converter (LDC) that possess a wide input-output voltage range. Furthermore, the restricted space within vehicles and the emphasis on high energy utilization necessitate converters with high power density and efficiency. Currently, in electric vehicles, the Active Clamp Forward Converter (ACFC) and the Phase Shift Full-Bridge Converter (PSFB) are commonly applied, as they readily achieve a wide input-output voltage range and high power density. However, ACFC and PSFB encounter difficulties in achieving high efficiency and power density due to the requirement for output inductors with high current specifications. To address these challenges, this study proposes a Two-Transformer Phase Shift Full-Bridge Converter (2-TR PSFB) based on planar transformers, which can replace conventional ACFC and PSFB. The proposed converter achieves high efficiency and power density without the need for high-current output inductors. Additionally, the utilization of GaN power semiconductors allows for a high switching frequency, enabling a significant reduction in the volume of magnetic components. This research presents the operational principles of the 2-TR PSFB and provides design directions. To validate the design, a 2.5 kW prototype was manufactured and tested.

INDEX TERMS DC/DC converter, LDC, GaN, high power density, high efficiency, PSFB, EV.

I. INTRODUCTION

Since the onset of the Industrial Revolution, there has been a pronounced increase in greenhouse gas emissions due to the combustion of fossil fuels, resulting in a notable elevation in the global average temperature. This phenomenon, driven by the emission of greenhouse gases, has given rise to adverse consequences such as erratic climate patterns, rising sea levels, and challenges in food production [1]. In response to these challenges, global efforts have been underway to address environmental conservation, notably exemplified by the Paris Agreement [2], [3]. This international accord aims

The associate editor coordinating the review of this manuscript and approving it for publication was Wei Quan.

to limit greenhouse gas emissions universally, seeking to curb the escalation of global temperatures. Consequently, there has been a growing emphasis on technologies that contribute to lower greenhouse gas emissions, particularly in the automotive sector. Electric vehicle (EV) technology has emerged as a prominent solution, attracting significant attention for its potential to reduce emissions compared to traditional internal combustion engine vehicles [3], [4], [5], [6]. The power conversion configuration for electric vehicles is depicted in Fig. 1.

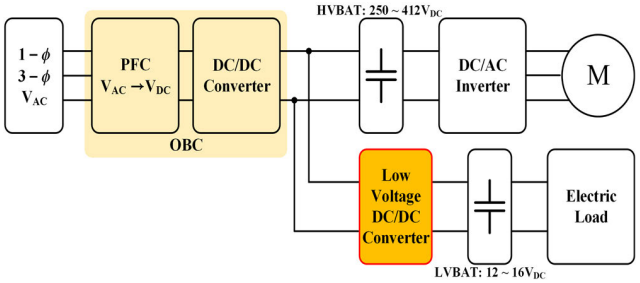

FIGURE 1. Power conversion configuration of electric vehicle (EV).

Electric vehicle batteries not only play a role in driving the motor for propulsion but also supply power to various electronic components within the vehicle. However, to adapt the high voltage of electric car batteries (250V-412V) to the low voltage specifications (8V-16V) required by various vehicle electronic systems, a Low Voltage DC-DC Converter (LDC) is essential. While conventional electric vehicle LDC have typically been designed with a rated capacity of around 1 kW, recent advancements, such as the electrification of traditional mechanical components like hydraulic systems, have led to an increased demand for higher-rated capacities, driven by developments in autonomous driving technologies.

For the performance enhancement of electric vehicles, the battery must exhibit characteristics such as high power-to-weight ratio, high energy density, and low mass. One of the suitable batteries with these features is the lithium-ion battery, widely employed in electric vehicles for its ability to deliver high performance [7], [8], [9], [10]. Lithium-ion batteries, owing to their wide voltage range, necessitate LDC to handle power conversion between high-voltage and low-voltage batteries. Consequently, research is underway to meet the conditions of LDC with a broad input-output voltage range, enhanced rated capacity, efficiency, and power density.

To achieve high power density in the LDC, reducing the volume of the magnetic core is an effective method. To achieve this reduction in the size of the magnetic core, a high operating frequency is required. However, using a high switching frequency leads to increased switching losses, making the use of topologies that enable soft switching essential to enhance efficiency. Additionally, the use of power semiconductors with low losses is crucial for achieving high efficiency. Currently, power semiconductors such as Si, SiC, and GaN are predominantly used in power conversion devices, with Si and SiC being more commonly employed. Si and SiC have limitations such as a low energy gap and low electron mobility compared to GaN [11], [12], [13], [14]. Consequently, GaN power semiconductors, with their small $R_{DS(ON)}$ and parasitic capacitance, resulting in lower losses even at high switching frequencies, have garnered interest [11], [12].

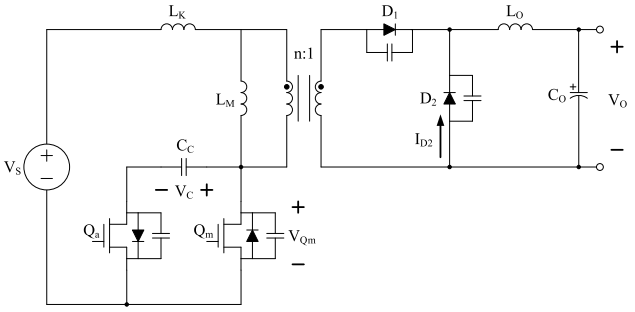

FIGURE 2. Active clamp forward converter.

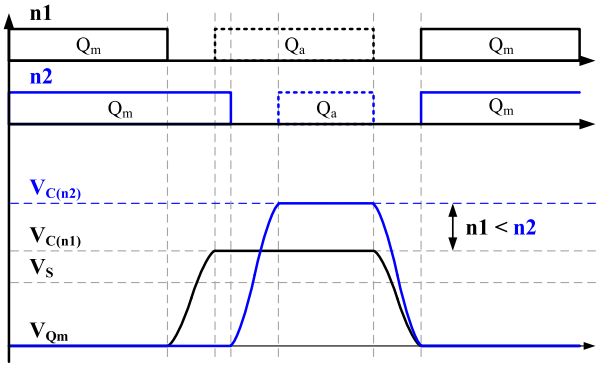

FIGURE 3. Key waveforms of active clamp forward converter.

The conventional LDC has been studied, and the Active Clamp Forward Converter (ACFC) has been investigated for satisfying a wide input-output voltage range and achieving high power density with the capability of soft switching [15], [16], [17]. ACFC is shown in Fig. 2. The ACFC, employing a topology with an output inductor, is a suitable configuration for reducing the output current ripple of the LDC, especially for its high current output specification. With two switches on the primary side, it minimizes the usage of power semiconductors, making it suitable for achieving high power density. The primary side switches of the ACFC can operate with Zero-Voltage-Switching (ZVS), enabling high-frequency operation and meeting the requirements for high efficiency. Additionally, through duty cycle control, it possesses a wide voltage transfer ratio, making it suitable for significant input and output voltage variations. However, increasing the turns ratio of the transformer to reduce primary side current and switch component losses can lead to an increase in voltage stress on the primary side switch due to the need for a higher duty cycle. As the turns ratio increases, the clamping voltage also rises, causing an issue where the

voltage stress on the primary side main switch increases as the sum of the input voltage and clamping voltage. Furthermore, while increasing the turns ratio can reduce the primary side current and losses in switch components, achieving higher efficiency, it requires a higher duty cycle. As the duty cycle increases, the clamping voltage also rises, resulting in increased voltage stress on the primary side main switch as shown in Fig. 3. Additionally, the ACFC has a disadvantage in that, while it allows a single switching cycle for one power transfer, it generates ripple at the switching frequency when observing the current of the output inductor. This leads to an increase in the inductance of the output inductor, which is unfavorable for minimizing volume. Therefore, the ACFC requires the use of high-voltage-rated switches and has the drawback of increased volume in the output inductor. GaN power semiconductor devices are primarily developed for electric vehicle specifications of 600-650V. However, integrating GaN components into LDC with an input voltage of 400V becomes challenging due to the additional voltage stress on the primary side main switch caused by clamping voltage on the input voltage.

To address the drawbacks of ACFC, an alternative known as the Phase Shift Full-Bridge Converter (PSFB) exists. PSFB, like ACFC, is a topology with an output inductor suitable for minimizing the output current ripple, meeting the specifications for the LDC with a large output current. It allows for two power transfers with a single switching, creating a ripple frequency at twice the operating frequency when observing the current of the output inductor. This advantageous feature contributes to reducing the volume of the output inductor. The primary-side switch of the PSFB can achieve ZVS, ensuring high efficiency. With control over the duty cycle, it maintains a wide voltage transfer ratio, making it suitable for significant variations in input and output voltages. Additionally, the primary-side switch of the PSFB experiences lower voltage stress compared to ACFC, making it compatible with GaN power semiconductor components. However, due to the high operating frequency, the output inductor necessitates the use of a ferrite core. This introduces a disadvantage as ferrite cores tend to have larger cross-sectional areas due to their characteristic of low saturation flux density, resulting in increased volume. Furthermore, the ripple frequency of the output current is twice the operating frequency, posing challenges in core losses. Consequently, the PSFB faces limitations in achieving both high efficiency and high power density for the LDC. Another drawback is the poor compactness in the output-side inductor's design.

To address the limitations of conventional converters (ACFC, PSFB), a Two-Transformer Phase Shift Full-Bridge Converter (2-TR PSFB) based on a planar transformer is proposed, as illustrated in Fig. 4. The proposed converter, similar to PSFB, exhibits a wide voltage transfer ratio and allows for ZVS. To facilitate the use of GaN power semiconductors, a clamping diode is applied to the primary-side rectifier stage, reducing the voltage ringing and lowering the voltage stress on the primary-side switch. In contrast

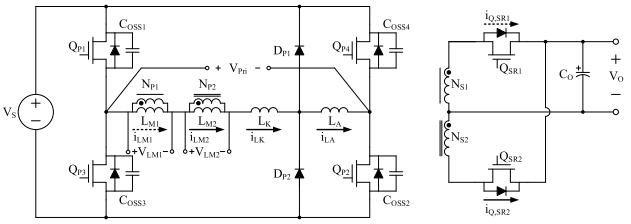

FIGURE 4. Two-transformer phase shift full-bridge converter.

to PSFB, Fig. 4 shows that the 2-TR PSFB does not have an output inductor on the output side. The primary-side transformer is configured in a 2-series structure. The 2-series primary-side transformer operates as a transformer or an output inductor depending on the circuit operation. Therefore, it offers the advantage of reducing output current ripple without using an output inductor, providing similar benefits as when using an output inductor. The absence of an output inductor simplifies the structure of the secondary-side circuit for high current specifications, and the role of the output inductor in high current specifications can be replaced by the primary-side inductor, resulting in volume reduction and high efficiency. Additionally, by applying a planar transformer to the primary-side transformer, the overall height of the converter can be lowered, making it suitable for achieving high power density.

In this paper, a flat transformer-based 2-TR PSFB is proposed to meet the increasing requirements of capacity, efficiency, and power density for the LDC. The operation of the 2-TR PSFB is analyzed, and the design method is introduced. Finally, a converter satisfying the specifications of 2.5 kW capacity, 250V-412V input voltage, and 12V-16V output voltage is designed. The performance of the designed converter is verified through the production of a prototype and testing.

II. TWO-TR PSFB CONVERTER

A. OPERATING PRINCIPLE

For the convenience of circuit operation analysis, the self-magnetizing inductance of the series transformer is assumed to be identical, and the analysis is conducted under the assumption of no leakage inductance and no on-state losses in the components. One cycle is divided into 14 modes, and since the half-cycle is symmetrical, the analysis is conducted for only 7 modes for each half-cycle.

Mode1(t_0-t_1, Powering$_1$) involves the conduction of Q_{P1} and Q_{P2}, resulting in the application of the input voltage V_S to the terminals V_{AB} of the primary rectifier. With the formation of current conduction paths through Q_{P1}, Q_{P2}, and Q_{S1}, the difference in current flowing through the leakage inductor of the transformer, as shown in Fig. 7, contributes to the current flowing to the output. Since the current difference flows to the output, I_{LM1} and I_{LM2} have offsets of $\pm I_O/2n$. Before t_0, the current I_{LA} of the external inductor has slightly increased compared to the primary side current I_{PRI} of the transformer,

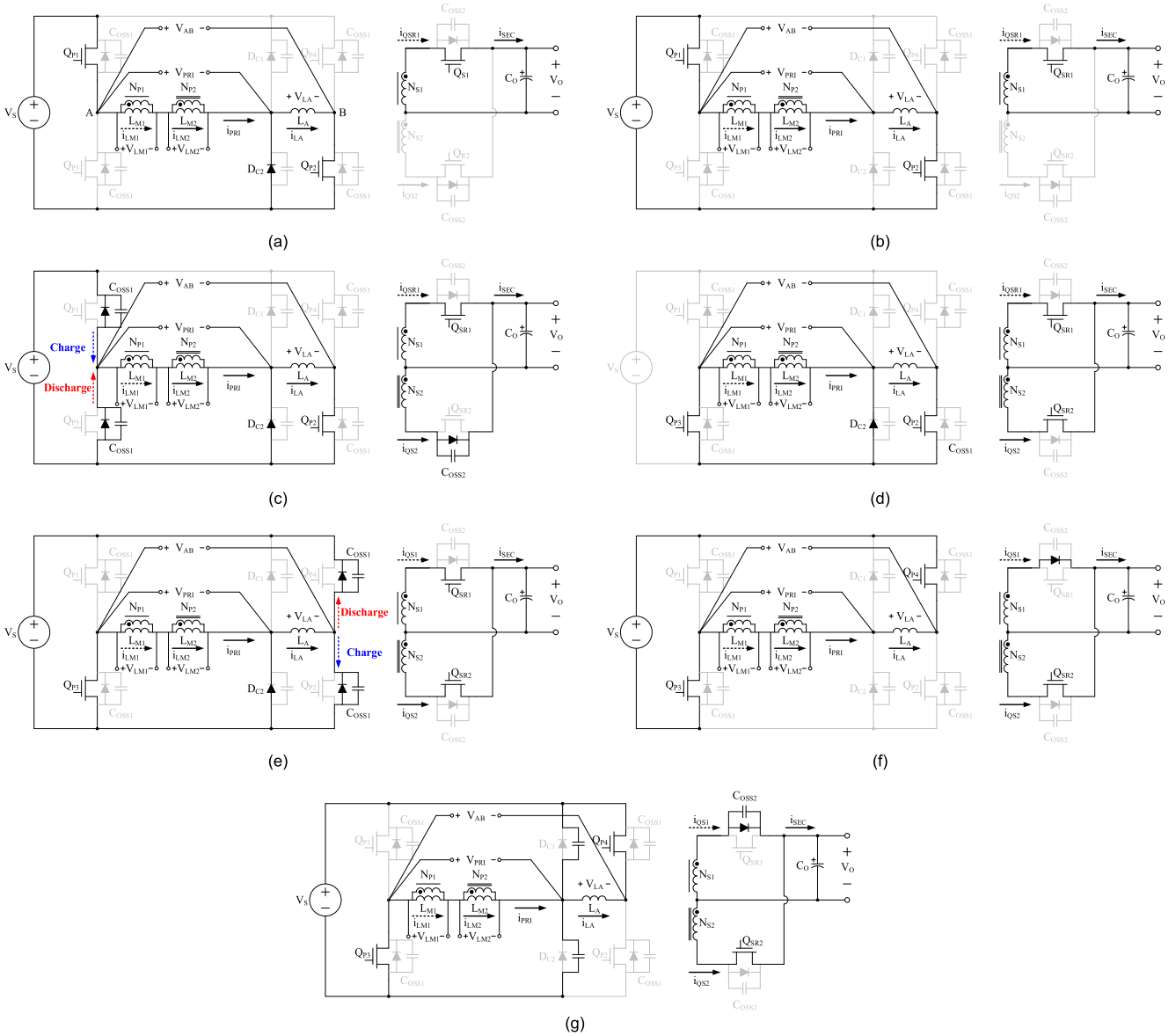

FIGURE 5. Current flow path in the operating mode of the proposed converter (a) Mode1 (t_0-t_1); (b) Mode2 (t_1-t_2); (c) Mode3 (t_2-t_3); (d) Mode4 (t_3-t_4); (e) Mode5 (t_4-t_5); (f) Mode6 (t_5-t_6); (g) Mode7 (t_6-t_7).

and the difference in currents flows through D_{C2}. As Q_{P2} and D_{C2} are conducting, the voltage across the terminals of the external inductor V_{LA} is applied as 0V, resulting in a flat flow of I_{LA}. The transformer (T_1) with the magnetizing inductor L_{M1} operates as a transformer because Q_{S1} is conducting, and the voltage across the terminals V_{LM1} of L_{M1} is applied with nV_O. The transformer (T_2) with the magnetizing inductor L_{M2} operates as an inductor because Q_{S2} is open, and the voltage across the terminals V_{LM2} of L_{M2} is applied with $V_S - nV_O$, which is the difference between the terminals of the rectifier and V_{LM1}. The current I_{SEC} projected to the secondary side is the projection of the difference between I_{LM2} and I_{LM1} and is expressed as equation (1).

$$I_{SEC} = n(I_{LM2} - I_{LM1}) \tag{1}$$

Mode2(t_1-t_2, Powering$_2$) involves the moment when the primary side current I_{PRI} of the transformer and the external inductor current I_{LA} become equal at t_1, resulting in zero current flowing through D_{C2}. Similar to Mode1, the current paths are formed through Q_{P1}, Q_{P2}, and Q_{S1}, and V_{LM1}, V_{LM2}, I_{SEC} remain the same as in Mode1.

Mode3(t_2-t_3, Leading-leg ZVS) involves the turn-off of Q_{P1} at t_2. Subsequently, energy stored in L_{M2} and L_A is utilized for charging Q_{P1}, discharging Q_{P3}, and discharging Q_{S2}. Therefore, the voltage across the terminals of Q_{P1} is charged from 0V to V_S, while the voltage across the terminals of Q_{P3} is discharged from V_S to 0V. At the same time, the voltage across the terminals of Q_{S2} is discharged from V_O to 0V. The energy required for the charging and discharging processes is $[(2C_{OSS1} + C_{OSS2}/n^2) \cdot V_S^2/2]$, and the energy

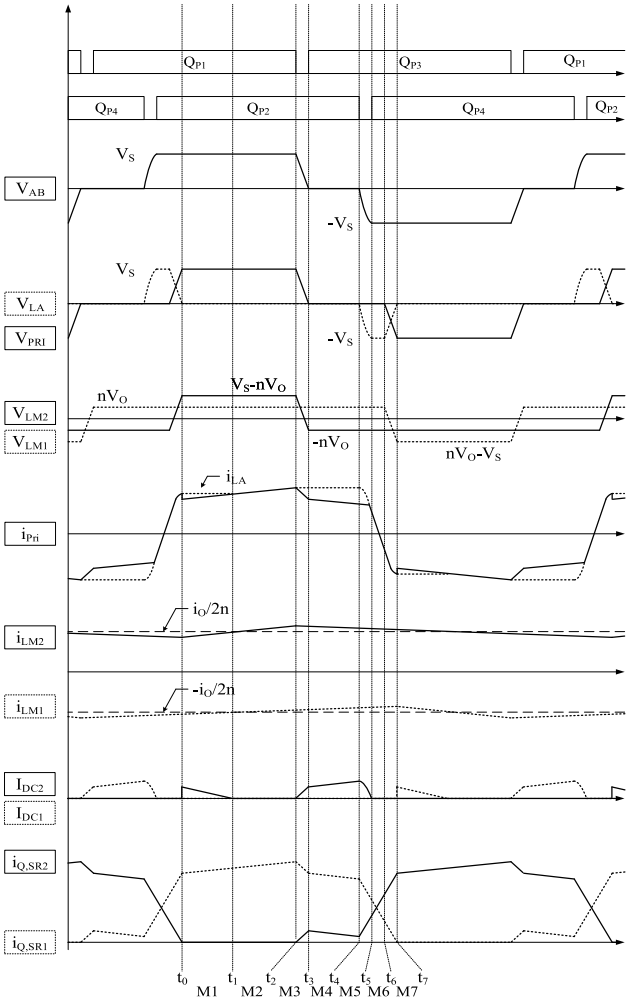

FIGURE 6. Key waveforms of the proposed converter.

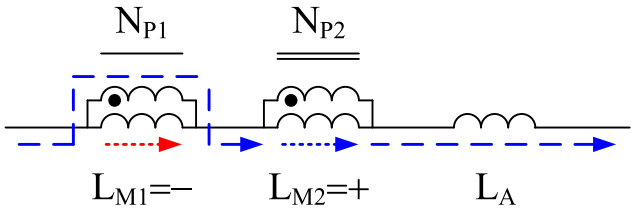

FIGURE 7. Current flow path in Mode1(t_0-t_1).

used for these processes is $[(L_{M2} + L_A) \cdot I_{PRI}^2/2)]$. Since the self-inductance L_{M2} has a large stored energy, achieving ZVS is easily accomplished. Due to the charging and discharging operation of the output capacitors of the 1st and 2nd stage switches, there is a small current ripple in I_{PRI}. On the other hand, I_{LA} remains flat without changes as D_{C1} is conducting, and V_{LA} is supplied with 0V, resulting in a difference between I_{LA} and I_{PRI}, causing a current ripple that flows through D_{C2}.

Mode4(t_3-t_4, Free-Wheeling) involves turning on Q_{P3} at t_3. Since the voltage across the terminals of Q_{P3} was discharged to 0V during Mode3, it performs ZVS turn-on operation. At this point, the rectifier section is disconnected from the input side, and 0V is applied to V_{AB}, initiating the freewheeling mode. All the 2nd stage switches are in the turned-on state during this mode, causing both T_1 and T_2 to operate as transformers. V_{LM1} becomes nV_O, I_{LM1} increases, V_{LM2} becomes $-nV_O$, and I_{LM2} decreases. With 0V across the terminals of the external inductor (L_A), I_{LA} flows flatly, and as I_{PRI} decreases with the slope of nV_O/L_{M2}, the difference between the two currents continues to increase, and D_{C2} is conducting continuously without any commutation occurring.

Mode5(t_4-t_5, Lagging-leg ZVS) occurs when Q_{P2} turns off at t_4. The secondary-side switches are all conducting, similar to Mode4, where V_{LM1} is nV_O, V_{LM2} is $-nV_O$, and V_{PRI} is 0V. Therefore, resonance occurs between the output capacitors of L_A, Q_{P2}, and Q_{P4}, with V_{QP2} charging from 0V to V_S and V_{QP4} discharging from V_S to 0V. As the output capacitors of V_{QP2} and V_{QP4} discharge due to L_A energy, I_{LA} begins to decrease. The required energy for this discharging process is $[2_{COSS1} \cdot V_{S2}/2]$, and the energy used for discharging is $[L_A \cdot I_{PRI2}/2]$. In this case, the energy stored in the external inductor L_A is small, satisfying the relationship in equation (2) is necessary for achieving ZVS. The stored energy depends on the sizes of L_A and I_{LA}, and under light-load conditions, as I_{LA} decreases, the required value of L_A increases. To achieve lagging-leg ZVS under full-load conditions, a large L_A is required. It is crucial to understand the main operating range and select the ZVS achievement condition range. The dead time for achieving ZVS is selected as 1/4 of the resonant period between L_A and $2C_{OSS1}$, as shown in equation (3).

$$\frac{L_A \times I_{LA}^2}{2} \geq \frac{2C_{OSS1} \times V_S^2}{2} \tag{2}$$

$$Dead\ Time = \frac{2\pi\sqrt{2L_A C_{OSS1}}}{4} \tag{3}$$

Mode6 (t_5-t_6, Commutation), Q_{P4} turns on at t_5. Since the Q_{P4} voltage across its terminals has discharged to 0V during Mode5, it performs ZVS turn-on operation. At this point, both Q_{P3} and Q_{P4} are conducting, applying $-V_S$ to the terminals of the 1st-stage rectifier V_{AB}. The 2nd-stage switches Q_{S1} and Q_{S2} are both in the conducting state, and V_{LM1} is nV_O, V_{LM2} is $-nV_O$, while V_{PRI} remains at 0V. Since $-V_S$ is applied to V_{LA}, I_{LA} linearly decreases with a slope of $-V_S/L_A$. As I_{LA} decreases and becomes equal to I_{PRI}, the current flowing through D_{C2} becomes 0A, and both I_{PRI} and I_{LA} decrease together. As a large negative voltage is applied to the external inductor, the current rapidly decreases, and the direction of the current in the 1st-stage rectifier reverses, demonstrating the commutation operation. During this commutation interval, I_{LA} decreases by I_O/n $[I_O/(2n) \rightarrow -I_O/(2n)]$. The longer this commutation interval, the shorter the Powering interval, leading to lower voltage gain. Therefore, the commutation interval is referred to as duty loss, as shown in equation (4). Through equation (4), it can be observed that duty loss increases with an increase in the switching

frequency (F_S) and external inductor (L_A).

$$Duty\ Loss = \frac{L_A \times I_O \times F_S}{n \times V_S} \tag{4}$$

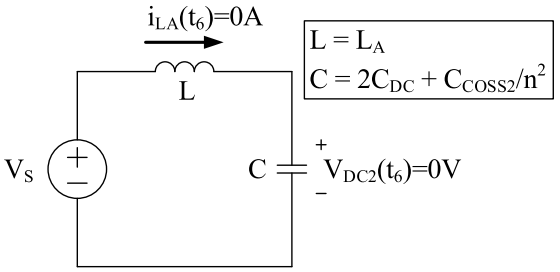

FIGURE 8. Equivalent circuit for Mode7 (t6-t7).

Mode7(t_6-t_7) occurs when the current flowing through Q_{S1} becomes 0A at t_7, concluding the commutation operation. An equivalent circuit, as shown in Fig. 8, is formed. The voltages across I_{LA} and the 1st-stage-projected Q_{S1} (V_{DC2}) containing only the resonant component are expressed in equations (5) and (6).

$$I_{LA}(t) = V_S\sqrt{\frac{C}{L}}sin\left(\frac{1}{\sqrt{LC}}(t - t_6)\right) \tag{5}$$

$$V_{DC2}(t) = V_S\left(1 - cos\left(\frac{1}{\sqrt{LC}}(t - t_6)\right)\right) \tag{6}$$

The current I_{LA} increases due to the resonant current in equation (5). After 1/4 of the resonant period at t_7, when V_{DC2} becomes equal to V_S, D_{C1} conducts, and I_{LA} flows with a flat current. Looking at the equivalent circuit in Fig. 8, the parasitic capacitance (C_P) of the clamp diode and the output capacitance (C_{OSS2}) of the secondary-side switch are arranged in parallel. Therefore, V_{DC2} can be considered the same as the value projected onto the primary side, V_{QS1}. Thus, when V_{DC2} is clamped to V_S, V_{QS1} is also clamped to $2V_S/n$, limiting voltage ringing.

B. INPUT&OUTPUT RELATIONSHIP

For the convenience of deriving the voltage gain, it is assumed that the dead time interval, which is very short, is ignored, and the external inductance can be neglected as it is much smaller than the magnetizing inductance ($L_M \approx L_{M1}+LA \approx L_{M2}+L_A$). Examining the operation from the perspective of L_{M2}, during $D_{eff} \cdot T_S$ in Mode1, the voltage of V_S-nV_O is applied, causing I_{LM2} to have a positive slope and rise. In the remaining interval (1-D_{eff}) $\cdot$ T_S, $-nV_O$ is applied, causing I_{LM2} to have a negative slope and decrease. Therefore, the ripple of I_{LM2} is given by equations (7) and (8).

$$\Delta I_{LM2}\uparrow = \frac{(V_S - nV_O)\,D_{eff}\,T_S}{L_M} \tag{7}$$

$$\Delta I_{LM2}\downarrow = \frac{-nV_O\left(1\text{-}D_{eff}\right)T_S}{L_M} \tag{8}$$

At this point, due to the characteristic of the inductor, voltage second balance, it can be considered that the amount of inductor charging energy ($\Delta I_{LM2}\uparrow$) and discharging energy ($\Delta I_{LM2}\downarrow$) are equal. By substituting equations (7) and (8) into the relationship $|\Delta I_{LM2}\uparrow| = |\Delta I_{LM2}\downarrow|$, the input-output relationship can be derived, expressed as equation (9).

$$V_O = \frac{V_S \times D_{eff}}{n} \tag{9}$$

TABLE 1. 2.5kW class LDC specifications.

Components	Parameters
Input Voltage (V_S)	250 ~ 412 (Nominal : 350) [V]
Output Voltage (V_O)	12 ~ 16 (Nominal : 14) [V]
Out Power (P_O)	2.5 [kW]
Switching Frequency (F_S)	200 [kHz]
Turn-Ratio	7:7:1:1

III. TWO-TR PSFB CONVERTER DESIGN

A. DESIGN SPECIFICATION

In order to meet the increasing rated capacity of the LDC, the design was carried out for a 2.5kW class. The input voltage is set according to the specifications of high-voltage batteries, ranging from 250V to 412V. The output voltage is designed for low-voltage battery specifications, ranging from 12V to 16V, with a rated capacity of 2.5 kW, as shown in Table 1.

The voltage gain is determined by the turns ratio (n) and the effective duty ratio (D_{eff}), where the effective duty ratio is influenced by duty loss. Setting a higher turns ratio is favorable for reducing voltage stress on the secondary-side switch and lowering primary-side current stress. Additionally, duty loss decreases as the turns ratio increases, leading to an increase in the effective duty ratio. However, under conditions where the input voltage is 250V and the output voltage is 16V, the voltage gain is minimized. Therefore, the turns ratio is set to its maximum value (N_{P1}:N_{P2}:N_{S1}:N_{S2} = 7:7:1:1) to satisfy the voltage gain requirement. Choosing the turns ratio determines the D_{eff} for achieving the desired voltage gain, which is set at 0.448. Considering $D_{eff} = 0.5 - D_{loss}$, the allowable duty loss is determined to be 0.052. To minimize the overall volume of the converter, a higher switching frequency (F_S) is advantageous. Increasing F_S helps reduce the size of $L_A + L_K$ for improved ZVS conditions. However, there is a trade-off, as duty loss tends to increase with higher values of switching frequency and L_A+L_K. Increasing F_S to enhance power density requires decreasing $L_A + L_K$, potentially worsening ZVS conditions. Conversely, increasing $L_A + L_K$ to alleviate ZVS conditions results in a decrease in F_S, negatively impacting the power density of the converter.

Fig. 9 depicts $L_A + L_K$ and ZVS conditions as a function of switching frequency under the conditions of a fixed duty loss of 0.045 and a turn ratio of 7:7:1:1. From Fig. 9, it is evident that for a switching frequency of 200kHz, $L_A + L_K$ can be used up to 2.2μH, and ZVS is achievable from the condition of 49.4%. However, increasing the switching frequency to 300kHz allows the use of $L_A + L_K$ up to 1.47μH, and ZVS is feasible from the condition of 60.4%.

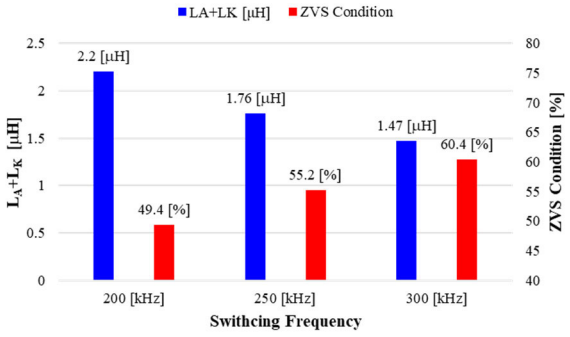

FIGURE 9. Inductor requirements and zvs conditions according to switching frequency (@ Duty loss: 0.045, turn-ratio: [7:7:1:1]).

Therefore, establishing the design direction based on the relationship between switching frequency and $L_A + L_K$ is crucial in designing the converter. In this study, we confirmed a design effective range that satisfies the duty loss tolerance of 0.52 and achieves ZVS under load conditions of 50% or more, as shown in Fig. 10. As a result, for load conditions of 50% or more, satisfying ZVS, and meeting the duty loss tolerance under the worst-case voltage gain conditions, the selected values are F_S of 200kHz and $L_A + L_K$ of 2.2μH.

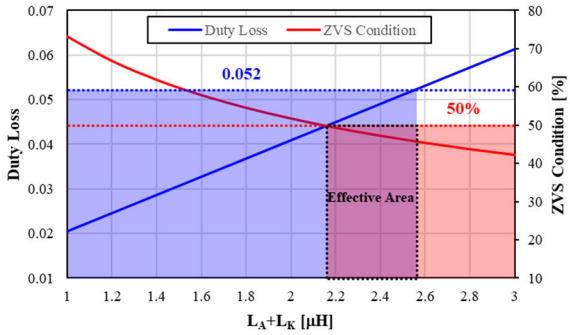

FIGURE 10. Duty loss and ZVS condition according to inductance (@F_S: 200kHz).

B. MAGNETIC CORE DESIGN

When designing the magnetic core, it is essential to use a core that meets the specifications. The core size is determined by the maximum flux density, so the design process should be conducted under the condition where the maximum flux density is the highest for magnetic core design. The maximum flux density is given by equation (10).

$$B_{MAX} = \frac{L_M \times I_{LM.MAX}}{A_C \times N_P} \tag{10}$$

$I_{LM.max}$ represents the maximum current of the magnetizing inductor, where A_C is the core's cross-sectional area, and N_P is the number of turns on the primary side. Under conditions where the magnetizing inductor, core's cross-sectional area, and the number of turns on the primary side are the same, the condition with the maximum current of the magnetizing inductor becomes the one with the highest maximum flux density. The maximum current of the magnetizing inductor is given by equation (11).

$$I_{LM.MAX} = \frac{I_O}{2n} + \frac{(V_S - nV_O) \times D_{eff} \times T_S}{2L_M} \tag{11}$$

Equation (11) indicates that the maximum inductor current increases when the output current is maximized and the current ripple is larger. Since the output current tends to have larger values when the output voltage is lower, we fix it at 12V for comparison purposes. Assuming the parameters such as power output (P_O), switching frequency (F_S), inductor (L_M), and turns ratio (n) are consistent, we can consider the condition where $(V_S\text{-}nV_O)D_{eff}$ is the largest as the one with the greatest $I_{LM.MAX}$. Therefore, $(V_S\text{-}nV_O)D_{eff}$ can be regarded as the current ripple gain, and the inductor current ripple is determined based on the magnitude of the input voltage. The current ripple gain with respect to the input voltage can be observed in Table 2. From Table 2, it is evident that the largest value occurs under the condition of an input voltage of 412V and an output voltage of 12V. Therefore, magnetic design should be conducted under the conditions of an input voltage of 412V, output voltage of 12V, and power rating of 2.5kW.

TABLE 2. Magnetized inductor current ripple gain.

Condition	Inductor Current Ripple Gain
V_S : 250V, V_O : 12V	55.776
V_S : 412V, V_O : 12V	66.874

The selection of the switching frequency at 200kHz requires careful consideration of a suitable material for the high-frequency operation. PM-16, a Ferrite material with minimal permeability changes up to 200kHz, was chosen. PM-16 exhibits a significant change in permeability when the maximum flux density exceeds 0.31T under 100°C conditions. Therefore, the size of the magnetic core needs to be selected within the range where the maximum flux density does not exceed 0.31T. The size of the magnetic core is determined by the core's cross-sectional area (A_C) and is calculated as shown in equation (12).

$$A_C = \frac{L_M \times I_{LM.MAX}}{N_P \times B_{MAX}} \tag{12}$$

The core's cross-sectional area (A_C) can be calculated using $I_{LM.MAX}$, N_P, B_{MAX}, and L_M. To perform this calculation, it is necessary to choose the value of the magnetizing inductance (L_M). The magnetizing inductance can be determined through the operation of a 2-series transformer.

Leakage inductance(L_K) in Table 3 results from Maxwell simulation, where the L_K of the Non-Planar transformer is 8.4μH, approximately 4 times higher than the 2.2μH of the Planar transformer. An increase in leakage inductance leads to an increase in duty loss, and in the case of Non-Planar transformers, the sum of effective duty and duty loss reaches 0.591, exceeding 0.5. In PSFB topology, the duty

TABLE 3. Comparison of duty by transformer type.

Specifications	Parameters	
	Non-Planar	Planar
Leakage Inductance (L_K)	8.4 [μH]	2.2 [μH]
Trun Ratio (n)	7	
Effective Duty (D_{eff}) @ 250V – 16V	0.448	
Duty Loss (D_{Loss}) @ 250V – 16V	0.143	0.039
$D_{eff} + D_{Loss}$ @ 250V – 16V	0.591 (> 0.5)	0.487 (<0.5)

cycle range is limited to 0 ∼ 0.5, necessitating a reduction in the turn ratio (n) for Non-Planar transformers. A decrease in turn ratio results in an increase in the current projected onto the primary side as $I_O/(2n)$ and the voltage projected onto the secondary side as V_S/n, leading to higher current on the primary side and higher withstand voltage requirements for secondary components. Consequently, this increases the current and voltage stress on the switches, making the use of Planar transformers more advantageous.

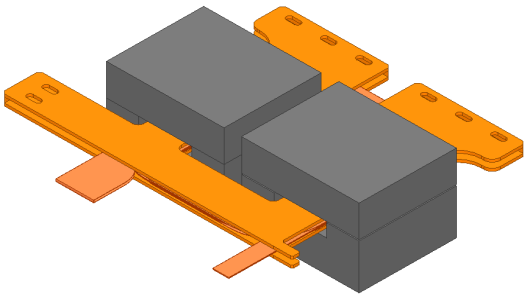

FIGURE 11. 2-serial transformer geometry.

In addition, constructing a two-series transformer with conventional winding Non-Planar transformers requires two EI cores due to structural limitations. However, using PCB winding techniques to configure a planar transformer allows for the emulation of a unified magnetic core structure with two UI cores, as shown in Fig. 11, effectively simulating the use of a single EI core. The required core cross-sectional area remains the same, whether two EI cores are used or a unified structure with two UI cores is simulated, thus increasing the core volume. Moreover, the fill factor for planar transformers is superior to that of wound transformers. As a result, using planar technology to construct a two-series transformer significantly reduces the magnetic core's volume.

Fig. 12 illustrates the operation of a 2-series transformer. In Fig. 12(a), when Q_{SR1} is turn-on, current flows through both the primary and secondary windings of the upper core, functioning as a transformer where the primary and secondary are coupled. Conversely, in the lower core, with Q_{SR2} turn-off, no current flows through the secondary winding, and it operates as an inductor where the primary and secondary do not couple. At this time, the difference

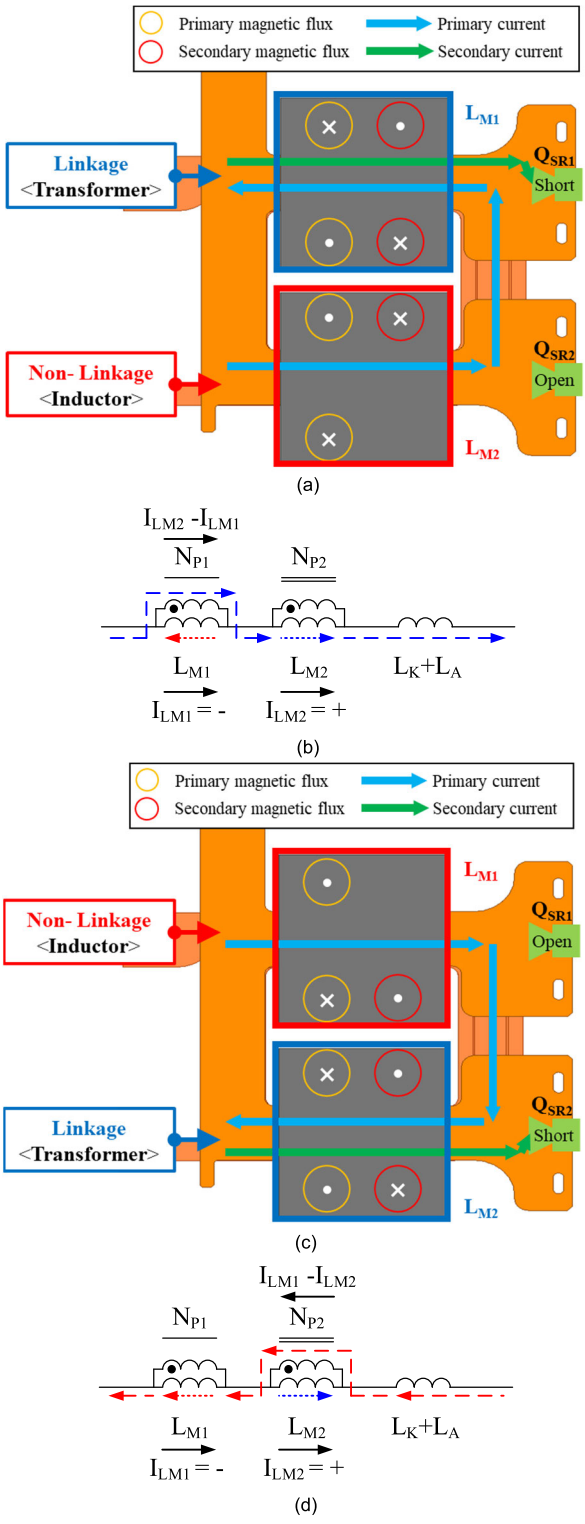

FIGURE 12. 2-serial transformer operation (a) Mode1&Mode2 (t_0-t_2); (b) Mode1&Mode2 current flow; (c) Mode8&Mode9; (d) Mode8&Mode9 current flow.

(I_{LM2}-I_{LM1}) between the magnetizing current of the upper transformer (I_{LM1}) and the current of the lower inductor (I_{LM2}) flows in the dot direction of the transformer, and the current projected onto the secondary side is represented as

$n(I_{LM2}\text{-}I_{LM1})$. In Fig. 12(c), when current flows as shown in Fig. 12(d) and Q_{SR1} is turn-off, no current can flow through the secondary winding of the upper core, and only the primary winding conducts, thus operating as an inductor where the primary and secondary windings are uncoupled. However, in the upper core, when Q_{SR2} is turn-on, current flows through the secondary winding, and both windings of the transformer are coupled, functioning as a transformer. At this time, the difference (I_{LM1}-I_{LM2}) between the magnetizing current of the lower transformer (I_{LM2}) and the current of the upper inductor (I_{LM1}) flows in the un-dot direction of the transformer, and the current projected onto the secondary side is represented as $n(I_{LM1}\text{-}I_{LM2})$. This operation allows the 2-serial transformer to replace the role of the output inductor, even in the absence of an actual output inductor. Substituting Equations (7) and (8) into Equation (1), the ripple in the secondary side current can be calculated, as expressed in Equation (13). Increasing the magnetizing inductance is advantageous for reducing output current ripple, as a larger ripple necessitates a greater capacity of the output capacitor. However, according to Equation (11), the maximum magnetizing current has an offset of $I_O/2n$, leading to an issue where increasing the magnetizing inductance causes B_{MAX} to increase, as indicated by equation (10). Therefore, to maintain the output current ripple within 25% and prevent core saturation, the magnetizing inductance value is set at 40μH through the adjustment of the air gap.

$$\Delta I_{SEC} = \frac{n\,(V_S - 2nV_O)\,D_{eff}\,T_S}{L_M} \tag{13}$$

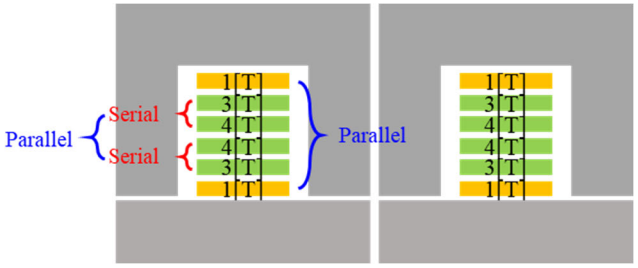

FIGURE 13. 2-serial transformer winding shape.

The winding of the magnetic core is designed considering low profile and small leakage inductance, incorporating both PCB winding and Busbar winding. For the primary side, which operates under low current specifications, PCB winding was deemed suitable. On the other hand, for the secondary side, which operates under high current specifications, Busbar winding was employed. The PCB consists of a total of 4 layers. The winding pattern follows a 3-turn configuration for layers 1 and 3, and a 4-turn configuration for layers 2 and 4. Layers 1 and 2 are connected in series, as well as layers 3 and 4, to simulate a 7-turn winding. This is then represented in a parallel connection, as shown in Fig. 13. The core window width was determined to be 19.5mm, taking into account the insulation distance between patterns, and the PCB wire width was set at 4 mm. The thickness of the PCB pattern is 3OZ, and due to the dual parallel winding, the total height of the primary side wire is 0.21mm. Thus, the area of the primary side PCB wire is 0.84mm^2. The total height of the PCB is approximately 1.6mm, and the core window height is 5mm, leaving a spare 3.4mm. Therefore, the secondary winding employs a Busbar wire with a thickness of 1mm and a width of 14mm in a dual parallel structure, resulting in a secondary side wire area of 28mm^2. The currents flowing through the primary and secondary windings of the transformer are highest under a low output voltage condition of 12V, with the primary winding carrying 14.88A and each tap of the secondary winding carrying an effective current of 147.31A. Consequently, the current density for the primary winding is designed at 17.7A/mm^2, and for the secondary winding at 5.4A/mm^2.

TABLE 4. Design Specifications for 2.5kW class 2-serial transformer.

Specifications	Parameters	
	Primary Winding	Secondary Winding
Wire: Width × Height	4 × 0.21 [mm]	14 × 2 [mm]
Wire: Area	0.84 [mm^2]	28 [mm^2]
Magnetizing Inductance (L_M)	40 [μH]	
Max Current to Primary	19.06 [A] (@ V_S : 412V, V_O : 12V)	
Core Cross-sectional Area (A_C)	432 [mm^2]	
Core : Width × Height × Depth	34.52 × 23.6 × 31 [mm]	
Turn Ratio	7 : 7 : 1 : 1	
Max Magnetic Flux Density	0.252 [T] (@ V_S : 412V, V_O : 12V)	

To analyze the losses in the designed magnetic core, it is essential to identify the conditions under which core losses occur significantly. In the case of core losses, the condition with the highest magnetic flux density ripple is considered the worst condition. The magnetic flux density ripple can be expressed by equation (14).

$$\Delta B = \frac{L_M \times \Delta I_{LM}}{A_C \times N_P} \tag{14}$$

Here, the magnetizing inductance (L_M), core cross-sectional area (A_C), and primary-side turns (N_P) are predetermined values determined by the design. It can be observed that the ripple of the magnetizing inductor current affects the ripple of the magnetic flux density. The ripple of the magnetizing inductor current increases with higher input voltage and effective duty ratio. Therefore, under the conditions of 412V input voltage and 16V output voltage, the magnetic flux density ripple takes the highest value. Consequently, the magnetic core losses are analyzed under the conditions of 412V input voltage and 16V output voltage. The final specifications and loss analysis for the magnetic core are summarized in Tables 4 and 5.

Through MAXWELL simulations, the effectiveness of the magnetic core design was verified. Fig. 14 illustrates the magnetic flux density distribution under the worst-case condition of magnetic flux density for the specified conditions of 412V input voltage and 12V output voltage.

TABLE 5. Loss for 2.5kW class 2-serial transformer.

Specifications	Parameters	
	Primary Winding	Secondary Winding
RMS Current	11.16 [A]	110.49 [A]
Copper Resistance	35.58 [mΩ]	0.114 [mΩ]
Copper Loss	4.43 [W]	1.39 [W]
Switching Frequency (F_S)	200 [kHz]	
Magnetic Flux Density Ripple	0.134 [T]	
Core Loss Constant (Cm/X/Y)	1.427 / 1.474 / 2.965	
Core Effective Volume (V_{CORE})	41,904 [mm^3]	
Core Loss (P_{CORE})	1.27 [W]	

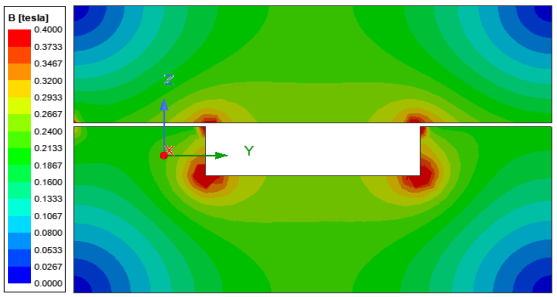

FIGURE 14. 2-series transformers magnetics distribution.

The theoretically derived maximum magnetic flux density is 0.252T, and the simulation results show a similar range of 0.213 to 0.267T for the main magnetic flux path.

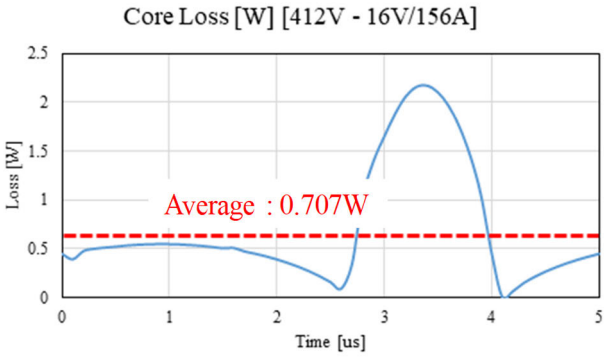

FIGURE 15. 2-Series transformers 1 cycle loss.

Fig. 15 shows the one-cycle loss results of the magnetic core under the worst-case condition of magnetic core loss for the specified conditions of 412V input voltage and 16V output voltage. The simulation results indicate an average loss of 0.707W for one cycle.

C. SWITCH DESIGN

To select suitable switches for the primary and secondary sides, it is necessary to understand the voltage and current stresses occurring at each switch. The voltage stress on the primary side switch is the input voltage, and the turn-off current of the primary side switch can be derived from the maximum external inductor current, considering the current offset and ripple of the magnetizing inductor. It is expressed as equation (15). The RMS current of the primary side switch can be approximated by assuming no ripple in the magnetizing inductor current, and the magnitude of the current offset flows during 0.5TS, as shown in equation (16).

$$I_{QP.turn-off} = \frac{I_O}{2n} + \frac{(V_S - nV_O)\, D_{eff}\, T_S}{2L_M} \tag{15}$$

$$I_{QP.rms} = \sqrt{0.5} \times \frac{I_O}{2n} \tag{16}$$

As the current projected onto the primary side increases when the output voltage is lower, the turn-off current and RMS current of the primary side switch are maximized under the condition of an output voltage of 12V. Additionally, the primary side switch component experiences maximum voltage stress under the highest input voltage condition of 412V. Therefore, the primary side switch should be selected based on the component that meets the conditions of an input voltage of 412V and an output voltage of 12V. Under the condition of an input voltage of 412V, the voltage stress on the primary side switch is 412V. Under the condition of an output voltage of 12V, the turn-off current of the primary side switch is 19.06A, and the RMS current is 10.52A. Consequently, the primary side switch is chosen as the GaNSystems GS66516B, a 650V/60A-rated component, capable of withstanding the voltage stress of 412V and current stress of 19.06A.

The voltage stress on the secondary side switch is the sum of the voltage projected from the primary side and the snubber voltage. The maximum current flowing through the secondary side switch is given by equation (17). The RMS current of the secondary side switch can be approximated by assuming that the output current flows for $0.5T_S$ without ripple in equation (18).

$$I_{QS.MAX} = I_O + \frac{n\,(V_S - 2nV_O)\, D_{eff}\, T_S}{2L_M} \tag{17}$$

$$I_{QS.rms} = \sqrt{0.5} \times I_O \tag{18}$$

The voltage stress on the secondary side switch is the sum of the voltage projected from the primary side and the snubber voltage. The maximum current flowing through the secondary side switch is highest when the output voltage is 12V, as the output current increases with a lower output voltage. Additionally, the voltage stress on the secondary side switch is highest when the input voltage is at its maximum. Therefore, the secondary side switch should be selected to meet the conditions of an input voltage of 412V and an output voltage of 12V. Under these conditions, the voltage stress on the secondary side switch is 79V, comprising the projected secondary side voltage of 58.86V and a snubber voltage of 20V. The maximum current for the secondary side switch is 224.4A, and the RMS current is 147.31A when the output voltage is 12V. Therefore, the secondary side switch is selected as the Infineon IAUT300N10S5N015, which meets the requirements of 79V voltage stress and 224.4A current stress.

The component selection for the primary and secondary side switches is determined considering the limited Power Dissipation (P_D). For the secondary side SiC component, the

TABLE 6. Primary side switch loss (1-Parallel and 2-Parallel).

Components	Parameters	
	1-Parallel	2-Parallel
RMS Current	10.52 [A]	5.26 [A]
Turn-off Current	19.06 [A]	9.53 [A]
Selected GaN FET	GaNSystems-GS66516B	
$R_{DS(on)}$	65 [mΩ] (@ 150°C)	
Turn-off Energy	17.51 [μJ] (@ 412V, 19.06A)	8.76 [μJ] (@ 412V, 9.53A)
Turn-off Loss	4.38 [W]	2.19 [W]
Conduction Loss	7.2 [W]	1.8 [W]
Power Dissipation	9.2 [W]	
Total Loss	11.58 [W]	3.99 [W]

TABLE 7. Secondary side switch loss (3-Parallel).

Components	Parameters	
	1-Parallel	3-Parallel
RMS Current	147.31 [A]	49.11 [A]
Selected SiC FET	Infineon-IAUT300N10S5N015	
$R_{DS(on)}$	2.3 [mΩ] (@ 150°C)	
Power Dissipation	12.5 [W]	
Total Loss	49.91 [W]	5.55 [W]

P_D value is set to 12.5W, which is approximately 1/30 of the 25°C condition P_D of 275W, to avoid exceeding this level. In the case of the primary side GaN component, although the P_D value is relatively high, designing based solely on P_D may lead to a design with high losses. Considering the potential increase in the size of the heat sink required for efficient heat dissipation, the structure is determined to not exceed 9.2W, which is about 1/50 of the 25°C condition P_D of 460W. Since the worst-case conditions align with the switch selection conditions, the loss analysis is conducted under the condition of an input voltage of 412V and an output voltage of 12V.

The primary-side switch component, being under ZVS conditions, incurs no turn-on losses. Therefore, considerations are focused on turn-off and conduction losses. In the case of a 1-parallel structure, the individual losses per switch amount to 11.58W, exceeding the proposed P_D of 9.2W. Consequently, using a 1-parallel structure proves challenging. Adopting a 2-parallel structure for loss analysis yields a total loss of 3.55W, satisfying the proposed P_D conditions. Hence, for the primary-side switch, a 2-parallel structure with a total of 8 switches is employed.

The secondary-side switch component experiences minimal turn-on and turn-off losses due to the extremely low current during these points. Therefore, considerations focus mainly on conduction losses. In the case of a 1-parallel structure, individual losses per switch amount to 49.91W, significantly exceeding the proposed P_D of 12.5W. Therefore, employing a 1-parallel structure is deemed impractical. Adopting a 3-parallel structure for loss analysis yields a total loss of 5.55W, satisfying the proposed P_D conditions. Consequently, for the secondary-side switch, a 3-parallel structure with a total of 6 switches is used.

D. SYNCHRONOUS RECTIFIER DESIGN

When constructing the secondary-side rectifier stage with diodes, high conduction losses occur due to the elevated forward voltage(V_f) of the diodes. To achieve the high-efficiency specifications of the converter, the secondary-side rectifier stage is constructed with a synchronous rectifier (SR). When configured with an SR, switch components can be used on the secondary side as substitutes for diodes. Switch components offer the advantage of lower conduction losses due to their small turn-on resistance compared to diodes. It is crucial to clearly distinguish between the turn-on and turn-off regions for SR operation. Analyzing the operating principles reveals that SR operation can be distinguished through the turn-on regions of the leading-leg and lagging-leg. Analyzing based on Q_{SR1} shows that current flows during the turn-on regions of Q_{P1} and Q_{P2}. Therefore, the SR can mimic the gate turn-on during the turn-on region of the primary-side switch through ORing.

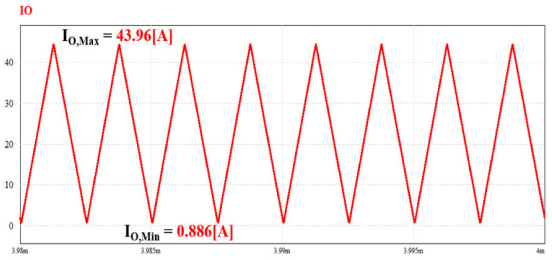

FIGURE 16. Secondary current [CCM] (@V_S: 412V, V_O: 14V, P_O: 315W).

In the case of the LDC, the load conditions change sequentially depending on the use of the front-end component. When operating in Discontinuous Conduction Mode (DCM) and driving the SR, circuit breakdown can occur due to negative current in the secondary side. Therefore, to ensure stability and prevent circuit damage, an SR enable algorithm is necessary. To determine the SR enable condition, analysis of the DCM condition is required. As shown in Fig. 16, with an input voltage of 412V, output voltage of 14V, and output power of 315W, it can be observed that Continuous Conduction Mode (CCM) operation is ending. Therefore, to ensure stability in SR operation, the enable signal should be activated after an output current of 22.5A. Setting a single current threshold of 22.5A for the enable algorithm can lead to issues where the enable and disable signals alternate continuously at specific load points due to output current ripple. Hence, for the SR enable circuit, a Schmitt trigger, as illustrated in Fig. 17, is adopted.

Schmitt trigger has two threshold voltages. These two threshold voltages serve as reference values to determine whether the Schmitt trigger will output a high level or a low level based on the input signal. The SR enable signal is represented when the voltage is higher than the High-level threshold voltage ($V_{th-high}$), and the SR disable signal is represented when the voltage is lower than the Low-level threshold voltage (V_{th-low}). The resistor values for the

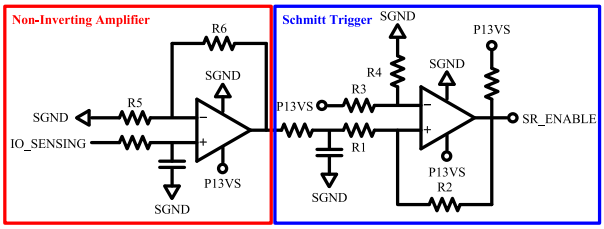

FIGURE 17. Schmitt trigger for SR enable circuit.

Schmitt trigger should be selected to establish these threshold voltages, which are determined by equations (19) and (20).

$$V_{th-high} = \frac{R_4\,(R_1 + R_2)}{R_2\,(R_3 + R_4)} \times P13VS \tag{19}$$

$$V_{th-low} = \left(\frac{R_4\,(R_1 + R_2)}{R_2\,(R_3 + R_4)} - \frac{R_1}{R_2}\right) \times P13VS \tag{20}$$

Selecting the Low-level threshold voltage based on the 22.5A, which represents the operation in CCM, ensures high efficiency under light load conditions. However, for stability assurance, the Low-level threshold voltage should be chosen with some margin. Therefore, the SR enable current level is set at 58.5A, and the SR disable current level is set at 38.5A.

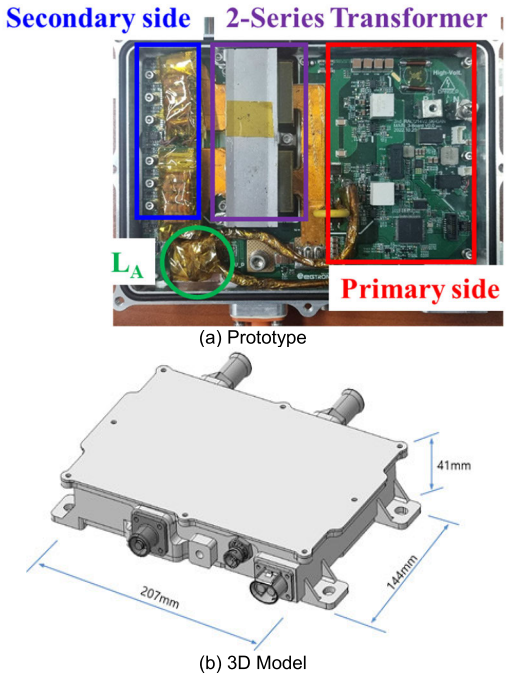

FIGURE 18. 2.5kW-class 2-TR PSFB prototype.

IV. EXPERIMENTAL

To verify the achievement of high efficiency and power density in the proposed converter, a prototype of a 2.5kW-rated 2-TR PSFB converter was fabricated, as shown in Fig. 18. The converter system consists of the converter, power semiconductor components, and a heatsink to prevent the heating of magnetic components. The specifications of the fabricated converter components are listed in Table 8. Additionally, the volume of the fabricated prototype was calculated by multiplying its width, height, and depth, as shown in Table 9.

TABLE 8. Device Specifications of the 2.5kW-class 2-TR PSFB prototype.

Components	Parameters
Primary Switch (Q_{Pn})	GaSystems-GS66516B 2-Parallel (600V / 60A)
Secondary Switch (Q_{SRn})	Infineon-IAUT300N10S5N015 3-Parallel (100V / 300A)
Transformer (T_n)	Fig. 19. (Pri: PCB / Sec: Busbar)

TABLE 9. Volume of the 2.5kW-class 2-TR PSFB prototype.

Components	Parameters
Width	207 mm
Depth	144 mm
Height	41 mm
Volume	1.222 cm^3

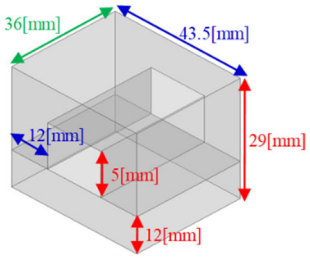

FIGURE 19. Transformer of 2.5 kW class 2-TR PSFB prototype.

The overall dimensions of the prototype are 207mm in width, 144mm in depth, and 41mm in height, resulting in a volume of 1.222cm^3. The power density is calculated as 2.5kW/1.222cm^3 = 2.04kW/L, confirming that it achieves a power density of 2.0kW/L.

The design specifications for the converter include an input voltage range of 250V to 412V and an output voltage range of 8V to 16V. The nominal condition for this converter is an output voltage of 14V. Given the importance of operation and efficiency under nominal conditions, verification testing and efficiency measurements will be conducted under these conditions.

Fig. 20 depicts the waveforms of V_{AB}, I_{LK}, and V_{QSR} under the conditions of output voltage 14V, output power 2.5kW, and input voltages of 250V, 350V, and 412V. The converter operates as analyzed in the operational principles.

Fig. 21 shows the efficiency measurement results under the conditions of output voltage 14V and input voltages of 250V, 350V, and 412V. The maximum efficiency of 97.05% was measured at an input voltage of 250V and output voltage of 14V with a load condition of 60% (1.5kW). Under light load conditions where ZVS conditions are not satisfied, the efficiency is measured lower. However, for load conditions exceeding 50% with satisfied ZVS conditions,

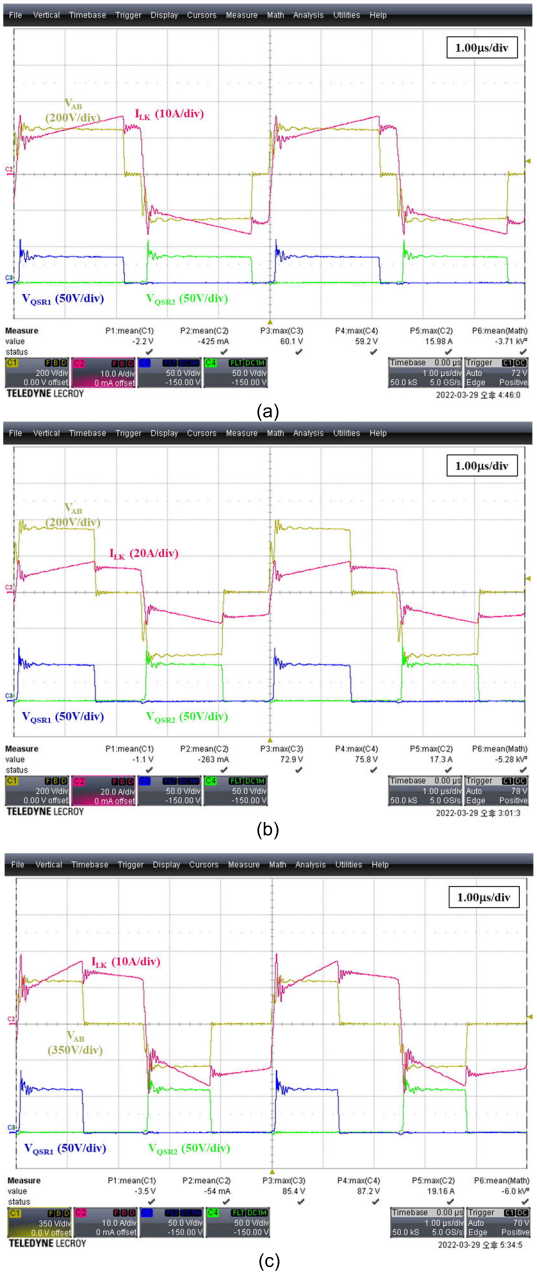

FIGURE 20. 2.5 kW-class 2-TR PSFB prototype experimental waveform. (a) 250V-14V[2.5kW]; (b) 350V-14V[2.5kW]; (c) 412V-14V[2.5kW].

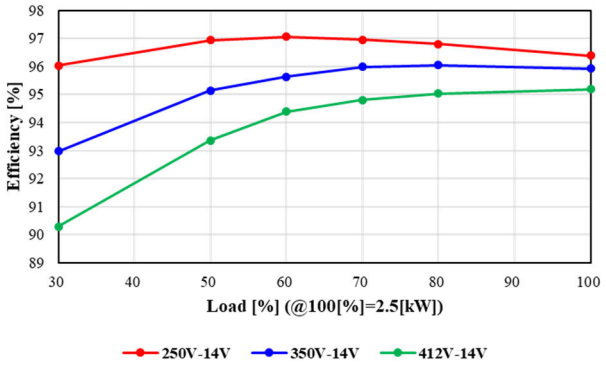

FIGURE 21. Efficiency of 2.5 kW-class 2-TR PSFB prototype.

FIGURE 22. 2.5kW 2-TR PSFB prototype efficiency comparison (@2.5[kW]).

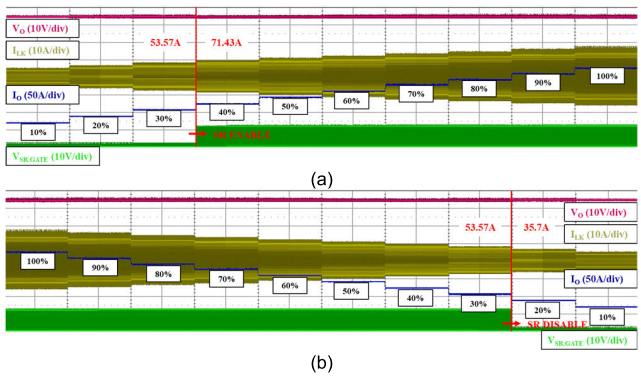

FIGURE 23. 2.5kW 2-TR PSFB prototype dynamic experimental waveform (@Step: 10% Load).

alternative efficiencies of over 95% were confirmed. Under the test conditions of output voltage 14V and 100% load, the results showed efficiencies of 96.38% for 250V, 95.93% for 350V, and 95.19% for 412V. The theoretical analysis results indicated efficiencies of 97.84% for 250V, 97.49% for 350V, and 97.25% for 412V. Comparisons between theoretical analysis results and test results can be seen in Fig. 22. Considering losses, including those from the switch, magnetic component, and snubber, as well as additional losses such as PCB pattern losses, the obtained results are deemed valid.

Fig. 23 shows the dynamic (10% step load) experimental results under the conditions of input voltage 350V and output voltage 14V. The SR drive circuit is designed with an SR enable current level of 58.5A. It can be observed that the SR enable is performed as the load increases from 30% (53.57A) to 40% (71.43A). The SR drive circuit is designed with an SR disable current level of 38.5A. It is confirmed that the SR disable is performed as the load decreases from 30% (53.57A) to 20% (35.7A).

Fig. 24(a) displays the temperature measurement points, and Fig. 24(b) presents the test results after aging for 60 minutes with the coolant temperature set at 60°C. The

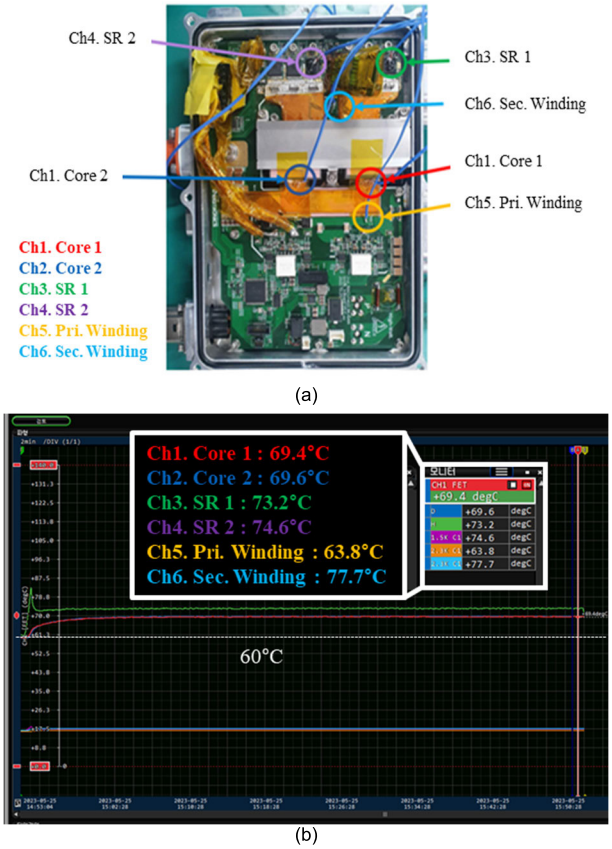

FIGURE 24. 2.5kW-class 2-TR PSFB prototype temperature distribution.

core temperature reached 69.6°C, the secondary side FET registered 74.6°C, the primary winding was at 63.8°C, and the secondary winding at 77.7°C. Observations confirmed that the temperatures of all heat-generating components stabilized below 80°C.

V. CONCLUSION

In this paper, a planar transformer-based 2-TR PSFB converter is proposed to meet the high-power specifications and wide input-output voltage range of the LDC, one of the power conversion devices in electric vehicles. The proposed converter, utilizing an integrated magnetic core with small output current ripple without the need for an output inductor, simplifies the structure of the output circuit. Additionally, by applying GaN power semiconductors, the switching frequency can be increased to reduce the volume of the magnetic components. Through the operational analysis of the proposed converter in this study, the losses of each component and the worst-case design conditions are identified, providing a general design direction. Furthermore, a secondary-side synchronous rectifier circuit is proposed for loss reduction, and the use of a Schmidt trigger is suggested to ensure stability during Discontinuous Conduction Mode operation. Finally, the prototype of the proposed converter is manufactured, achieving a power density of 2.0 kW/L and confirming a maximum efficiency of 97.05%. The operation of the SR drive circuit is also validated.

REFERENCES

[1] E. Erdogdu, "Turkish support to Kyoto protocol: A reality or just an illusion," *Renew. Sustain. Energy Rev.*, vol. 14, no. 3, pp. 1111–1117, Apr. 2010, doi: 10.1016/j.rser.2009.10.020.

[2] L. A. Wehinger, M. D. Galus, and G. Andersson, "Agent-based simulator for the German electricity wholesale market including wind power generation and widescale PHEV adoption," in *Proc. 7th Int. Conf. Eur. Energy Market*, Madrid, Spain, Jun. 2010, pp. 1–6, doi: 10.1109/EEM.2010.5558718.

[3] Y. Xu, J. Liang, B. Cheng, W. He, J. Shu, K. Li, and Y. Xie, "Research on the impact of re-electrication in the transportation sector on carbon emission and pollutant emission in Yunnan province," in *Proc. Power Syst. Green Energy Conf. (PSGEC)*, Shanghai, China, Aug. 2021, pp. 407–412, doi: 10.1109/PSGEC51302.2021.9542680.

[4] H. Ma, Y. Tan, L. Du, X. Han, and J. Ji, "An integrated design of power converters for electric vehicles," in *Proc. IEEE 26th Int. Symp. Ind. Electron. (ISIE)*, Edinburgh, U.K., Jun. 2017, pp. 600–605, doi: 10.1109/ISIE.2017.8001314.

[5] H. Glickenstein, "March 2020 land transportation news [transportation systems]," *IEEE Veh. Technol. Mag.*, vol. 15, no. 1, pp. 12–13, Mar. 2020, doi: 10.1109/MVT.2019.2959675.

[6] P. Thounthong, S. Rael, and B. Davat, "Energy management of fuel cell/battery/supercapacitor hybrid power source for vehicle applications," *J. Power Sources*, vol. 193, no. 1, pp. 376–385, Aug. 2009.

[7] R. R. Kumar, C. Bharatiraja, K. Udhayakumar, S. Devakirubakaran, K. S. Sekar, and L. Mihet-Popa, "Advances in batteries, battery modeling, battery management system, battery thermal management, SOC, SOH, and charge/discharge characteristics in EV applications," *IEEE Access*, vol. 11, pp. 105761–105809, 2023, doi: 10.1109/ACCESS.2023.3318121.

[8] M. A. Hannan, M. M. Hoque, A. Hussain, Y. Yusof, and P. J. Ker, "State-of-the-art and energy management system of lithium-ion batteries in electric vehicle applications: Issues and recommendations," *IEEE Access*, vol. 6, pp. 19362–19378, 2018, doi: 10.1109/ACCESS.2018.2817655.

[9] S. Manzetti and F. Mariasiu, "Electric vehicle battery technologies: From present state to future systems," *Renew. Sustain. Energy Rev.*, vol. 51, pp. 1004–1012, Nov. 2015.

[10] T.-F. Yi, J. Mei, and Y.-R. Zhu, "Key strategies for enhancing the cycling stability and rate capacity of $LiNi_{0.5}Mn_{1.5}O_4$ as high-voltage cathode materials for high power lithium-ion batteries," *J. Power Sources*, vol. 316, pp. 85–105, Jun. 2016.

[11] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2208–2219, May 2014, doi: 10.1109/TPEL.2013.2267804.

[12] W. Zhang, X. Huang, F. C. Lee, and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Fort Worth, TX, USA, Mar. 2014, pp. 1484–1489, doi: 10.1109/APEC.2014.6803503.

[13] E. A. Jones, F. Wang, and B. Ozpineci, "Application-based review of GaN HFETs," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, Knoxville, TN, USA, Oct. 2014, pp. 24–29, doi: 10.1109/WIPDA.2014.6964617.

[14] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600 v GaN HEMT in cascode structure," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014, doi: 10.1109/TPEL.2013.2276127.

[15] B.-R. Lin, K. Huang, and D. Wang, "Analysis, design, and implementation of an active clamp forward converter with synchronous rectifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 6, pp. 1310–1319, Jun. 2006, doi: 10.1109/TCSI.2006.870900.

[16] Q. Li, F. C. Lee, and M. M. Jovanovic, "Design considerations of transformer DC bias of forward converter with active-clamp reset," in *Proc. 14th Annu. Appl. Power Electron. Conf. Expo. Conf. (APEC)*, Dallas, TX, USA, 1999, pp. 553–559, doi: 10.1109/APEC.1999.749735.

[17] H. Wu and Y. Xing, "Families of forward converters suitable for wide input voltage range applications," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 6006–6017, Nov. 2014, doi: 10.1109/TPEL.2014.2298617.

SANG-GYUN RYU received the B.S. and M.S. degrees from Korea National University of Transportation, Gyeonggi-do, South Korea, in 2021 and 2023, respectively, where he is currently pursuing the Ph.D. degree. His research interests include the design, control, and analysis of DC/DC converters for electric vehicles.

SEONG-YONG HONG received the B.S. and M.S. degrees from Korea National University of Transportation, Gyeonggi-do, South Korea, in 2019 and 2023, respectively, where he is currently pursuing the Ph.D. degree. His research interests include the design and analysis of DC/DC converters for high-efficiency and high-density.

CHAN-BAE PARK received the M.S. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2003, and the Ph.D. degree in electrical engineering from Hanyang University, Seoul, in 2013. From 2003 to 2006, he was a Senior Engineer at the Digital Appliance Research and Development Center, Samsung Electronics. From 2007 to 2015, he was a Senior Researcher at Korea Railroad Research Institute. Since 2015, he has been an Associate Professor with Korea National University of Transportation, Uiwang-si, South Korea. His research interests include design and analysis of various electric machines for electric vehicles and railways.

HYUNG-WOO LEE received the M.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 2000, and the Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2003. From 2006 to 2013, he was a Senior Researcher at Korea Railroad Research Institute. In March 2013, he joined as a Professor with the Department of Railway Vehicle System Engineering, Korea National University of Transportation. His research interests include design and analysis of motors/generators, and applications of motor drive, such as Maglev trains, conventional railway propulsion systems, and modern renewable energy systems.

JAE-BUM LEE received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2010, and the M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2012 and 2016, respectively. From 2016 to 2019, he was a Senior Researcher at Korea Railroad Research Institute, Uiwang-si, South Korea. He is currently an Assistant Professor with Korea National University of Transportation, Uiwang-si. His research interests include high-voltage/power transformer design, high-efficiency ac–dc and dc–dc converters, and digital control method in high-power vehicles, such as electric vehicles and rolling stock and medium power, such as electronic equipment.