IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 17 May 2024, accepted 12 July 2024, date of publication 23 July 2024, date of current version 5 August 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3432611

TOPICAL REVIEW

Challenges and Trends of Implantable Functional Electrical Neural Stimulators: System Architecture and Parameters

MOSTAFA KATEBI[1,2], (Member, IEEE), ABBAS ERFANIAN[1], (Member, IEEE), MOHAMMAD AZIM KARAMI[1], (Member, IEEE), AND MOHAMAD SAWAN[2], (Life Fellow, IEEE)

[1]Department of Bioelectronics, Iran University of Science and Technology, Tehran 16846-13114, Iran
[2]CenBRAIN Neurotech Center of Excellence, Westlake University, Hangzhou, Zhejiang 310024, China

Corresponding authors: Abbas Erfanian (erfanian@iust.ac.ir) and Mohamad Sawan (sawan@westlake.edu.cn)

This work was supported in part by Westlake University under Grant 10318A992001.

ABSTRACT Electrical neural stimulators (ENS) play a crucial role in medical applications and have emerged as promising therapeutic techniques for neurological disorders. The purpose of designing this device in medicine and research is to provide therapeutic benefits, aid in rehabilitation, restore sensory perception, advance scientific knowledge, and enable personalized treatment approaches. The utilization of ENS can significantly improve the quality of life for individuals with neurological disorders and contribute to advancements in neuroscience. Recently, there has been a growing inclination towards implantable biomedical microsystems, which has enticed biomedical engineers and researchers to integrate and implement electrical neural stimulators using CMOS technology. Thus, we present this review to provide a comprehensive overview of integrated circuits in the ENS field. The review aims to discuss the operational principles, design considerations, and approaches while highlighting advancements, applications, and future directions. The review begins with an introduction, emphasizing the necessity of stimulation and the fundamental principles of the ENS. It then discusses the various stimulation patterns, exploring how these patterns can modify neural circuits and restore normal function, as well as the circuit implementations involved in generating the stimulation. Design considerations specific to stimulators are also discussed. Furthermore, the review summarizes the state-of-the-art circuits and systems for the ENS, employing a top-down approach that covers specifications, circuits, and system design. Additionally, it briefly provides an overview of experimental approaches and results from various biomedical tests. Finally, this review outlines future directions, trends, and challenges for enhancing precision, safety, and patient outcomes in stimulation therapies.

INDEX TERMS Functional electrical neural stimulation (FENS), electrical neural stimulator (ENS), charge-balance, monophasic, biphasic, current stimulator, voltage stimulator, H-bridge, voltage compliance, anodic/cathodic phase, implantable medical devices (IMD).

I. INTRODUCTION

Functional electrical neural stimulation (FENS) is a promising method for treating various neural disorders, including central and peripheral nervous system dysfunction [1], [2], [3], [4], [5], [6], [7], [8], which has recently gained significant attention. Figure 1 depicts the significantly increasing number of recent FENS-related publications, indicating a growing interest in this field. FENS has also been utilized in many biomedical applications to restore physical sensory damage caused by injury or disease [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27]. Notable applications include cardiac pacemakers [9], cochlear and retinal implants [10], [11], [12], [13],

The associate editor coordinating the review of this manuscript and approving it for publication was Ganesh Naik.

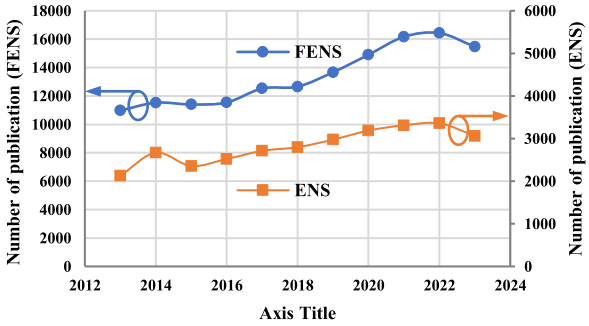


FIGURE 1. FENS-related and ENS-related papers published over the last years.

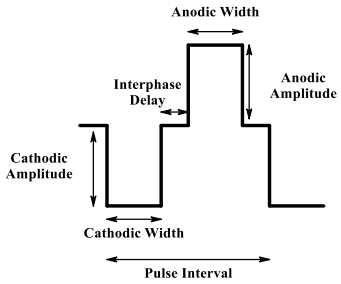


FIGURE 2. Biphasic current pulse with interphase delay.

[14], [15], [16], seizure control [17], [18], and vestibular prostheses [21]. The primary objective of these prostheses is to establish a direct connection between the neural stimulator and the nervous system, providing therapeutic interventions and restoring or enhancing compromised neural functions. These advancements in electronic devices have the potential to significantly improve the quality of life for individuals with neural disorders or dysfunctions. Figure 2 depicts a widely used type of stimulation current wave known as biphasic stimulation and its specifications. According to numerous research results, the stimulation parameters such as pulse interval, pulse width for each phase, interphase delay, voltage/current amplitude for each phase, and monophasic/biphasic waveform can be optimized based on patient symptoms [28], [29], [30]. Moreover, by adjusting these parameters in certain neuro-stimulation techniques such as deep brain stimulation (DBS), cortical stimulation, and Vagus nerve stimulation (VNS), safe and efficacious stimulation can be achieved for treating diseases like Parkinson's and epilepsy [31].

Neuro-stimulation devices are used to generate the desired stimulation wave and are employed in implantable medical devices (IMDs), as shown in Figure 3, which consist of external and internal parts. The external part transmits power and data through an inductive link to the inner part. The internal part includes wireless power and data telemetry to supply power and input data to the chip, a processor to control the system's operation procedure, an acquisition unit to record neural signals, and a stimulator that must stimulate the tissue based on the received data from the external part. The ENS is

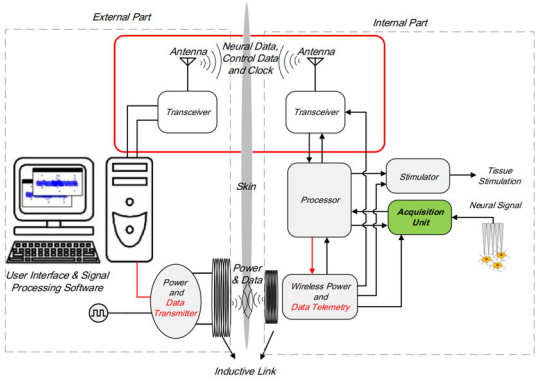


FIGURE 3. Block diagram of an implantable medical device.

one of the essential blocks in IMDs and has recently gained significant attention and development. As shown in Figure 1, the number of published ENS-related papers has increased over the last ten years. The ENS operates by delivering electrical charges to nerve tissues to elicit action potentials, thereby effectively modulating neural activity. The electrical charge can be injected into the nerve tissues via constant voltage (CV) or constant current (CC) stimulation [32]. Recently, the current stimulator has been preferred over the voltage stimulator. The ability to directly regulate the current output, along with the improved stability and protection benefits, make current mode stimulation the preferred choice in many power electronics applications, especially where precise current control and high reliability are critical.

However, the voltage stimulator still plays a significant role in electrical therapeutics and remains the subject of recent studies [30], [33], [34], [35]. ENS consists of analog circuits, such as high-voltage-tolerant switches, a level shifter, a Digital-to-Analog Converter (DAC), a current mirror, and a current-source reference. Designing these circuits with the necessary constraints is vital for Integrated Medical Devices (IMDs) and various other applications in integrated circuits and systems. Two significant considerations are reducing size and power consumption. Power is consumed due to the voltage drop on electrodes and heat dissipation. Therefore, reducing these factors improves power efficiency [36], [37], [38].

Voltage compliance is another crucial aspect of the ENS. Certain applications, such as deep brain stimulation, require high-current stimulation [39]. Additionally, in these cases, the tissue impedance is typically high, necessitating a sufficiently high electrode voltage to provide the desired current. Ensuring safe electrical stimulation is one of the primary challenges in ENS design. If the residual voltage exceeds the safe range after each stimulation, tissue damage can occur. Therefore, to prevent tissue damage under any condition, charge-balanced stimulation is necessary to mitigate the risk of tissue damage [40]. Another critical issue in designing the ENS is the consideration of tissue and electrode impedance. It is important to model this impedance to better estimate the

circuit's performance. The impedance varies for each organ in the body [41], [42].

In certain cases, circuits have been designed specifically to measure tissue impedance [43]. The number of stimulation channels is another important factor in stimulator design. The required number of channels depends on the targeted organs and diseases. For example, eye stimulators typically require a higher number of channels [44], [45], while for disorders like epilepsy, one or two channels may be sufficient [39]. The stimulation amplitude, frequency, and pulse width of the stimulators are other critical parameters. These parameters should be carefully designed and tailored to the target tissue, and they can also be adjusted in specific steps. The ability to adjust stimulation parameters allows for better and more efficient performance [31].

This review paper focuses extensively on ENS design and describes advanced circuits and systems for ENS using a top-down approach, starting from specifications and moving towards circuits and systems. Various stimulation types and system structures will be analyzed.

Design challenges and considerations for ENS will be discussed to provide a thorough comparison and identify bottlenecks and potential solutions. The rest of the paper is organized as follows: Section II outlines the operational principles of stimulation and the stimulator. Design considerations and critical issues will be discussed in section III, while section IV will explain design approaches and recent circuit implementation methods for each block of the ENS. Section V focuses on application-specific stimulators, emphasizing the results of in vitro and in vivo experiments conducted with implantable stimulators. Section VI will present future trends and potential improvements, and finally, the conclusion will be presented in section VII.

II. STIMULATOR OPERATION PRINCIPLE

In ENS, ensuring safe and efficacious stimulation is critical. Efficacious stimulation refers to the ability to achieve the desired physiological outcomes. On the other hand, it is crucial to prevent any damage to the tissue and electrodes during the stimulation process to ensure safety. To address these requirements, two different types of stimulation waveforms have been introduced [46].

The first type of stimulation waveform is monophasic stimulation, as depicted in Figure 4(a). It involves the application of current pulses in one direction without any current pulses in the opposite direction. Typically, the cathodic pulse shape is used for monophasic stimulation, although in some cases, the anodic form may also be employed. Based on experimental studies and results, monophasic stimulation has shown the best efficacy in preventing electrode damage [46]. However, for long-term stimulation, tissue damage cannot be completely avoided due to the residual voltage that remains on the tissue. The symbols "+ + +" and "- - -" represent the best and worst cases, respectively, in terms of efficacy and minimal tissue or electrode damage. Figure 4(b) and Figure 4(c) illustrate monophasic stimulators. The current can

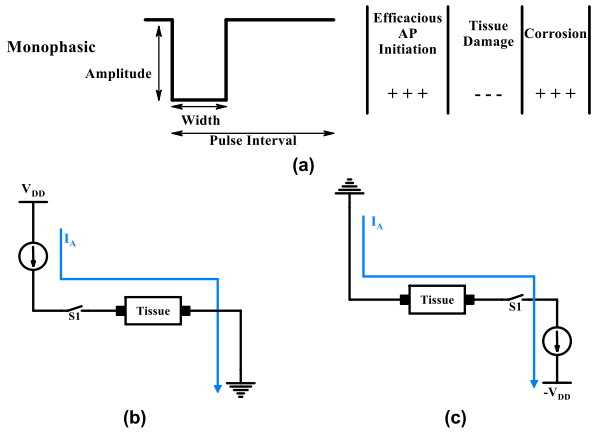


FIGURE 4. Monophasic signal and generator circuits: (a) Stimulation waveform, (b) Current-source stimulator, (c) Current-sink stimulator.

either be sourced to the tissue or sunk from the tissue to a lower potential.

Each type of stimulator incorporates a switch to control the pulse width of the stimulation. In the case of the current-source stimulator, the switch is connected to the supply and current flows from the supply to the tissue. Conversely, in the current-sink stimulator, the switch is connected to the negative supply, and the current path is from the tissue to the negative supply.

The second type is biphasic stimulation, which consists of two phases. There are five different types of biphasic stimulation, as shown in Figure 5. In biphasic stimulation, the desired physiological effects occur in the first phase, and the second phase applies an opposite-direction pulse shape to remove any remaining residual voltage on the tissue. This stimulation technique significantly reduces tissue damage by using a pulse in the reverse direction. Figure 5(a) shows the first type of biphasic stimulation, known as charge-balanced biphasic, which is widely used to prevent tissue damage.

Figure 5(b) demonstrates charge-imbalanced stimulation, which can prevent electrode corrosion [47]. Ideally, during the stimulation, the charge on the reversal phase should equal the charge involved in reversible processes. In this case, the pre-pulse value of the electrode potential can be restored at the end of the reversal phase. Charge-balanced biphasic stimulation, in addition to preventing electrode corrosion, can also reverse other concerns such as electrochemical processes and some desired physiological effects of the stimulation. It has been shown that this effect increases the threshold in biphasic stimulation compared to monophasic stimulation [46]. To make the threshold similar for biphasic and monophasic stimulation, an open circuit interphase delay between the two phases, as shown in Figure 5(c), was introduced [48]. An interphase delay of 100μs is sufficient to prevent the mentioned effects, including the reversal phase and Faradaic reaction, and improve the threshold of biphasic stimulation [46]. Figure 5(d) and Figure 5(e) depict two other types of charge-balanced biphasic stimulation. In these cases,

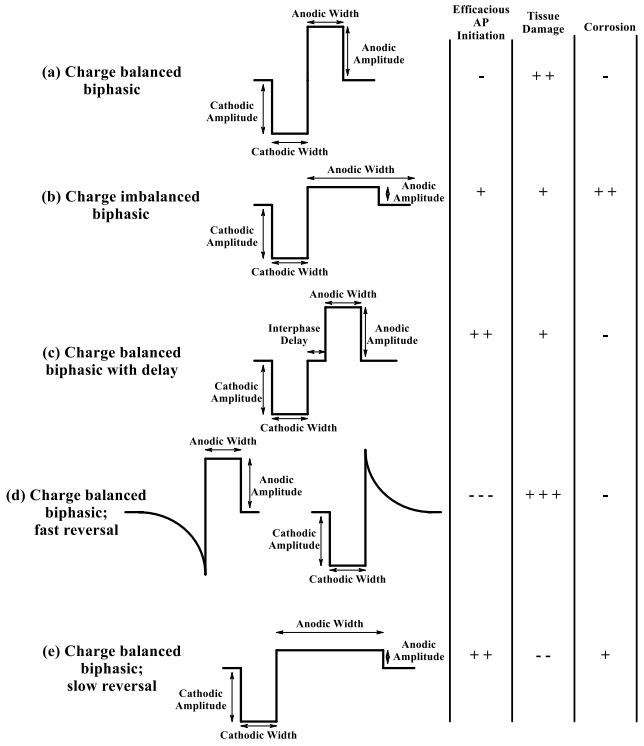


FIGURE 5. Biphasic stimulating waveform [46].

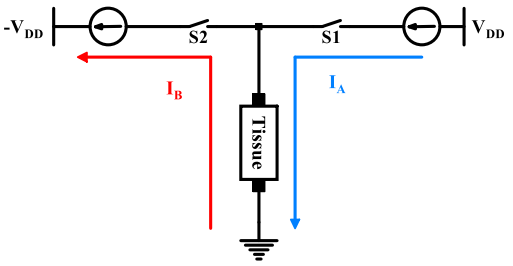


FIGURE 6. Dual supply biphasic current stimulator.

tissue damage is directly related to the discharge time of the reversal phase. Less tissue damage occurs when the tissue rapidly gets discharged in the second phase, which brings the electrode potential out of the negative range. However, a high current in the fast reversal phase can lead to electrode corrosion.

Figure 6 and Figure 7 display two neuro-stimulator structures capable of producing biphasic stimulation. The first structure, known as the dual-supply voltage architecture, is based on sourcing and sinking current, as shown in Figure 6. It includes two current sources connected to positive and negative supply voltages, as well as two switches to control the phases and pulse width of the stimulation. In this type of stimulator, one electrode is connected to the point between the two current sources and switches, while the other electrode, known as the reference electrode, is connected to the reference point (ground). Current can be sourced to the tissue or sunk from the tissue, depending on the stimulation

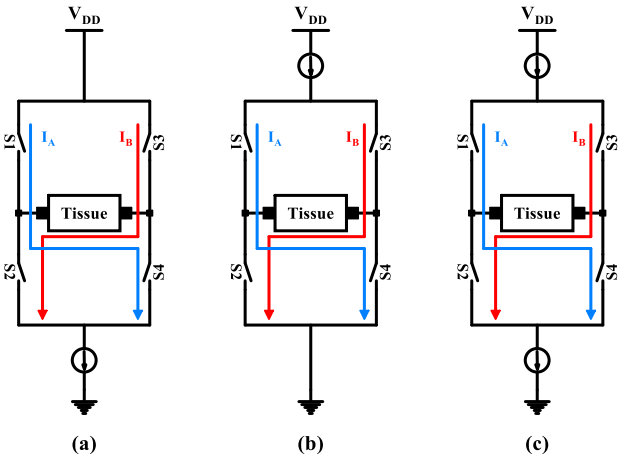


FIGURE 7. Single supply (H-bridge) biphasic current stimulator with: (a) the bottom-side current source, (b) the top-side current source, and (c) both-side current source.

type. The upper switch is turned on to allow current flow to the tissue with a specific pulse width. If an interphase delay is required, the switches are opened. The bottom switch is closed for the next phase, and the current is sunk from the tissue to the negative supply. The dual-supply architecture, with a common ground electrode across the channels, is commonly used in applications requiring multiple electrodes. This technique reduces the number of electrodes to N-1 for an N-channel stimulator.

In the dual-supply structure, voltage compliance is limited by the amount of supplies [49]. Therefore, to achieve high voltage compliance on the tissue, both positive and negative supply voltages need to be increased. However, generating high negative and positive voltages is complex and leads to increased power consumption. To address this issue, another type of stimulator, known as the H-bridge stimulator, was introduced. Figure 7 illustrates the H-bridge stimulator with a single-supply voltage. The H-bridge stimulator requires two electrodes for each channel to produce biphasic stimulation, resulting in a total of 2N electrodes. However, unlike the dual-supply stimulator, there is no need for a negative supply, and the voltage compliance is doubled. In the H-bridge stimulator, biphasic stimulation is generated by switching the current direction. To produce the anodic phase, the switches at the top left and bottom right are closed, allowing the current to pass through the tissue. If an interphase delay is required, all the switches open. For the cathodic phase, the top right and bottom left switches are turned on, enabling the current to flow through the tissue on the opposite side of the first phase. In Figure 7 depicts three types of H-bridge stimulators. The difference between these stimulators lies in the placement of the current source. The current source can be positioned at the bottom, top, or on both sides. Placing the current source on both sides ensures accurate current delivery but requires more area and consumes more power.

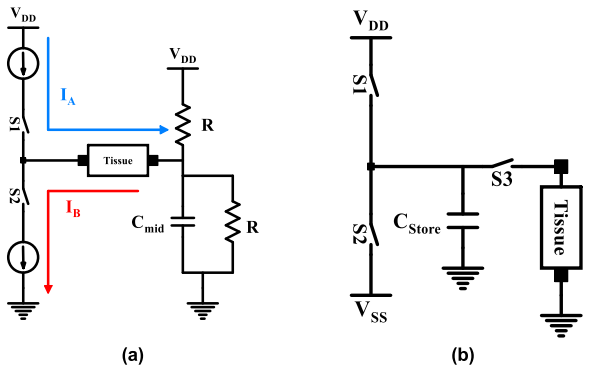


FIGURE 8. Biphasic current stimulators: (a) Using a single supply and generating middle voltage (b) Exponential current generator.

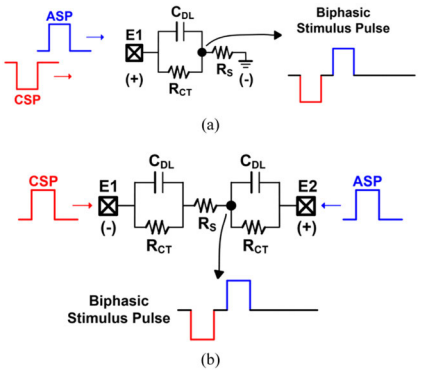


FIGURE 9. Two different configurations for stimulation: (a) Monopolar, (b) Bipolar [31].

Another form of biphasic current stimulator, which uses a single supply voltage and generates a middle voltage, is shown in Figure 8(a) [49]. Generating a middle voltage involves creating a voltage between the positive and negative phases. This middle voltage, often referred to as the common mode or midpoint voltage, is necessary to ensure that the average voltage over time is zero. This helps prevent charge accumulation and minimize tissue damage in specific applications such as neural stimulation. Various approaches exist for generating a middle voltage in biphasic stimulation using a single supply. One common approach is to use a voltage divider or virtual ground circuit to create a reference voltage between the positive and negative supply voltages. This reference voltage can then serve as the common mode voltage for the biphasic stimulation waveform. As shown in Figure 5(d), one of the biphasic stimulation methods is performing exponential waveform, which can be implemented using an RC-based circuit. Figure 8(b) depicts the exponential waveform stimulator, including a capacitor at the output and the switches. In the first step, the capacitor is charged to a specific voltage by activating one of the switches connected to V_{DD} and V_{SS}, depending on the desired rising or falling exponential waveform. In the next step, the capacitor delivers the desired charge to the load by activating the switch between the electrode and the capacitor.

The generation of biphasic stimuli involves different configurations, as depicted in Figure 9 [31], [46]. In the monopolar structure, stimulation is delivered through a single chosen channel. On the other hand, the bipolar method utilizes two channels to stimulate the tissue in opposite directions, typically with a positive supply voltage. The main difference between these two techniques is the generation of negative stimulus pulses. In the monopolar configuration, the cathodic stimulus pulse (CSP) is generated within a circuit operating in the negative power domain. In contrast, the bipolar configuration generates the CSP from another channel operating in the positive power domain, similar to the generation of the anodic stimulus pulse (ASP) in both setups. Monopolar stimulation allows for deep penetration of the electrical current and can cover a large area of tissue. However, it may result in a less focused stimulation and a broader dispersion of current. Bipolar stimulation is commonly used in situations where precise and targeted stimulation is desired, such as in neurosurgery or in the treatment of specific neural disorders. However, this configuration requires larger number of channels and electrodes, which occupies large area. It's important to note that the choice between monopolar and bipolar stimulation depends on the specific application, the desired depth and area of stimulation, and the intended therapeutic objectives. Monopolar stimulation is used in some application such as cardiac pacemakers, spinal cord stimulation, and retinal implants, while bipolar stimulation is employed in deep brain stimulation, cochlear implants, transcranial magnetic stimulation, and functional electrical stimulation.

Another consideration in biphasic stimulation involves the choice of first-anodic or first-cathodic biphasic stimulation. They are two variations of electrical stimulation that differ in the order in which the anodic (positive) and cathodic (negative) phases of the electrical pulse are delivered. The choice between first-anodic and first-cathodic stimulation depends on various factors, including the specific application, target tissue or neural system, and desired physiological response. The order of the phases can influence the activation of neural cells, the direction of current flow, and the recruitment of neuronal populations [46]. Both variations have been studied and utilized in different contexts, including neurostimulation, neuromodulation, and bioelectric therapies. The selection of first-anodic or first-cathodic stimulation is often based on empirical evidence, experimental findings, and clinical considerations specific to the particular application and treatment goals [46].

It is important to note that since the elements to design and implant the stimulator are not ideal, the two phases in charge-balanced biphasic stimulation cannot be perfectly equal. This results in a charge mismatch between the two phases, leading to a residual voltage on the tissue. This residual voltage can cause tissue damage in long-term stimulation and should be mitigated to a safe region. Therefore, an additional circuit should be employed to minimize the charge mismatch on the tissue (further explained in Section III).

Based on mentioned information, the optimal operation principle for Electro-Neural Stimulation (ENS) in medical applications is charge-balanced biphasic stimulation. This involves delivering a positive (cathodic) phase followed by a negative (anodic) phase, ensuring the total charge is balanced. This approach improves safety, selectivity, and long-term reliability of neural stimulation devices used in applications like cardiac pacing, cochlear implants, and deep brain stimulation.

III. STIMULATOR AND STIMULATION DESIGN CONSIDERATIONS

This section outlines the key performance specifications that are essential to consider when designing stimulators and aiming for precise, accurate, and efficient tissue stimulation. By addressing these primary and critical issues, the design of stimulators can be improved to meet the desired objectives effectively.

A. STIMULATOR AND STIMULATION MODE

In ENSs, electrical charge can be delivered to nerve tissues through different modes: constant voltage (CV), constant current (CC), or charge mode (switched-cap), aiming to prevent neural disorders by stimulating the target tissues [50], [51], [52]. Figure 10 illustrates the system-level schematic and current/voltage waveforms for each mode. In the CV mode (Figure 10(a)), the loss can be considered negligible since the voltage is directly applied to the tissue, resulting in high efficiency.

However, the delivered charge to the tissue cannot be controlled due to the change in the impedance of the neural tissue. On the other hand, as illustrated in Figure 10(b), the CC mode has a high accuracy in controlling the delivered charge to the tissue because a constant current directly provides the charge, and its quantity can be governed by the duration and amplitude of the stimulation under impedance changes. In the CC mode stimulation, higher voltage compliance causes more comprehensive current ranges to the tissue.

However, in this mode, due to the use of a current source, the difference between the supply and the electrode voltage causes power to be consumed on the current source. Additionally, the current source needs a minimum voltage for proper operation, which reduces efficiency. In the switched capacitor mode, a capacitor is first charged to a specific voltage for the charge mode and then discharged to deliver the charge to the load. Figure 10(c) depicts this method, which aims to combine the advantages of both voltage and current mode techniques.

By eliminating the headroom voltage of the current source, the switched capacitor mode improves efficiency and provides better control over the delivered charge. However, in this mode, it is not possible to precisely identify the exact stimulus charge, except by limiting the maximum charge amplitude, as the maximum charge delivered is determined by the amount of charge stored in the capacitor.

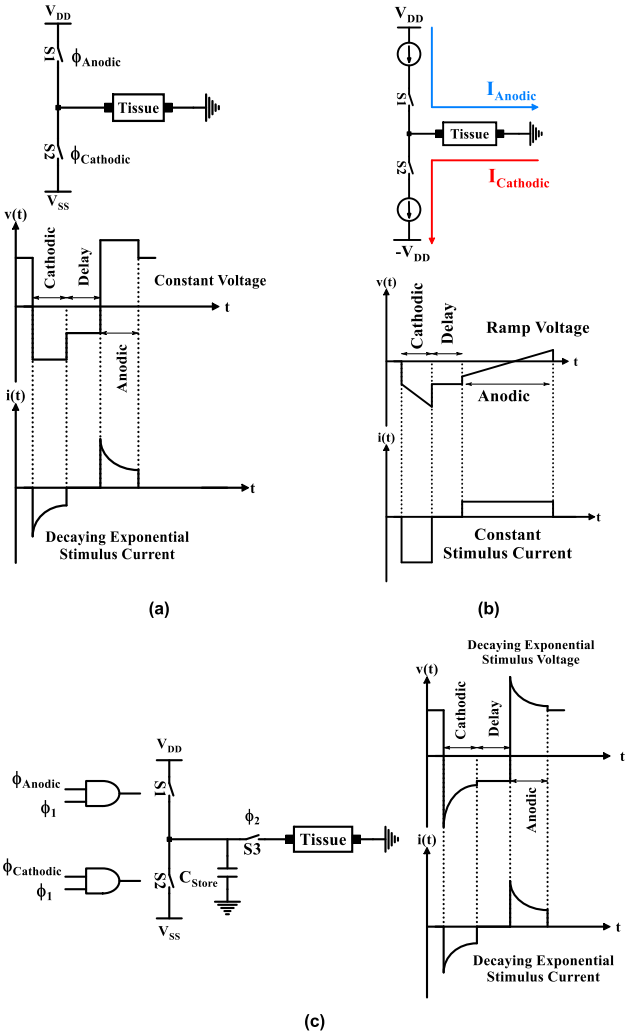


FIGURE 10. Types of electrical charge injection: (a) Voltage mode, (b) Current mode, (c) Charge mode.

B. ELECTRODE-TISSUE MODEL

A simplified electrode-tissue electrical circuit model, comprising a capacitor and resistor, is depicted in Figure 11(a) [46], [53], [54], [55]. C_{dl} (double-layer capacitance) represents the capacitance of the electrical double layer formed at the interface between the electrode and the electrolyte. It quantifies the electrode's ability to induce charge flow in the electrolyte without involving electron transfer. On the other hand, Z_F (Faradaic impedance) represents the impedance associated with the Faradaic processes, which involve electron transfer between the electrode and the electrolyte. These processes typically encompass reduction and oxidation reactions, and the Faradaic impedance reflects the resistance to these electron-transfer reactions. C_{dl} and Z_F are important parameters used to characterize the behavior of electrodes in electrochemical systems. C_{dl} (0.5-1.5 μF) relates to the charge storage capacity at the electrode-electrolyte interface, while Z_F relates to the impedance associated with electron transfer reactions. The electrode

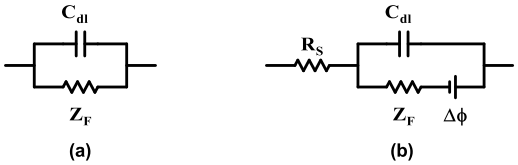


FIGURE 11. Electrode-tissue electrical circuit model: (a) Simple model with two elements, (b) Accurate model [46].

interface model shown in Figure 11(a) illustrates charge injection mechanisms from an electrode. However, it does not consider the equilibrium interfacial potential $\Delta\varphi$ across the interface in equilibrium. Figure 11(b) presents an alternative model that incorporates this aspect. Additionally, R_S models the solution resistance existing between two electrodes in solution. A more comprehensive understanding of the electrochemical system can be achieved by incorporating the equilibrium interfacial potential and the solution resistance into the model. Based on experimental results, R_S typically has a nominal value of 1200 ohms with a variance of 500 ohms due to its variations [56]. These factors provide a more accurate representation of the electrical behavior and performance of the electrodes and electrolyte solution in various electrochemical processes and devices [46].

C. CURRENT LEVEL AND RESOLUTION

The change in current steps represents the resolution of the stimulator current. The difference between each step determines the current resolution, which can vary depending on the application and the specific disease or neural disorder being targeted.

A current DAC is used to control the change in current, and the number of DAC bits determines the current resolution. The designed stimulators can achieve 2 to 10 bits [31], [44], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66]. The maximum stimulation current delivered to the tissue defines the current level in stimulators.

This current level is directly influenced by the supply voltage and tissue impedance. Increasing the supply voltage results in a higher voltage across the tissue; consequently, more current can go through the tissue. To ensure a well-designed stimulator, a suitable range for the tissue impedance is considered [67], and in some cases, a circuit is designed to measure the impedance [43]. The maximum current can be achieved by considering the voltage across the tissue and its impedance. Another crucial aspect is the accuracy of the injected current into the tissue, which is achieved through a well-designed current source and current mirror. The output impedance of the current mirror should be as high as possible to accurately mirror the current. Recent advancements in stimulator design have focused on achieving high currents using both low and high-voltage technologies [39], [68].

D. VOLTAGE COMPLIANCE

Voltage compliance is a critical aspect of stimulator design and operation, referring to the maximum voltage that the stimulator can deliver to the target tissue or electrode without exceeding its operational limits. In medical and neurostimulation applications, where electrical stimulation is used to modulate neural activity or treat medical conditions, voltage compliance plays a crucial role [44], [57], [69], [70].

One of the factors influencing voltage compliance is the impedance of the tissue-electrode interface. The resistance of the electrodes used and the tissue impedance can be high, necessitating a high voltage on the tissue, known as voltage compliance, to achieve the desired current flow. For example, in certain applications, electrodes with a resistance of 100 kΩ may require a 10V voltage across the electrodes and tissue to deliver a current of 100 μA. It means that more current needs more voltage compliance. Consideration of voltage compliance is essential in electrical stimulation systems to ensure both the safety and effectiveness of the stimulation. Increasing the supply voltage can enhance voltage compliance, but it is necessary to consider specifications for the components used in the stimulator design, such as voltage tolerance, to prevent device damage.

The voltage compliance limit is typically set based on the characteristics of the target tissue and the desired stimulation parameters. It is influenced by various factors, including the tissue type, cellular composition, and the specific stimulation parameters used. For example, smaller-diameter nerve fibers require lower stimulation voltages compared to larger fibers. Additionally, factors like stimulation frequency, electrode configuration, and the distance between the electrodes and target tissue can also affect the optimal voltage range. Table 1 shows the voltage compliance limits for different tissues in the body when using electrical stimulation [83]. Exceeding the voltage compliance limit can lead to various issues, including tissue damage, unwanted side effects, or even electrical breakdown in the stimulator circuitry. Stimulators often incorporate safeguards such as voltage limiters or current-limiting circuits to prevent exceeding the voltage compliance. These safety features monitor the output voltage or current and automatically adjust or terminate the stimulation if the limits are exceeded. Proper configuration of the voltage compliance settings, based on the specific requirements of the stimulation application, and adherence to the guidelines and recommendations provided by the stimulator manufacturer are crucial to ensuring safe and effective stimulation. This ensures that the stimulation is delivered safely and effectively, minimizing the risk of adverse effects and maximizing the therapeutic benefits of electrical stimulation.

E. EFFICIENCY

The efficiency of a stimulator refers to its ability to convert electrical power into the desired output, typically in the form of electrical stimulation. The efficiency (η_{eff}) from the power source to the tissue is calculated as [71]

$$\eta_{eff} = \frac{I_{STIM} \times V_{supply}}{P_{total}} \tag{1}$$

TABLE 1. Voltage compliance limits for different tissues in the body.

Tissue	Voltage Compliance Limit (V)	Factors Affecting Limit
Nerve	10-15	Nerve fiber diameter, myelination, stimulation frequency
Muscle	5-10	Muscle fiber type, stimulation frequency, muscle length
Heart	5-10	Cardiac tissue type (atrial vs ventricular), stimulation timing
Brain	1-5	Brain region, neuronal density, blood-brain barrier integrity
Retina	1-3	Retinal cell type, distance from epiretinal/subretinal electrodes
Cochlea	1-3	Hair cell type, distance from intracochlear electrodes
Spinal Cord	5-10	Spinal cord region, fiber tracts, stimulation parameters
Skin	10-50	Skin thickness, hydration, stimulation electrode configuration

where I_{STIM}, V_{supply}, and P_{total} indicate stimulation current, supply voltage, and total consumption power. It is an important parameter to consider in electrical stimulation systems, as higher efficiency results in the more effective power utilization. There are two ways to supply the stimulator: using a battery or a coil for wireless power transfer. When a battery is used, higher efficiency improves the battery's lifetime, reduces its size, and minimizes heat generation. Conversely, when a coil is employed, improving efficiency directly contributes to reducing the size of the power coil. Several key factors can affect the efficiency of a stimulator [71], [72]. The first factor is power conversion, which measures how effectively electrical energy is converted from the power source into stimulation output. High power conversion leads to minimized losses and improved efficiency. Another important parameter is impedance matching between the load and the stimulator's output, which maximizes power transfer to the load and reduces power losses. Proper circuit design, component selection, and topology play a significant role in enhancing stimulator efficiency. Control Algorithms are another factor that can impact efficiency. The control signals should optimize stimulation parameters based on the desired therapeutic effect. Adjusting stimulation parameters, such as time interval, interphase delay, pulse width, etc., contributes to improved efficiency. Lastly, the stimulation waveform, as explained in Section II, is another key parameter that can affect stimulator efficiency [46], [73], [74].

F. SPIKES

During the switching procedure, the parasitic elements can cause unexpected issues. When a transistor is used as a switch, Source and Drain inductance are parasitic elements restricting switching performance. During the switching off process, the instantaneous rate of change in current over time (di/dt) can be high. According to the equation $v = L \bullet di/dt$, the high variation in di/dt can result in significant turn-off spikes. These voltage spikes can lead to instantaneous current spikes that cause discomfort or pain for patients undergoing stimulation. Additionally, high-amplitude voltage spikes can generate sharp sensations or even result in tissue damage [21], [39], [75], [76]. Furthermore, these spikes can cause the potential differences across the transistor terminals to exceed their maximum tolerable range, resulting in damage to the transistors (switches). The presence of spikes can also impact the accuracy and consistency of the stimulation waveform, leading to a reduction in efficiency. Moreover, spikes in the stimulation waveform can influence other nearby electronic devices, causing some conflicts that should be prevented. Reducing and mitigating these unwanted spikes at the stimulator output requires considering some solutions. Decreasing the switching speed for a smooth transition is one solution leading to reducing di/dt and consequently minimizes the buildup of charge as well as the levels of voltage and current spikes [75]. Other solutions include filtering the output and employing proper circuit design techniques [76].

G. POWER AND AREA

Reducing power consumption and size are two critical challenges in stimulator design. In stimulators, certain elements and voltage drops contribute to power consumption, while the remaining power is dissipated as heat. Minimizing heat dissipation is crucial for decreasing power consumption and improving power efficiency [36], [37], and [38]. High-voltage technology is one approach to design a stimulator that can handle high currents and avoid design complexity [12], [44], [57], [77], [78], [79]. However, this approach leads to increased power consumption and large area. To address this issue, low-voltage technology can be employed, and stacked structure can be utilized to achieve high currents and voltages on the tissue [18], [26], [80], [81], [82]. The use of low-voltage technology topologies reduces power consumption and occupies a smaller area.

H. SAFE STIMULATION

A critical concern in neural stimulators is ensuring safe long-term electrical stimulation. Safe stimulation is an essential consideration in electrical stimulation systems, particularly in medical and neurostimulation applications [83], [84]. It aims to ensure the safety, efficacy, and durability of the stimulation while minimizing potential risks and adverse effects. It is crucial to avoid any situation that could lead to an accumulation of charge on the tissue exceeding the safe threshold, as this can result in tissue damage [40]. Safe stimulation involves delivering electrical currents or pulses within established safety limits to prevent tissue damage, discomfort, or unintended side effects. The specific safety limits depend on various factors, including the characteristics of the target tissue, the stimulation parameters, and

the intended purpose of the stimulation. Understanding the electrical properties and thresholds of the target tissue is crucial in designing the stimulation parameters accordingly. This includes determining appropriate voltage, current, pulse duration, frequency, and waveform characteristics to achieve the desired therapeutic effect while avoiding harm.

To address these concerns, the charge-balanced biphasic method is often employed to reduce the residual charge on the tissue, prevent tissue damage, and ensure a safe stimulation. Imbalances in charge delivery can lead to harmful electrochemical reactions, tissue damage, or electrode degradation. The use of charge-balancing circuits has become widespread in stimulators to ensure the delivery of equal amounts of positive and negative charge over time, reduce charge mismatch, and achieve a safe stimulation region [39], [45], [58], [62], [66], [69], [85], [86], [87], [88], [89], [90], [91], [92], [93], [94], [95], [96], [97]. Implementing safe stimulation and charge balancing requires a comprehensive understanding of the electrical properties of the target tissue, careful selection of stimulation parameters, appropriate electrode design, and adherence to established safety guidelines and standards. Researchers, clinicians, and device manufacturers must consider these factors to ensure the effectiveness and safety of electrical stimulation therapies.

I. CHANNEL NUMBERS

Channel number in neural stimulators is a critical feature that determines the level of control and specificity achievable in the stimulation process. Each channel represents an independent pathway through which the stimulator can deliver stimulation. Having multiple channels allows the stimulator to independently inject stimulation currents into different regions of neurons, with varying parameters such as pulse amplitude, frequency, and width. The number of channels in an electrical neural stimulator depends on the specific application. Some stimulators may require only one or a small number of channels [10], [21], [39], [72], while others may have dozens or even hundreds of channels for more complex and fine-grained stimulation patterns [36], [43], [44], [57]. In some cases, such as stimulator in [43], a massive number of channels were used to target the cortical neurons, which occupied an area of 4.48×2.43 mm^2.

The increase in the number of channels has a significant impact on the performance and various parameters of the ENS. Higher channel counts enhance the accuracy, precision, and localization of the stimulation effect. It allows for more precise positioning of the electrical field and enables better control over the stimulation process. The number of channels in a neural stimulator is closely related to its recording capabilities. Many neural stimulators include neural recording functionality [18], [36], [43], [81], which enables simultaneous stimulation and recording of neural activity. The channels in neural stimulators can be utilized to record electrical signals from neural tissue. With a high number of channels, the stimulator can capture signals from many neurons or different regions simultaneously, providing a more comprehensive monitoring of neural activity. It is important to note that the number of channels for recording part may not always be the same as the number of stimulation channels in an ENS. Different channel counts for stimulation and recording can be implemented based on specific application requirements and design considerations.

It is worth mentioning that this subsection provides a brief explanation of the importance of channel numbers and the recording part, which is not included in this review. The review focuses on the stimulator circuits and their related aspects.

IV. NEURO STIMULATOR DESIGN APPROACHES

In this section, the main approaches to ENS will be discussed. This section will explain the structures and topologies used in the introduced ENSs. This section will review and discuss the primary challenges, advantages, and disadvantages associated with the ENS implementations.

A. THE OUTPUT STAGE AND CURRENT DRIVER APPROACHES AND CONSIDERATIONS

The first step in designing any circuit is selecting the appropriate technology. Each technology has limitations regarding the maximum supply voltage and the voltage tolerated by its elements. In ENSs, the output stage driver plays a crucial role in delivering the current to the tissue. The voltage compliance and output current in ENSs are determined by the characteristics of this output stage, making the choice of technology essential, as the current and voltage compliance directly depend on the supply voltage. Other essential components in ENSs include the current source, current DAC, and current mirror, which generate the desired current amplitude for the output stage. Therefore, selecting the appropriate technology that aligns with the desired current and voltage compliance for the specific application poses a significant challenge in the initial stages of ENS design. High-voltage CMOS [12], [19], [21], [38], [44], [57], [58], [59], [60], [61], [62], [68], [69], [78], [86], [89], [98], [99], [100], [101], [102], [103], [104], [105], [106], [107], [108], [109], [110], [111], [112], [113] and low-voltage CMOS [18], [31], [36], [39], [45], [63], [64], [65], [66], [71], [72], [75], [76], [80], [81], [82], [87], [90], [92], [106], [114], [115], [116], [117], [118], [119], [120], [121], [122], [123], [124], [125], [126], [127], [128], [129], [130], [131], [132], [133], [134], [135], [136], [137], [138], [139], [140], [141], [142], [143] technologies have been widely employed in many introduced ENSs. In some cases, other technologies such as BJT [98], BCD [106], [144], and BiCMOS [87], [145] have also been utilized. Additionally, discreet circuits have been designed using pre-designed stimulator chips [146], [147], [148], [149], [150], [151], [152], [153].

Many designed ENSs have utilized high-voltage CMOS technology to overcome the limitations of supply and tolerated voltage. In recent developments, BCD technology has also been employed for ENSs. These technologies enable operation at voltages higher than the standard voltage for

the specific technology and offer increased device resistance under higher voltages. Notably, this voltage can grow to 38V [61] and 49V [94], providing the tissue with higher current and voltage compliance. The high current levels of 16mA [78] and 150mA [151] have been achieved. All of the presented ENSs in the literature employ biphasic stimulation, which is preferred due to reduced charge mismatch, safe stimulation, and prevention of tissue damage [46]. Two common structures have been used in these stimulators to generate biphasic stimulation. The first approach involves a dual supply prototype or sourcing/sinking-current methods [31], [36], [38], [44], [45], [57], [59], [61], [62], [66], [69], [78], [86], [87], [89], [90], [102], [116], [118], [119], [121], [132], [133], [140], [144]. The second approach uses a single supply method with a single/dual current source, known as the H-bridge output stage [12], [18], [21], [39], [58], [63], [65], [71], [72], [73], [74], [75], [76], [82], [101], [104], [108], [111], [113], [115], [122], [130], [141], [142], [143]. These two approaches were illustrated in Figure 6 and Figure 7.

Since the output resistance of the current mirror is crucial for accurately mirroring high currents, two types of high-output resistance current mirrors are commonly used in ENSs. The first type is the cascode current mirror [18], [21], [31], [38], [39], [44], [57], [59], [63], [65], [66], [71], [78], [82], [87], [89], [90], [101], [102], [115], [118], [122], [130], [133], [135], [144], as depicted in Figure 12(a). The second type is the high output impedance current mirror based on the gain boosting technique [12], [45], [58], [61], [62], [68], [69], [75], [76], [86], [104], [108], [116], [119], [121], [123], shown in Figure 12(b). In some designs, the modified version of these two common structures have been employed [38], [61], [62], [68], [99], [105], [123], [135], [136]. To reduce the size of the DAC transistors, the output transistors of the current mirror are appropriately sized to mirror n$\times$ I_{DAC}. The output resistance of the cascode current mirror and gain boosting technique can be expressed as follows:

$$R_{out} \cong g_{m4} r_{ds3} r_{ds4} \tag{2}$$

$$R_{out} \cong g_{m4} r_{ds3} r_{ds4} (1 + A) \tag{3}$$

where g_{m4}, r_{ds4}, r_{ds3}, and A are transconductance of M_4, output resistance of M_4, output resistance of M_3, and DC gain of the Op-amp, respectively. These architectures are employed for both sinking and sourcing the current to the tissue in ENSs. At the output of the current mirror, there are switches that control whether the current is sourced to the tissue or sunk from the tissue. These switches play a crucial role in directing the flow of current and providing control over the stimulation process. By appropriately configuring these switches, the ENS can deliver the desired current waveform and achieve the desired stimulation effect.

In addition to controlling the direction of current flow, these switches also play a role in controlling the pulse width and period of biphasic stimulation in ENSs. Depending on the design, there are two different approaches for implementing

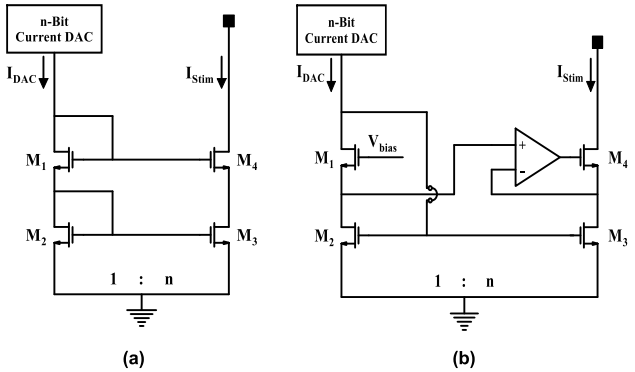


FIGURE 12. High-output resistance current mirror: (a) Cascode current mirror (b) Gain boosting technique.

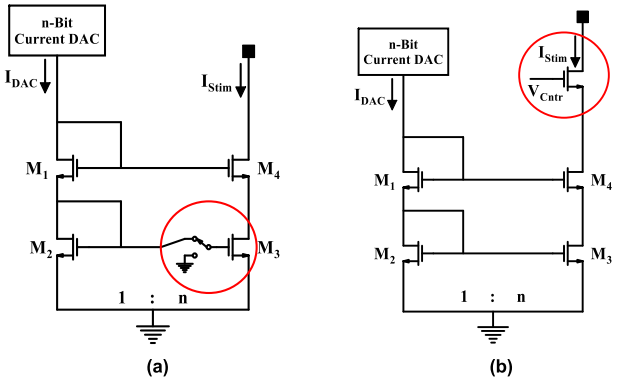


FIGURE 13. Current mirror with switch using: (a) A transistor in the current mirror (b) An extra transistor.

these switches. In some designs, the bottom transistor at the output of the current mirror can act as the switch, effectively controlling the current flow to the tissue. Alternatively, in other circuits, an additional switch is placed between the output of the current mirror and the tissue, providing further control over the stimulation parameters. Figure 13 illustrates these two types of switches. The two types of current mirrors mentioned earlier can also be utilized in the H-bridge structure shown in Figure 7. These current mirrors can be positioned at the top using PMOS transistors or at the bottom using NMOS transistors, depending on the specific implementation. Figure 14 depicts an H-bridge-based stimulator with the current mirror positioned at the bottom.

It's common to use low-voltage transistors in high-voltage ENS systems for components other than the output stage to decrease the cost, occupied area, and power consumption. Consequently, a low-voltage to high-voltage shifter is employed to achieve the high voltage for the output stage. This level shifter is designed using low-voltage technology and serves the purpose of generating the necessary high voltage to control the switches in the output stage. By using this level shifter, the ENS system can operate with low-voltage transistors for most of its components while still achieving the desired high voltage at the output stage.

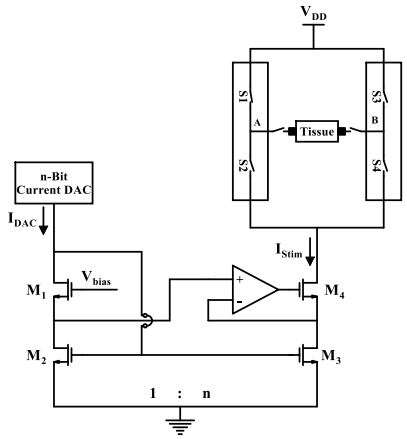


FIGURE 14. H-bridge-based stimulator with the current mirror.

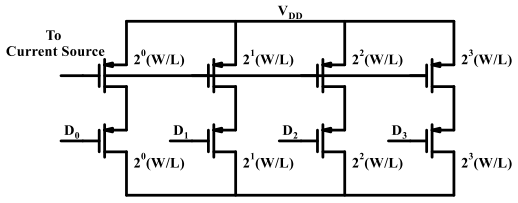


FIGURE 15. The 4-bit current mode DAC.

As mentioned earlier, a current DAC is utilized to control the current level in ENSs. A commonly used 4-bit current DAC, which can be found in many ENS designs, is depicted in Figure 15. The number of bits (N) in the DAC can vary from 2 to 10, depending on the current resolution of the circuits [31], [44], [57], [58], [59], [60], [61], [62], [63], [64], [65], [66]. In Figure 15, the sizing of the transistors is chosen based on a multiple of 2^n, where n ranges from 0 to N-. This means that the transistors are sized from $2^0 \times \frac{W}{L}$ to $2^{N-1} \times \frac{W}{L}$, where W and L represent the width and length of the transistors, respectively. By carefully selecting the transistor sizes according to this scaling factor, the desired current can be achieved. Furthermore, the upper PMOS transistors have their gates connected to the current source, while the digital code controls the bottom transistors to generate the desired current. This configuration allows for precise control of the current output based on the digital input.

As previously mentioned, the high-voltage technology offers advantages such as less design complexity, increased reliability, and tolerance to higher voltages. However, it also comes with drawbacks such as larger occupation areas, higher cost, and increased power consumption, which are significant concerns in implantable devices. Consequently, low-voltage technology has emerged as an alternative solution to address these issues. Many ENSs have been designed using low-voltage technology, employing the same topology for the output stage. This includes the single supply configuration with a current source or the double supply configuration with both sinking and sourcing of the current. The current mirror and current DAC used in these low-voltage ENSs are similar to those utilized in the high-voltage technology, as shown in Figure 11 and Figure 14. However, it is important to note that the low-voltage transistors used in these designs have limitations in terms of supply voltage and voltage tolerance. As a result, the proposed low-voltage ENSs may not support high-voltage compliance or high current output.

To overcome this limitation, some designs have employed larger technology nodes, such as 2μm [115], 1.5μm [116], 1.2μm [114], [131], [133], 1μm [117], 0.6μm [87], [134], 0.5μm [121], and 0.35μm [119], [128]. Applying this technology can enhance the tolerated voltage for transistors to 6.5V, increasing the voltage compliance to 5V [116]. Depending on the specific application and tissue impedance, the current varies from 50μA to 1.3mA in these ENSs [121]. It is important to note that even with the application of mentioned low-voltage technologies, the voltage compliance and current capabilities may still be insufficient. Moreover, these low-voltage technologies often occupy significant areas, further adding to the limitations of the designs.

Using a CCII (Current Conveyor II) current conveyor for the output stage of ENSs is a solution to overcome the aforementioned problems [123]. The circuit employs a class-B second-generation current conveyor and digitally programmable time constants and DACs to generate exponential current pulses for stimulation. This approach offers more versatility and control over stimulation waveforms compared to traditional rectangular pulses. The exponential current pulses are generated by controlling the charging and discharging of a capacitor. The capacitor is connected to the output of the current conveyor. When the input current to the current conveyor is high, the capacitor charges exponentially. Conversely, when the input current is low, the capacitor discharges exponentially. Adjusting the time constants of the charging and discharging processes can control the rise and fall times of the exponential pulses. In the presented circuit, two modified gain-boosting current mirrors were used to design the current conveyor [154]. Figure 16 shows the modified current mirror and the current conveyor. The output resistance for the modified current mirror can be written as

$$Rout = A_2 g_{m2} g_{m4} r_{o1} r_{o4} R_{oCS} \tag{4}$$

where R_{oCS} is the output resistance of the current source. Based on the equation mentioned, the output resistance increased significantly, which resulted in a more accurate output current. Using the current convey in the output stage offers several advantages over other low-voltage techniques, including low power consumption, high dynamic range, and improved voltage compliance [155]. However, despite these benefits, the proposed stimulator still faces challenges related to low voltage compliance and output current. These limitations indicate that the stimulator may not be able to provide sufficiently high voltage levels or deliver the desired output current for certain applications or requirements.

To address the issues of low voltage compliance and output current, the stacked transistor method has been introduced in

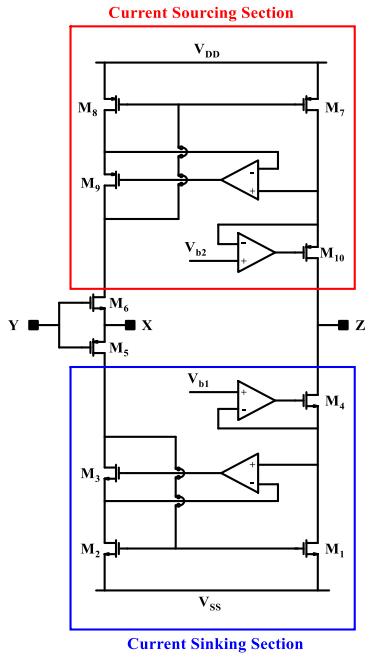


FIGURE 16. Circuit schematic of proposed class B CCII [123].

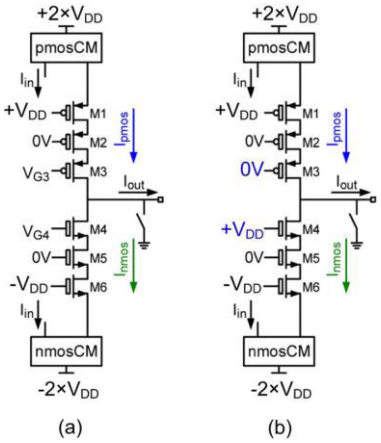


FIGURE 17. Stacked method for transistors in the output stage [36].

the output stage to increase voltage compliance, particularly in smaller-size technologies like 180nm and 65nm [18], [36], [39], [63], [66], [71], [72], [75], [76], [81], [122], [124], [142]. This technique can be applied to any device by stacking multiple transistors, effectively increasing the supply voltage. Using this concept can make the circuit fully integrated with the digital control unit in a digital process without needing any extra technology. However, in these designs, it is necessary to set dynamic bias voltages for each phase of stimulation. The dynamic bias voltages must be adjusted according to the specific requirements of each stimulation phase. This ensures proper operation and control of the circuit throughout the stimulation process.

Figure 17 shows an example stimulator that utilizes the stacking technique [36], [39]. As illustrated in Figure 17, the gate voltage of transistor M_3 is set at 0 and $-V_{DD}$ during the anodic and cathodic phases, respectively. In this kind of stimulator, since the output of the stimulator may be shorted to the positive or negative power supply by accident, some failures can happen because the voltage drop between two terminals of the transistors goes beyond the standard value [39]. Therefore, for considerations of device reliability, setting the dynamic bias voltage based on the stimulation phases is not an appropriate choice. To address this issue, a self-adaption bias circuit has been introduced to control the stimulator and overcome the mentioned limitations [39]. Figure 18 depicts the proposed circuit, representing half of the stimulator. In this circuit, four stacked transistors are utilized as the pull-up and pull-down switches. This configuration enables the switches to tolerate four times the standard supply voltage without compromising device reliability.

The self-adaption bias circuit was performed to regulate the voltage between stacked transistor terminals, ensuring that the voltage drop across them remains within the nominal supply voltage range of the technology. Two voltage dividers, including NMOS transistors M_{BN1-4} with resistors R_{5-8} and PMOS transistors M_{BP1-4} with R_{1-4}, provided the desired voltage for different part of the circuit and ensured specific gate voltages for certain transistors. A non-overlap clock generator is employed as an input for the level shifter, which controls the output stage to prevent short-circuit currents. The level shifter converts low-level voltage to a high-level voltage with a DC offset of 3 times V_{DD} [39]. The self-adaptive bias circuit is implemented to maintain voltages within the nominal supply voltage limits, including for transistors M_{B1-6}. Since the bodies in transistors M_{B6} and M_{B7} are connected to the drains (n_7 and n_9), if the voltage at n_7 tends to decrease below than $2V_{DD}$ or the voltage at n_9 tends to increase beyond than $2V_{DD}$, the parasitic diodes will turn on and fix n_7 and n_9 to $2V_{DD}$. Transistors M_{B1-4} then control the voltage of the transistors in the output stage based on these procedures and the node voltages. Transistor stacking with self-adaption or dynamic bias has been widely used in various designs to overcome technology limitations and achieve higher voltage compliance and, consequently, higher current [18], [39], [63], [71], [72], [75], [76], [81], [122], [124], [142]. The 180nm CMOS process is often chosen for stimulator design due to its reliability and lower cost compared to deep sub-micron low-voltage technologies [18], [31], [39], [63], [65], [66], [71], [72], [75], [80], [81], [82], [92], [120], [122], [124], [132], [142], [143], [144]. Other technologies, such as 130nm [64], [90], [123] and 65nm [36], [45], [63], [76], [129], have also been used, with the use of 2.5V/3.3V voltage transistors to achieve higher voltage compliance. While low-voltage technology offers advantages in terms of power consumption, cost, and occupied area, it also presents complexities and challenges in implementing the stimulator.

Figure 19 provides a comparison of three different methods used to design the stimulator, based on the reported

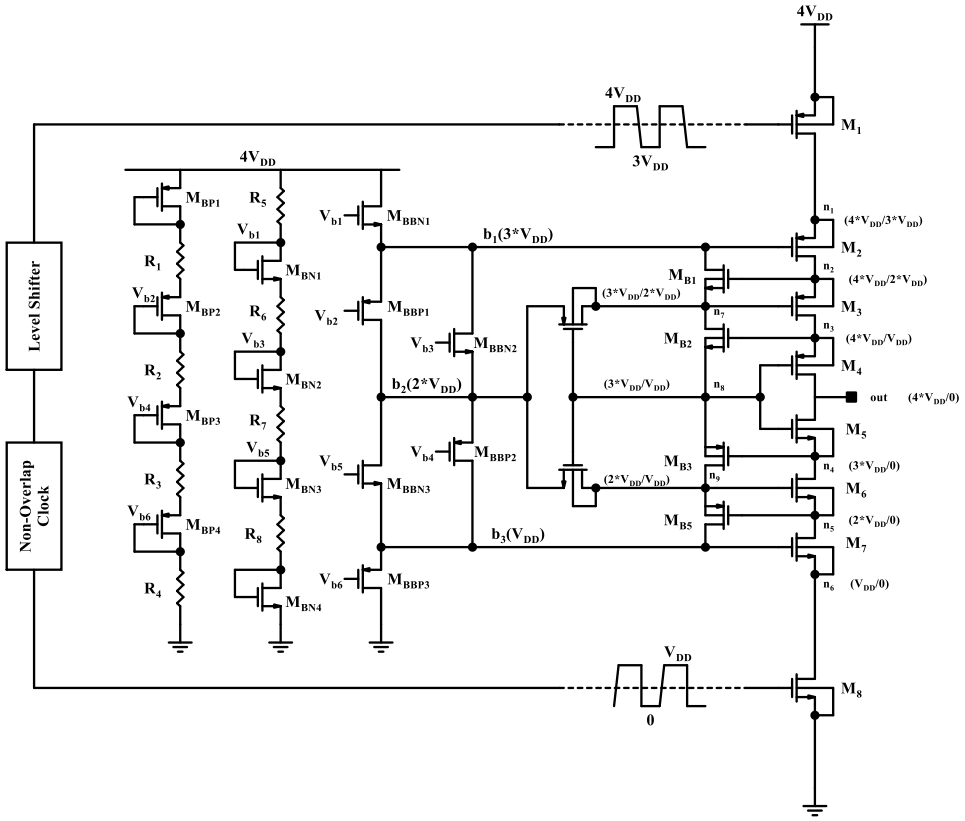


FIGURE 18. Proposed stimulator using stacked transistor and self-adaption bias [39].

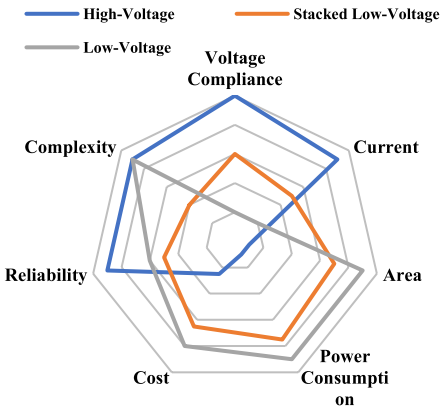


FIGURE 19. Comparison of three applied methods for the stimulator output stage.

results. The comparison takes into account several parameters, including voltage compliance, current, occupation area, power consumption, cost, reliability, and design complexity are compared. The performance of each method is evaluated and presented in Figure 19. According to the illustration in Figure 19, it can be observed that high-voltage circuits outperform the other two methods in terms of voltage compliance, current, and reliability. These high-voltage circuits are capable of meeting the required voltage levels and delivering higher currents. However, they exhibit drawbacks in terms of cost, occupation area, and power consumption. On the other hand, the stacked low-voltage and low-voltage methods show better performance in terms of power consumption, occupation area, and cost. These methods are able to reduce power consumption, occupy less area on the integrated circuit, and are relatively more cost-effective. The design complexity for both high-voltage and low-voltage methods is similar, while the stacked structure introduces additional complexity to the circuit design.

B. SPIKE AND VOLTAGE EXCEEDING CONSIDERATION

As discussed, the drain-source voltage (V_{DS}) may exceed the nominal voltage (spikes) when the transistor switches from 0V to V_{DD} or V_{DD} to 0V. This issue becomes more critical when the current is high. Thus, since the output stage is responsible for the stimulation current, the spikes and removing them are crucial concerns, especially in high-current stimulators. The spikes become more severe while using a low-voltage process because of limitations in tolerated voltage. Figure 20 illustrates the stimulation profile and spike-removing technique in [21] using a dummy load. The technique utilizes a dummy load in addition to the cathodic and anodic phases in the stimulation profile. After each phase, the switch connected to the dummy load is

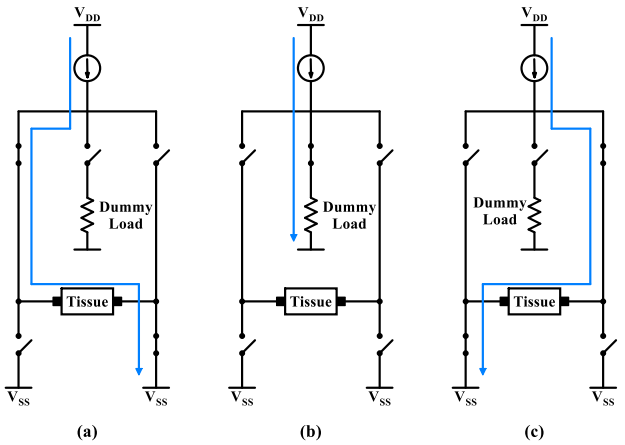


FIGURE 20. Stimulator prototype and stimulation phases: (a) Cathodic current path, (b) Current path to dummy load, (c) Anodic current path [21].

closed, redirecting the current towards the dummy load. This approach helps achieve a smooth transient response, minimizing charge buildup and spikes. However, this structure occupies more area and can produce thermal noise because of the resistor.

In low-voltage technology, especially when the stacked transistors are performed, these spikes happen during the ON to OFF and OFF to ON procedures. In this situation, to mitigate these spikes and maintain the drain-source voltage (V_{DS}) within a safe region, the transition time of the ON/OFF control pulse should be appropriately selected [39]. If we consider the transition time (fall/rise time) of the input signal for the switches as T, the approximate expression for V_{DS} (or V_{SD}) of each switch in the stacked method can be written as [39]

$$V_{DS} = \pm\frac{NV_{DD} - (N-1)V_{DD}}{T}t + NV_{DD} - (I_D R_t + \frac{I_D}{C_t}t) \tag{5}$$

where N is the number of stackings, I_D is the drain current, R_t is the total resistor seen from the drain, and C_t is the total capacitor seen from the drain. The negative or positive sign the context mentioned indicates whether the level is increasing or decreasing. According to (5), the rise/fall time should be adjusted suitably. One method to drive the switches, increase the transition time, and consequently prevent spiking is using a chain of scaled inverters known as taper [71], [75]. Another technique to prevent overvoltage in V_{DS} during current conduction is by properly sizing the stacked output transistors introduced in [76]. The sizing of transistors is determined by considering the highest current level used for stimulation, which corresponds to the transistor with the most significant voltage drop. The transistors should be sized in such a way that the V_{DS} remains below the maximum voltage tolerated by the technology.

C. CHARGE BALANCING APPROACHES AND CONSIDERATIONS

One of the primary considerations in the design of stimulators is the assurance of safe long-term electrical stimulation. It is crucial to prevent tissue damage by avoiding the delivery of a net charge that exceeds a certain threshold. To mitigate the risk of tissue destruction, charge-balanced biphasic stimulation pulses are commonly employed. Charge-balanced biphasic stimulation pulses are designed to deliver equal amounts of positive and negative charge over time. By ensuring that the net charge is balanced, the stimulator minimizes the potential for harmful electrochemical reactions at the electrode-tissue interface. This helps maintain the safety and integrity of the stimulated tissue during electrical stimulation.

There are two general approaches to achieving charge balance in electrical stimulation: passive and active charge balancing. Passive charge balancing involves large DC-blocking capacitors that are inserted in series with each electrode [89], [101], [108], [115]. These capacitors serve to remove the residual DC voltage to balance the net delivered charge. However, due to their large size, these capacitors are typically implemented off-chip and cannot be fully integrated with the stimulation circuitry. This limitation presents challenges in the development of multichannel implantable stimulators. To overcome the limitation of off-chip capacitors, the High-frequency current switching (HFCS) technique has been proposed. This technique utilizes two high-frequency clocks with a phase difference of 180° [86], [103], [104]. The value of the DC-block capacitor in the stimulator can be expressed as

$$C = I_{stim}\frac{\Delta T}{\Delta V} \tag{6}$$

where I_{stim} is the stimulation current, ΔT is the pulse width, and ΔV is the voltage variation of the capacitor. According to equation (6), since $\Delta T \alpha 1/f$, if the frequency increases, the value of the capacitor will decrease. Figure 21 illustrates the HFCS topology, which enables on-chip integration by utilizing two small capacitors in the picofarad range. The circuit operates as follows during different clock phases. For phase φ_1, S_1 is closed, and S_3 and S_L are open. In this phase, D_1 is reversed-biased, while D_2 is forward-biased. The constant current I_{stim} passes through C_1 and D_2, resulting in current flow through the load (I_{s1}). Simultaneously, S_2 will be open, S_4 will be closed, and D3, S4, and C2 will create a loop for discharging C_2 to one diode voltage drop. For phase φ_2, the circuit operates like the first phase, generating current I_{s2} flow through the load and discharging loop for C_2. This alternating charging and discharging of the two blocking capacitors continue throughout the cathodic phase, resulting in the generation of the cathodic current by the summation of these high-frequency currents. During the final clock phase, the load switch is closed, and all other switches are open, allowing for the passive discharge of the load and forming the anodic phase.

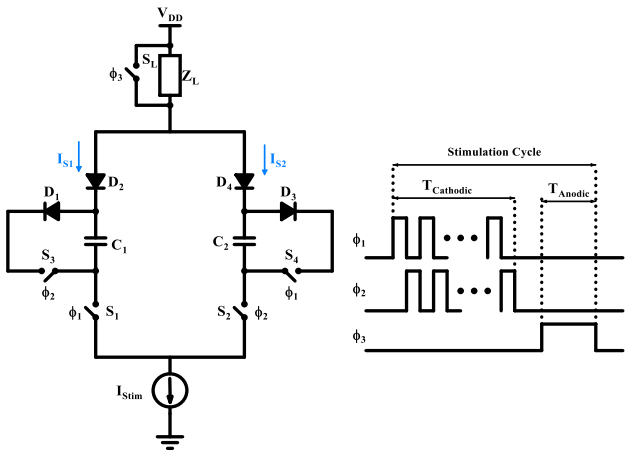


FIGURE 21. HFCS topology for Stimulator [86].

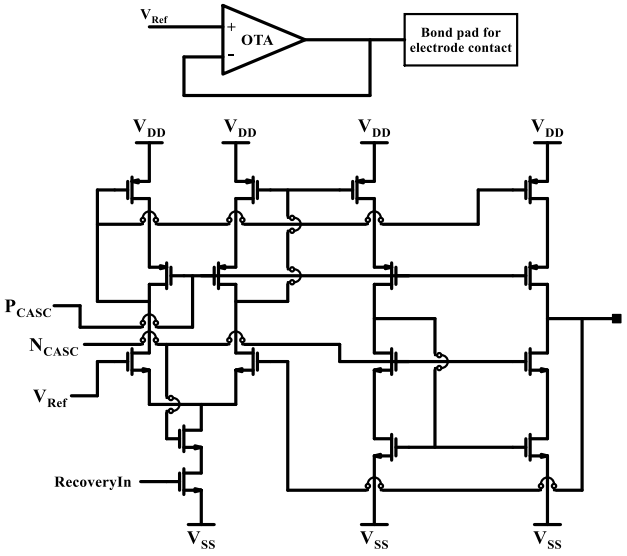


FIGURE 22. Using buffer as a limiter for charge balancing [87].

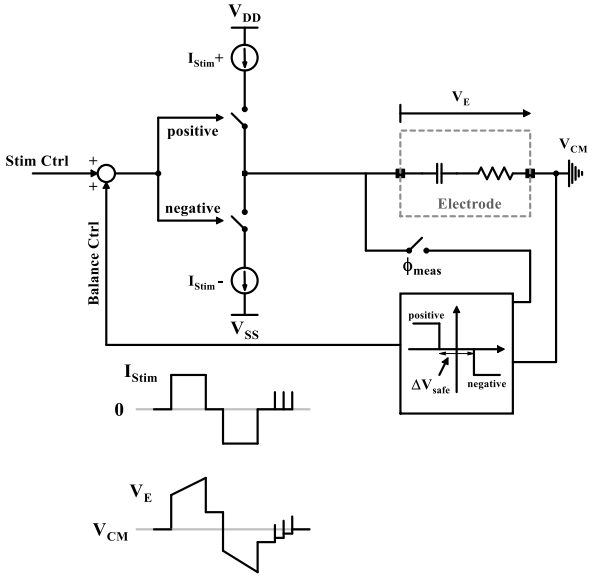


FIGURE 23. Pulse insertion technique for charge balancing [88].

Several charge-balancing methods based on electrode shorting have been implemented in [12], [21], [31], [36], [45], [57], [58], [61], [62], [65], [75], [76], [82], [116], [119], [122], [126], [130], [141], and [142]. In this approach, the electrodes are shorted for a specific duration after stimulation. However, the exact discharge time cannot be determined precisely due to factors such as unknown current mismatch and varying electrode impedance. It is important to note that this approach is often used in combination with other active charge balancing techniques to achieve better performances in terms of charge mismatches.

Active charge balancing circuits have been proposed in various studies. including those referenced in [36], [38], [39], [44], [59], [60], [63], [65], [68], [69], [70], [76], [82], [87], [90], [91], [92], [121], [126], and [130]. These circuits employ different techniques to achieve charge balance. The specific techniques utilized may vary across studies, but the overall goal is to actively monitor and adjust the charge delivered to each electrode to maintain balance and prevent net charge accumulation. In [87], an Operational Transconductance Amplifier (OTA), is employed as a buffer and connected to the electrode to balance the output currents of the anodic and cathodic phases. Figure 22 illustrates the circuit configuration. The OTA serves as a current limiter, ensuring the equalization of the anodic and cathodic currents. Depending on the output current, this circuit can either inject or absorb current.

Some of the other methods include pulse insertion [44], [59], [76], [88], [102], [121], [126], charge balancing based on offset regulation [36], [58], [60], [65], [69], [70], [88], [90], [91], [92], [110], [130], and digital approaches to balance charge mismatch [65], [82]. Figure 23 shows the pulse insertion technique. In this method, a specific safe voltage range is defined for the tissue, which is determined by the residual charge remaining on the tissue after each stimulation cycle.

After each cycle, the remaining voltage is compared to the safe voltage region. If the voltage exceeds the safe region, the anodic and cathodic phases are out of balance. To address this, some pulses with small pulse width will be generated after each cycle to decrease the residual voltage and make a charge balance stimulation. This process is repeated until the measured residual voltage enters the desired range. The Offset Regulation method, shown in Figure 24, operates similarly to the pulse insertion technique. If the residual voltage exceeds the safe range, current is injected or drawn from the electrode, resulting in a stimulation pulse being applied to the electrodes.

The magnitude of this current is determined based on the exceeded voltage level to return the stimulation to the safe region. This process is performed in each stimulation cycle

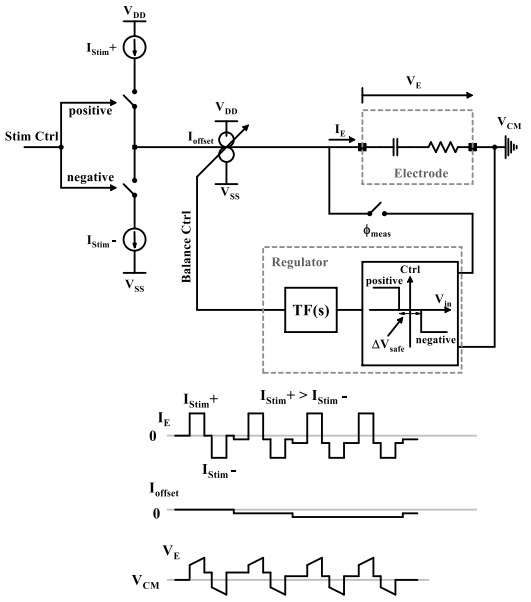


FIGURE 24. Offset Regulation technique for charge balancing [88].

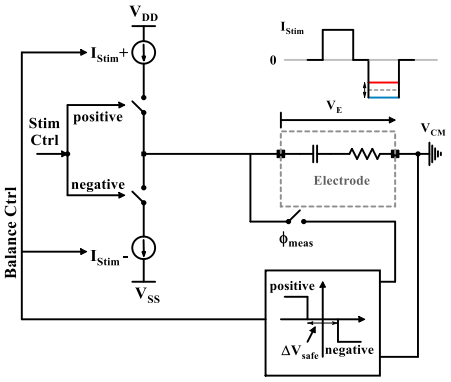


FIGURE 25. Pulse modulation technique for charge balancing [65].

and helps create charge balance. Another method for charge balancing is pulse modulation, which is depicted in Figure 25 [65]. The process of comparison in this method is similar to offset regulation and pulse insertion techniques. However, in pulse modulation, according to the exceeded voltage on the tissue after each cycle, the current level in the anodic or cathodic phase will be increased.

In this approach, the residual voltage is monitored, and if it exceeds the safe range, adjustments are made to the current level in the subsequent anodic or cathodic phase. The goal is to increase the current level in the phase corresponding to the exceeded voltage, thereby compensating for the charge imbalance. By modulating the current levels in response to the residual voltage, the charge delivery can be adjusted to achieve balance and maintain the stimulation within the safe region.

In [65], a hybrid method was presented, combining the shortening method, offset regulation, and pulse modulation

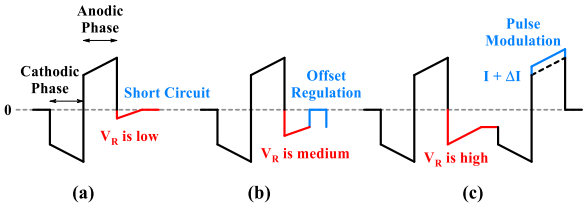


FIGURE 26. Hybrid method for charge balancing based on residual voltage (V_R): (a) V_R is low, (b) V_R is medium, and(c) V_R is high [65].

topologies. As shown in Figure 26, when the residual voltage is low, the shortening circuit is activated, while for medium and high remaining voltage, offset regulation and pulse modulation are used, respectively.

Many charge-balancing methods have been introduced based on the mentioned structures, as well as some digital circuits to monitor the voltage of the tissue. In these stimulators, the voltage on the tissue is monitored after each stimulation cycle and compared with a reference voltage defined based on the safe region for residual voltage.

The digital-based offset regulation charge balancing method was introduced in [58]. This method utilizes digital circuits to generate adjustable stimulation with controllable amplitude and pulse width. After each phase, a constant current is applied to the tissue based on the anodic-to-cathodic ratio and the unbalanced amount. In [82], a subtractor measures the difference between the two phases and compares it with a reference voltage. After each stimulation phase, the voltage difference between the two phases is applied according to the pulse modulation technique.

Another stimulator, introduced in [91] and [92], is a modified version of the pulse modulation structure. This stimulator incorporates a calibration loop consisting of an integrator and comparator. It monitors the tissue voltage and calibrates the current DAC to reduce the mismatch between the anodic and cathodic phases. A different modified charge balancing method was presented in [126] and [127]. Instead of changing the amplitude, this stimulator adjusts the pulse width to achieve charge-balanced biphasic stimulation. This technique operates by sampling the electrode-tissue voltage (VE) of the electrode at specific moments before and during the first phase of the stimulation pulse. This sampling provides information about the capacitive and resistive components of the electrode-tissue interface impedance and the voltage during the rest period induced by the residual charge. An on-chip processor uses this information to calculate precise timing adjustments for the second phase of the pulse, ensuring complete neutralization of the residual charge by the time the pulse is terminated. This adjustment is applied to the duration of the second phase (e.g., cathodic phase) of the pulse. Importantly, this method imposes no minimum time requirement before starting the next pulse, allowing for flexible and continuous stimulation. The stimulator in [38] utilized a CMOS-integrated Twin-Track active charge balancer. The Twin-Track system, shown in Figure 27, employs

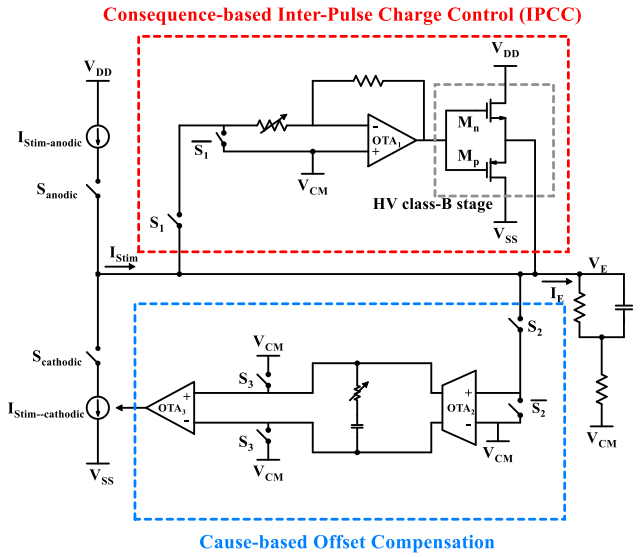


FIGURE 27. Concept of the cause and consequence-based Twin-Track active charge balancer [38].

two complementary approaches for charge balancing: long-term balanced conditions and instantaneous autonomous balancing. A cause-based proportional-integral (PI) controlled offset compensation method is used for long-term charge balancing.

It compensates for any remaining electrode voltage offset by adjusting the compensation currents. This approach achieves balanced conditions over an extended period. For instantaneous autonomous balancing, a consequence-based Inter-Pulse Charge Control method is employed. It utilizes a class-B architecture to generate compensation currents without the need for additional references. This method ensures immediate charge balancing during stimulation. By combining these two approaches, the system achieves better performance. Another form of pulse injection charge balancing was introduced in [96]. The charge-balance structure includes a closed loop path for the adaptive, which applies small current pulses after each stimulation cycle. This process is designed to push or pull charges to maintain residual charges within the safety limit.

Since amplitude regulation techniques impose analog matching constraints and require a larger circuit area, another charge balancing method based on pulse width changing was introduced [76]. This method, known as digital time-domain calibration (DTDC), digitally adjusts the second phase of the biphasic stimulation pulses based on a one-time characterization of all stimulator channels using an on-chip analog-to-digital converter. The second phase of the biphasic pulse is responsible for bringing the delivered charge back to zero and achieving charge balance. The DTDC method recognizes that the second phase does not have a direct stimulating effect and can be adjusted without significantly impacting stimulation efficacy. By digitally modifying the pulse lengths in the time domain, the charge balance can be achieved, even in the presence of circuitry mismatches.

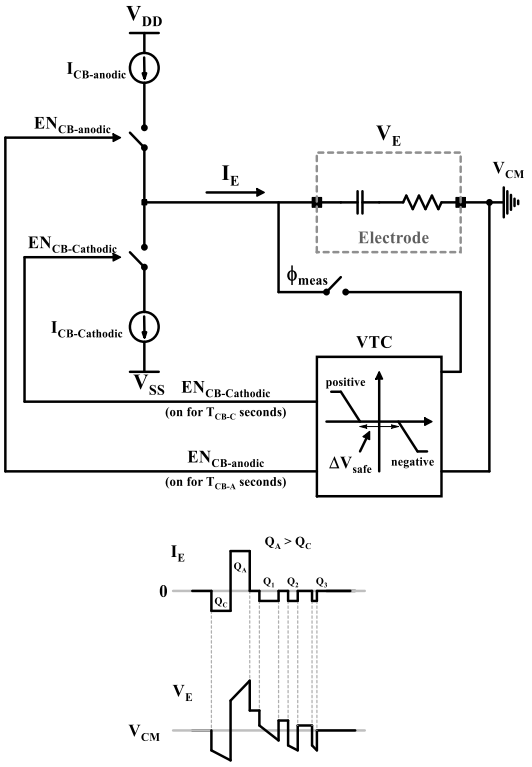


FIGURE 28. Time-based charge balancing method [97].

Another method for pulse duration control method was proposed, which employed a time-based charge balancing circuit to reduce charge imbalance. This circuit is depicted in Figure 28 [97] and consists of a voltage-to-time converter and a compensation current source/sink. A feedback mechanism utilizing a comparator-based voltage-to-time converter (VTC) was implemented to monitor the residual voltage after each stimulation cycle. The voltage-to-time converter played a crucial role in the charge-balancing phase. After monitoring the residual voltage, it converted the voltage across the electrode-electrolyte interface into a corresponding time duration. By repetitively injecting current pulses, the circuit achieved charge-balanced stimulation, with the durations of the pulses controlled by the voltage-to-time converter.

Other structures have been introduced to achieve charge-balanced stimulation [39], [45]. In [39], two sample and hold-based current memory cells were presented to decrease the charge mismatch between the anodic and cathodic phases. The block diagram of the stimulator is shown in Figure 29(a). In this configuration, a memory cell samples the output of the DAC during the first phase. Subsequently, a switch disconnects the path of the DAC, allowing the stored current in the memory cell (from the first phase) to flow to the second memory cell through a closed high-voltage tolerated switch. This arrangement ensures precise current matching between the two memory cells.

During the stimulation phase, the anodic, interphase delay, and cathodic phases are generated by opening and closing

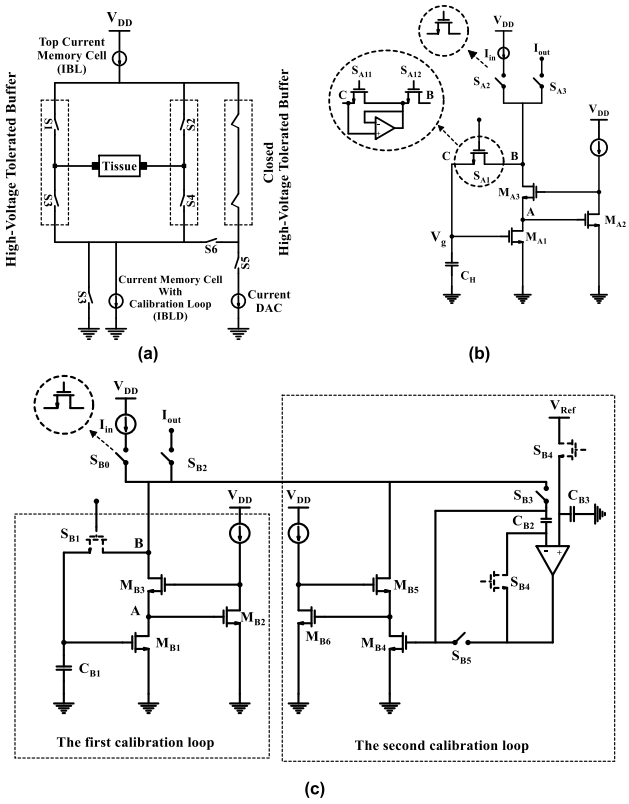


FIGURE 29. Sample and hold-based stimulator with two current memory cells: (a) Block diagram of the stimulator, (b) Top current memory cell, (c) Bottom current memory cell with two calibration loops [39].

the switches. Figure 29(b) illustrates the current memory cell (IBL). During the sampling mode, S_{A1} and S_{A2} are closed, while S_{A3} is open. The input current passes through transistor S_{A1} and causes the capacitor C_H to store the voltage V_g. When S_{A1} becomes off, a percentage of charge due to the charge injection and clock feed through is injected into the sample capacitor, causing V_g change as follows [153]:

$$\Delta V = \frac{WLC_{ox}\left(V_{DD} - V_g - V_{TH}\right)}{2C_H} + V_{ck}\frac{WC_{ov}}{WC_{ov} + C_H} \quad (7)$$

where V_{ck}, C_{ov}, and V_{DD} are clock amplitude, overlap capacitance per unit width, and power supply, respectively. In equation (7), the first term represents charge injection, and the second part shows the effect of clock feedthrough. For holding phase, S_{A1}, S_{A2}, and S_{A3} will be open. A discharge path will be provided for C_H, and simultaneously, the gate-drain parasitic capacitor causes V_g change by

$$\Delta V(t) = V_g(1 - e^{-\frac{t}{r_o C_H}}) + \frac{C_{gd}V_{TH}}{C_{gd} + C_H} \quad (8)$$

where r_o represents the off-state resistance of S_{A1}. The first and second parts in equation (8) represent the effect of off-state resistance and coupling effects of C_{gd}. S_{A1} and S_{A2} are still open during the next phase while S_{A3} becomes on. In this case, the parasitic capacitor, C_{gd}, causes the voltage variation at node A to transfer to C_H, which can be expressed as

$$\Delta V\,(t) = -\frac{C_{gd}V_{TH}}{C_{gd} + C_H} \quad (9)$$

Thus, based on 6, 7, and 8, the total voltage error for V_g can be written as follows:

$$\Delta V = \frac{WLC_{ox}\left(V_{DD} - V_g - V_{TH}\right)}{2C_H} + V_{ck}\frac{WC_{ov}}{WC_{ov} + C_H} + V_g(1 - e^{-\frac{t}{r_o C_H}}) \quad (10)$$

This error in voltage will result in a mismatch between I_{out} and I_{in}, which can be described by

$$\Delta I = I_{out} - I_{in} = \Delta V g_m \quad (11)$$

where g_m indicates the transconductance of M_{A1}. Equation (11) shows that the current error is directly influenced by g_m, indicating that a larger off resistance of S_{A1} can result in reduced current error. To address this, the current memory cell utilizes a modified switch that reduces the on-state resistance and increases the off-state resistance. Figure 29(b) illustrates this structure, which consists of two transistors, S_{A11} and S_{A22}, and one unity gain amplifier. By employing this configuration, the drain-source voltage becomes zero, leading to an infinite off-resistance. Consequently, based on equations (8) and (10), the effect of off-resistance is negated, and the voltage error can be written by

$$\Delta V = \frac{WLC_{ox}\left(V_{DD} - V_g - V_{TH}\right)}{2C_H} + V_{ck}\frac{WC_{ov}}{WC_{ov} + C_H} \quad (12)$$

The second current memory cell is employed on the bottom side to mitigate the impact of charge injection and clock feedthrough. Figure 29(c) shows the bottom current memory cell, including two calibration loops. The first loop is responsible for initial calibration, while the second loop compensates for errors caused by the first loop. This circuit has 3 phases for its operation. During the first phase, S_{B0}, S_{B1}, S_{B3}, and S_{B4} are turned on, while switches S_{B2} and S_{B5} are open.

Assuming a ratio of $(W/L)_1 : (W/L)_4 = N$, transistors M_{B1} and M_{B4} have drain current of $[N/(N+1)]\times I_{in}$ and $[1/(N+1)]\times I_{in}$, respectively. In the next phase, SB1 is turned off, and S_{B0} and S_{B2-5} remain on. Similar to the top current memory cell, C_{B1} will have a portion of charge due to charge injection and clock feedthrough effects. Consequently, the drain currents of M_{B1} and M_{B4} change to $[N/(N+1)]\times I_{in} \pm \Delta I$ and $[1/(N+1)] \times I_{in} \mp \Delta I$, respectively. In the last phase, S_{B3-5} are turned off, while the other remain on. This configuration eliminates charge injection from S_{B3}.

As S_{B4} is positioned at the input of the amplifier and the charge injection appears as a common-mode disruption, it is also eliminated. Based on amplifier gain, the gate voltage error for M_{B4} and the current error during the second and third phases can be expressed as

$$\Delta V = V_{out} - V_{in} = \frac{V_{in}}{1 + A_V} \quad (13)$$

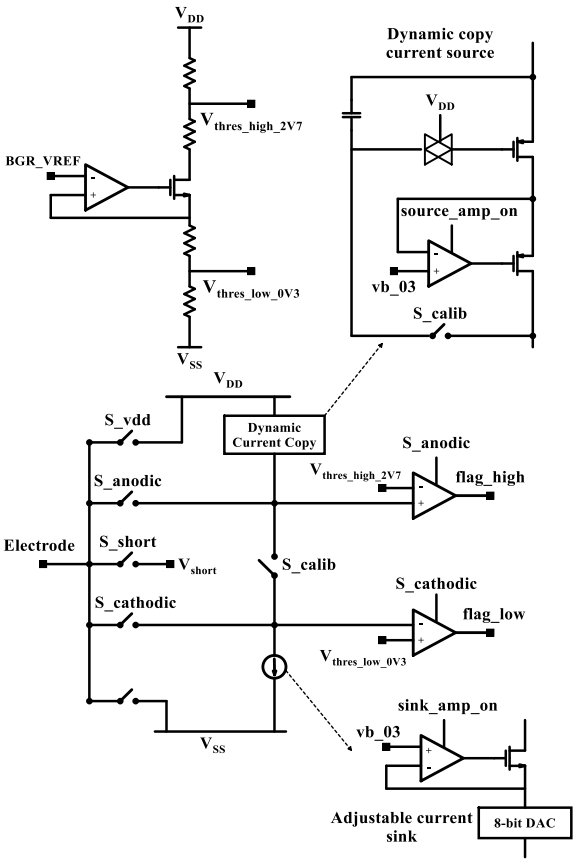


FIGURE 30. Dynamic current copy electrode driver architecture [45].

$$\Delta I = I_{out} - I_{in} = \frac{V_{in}}{1 + A_V} g_m \tag{14}$$

where V_{in} and V_{out} are the gate voltages of M_{B4} at phases 2 and 3, respectively. A_V is the amplifier's open loop gain, and g_m is the transconductance of M_{B4}. The dual calibration loop described earlier effectively mitigates the total current error by a factor of (N+1). However, the design method for this approach is complex, and the use of capacitors and operational amplifiers in the current memory cells results in a larger occupied area. Another approach to achieve current balancing is the dynamic current copy structure, depicted in Figure 30.

This structure is designed to balance the current for the anodic and cathodic phases and provides precise and flexible control over the stimulation current delivered to the electrodes [45]. It ensures that each electrode receives the desired stimulation current while maintaining high accuracy and fidelity. This structure is responsible for generating individual current pulses for each electrode driver. The circuit has several components, including an 8-bit DAC, current mirrors, and OTAs. The DAC converts the digital stimulation commands from the digital controller into the desired current. This current is then replicated and mirrored using the current mirror circuit. The replicated current is then distributed to the individual electrode drivers, ensuring that each electrode

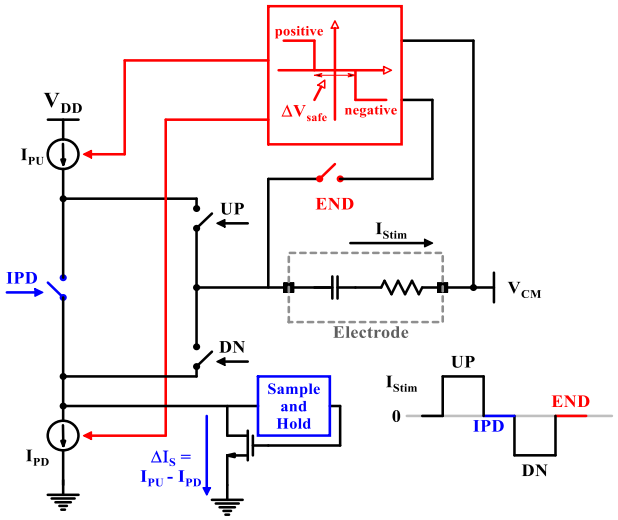


FIGURE 31. Sample and Hold charge balancing topology [90].

receives the intended stimulation current. This allows for precise and independent control over the stimulation of each electrode. In this method, the current of one driver was duplicated for the other one during a calibration period. To reduce residual charge and ensure accurate stimulation, a discharge circuit is implemented to short the electrodes to the ground. This helps in quickly dissipating any remaining charge.

Another active charge-balancing method, based on pulse modulation, is introduced in [90] and illustrated in Figure 31. This method utilizes two structures. The first structure, labeled as number 1, incorporates a sample and hold circuit. During the anodic phase, switch UP is turned on, allowing current to flow from the current source to the electrode. Subsequently, switch UP is opened, and switch IPD is closed, causing the difference between the two current sources to pass through the transistor M_1. This current generates a gate-source voltage that is stored in the sample and hold circuit. This voltage represents the current difference between I_{PU} and I_{PD}. In the next step, switch DN is turned on, while other switches are turned off. As a result, the cathodic current, along with the stored current difference (Δ IS = IPU – IPD), is injected into the tissue. Additionally, the offset regulation technique is employed after the cathodic phase for better charge balancing. However, it should be noted that this structure has no solution if IPU becomes greater than IPD, as it may lead to limitations or challenges in achieving charge balance. The proposed stimulator in [143] employed charge-mode neural stimulator. It utilizes a capacitor-reuse technique with a residual charge detector and achieves active charge balancing. It consists of a digital controller and an integrating ADC for residual charge detector. The stimulator in [144] proposed a new method including a CC mode and a VC mode stimulator to achieve accurate anodic pulse generation. The CC operation compensates for the majority of stimulation charge quickly, while the VC operation ensures

TABLE 2. Comparison table for charge balancing method.

Method	Occupation area	Scalable	Charge balancing duration	Design complexity	Precision	Unwanted spike or stimulation
Electrode shortening [142]	Very low	✓	Unknown	Very Low	Moderate	Yes
DC-block capacitor [108]	Very High	×	Low	Very Low	High	No
HFCS [86]	High	×	Low	Low	High	No
Limiter buffer [87]	Moderate	✓	Low	Moderate	Moderate	No
Pulse insertion [88]	Low	✓	Very High	Moderately High	Moderately High	Yes
Offset regulation [88]	Low	✓	Very Low	Moderately High	Moderately High	No
Pulse modulation [65]	Low	✓	Very Low	Moderately High	Moderately High	No
Twin-Track [38]	Moderate	✓	Very High	High	High	No
DTDC [76]	Moderate	✓	Low	Moderately High	High	No
VTC-based method [97]	Moderately High	✓	Moderately High	Very High	Very High	No
Current memory cell [39]	Moderately High	✓	Low	Very High	High	No
Dynamic current copy [45]	Moderately Low	✓	Very Low	High	High	No
Sample & hold [90]	Moderate	✓	Moderately Low	High	Moderate	No

high charge balancing precision. Several passive and active methods have been discussed in this section.

The passive topologies were based on electrode-shortening, the use of DC-block capacitors, and HFCS, which offer ease of design. However, the discharge time cannot be determined with the shortening method, and it may result in some unwanted stimulation. On the other hand, since DC-block and HFCS methods involve the use of capacitors, the occupation area will be increased, and they cannot be suitable for multi-channel stimulators. Active methods such as pulse insertion, offset regulation, pulse modulation, modified methods based on these methods, sample and hold methods, and current memory cells have been introduced. Implementing these methods eliminates the need for capacitors and allows for scalable and integrated stimulation system. However, each method has its own disadvantages. In the pulse insertion method, the number and duration of current pulses during the charge balancing phase can vary depending on the accumulated charge in the tissue. If the imbalanced charge is relatively small, a lower number of current pulses is required.

Conversely, achieving charge-balanced stimulation may necessitate a larger number of current pulses and, consequently, a longer duration. Longer duration and imposing significant time constraints can potentially lead to tissue failures. Furthermore, similar to electrode shortening, pulse insertion may result in undesired spikes and stimulations. In the offset regulation method, charge balancing is a continuous process, and the accumulated and imbalanced charge is not removed after each single stimulation phase. This eliminates the need for long durations. However, it does require additional control circuits and suffers from higher design complexity. Pulse modulation is another method that can address the long-duration issue by applying the difference between the two phases to the subsequent phase (cathodic or anodic) within a stimulation cycle. This difference can be used to adjust the level or pulse width of the next cathodic/anodic phase. Nevertheless, determining this difference precisely can be challenging and requires careful parameter selection and optimization. The current memory cell method ensures consistent and precise delivery of the current, even in the presence of impedance variations. However, it utilizes capacitors that occupy a large area, and necessitates accurate design, leading to increased design complexity. To have better comparisons between the proposed methods, Table 2 summarizes the advantages and disadvantages of the main charge balancing methods discussed in this section.

D. POWER EFFICIENCY APPROACHES AND CONSIDERATIONS

Power efficiency is a crucial parameter to consider in ENSs as it helps to minimize power losses. Some methods have been proposed to improve performance in terms of power efficiency [71], [72], [103], [106], [111], [112], [124], [125], [136], [137], [138].

A dynamic power supply technique and adaptive power supply [71], [72] were presented for ENSs. Both stimulators were designed based on transistor-stacking and self-adaptive bias methods. Figure 32 illustrates the ENS and dynamic power supply control system block diagram in [71] and [72]. The electrode is continuously monitored using a block

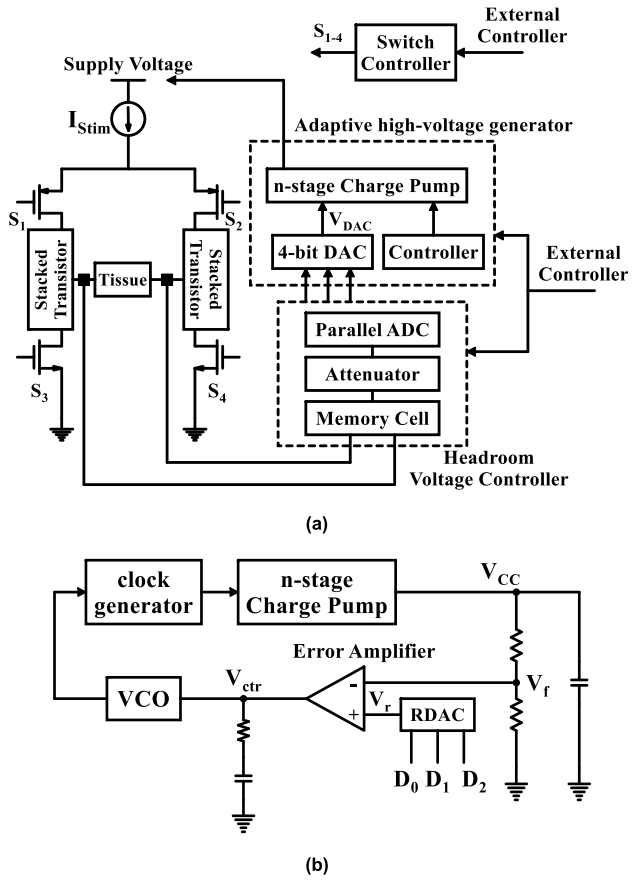


FIGURE 32. Dynamic and adaptive power supply technique: (a) Whole system block diagram, (b) Power supply controller block diagram [71], [72].

diagram consisting of a memory cell, an attenuator, and an analog-to-digital converter (ADC). This monitoring system outputs a digital code based on the electrode voltage. This code serves as the input for the dynamic power supply controller, which includes a voltage divider, error amplifier, DAC, voltage-controlled oscillator, 4-phase clock generator, and 3-stage charge pump. When the ENS does not require high voltage on the tissue, the monitoring part generates a code based on the electrode voltage. This digital code is then applied to the DAC in the dynamic power supply. The VCO, through a feedback loop controls the clock generated from the phase generators. These clock signals manage the charge pump and reduce the output voltage, which serves as the power supply for the stimulator. This technique effectively reduces power consumption and improves efficiency. The same process is followed when increasing the power supply for stimulating the electrode with higher voltage compliance.

In [71], a simple current source with a triode indicator was utilized to prevent the current source from entering the triode region. The triode indicator monitors the drain-source voltage of the cascode current source, which includes push-up and pull-up switches. When the transistor in the current source exits the saturation region, the monitoring part generates a digital code to control the dynamic power supply and increase the supply voltage. Additionally, a quick discharge path was designed to rapidly discharge the supply charge after each stimulation phase within a short period. Figure 33 (a) illustrates the stimulator core with the triode indicator and quick discharge path. Furthermore, Figure 33(b) depicts the output stimulation based on the dynamic power supply. As shown in Figure 33(b), when the voltage drops on transistors M_{C3} and M_{C4} becomes less than a threshold, the triode indicator is activated and outputs an "error" signal. Consequently, the power supply voltage is incrementally increased to reach the desired voltage and cause the transistor to leave the triode region. This method significantly improves power efficiency; however, coordinating the digital control signals and ensuring proper timing and synchronization can introduce complexity to the design.

The technique employed in [138] enhances the efficiency of ENS through a voltage-switching method, similar to the dynamic power supply approach in [71] and [72]. It utilizes a secondary power telemetry coil to generate a programmable set of voltage supplies, which are used for stimulating the target tissue. In this technique, the circuit sequentially switches the electrode through voltage steps instead of injecting constant current into the tissue. These voltage steps can effectively stimulate the target tissue, similar to the constant-voltage stimulation. The selection and careful switching of voltage steps are crucial to make the proposed method behave more similarly to the constant-voltage approach.

While this method increases the power efficiency, the process of selecting and switching voltage steps introduces higher complexity due to the consideration of numerous design parameters. Furthermore, the accuracy and precision in current delivery are sacrificed to achieve higher efficiency.

In [103], the stimulator presents a high-frequency switched capacitor (HFSC) stimulation prototype that combines the voltage-mode stimulation (VMS) and constant-current stimulation (CCS) methods. When V_E is smaller than V_{ref}, the gate voltage PMOS transistor, P_c, becomes low, causing the capacitor C_{stim} to charge to V_{DD}. Subsequently, Switches S_1 and S_3 are turned on, and the charge is transferred to the electrode to generate the anodic phase for charge balancing. Opening switches S_2 and S_4 during this phase is necessary to prevent disturbance to the gate voltage of Pc, caused by sampling and comparing the transient voltage before V_E stabilization. This hybrid approach benefits the advantages of both methods while mitigating their drawbacks, resulting in improved energy efficiency. According to the results and theoretical analysis in [103], employing this method leads to higher efficiency.

Figure 34 illustrates the proposed HFSC stimulator circuit in [103]. The switches S_1 and S_{1b} are controlled by two non-overlapping clocks to generate the cathodic phase and remove the charges from the electrode. For the subsequent phase, switches S_2 and S_4 are activated, and a comparator compares the electrode voltage (V_E) with a reference voltage (V_{ref}).

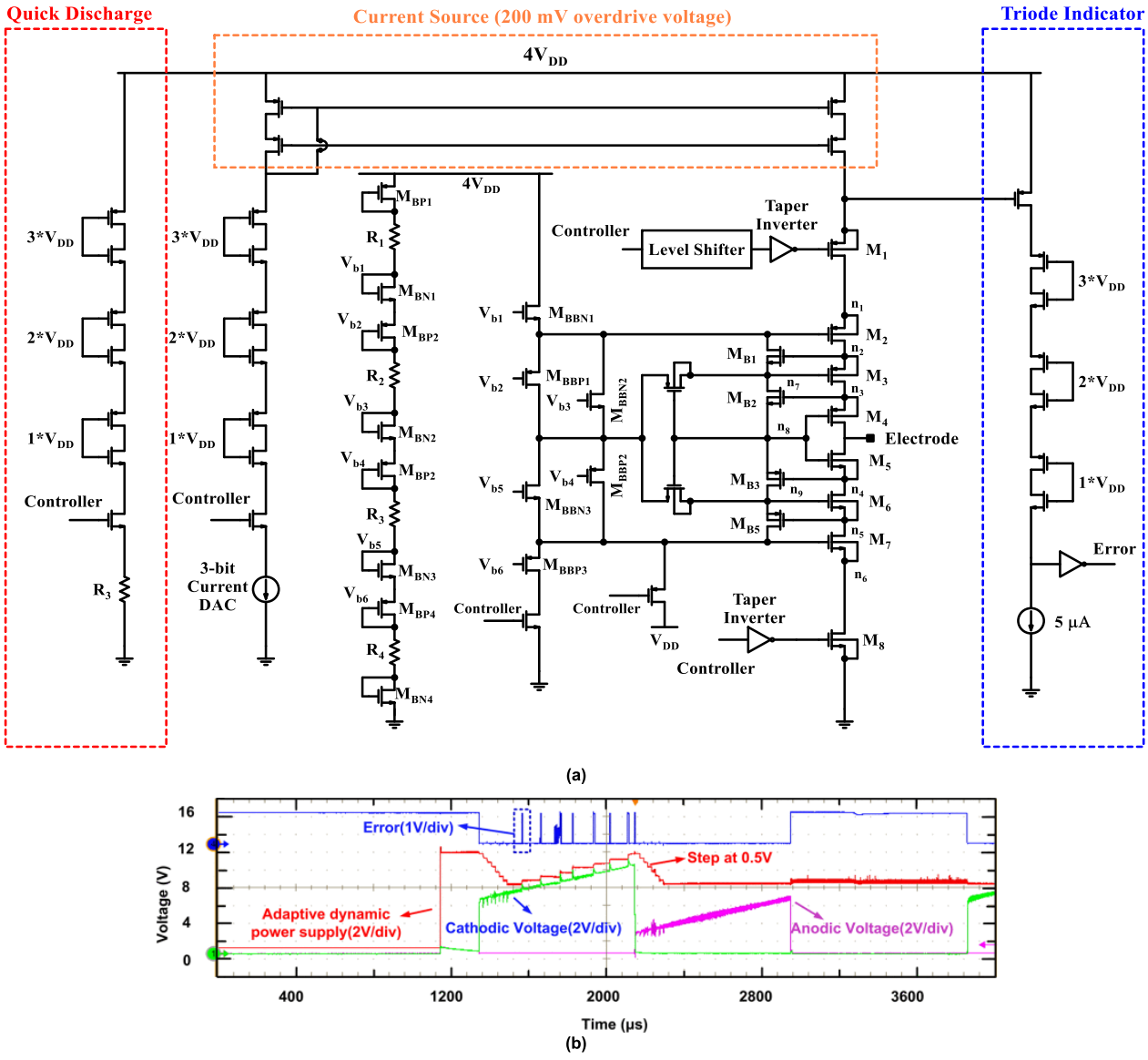


FIGURE 33. High-voltage-tolerant stimulator and its stimulation waveform: (a) Output stage with triode indicator, self-adaption bias, and quick-discharge circuits, (b) The power supply self-adjusting procedure during stimulation in the dynamic power supply technique [71].

The stimulator operation and the charge balancing are completed when V_E exceeds V_{ref}. Since this stimulator utilizes a capacitor in its structure, it occupies a significant area. Additionally, implementing appropriate timing and synchronization for the neural stimulator can be challenging. In [106], to achieve high energy efficiency, the use of a Single Ended Primary Inductor Converter (SEPIC) and optimization of the switching frequency and gate width of the power MOSFET are introduced. By employing a wireless charger with closed-loop control feedback, the received energy can be adjusted, eliminating the need for complex DC-DC converters and improving efficiency. Furthermore, the system includes an energy distribution circuit that allows the pulse generator (the stimulator) to be powered either by wireless energy or the implantable battery, depending on the situation. The energy distribution circuit manages the power source to ensure that the stimulator receives the appropriate power supply under different conditions. However, the output stage of the stimulator in this structure includes an inductor, which occupies large area.

Another stimulator introduced in [111] utilizes the ultra-high frequency (UHF) concept, which has been proven to be as effective as current mode stimulation. This method stimulates the tissue by a burst of current pulses with adjustable amplitude at a high frequency. The ENS core includes an inductor-based buck-boost DC-to-DC converter. The system in [111] presents a novel zero-current detection scheme to eliminate the need for a freewheel diode.

By accurately detecting the moment when the current flowing through the inductor reaches zero during the switching

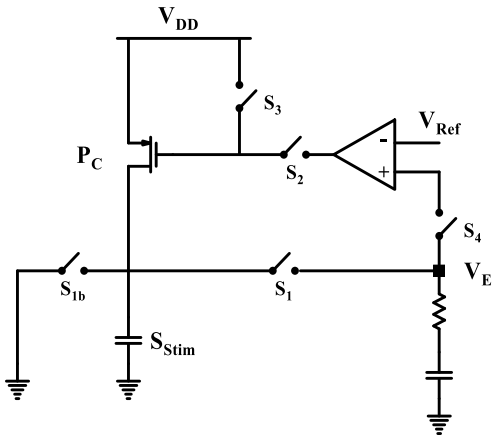


FIGURE 34. Stimulator configurations in the cathodic stimulation phase and anodic charge balancing phase [103].

cycle, the stimulator dynamically adjusts the switching signals to maintain a constant voltage across the inductor. This constant voltage across the inductor prevents reverse flow current from the load to the inductor without the use of a freewheel diode. This scheme enables more efficient energy transfer and contributes to achieving higher peak power efficiency for the ENS.

However, the design suffers from a large occupation area, sensitivity to noise and variations, design complexity, and complex timing synchronization. As previously mentioned, the stimulation waveform directly impacts the power efficiency of the stimulators.

According to this issue, some stimulators have been designed to output an exponential waveform [112] and multi-waveform current stimulation [137]. The stimulator in [112] generates a flexible rising exponential pulse, which provides higher energy efficiency for stimulating action potentials while releasing fewer toxic ions in cortical tissues. Analytical studies and computational models have demonstrated that rising exponential pulses can increase power efficiency compared to rectangular pulses [73]. Additionally, careful design of exponential waveform parameters, such as amplitude, duration, and time constant, can deliver the required stimulation while minimizing charge accumulation on the tissue and achieving better charge balancing to prevent tissue damage. The system introduced in [137] presents a multi-wave output stimulator that generates three waveforms: rising exponential, falling exponential, and rectangular pulse. This method can produce the appropriate stimulation waveform to reach superior energy efficiency in several applications.

While employing exponential waveform as output in stimulators offers higher energy efficiency and improved charge balancing, it does come with some disadvantages. Designing the circuit to generate exponential waveforms can be more challenging and complex compared to rectangular pulses. This complexity can increase the overall system complexity and potentially affect the cost and manufacturability of the stimulation device. Another concern is the sensitivity of rising exponential pulses to variations in their parameter, such as amplitude, duration, and time constant. Even slight deviations or mismatches can impact the characteristics of the exponential waveform. Achieving precise and consistent control over these parameters may require more sophisticated calibration and control mechanisms, adding complexity to the system. Moreover, the use of rising exponential pulses limits the flexibility of changing the parameters within specific ranges to meet different stimulation requirements in various application. These limitations make the rising/falling exponential-based stimulators incompatible with existing systems.

The stimulator in [125] utilizes adiabatic supply voltage to bypass losses introduced by a conventional system supply-generating, thereby improving efficiency. Adiabatic supply voltages can provide a high differential voltage range to deliver a higher voltage level to the stimulator and inject more efficient current into the tissue. Another approach employed in [125] is energy replenishment, which redirects charges accumulated across the electrodes back to the system power supplies for recycling. This method aims to overcome drawbacks and limitations of conventional stimulation methods where the tissue delivers a fixed or pulsed current. In traditional topologies, the current amplitude gradually decreases over time due to the electrical properties of the tissue and the electrode-tissue interface. This phenomenon can lead to a reduction in the overall power efficiency of the stimulator. To address this issue, the charge replenishing technique uses a feedback loop to continuously monitor the charge delivered to the tissue for each stimulation phase and adjust the stimulation parameters, such as amplitude or pulse width. If the measured charge exceeds the desired value or falls below it, the circuit adjusts the parameter accordingly to prevent overstimulation or compensate for charge loss.

E. PERFORMANCE COMPARISON OF STATE-OF-THE-ART ELECTRICAL NEURAL STIMULATOR

Table 3 presents recent work in the field of stimulator design for various electrical neural stimulator application, including peripheral nervous system, DBS, cochlear implants, and retinal implants. According to Table 3, all the stimulators were predominantly designed in Constant Current Mode (CCM) due to its precise control of the injected charge into the tissue. In CCM, the amplitude and pulse width of the applied constant current can be regulated within a range of impedance. However, some stimulators, such as those in [31], [86], and [108] employed the Switched Capacitor Mode (SCM) and Constant Voltage Mode (CVM), while [31] and [108] incorporated the CCM mode as well. The table also indicates that these stimulators were implemented using various CMOS technology processes, which are popular and preferred for their reliability and lower cost.

Among the CMOS technologies, the 0.18 μm process has been widely utilized in recent years due to its compatibility, cost-effectiveness, and reliability, while still accommodating

TABLE 3. Performance comparison of state-of-the-art electrical neural stimulators.

Year Ref.	Structure	CMOS Tech.	Supply (V)	Channels Number	Max. Current (mA)	NOB*** (bit)	Output Voltage (V)	Charge Mismatch (%)	Efficiency (%)	Total Power (mW)	Total Area (mm^2)	Application
2005 [116]	Dual Supply (CCM)	1.5 µm LV	±6.5	4	0.6	6	0 ~ 3	1.2	-	2.9	4.84	Retinal
2006 [10]	Dual Supply (CCM)	0.5 µm LV	±2.5	4	0.5	8	-2 ~ 2	< 1	-	2.5	6.96	Cochlear
2007 [44]	Sink/Source CCM	0.35 µm HV	35	232	1	5	0 ~ 22.5	4	38	10	22	Epiretinal
2008 [21]	H-Bridge (CCM)	0.35 µm HV	10	3	0.735	7	0 ~ 2	0.5	-	0.198	1.35	Vestibular
2008 [86]	HFCS (SCM)	1 µm HV	18	4	1	4	0 ~ 10	N.A.	36	9.9	1.636	Cochlear Nerve
2009 [87]	Dual Supply (CCM)	0.6 µm BiCMOS	±2.5	100	0.216	8	-2 ~ 2	< 4	10.8	25	24.84	Leg nerve
2010 [57]	Dual Supply (CCM)	0.18 µm HV	±12	256	0.5	3	-10 ~ 10	< 2.9	-	1.45 @ 100 µA	27.03	Epiretinal
2011 [119]	Sink/Source CCM	0.35 µm LV	5.05	4	0.094	6	0 ~ 4.68	N.A.	-	0.014	0.43	DBS
2012 [90]	Sink/Source CCM	0.13 µm LV	3.3	>10	1	5	-	*9.8 nA	-	6.8	12.5	Electro-Acupuncture
2013 [19]	H-Bridge (CCM)	0.18 µm HV	12	8	0.5	6	0 ~ 11.5	< 0.45	-	6	2.8	Proprioceptive
2014 [77]	H-Bridge (CCM)	0.35 µm HV	15	2	1	5	0 ~ 12	< 0.3	-	15	3.74	Retinal Prosthesis
2015 [101]	H-Bridge (CCM)	0.6 µm HV	12	3*8	1	8	-	-	-	29.7	25.32	Vestibular
2016 [39]	H-Bridge (CCM)	0.18 µm LV	12	1	3	4	0 ~ 10	0.25	-	0.15	1.08	DBS
2017 [71]	H-Bridge (CCM)	0.18 µm LV	12	16	3	3	0 ~ 11.3	< 0.8	69	-	3.5	DBS
2018 [72]	H-Bridge (CCM)	0.18 µm LV	12.3	1	3	4	0 ~ 11.3	0.3-1.7	56	-	5	DBS
2019 [125]	Dual supply (CCM)	0.18 µm LV	-3~3.9	1	0.145	-	-2.3 ~ 3.3	-	-	-	9	DBS
2020 [108]	H-Bridge (VCM/CCM)	0.25 µm LV	2.5/5	4	5	6	0 ~ 10	-	-	-	3.86	DBS
2020 [140]	Sink/Source CCM	0.18 µm LV	3.3	1225	1	4	-	-	-	2.7	15	Retinal
2021 [62]	Sink/Source CCM	0.18 µm HV	20	16	0.55	10	0 ~ 18.2	3.86	-	**23.3 µW	11.95	Vagal Cardiac
2021 [66]	Dual Supply (CCM)	0.18 µm LV	±6	8	3	4	-4.1 ~ 3.8	1.94	-	-	4.15	DBS
2022 [97]	H-Bridge (CCM)	0.18 µm HV	> 40	16	12.75	8	40	< 1.5	-	-	30.25	DBS
2022 [130]	H-Bridge (CCM)	65 nm LV	8	16	0.6	-	-3.6 ~ 3.6	< 1	-	-	0.7	DBS
2023 [31]	Dual Supply (VCM/CCM)	0.18 µm LV	±6	4	3.6	5	-3.6 ~ 3.6	< 1	-	-	1.16	DBS
2023 [76]	H-Bridge (CCM)	65 nm LV	11	16	0.16	7	0 ~ 10.4	*95.6 nA	-	0.325	0.225	Cochlear/Visual
2024 [141]	H-Bridge (CCM)	0.18 µm LV	9	8	0.07	3	-7.5 ~ 5.5	1.73	-	-	0.79	-

* Current Error
** Static Power
*** Number of Bits

high current and voltage levels. Moreover, considering all the mentioned advantages, this process does not occupy much area. Furthermore, most of the recent designs adopted the LV topology due to its cost-effectiveness, compact size, and lower power consumption. The number of channels in a stimulator depends on the target application. As claimed by Table 3, the number of channels in ENSs can range from 1 to 1225, depending on the device's intended use. The required channels in these stimulators are determined by the medical condition being treated and the desired treatment

approach. For instance, stimulators in [39], [72], and [125] employ a single channel as they target a specific area in the brain for treatment. On the other hand, stimulators like those in [44], [57], and [140], aim to restore vision in limited vision individuals by targeting the epiretinal area, requiring a large number of channels.

The other two parameters, stimulation current and voltage compliance, are also directly related to the intended application. The current must fall within a safe stimulation range to prevent tissue damage. Additionally, each patient may exhibit different impedances in different body organs. Therefore, the current level in the stimulators should be adjustable within a range, considering the issues mentioned earlier. The output voltage range or voltage compliance is also dependent on the mentioned parameters. In some cases, a higher voltage compliance is necessary due to the high impedance of electrodes. The table highlights the characteristics of various stimulator designs. For instance, in [97], the stimulator achieved a voltage compliance of 40V and a current amplitude of 12.75mA, utilizing High-Voltage (HV) technology. However, these stimulators also exhibited a high-power consumption of 30.25mW. Conversely, design such as [39], [71], [72], and [76] achieved significant voltage compliance (ranging from 10 to 11.3) using Low-Voltage (LV) process. These designs also had a current amplitude of up to 3mA for tissue stimulation. Efficiency was not reported in many designs, while it is a challenging issue in the stimulator, primarily when the stimulator is powered by a battery However, in [44], [71], and [72], efficiencies of 38%, 69%, and 56% were achieved, respectively, by employing dynamic and adaptive power supply techniques in the stimulator design. Additionally, the stimulator in [86], which employed the SCM prototype, achieved an efficiency of 36%. Charge mismatch is another crucial aspect in the ENS implementation, referring to the residual voltage in the tissue caused by an imbalance between the anodic and cathodic phases. Recent state-of-the-art stimulators have achieved a mismatch of less than 1%, such as 0.25% [39], 0.3% [77], 0.45% [19], and 0.8% [71] for biphasic stimulation. Furthermore, in [90], a current error of 9.8nA was reported in the presented circuit. These low levels of mismatch were achieved by employing novel methods, including a current memory cell with dual calibration loops in [39], an accurate current mirror with shortening in [19] and [77], adaptive supply voltage control with shortening in [71], and a sample & hold method with offset regulation in [90].

V. IN VITRO AND IN VIVO EXPERIMENTS IN THE STIMULATOR

In vitro and in vivo experiments play essential roles in scientific research and contribute to our understanding of various biological processes and diseases. Both types of experiments are necessary and complement each other, contributing to our overall knowledge of biology, disease mechanisms, and the development of new treatments and interventions.

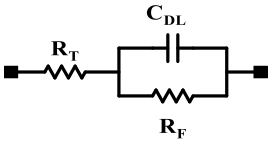


FIGURE 35. The standard electrode-tissue model used for in vitro experiments.

A. IN VITRO EXPERIMENTS

Historically, "In vitro" is Latin for "In glass," reflecting the use of glass containers to conduct these experiments. In vitro experiments refer to studies conducted outside a living organism, typically in a controlled laboratory setting. Applying these experiments allows researchers to study and manipulate biological materials such as cells, tissues, or isolated molecules in special situations and environments. These experiments offer the opportunity to learn about cellular and molecular mechanisms in a simplified and controlled manner. The ENS can interface with organ tissue via micro-electrodes. In vitro experiments are used in a ENS to verify the output results of the presented methods using real electrodes. The selection of electrodes for stimulation needs various requirements, such as biocompatibility, mechanical suitability, efficacy in delivering electrical stimulation, prevention of Faradaic reactions and corrosion, and stable material characteristics during implantation [46]. The chosen material must be biocompatible to avoid toxic or necrotic responses in nearby tissue, as well as excessive immune or foreign body reactions.

Mechanical suitability ensures compatibility with the desired application, maintaining integrity during surgical procedures and throughout usage. Efficacy is important to ensure the device can deliver sufficient charge into the tissue. Minimizing Faradaic reactions and corrosion is crucial to prevent premature electrode failure, with corrosion rates depending on the intended period of use. The stability of the material features must be sufficiently high to ensure the device's electrical impedance, as well as intact conducting and insulating properties. As mentioned in Section II, the electrode-tissue model can be represented by a resistor in series with a parallel capacitor-resistor, as shown in Figure 35. The values of these elements directly relate to the stimulation application and the material used for the electrodes. Table 4 summarizes the element values for the capacitor-resistor electrode model based on the application.

In the next step, before conducting in vivo experiments, the stimulator chip is verified in a simulated environment that mimics the target nerve and replicates tissue features (ex vivo experiments). The stimulator can be tested in this environment, especially before animal or human tests, to verify correct functionality. Different materials can be used according to the target tissue. Based on research, a phantom gel made of sodium chloride, agar, deionized water [31], [66], phosphate-buffered saline (PBS) [36], [68], [79], [127], saline solution [38], [62], [69], [104], sciatic nerve of a frog in Ringer's solution [86], peripheral nerve in Ringer's

TABLE 4. Element values for the capacitor-resistor electrode model.

	Material	Diameter (µm)	R_F (MΩ)	C_{DL} (nF)	R_T (kΩ)	Application
[31]	Platinum/Iridium	1500	1	500	1	DBS (Parkinson)
[36]	Platinum/Iridium	75 / 300	-	160	20	Epiretinal
[38]	polyimide thin-film cuff (Pt/Ir)	800	0.1	1300	3	DBS (Vagus nerve)
[39]	Platinum/Iridium	-	10	100	2	DBS (epilepsy)
[44]	Platinum	200	6.8 kΩ	10	1	Retinal
[57]	Platinum	500	>10	100	10	Retinal
[68]	Polyimide based platinum	220	0.075	1100	2.1	Spinal cord
[69]	Platinum	200	>10	100	10	Epiretinal
[76]	Iridium oxide	-	-	200	8	Visual Cortex
[77]	Platinum	-	1	100	10	Retinal
[79]	Cuff electrodes (Pt/Ir)	100		100/240/300	3.7/8/10	Hand muscle
[86]	Platinum	400	0.107	70 µF	0.1	Cochlear Nerve
[88]	Platinum	150/580	-	240/1200	3.7/1.35	-
[97]	Platinum	4000	2	880	1	Spinal cord
[104]	Platinum	245	60	100	5.6	vestibular nerve
[108]	-	-	1	150	3	General
[118]	platinum	200	2	-	1	DBS
[127]	Polyimide based platinum	220	2 kΩ	1600	0.7	Motor Function Recovery
[138]	Platinum	20	>10	100	10	Retinal

TABLE 5. Measured parameters within "in vitro" experiments.

	Current Level (µA)	Pulse Width (µS)	Output Voltage (V)	Residual Voltage (mV)	Time Interval (mS)
[31]	1000	750	1	5	7.96
[36]	44	1000	1.5	11.2	3.5
[38]	NA	75	4	20	10
[39]	3000	16	10	11.98	1
[66]	3000	60	3.5	3.42	0.15
[71]	2000	160	12	18.78	1
[72]	2500	160	12.3	1.492	350
[108]	5000	56	10	NA	0.15

solution [19], and phantom brain tissue [97], were used to create the virtual environment. Performing this method leads to more realistic results for the stimulators and ensure that animal or human tests are preceded by appropriate validation. During in vitro experiments, scientists often adjust certain parameters to examine their effects on neural activity and achieve desired outcomes. Table 5 summarizes some important parameters that have been applied and measured during these experiments.

B. IN VIVO EXPERIMENTS

The term "In vivo" is derived from Latin and translates to "within the living" or "in the living." These experiments provide more comprehensive information about biological phenomena and their relevance to the whole organism. Scientists can use in vivo experiments to describe experiments or studies conducted within a living organism or its natural environment. In vivo experiments consider the interactions and complexities of the biological systems within the organism, consisting of anatomical, physiological, and behavioral features. These experiments are particularly valuable because they allow researchers to learn about the effects of intervention or treatments in a more holistic manner. Moreover, more comprehensive details can be achieved about complex diseases, assessing the impact of therapies and understanding the physiological and behavioral responses to various stimuli. These data are critical for translating scientific findings into clinical or real-world applications. As mentioned in the previous section, electrodes serve as the interface between the stimulators and the tissue, and it is crucial to choose the appropriate material for the electrodes. The toxicity and biocompatibility of different metals and materials have been studied in animal experiments [46].

Noble metals such as gold, palladium, iridium, platinum, and rhodium have shown good resistance to corrosion during electrical stimulation. However, for long-term stimulation, they exhibit some toxic effects on the tissue [156], [157], [158], [159], [160], [161], [162], [163]. Other materials like platinum and platinum-iridium alloys have shown good performance in terms of reversible charge storage capacity

during electrical stimulation. This capability refers to the electrode's ability to store and deliver the electrical charge to the tissue without corrosion or unwanted side effects [159], [164], [165], [166], [167]. Based on experiments, the use of Iridium-platinum alloy-based electrodes can increase the mechanical strength. Bare iridium or rhodium electrodes have the same performance in terms of charge storage capacities as platinum, while applying an oxide surface can improve the charge storage capacity and density [163]. There are also other materials for electrodes, such as Nickel-titanium, nickel-chromium, cobalt-chromium, etc., which have been performed based on their advantages [46]. Animal tests have indicated that platinum, titanium, ceramic, and platinum-iridium wire are preferred materials for electrodes in cochlear, epiretinal, and DBS stimulation due to their biocompatibility [168], [169], [170]. In vivo experiments in ENS-related research involve implanting fabricated chips in animals and testing them based on the target diseases.

The experiments aim to verify the effectiveness of the implantable stimulators in suppressing the disease effects with loading impedance adaptability. Furthermore, these tests help to assess the stimulator's ability to produce the desired electrical stimulation waveforms and evaluate the safety and efficacy in living organisms. Based on the animal tests presented, most of them utilized Long-Evan rats and implanted the stimulator according to the target tissue [17], [39], [66], [72], [78], [79], [81], [91], [92], [94], [102], [120], [128]. The target disease in these studies were epileptic seizure and, in some cases, Parkinson's disease. Depending on the disease, the electrodes were inserted in a specific region, such as the subthalamic nucleus for Parkinson's [31], [33], [66], [171] and the frontal barrel cortex for epilepsy [17].

The results showed that epileptic seizures can be significantly suppressed by delivering the current in the range of ± 28 to $\pm 50\mu$A. For Parkinson's, the reported current levels were higher, ranging from 200 to 250μA [66], [91]. In other cases, mini-pigs and guinea pigs were selected to provide a closer estimation of the human body [18], [31], [71], [108]. A stimulation range of 1.5 to 3 mA current was applied to the cortical surface to suppress epileptic seizures, which has been proven by clinical data [18]. The pulse widths reported for each anodic and cathodic phase during the stimulation were 0.5ms [17], [39], [72], 100μs [71], 50μs [91], and 100$\sim$250μs [94]. The reported stimulation periods were 2.5ms and 40ms in [17], [39], [72], and [71], respectively. Furthermore, the duration of stimulation for in vivo tests in [17], [39], [72], and [78] was 0.5s, and the stimulator in [71] had a duration of 1s.

Based on some experiment results on EEG signals to treat epilepsy during in vivo tests for closed-loop systems, the seizure onset was detected within 760ms [18] and 800ms [81]. Other systems aiming to suppress EEG signals associated with epilepsy seizures showed successful results after a single stimulation [17], [39], [72], [78], [120]. In these systems, the detection time typically ranged from 1 to 1.5 seconds. Parkinson's disease, on the other hand, is characterized by abnormal beta peaks (13)-35 Hz) in the local field potential (LFP) of the subthalamic nucleus. This biomarker can be used to identify and monitor symptoms related to Parkinson's disease [172], [173], [174]. Based on experiments [31], [66], the injection of stimulation current into the target tissue should lead to the suppression of these beta peaks for the treatment of Parkinson's disease. The auditory brainstem response (ABR) is another method that can be employed in in vivo tests. In this technique, the peripheral hearing nerves are stimulated with sound, resulting in numerous nerve discharges before alteration of nerve potentials [108], [175], [176]. The ABR waveform typically consists of six or seven peaks, which correspond to different auditory structures assessed in the medical and biomedical fields. An electrically elicited auditory brainstem responses (ee-ABR) trigger technique is utilized to verify the functionality of the stimulator. If the peaks are observed in this test, it indicates that the stimulator is working correctly [108].

It is important to note that the loading impedance in the stimulator can vary within a range of ohm, and this should be considered based on factors such as the target tissue, tissue location, distance, stimulation duration, and implantation time. The stimulator should be capable of delivering sufficient currents into the tissue based on the loading impedance. This means that the circuit should be able to adjust voltage levels to accommodate the varying loading impedance.

VI. RESEARCH CHALLENGES AND FUTURE PERSPECTIVES

ENS plays a crucial role in biomedical and bioengineering systems and has emerged as a popular research subject in recent years. Implantable ENS is expected to be a widespread and promising method to treat many neural diseases. As discussed in this review, some principles and trade-offs should be considered in ENS designing based on the target application. One important consideration is the choice of technology, as it directly impacts factors such as power consumption, area, cost, current amplitude, and voltage compliance. Implementing the circuit in a larger process will result in increased power consumption, area, and cost. However, it allows for higher current amplitude, voltage compliance, and reliability. According to recent research, we have recognized some research trends and challenges that we forecast for future designs to optimize performance and enhance the commercial market's embrace of technology.

A. STIMULATION TARGET, METHOD, AND APPLICATION

Paralysis of organs is a common condition affecting many individuals worldwide, with walking or movement disabilities being among the most severe forms. Movement disorders refer to neurological situations categorized by abnormal or difficulty controlling movement. Implantable microsystems, particularly DBS, have emerged as a treatment approach for these disabilities. Non-implanted devices have also been introduced to restore movement in humans [152]. Recent advancements in integrated circuit field have designed and implanted the DBS for various applications, including

Parkinson's disease and epilepsy seizures. However, the treatment of paralysis and movement recovery remains a critical challenge, and future DBS systems are expected to address this issue.

Another area of focus for future stimulators is visual applications aimed at restoring or enhancing functional vision in individuals with visual impairments or blindness. This includes retinal prostheses, visual cortex stimulation, and optogenetic stimulation. Optogenetic stimulation is a cutting-edge field that combines optics and genetics to control neural activity using light-sensitive proteins. It involves genetically modifying cells in the visual system to stimulate target cells or neural pathways involved in vision. Furthermore, future ENS system are expected to incorporate optogenetic stimulation technique to accurately and precisely control neural activities with high temporal and spatial resolution. This approach holds promise for developing new therapies for various neural disorders, such as epilepsy seizures, hearing loss, and Parkinson's disease.

Based on the forecast, a future perspective in target applications involves the potential elimination of drug use for many neurological disorders. Currently, there are numerous medications available for various diseases, particularly psychiatric disorders, but they often come with significant side effects for patients. Moreover, in some cases, drug treatments may be ineffective, and patients may respond poorly to them. Therefore, it is predicted that integrated circuit designers will be motivated to develop stimulators aimed at reducing or eliminating the need for drug-based treatments.

B. TECHNOLOGY

One of the severe challenges in biomedical devices is the ability to be implanted in the human body. This feature is directly influenced by the size and occupation area of the chip. Future trends in ENSs are likely to concentrate on miniaturization and the development of smaller implantable stimulators device. This would enable more flexibility and adaptability in electrode placement, as well as increased customization and targeting options. Therefore, choosing the appropriate technology for implementing the ENS circuit is a critical issue. In addition to size and occupation area, power consumption and cost are two other important factors that need to be carefully considered when selecting the technology. Regarding the mentioned concerns, researchers tend to prefer low-voltage process for designing micro-stimulator due to their smaller occupation area, lower power consumption, and reduced cost. Recent studies have shown the implementation of ENS circuits in 65nm LV CMOS, occupying a total area of 0.225 and 0.7 mm^2 for a 16-channel stimulator [76], [130]. These designs achieved a significant voltage compliance of 11V. It is expected that bioengineers will increasingly utilize low-voltage deep sub-micron technologies, such as 180nm and 65nm, to design ENS devices in the coming years. They may also employ unique techniques, such as transistor stacking to enhance the voltage tolerance and reliability of the transistors. However, it should be noted that, in certain cases, HV process may be adopted when a higher voltage is required to deliver tissue stimulation at higher current levels, surpassing the tolerance of low-voltage technologies. For example, according to Table 3, the stimulator in [97] utilized HV 180nm CMOS with a high voltage compliance and current amplitude of 40V and 12.75mA, respectively. However, it occupied a large area of 30.25mm^2.

C. TOPOLOGY OF THE ENS

According to the information provided in Table 3 most stimulators have been designed in the constant current mode. This mode delivers a consistent current to the neural tissue, making the stimulator independent of impedance variations and other factors that could influence the stimulation. Constant current stimulators offer several advantages, including higher stimulation precision, stability, reliability, patient safety, adaptability to tissue changes, compatibility with electrode arrays, and flexibility in programming. Given these advantages, it is expected that stimulator designers will continue to prefer the use of constant current mode topology and work on addressing challenges associated with this mode in the future. Biomedical engineers may focus on implementing constant current stimulators while considering certain aspects, such as closed-loop current regulation and adaptive control of the current. These measures would ensure consistent and precise stimulation delivery of stimulation to the tissue.

D. EFFICIENCY

Considering the results in Table 3, it appears that efficiency is an important parameter that has barely been paid attention to in ENS design. Also, preferring constant current mode over constant voltage mode, which is more efficient, leads to dealing with improving efficiency by employing some novel methods. Based on our expectations, new neurostimulator topologies will focus on improving power efficiency by adopting advanced techniques. Future stimulator structures are predicted to incorporate energy harvesting techniques and advanced power management systems. Energy harvesting methods, including wireless recharging or converting body heat or motion to energy to supply the stimulator, lead to decreasing or eliminating the requirement for frequent battery replacement or recharging. Employing this technique increases patient convenience and reduces the burden of device maintenance. Since the stimulator's lifetime is a vital necessity, improving efficiency and using efficient power management systems will optimize energy consumption, consequently enhancing the longevity and convenience of neurostimulator devices and extending the operating lifespan of the neurostimulator.

E. CHARGE MISMATCH

The future trends in charge mismatch and safe stimulation of neurostimulators will concentrate on enhancing the accuracy, precision, and safety of neuro-stimulators. The discrepancy between the amount of delivered charge during the cathodic and anodic phases of electrical stimulation causes charge

mismatch. More charge mismatch may harm the tissue for long-term stimulation. Considering the reported result in Table 3, the designed stimulators achieved a charge mismatch of less than 1%, which results in a high accuracy and decreases the probability of tissue damage. Future stimulators aim to develop advanced charge-balancing techniques to have high-precision charge equity between the anodic and cathodic phases and minimize charge mismatch for safe long-term stimulation. We expect that designers utilize high output impedance and precise current mirrors for the output stage, design the switches on the output stage with minimum mismatch for both cathodic and anodic current paths, perform novel active approach and closed-loop stimulation to monitor the residual voltage on the tissue continuously to reach as less as possible charge mismatch. These techniques involve adjusting stimulation parameters, such as pulse width, amplitude, and electrode configurations, to achieve balanced charge delivery, thereby reducing the potential for tissue damage and unwanted side effects.

VII. CONCLUSION

Due to their capability to treat numerous neurological disorders, implantable electrical neural stimulators have attracted much attention in recent years. Biomedical engineers employed various methods to implement these circuits using deep sub-micron CMOS technology, providing a promising therapeutic technique for patients suffering from neural diseases. These implantable devices have the potential to serve as a promising solution for treating certain neural dysfunctions of the peripheral and central nervous system, for which there are currently no available or curative treatments. In this paper, we reviewed the fundamental principles, operation principles, design considerations, and performance metrics in electrical neural stimulation and stimulators. Furthermore, we discussed the advanced circuits and systems for electrical neural stimulators, considering the most critical concerns in their design. In addition, practical results and experiment methods were explained. Finally, we conclude the paper by describing future research challenges and perspectives that are essential in the coming years. Addressing these issues is expected to improve the design parameters of electrical neural stimulators for the next generation of implantable biomedical devices, thereby increasing the accuracy of treatment for patients.

REFERENCES

[1] S. Bhunia, S. J. A. Majerus, and M. Sawan, *Implantable Biomedical Microsystems*. Amsterdam, The Netherlands: Elsevier, 2015.

[2] K. Ashkan, P. Rogers, H. Bergman, and I. Ughratdar, "Insights into the mechanisms of deep brain stimulation," *Nature Rev. Neurol.*, vol. 13, no. 9, pp. 548–554, Sep. 2017.

[3] A. M. Lozano, N. Lipsman, H. Bergman, P. Brown, S. Chabardes, J. W. Chang, K. Matthews, C. C. McIntyre, T. E. Schlaepfer, M. Schulder, Y. Temel, J. Volkmann, and J. K. Krauss, "Deep brain stimulation: Current challenges and future directions," *Nat. Rev. Neurol.*, vol. 15, no. 3, pp. 148–160, Mar. 2019.

[4] C. Sinclair, P. Verrills, and A. Barnard, "A review of spinal cord stimulation systems for chronic pain," *J. Pain Res.*, vol. 9, pp. 481–492, Jul. 2016.

[5] P. Limousin and T. Foltynie, "Long-term outcomes of deep brain stimulation in Parkinson disease," *Nature Rev. Neurol.*, vol. 15, no. 4, pp. 234–242, Apr. 2019.

[6] N. Zangiabadi, L. D. Ladino, F. Sina, J. P. Orozco-Hernández, A. Carter, and J. F. Téllez-Zenteno, "Deep brain stimulation and drug-resistant epilepsy: A review of the literature," *Frontiers Neurol.*, vol. 10, p. 601, Jun. 2019.

[7] M. D. Bigelow and A. Z. Kouzani, "Neural stimulation systems for the control of refractory epilepsy: A review," *J. Neuroeng. Rehabil.*, vol. 16, no. 1, p. 126, Dec. 2019.

[8] R. Collu, E. J. Earley, M. Barbaro, and M. Ortiz-Catalan, "Non-rectangular neurostimulation waveforms elicit varied sensation quality and perceptive fields on the hand," *Sci. Rep.*, vol. 13, no. 1, p. 1588, Jan. 2023.

[9] S.-Y. Lee, C.-H. Hsieh, and C.-M. Yang, "Wireless front-end with power management for an implantable cardiac microstimulator," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 1, pp. 28–38, Feb. 2012.

[10] P. T. Bhatti and K. D. Wise, "A 32-site 4-channel high-density electrode array for a cochlear prosthesis," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2965–2973, Dec. 2006.

[11] M. Yip, R. Jin, H. H. Nakajima, K. M. Stankovic, and A. P. Chandrakasan, "A fully-implantable cochlear implant SoC with piezoelectric middle-ear sensor and arbitrary waveform neural stimulation," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 214–229, Jan. 2015.

[12] H. Ulusan, S. Chamanian, B. Ilik, A. Muhtaroglu, and H. Kulah, "Fully implantable cochlear implant interface electronics with 51.2-μW front-end circuit," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 7, pp. 1504–1512, Jul. 2019.

[13] R. K. Shepherd, "Chronic electrical stimulation of the auditory nerve using non-charge-balanced stimuli," *Acta Oto-Laryngologica*, vol. 119, no. 6, pp. 674–684, Jan. 1999.

[14] M. Dorman and B. Wilson, "The design and function of cochlear implants," *Amer. Sci.*, vol. 92, no. 5, p. 436, 2004.

[15] B. S. Wilson, "Cochlear implants: Current designs and future possibilities," *J. Rehabil. Res. Develop.*, vol. 45, no. 5, pp. 695–730, Dec. 2008.

[16] E. Bloch, Y. Luo, and L. da Cruz, "Advances in retinal prosthesis systems," *Therapeutic Adv. Ophthalmol.*, vol. 11, Jan. 2019, Art. no. 251584141881750.

[17] C.-Y. Lin, W.-L. Chen, and M.-D. Ker, "Implantable stimulator for epileptic seizure suppression with loading impedance adaptability," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 196–203, Apr. 2013.

[18] C.-H. Cheng, P.-Y. Tsai, T.-Y. Yang, W.-H. Cheng, T.-Y. Yen, Z. Luo, X.-H. Qian, Z.-X. Chen, T.-H. Lin, W.-H. Chen, W.-M. Chen, S.-F. Liang, F.-Z. Shaw, C.-S. Chang, Y.-L. Hsin, C.-Y. Lee, M.-D. Ker, and C.-Y. Wu, "A fully integrated 16-channel closed-loop neural-prosthetic CMOS SoC with wireless power and bidirectional data telemetry for real-time efficient human epileptic seizure control," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3314–3326, Nov. 2018.

[19] I. Williams and T. G. Constandinou, "An energy-efficient, dynamic voltage scaling neural stimulator for a proprioceptive prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 129–139, Apr. 2013.

[20] P. Khong, A. Lazzaro, and R. Mobbs, "Phrenic nerve stimulation: The Australian experience," *J. Clin. Neurosci.*, vol. 17, no. 2, pp. 205–208, Feb. 2010.

[21] T. G. Constandinou, J. Georgiou, and C. Toumazou, "A partial-current-steering biphasic stimulation driver for vestibular prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 2, pp. 106–113, Jun. 2008.

[22] Y. Tao and A. Hierlemann, "A 15-channel 30-V neural stimulator for spinal cord repair," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 10, pp. 2185–2189, Oct. 2018.

[23] P. H. Peckham and K. L. Kilgore, "Challenges and opportunities in restoring function after paralysis," *IEEE Trans. Biomed. Eng.*, vol. 60, no. 3, pp. 602–609, Mar. 2013.

[24] R. van den Brand, J. Heutschi, Q. Barraud, J. DiGiovanna, K. Bartholdi, M. Huerlimann, L. Friedli, I. Vollenweider, E. M. Moraud, S. Duis, N. Dominici, S. Micera, P. Musienko, and G. Courtine, "Restoring voluntary control of locomotion after paralyzing spinal cord injury," *Science*, vol. 336, no. 6085, pp. 1182–1185, Jun. 2012.

[25] N. Wenger, E. M. Moraud, S. Raspopovic, M. Bonizzato, J. DiGiovanna, P. Musienko, M. Morari, S. Micera, and G. Courtine, "Closed-loop neuromodulation of spinal sensorimotor circuits controls refined locomotion after complete spinal cord injury," *Sci. Transl. Med.*, vol. 6, no. 255, Sep. 2014, Art. no. 255ra133.

[26] E. Rouhani and A. Erfanian, "Block-based robust control of stepping using intraspinal microstimulation," *J. Neural Eng.*, vol. 15, no. 4, Aug. 2018, Art. no. 046026.

[27] R. L. Hart, N. Bhadra, F. W. Montague, K. L. Kilgore, and P. H. Peckham, "Design and testing of an advanced implantable neuroprosthesis with myoelectric control," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 19, no. 1, pp. 45–53, Feb. 2011.

[28] M. V. Simon, M. R. Nuwer, and A. Szelényi, "Electroencephalography, electrocorticography, and cortical stimulation techniques," in *Handbook of Clinical Neurology*. Amsterdam, The Netherlands: Elsevier, 2022, pp. 11–38.

[29] H. D. Simpson, A. Schulze-Bonhage, G. D. Cascino, R. S. Fisher, B. C. Jobst, M. R. Sperling, and B. N. Lundstrom, "Practical considerations in epilepsy neurostimulation," *Epilepsia*, vol. 63, no. 10, pp. 2445–2460, Oct. 2022.

[30] S. Abdollahifard, A. Farrokhi, S. Mosalamiaghili, K. Assadian, O. Yousefi, and A. Razmkon, "Constant current or constant voltage deep brain stimulation: Short answers to a long story," *Acta Neurologica Belgica*, vol. 123, no. 1, pp. 1–8, Feb. 2023.

[31] C.-C. Hsieh, Y.-H. Wu, and M.-D. Ker, "Design of dual-configuration dual-mode stimulator in low-voltage CMOS process for neuromodulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 17, no. 2, pp. 273–285, Apr. 2023.

[32] S. Luan and T. G. Constandinou, "A charge-metering method for voltage-mode neural stimulation," *J. Neurosci. Methods*, vol. 224, pp. 39–47, Mar. 2014.

[33] S. Little, A. Pogosyan, S. Neal, B. Zavala, L. Zrinzo, M. Hariz, T. Foltynie, P. Limousin, K. Ashkan, J. FitzGerald, A. L. Green, T. Z. Aziz, and M. A. P. Brown, "Adaptive deep brain stimulation in advanced Parkinson disease," *Ann. Neurol.*, vol. 74, no. 3, pp. 449–457, Sep. 2013.

[34] T. Kombos, O. Suess, T. Funk, B. Kern, and M. Brock, "Intra-operative mapping of the motor cortex during surgery in and around the motor cortex," *Acta Neurochirurgica*, vol. 142, no. 3, pp. 263–268, Mar. 2000.

[35] A. Polak, A. Franek, and J. Taradaj, "High-voltage pulsed current electrical stimulation in wound treatment," *Adv. Wound Care*, vol. 3, no. 2, pp. 104–117, Feb. 2014.

[36] M. Monge, M. Raj, M. H. Nazari, H.-C. Chang, Y. Zhao, J. D. Weiland, M. S. Humayun, Y.-C. Tai, and A. Emami, "A fully intraocular high-density self-calibrating epiretinal prosthesis," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 747–760, Dec. 2013.

[37] M. Ghovanloo and K. Najafi, "A compact large voltage-compliance high output-impedance programmable current source for implantable microstimulators," *IEEE Trans. Biomed. Eng.*, vol. 52, no. 1, pp. 97–105, Jan. 2005.

[38] N. Butz, A. Taschwer, S. Nessler, Y. Manoli, and M. Kuhl, "A 22 V compliant 56 μW twin-track active charge balancing enabling 100% charge compensation even in monophasic and 36% amplitude correction in biphasic neural stimulators," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2298–2310, Aug. 2018.

[39] Z. Luo and M.-D. Ker, "A high-voltage-tolerant and precise charge-balanced neuro-stimulator in low voltage CMOS process," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 6, pp. 1087–1099, Dec. 2016.

[40] F. P. Aplin and G. Y. Fridman, "Implantable direct current neural modulation: Theory, feasibility, and efficacy," *Frontiers Neurosci.*, vol. 13, p. 379, Apr. 2019.

[41] K. A. Sillay, P. Rutecki, K. Cicora, G. Worrell, J. Drazkowski, J. J. Shih, A. D. Sharan, M. J. Morrell, J. Williams, and B. Wingeier, "Long-term measurement of impedance in chronically implanted depth and subdural electrodes during responsive neurostimulation in humans," *Brain Stimulation*, vol. 6, no. 5, pp. 718–726, Sep. 2013.

[42] X. F. Wei and W. M. Grill, "Impedance characteristics of deep brain stimulation electrodesin vitroandin vivo," *J. Neural Eng.*, vol. 6, no. 4, Aug. 2009, Art. no. 046008.

[43] J. Dragas, V. Viswam, A. Shadmani, Y. Chen, R. Bounik, A. Stettler, M. Radivojevic, S. Geissler, M. E. J. Obien, J. Müller, and A. Hierlemann, "In vitro multi-functional microelectrode array featuring 59 760 electrodes, 2048 electrophysiology channels, stimulation, impedance measurement, and neurotransmitter detection channels," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1576–1590, Jun. 2017.

[44] M. Ortmanns, A. Rocke, M. Gehrke, and H.-J. Tiedtke, "A 232-channel epiretinal stimulator ASIC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2946–2959, Dec. 2007.

[45] W. Lemaire, M. Benhouria, K. Koua, M. Besrour, L.-P. Gauthier, G. Martin-Hardy, T. Rossignol, S. Roy, and R. Fontaine, "Retinal stimulator ASIC architecture based on a joint power and data optical link," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2158–2170, Jul. 2021.

[46] D. R. Merrill, M. Bikson, and J. G. R. Jefferys, "Electrical stimulation of excitable tissue: Design of efficacious and safe protocols," *J. Neurosci. Methods*, vol. 141, no. 2, pp. 171–198, Feb. 2005.

[47] A. Scheiner, J. T. Mortimer, and U. Roessmann, "Imbalanced biphasic electrical stimulation: Muscle tissue damage," *Ann. Biomed. Eng.*, vol. 18, no. 4, pp. 407–425, Jul. 1990.

[48] P. H. Gorman and J. T. Mortimer, "The effect of stimulus parameters on the recruitment characteristics of direct nerve stimulation," *IEEE Trans. Biomed. Eng.*, vol. BME-30, no. 7, pp. 407–414, Jul. 1983.

[49] R. Shirafkan and O. Shoaei, "Current-based neurostimulation circuit and system techniques," in *Handbook of Biochips*. New York, NY, USA: Springer, 2020, pp. 1–26.

[50] M. Ghovanloo, "Switched-capacitor based implantable low-power wireless microstimulating systems," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2006, pp. 1–4.

[51] J. Simpson and M. Ghovanloo, "An experimental study of voltage, current, and charge controlled stimulation front-end circuitry," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2007, pp. 325–328.

[52] H.-M. Lee, K.-Y. Kwon, W. Li, and M. Ghovanloo, "24.2 a power-efficient switched-capacitor stimulating system for electrical/optical deep-brain stimulation," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2014, pp. 414–415.

[53] J. E. B. Randles, "Kinetics of rapid electrode reactions," *Discuss. Faraday Soc.*, vol. 1, p. 11, Jan. 1947.

[54] R. Reeves, "Interfacial electrochemistry: An experimental approach by E. Gileadi, E. Kirowa-Eisner and J. Peniciner, Addison-Wesley, London, 1975, XII + 522 pages, Price: Hardbound $10.75, paperbound $7.45," *J. Electroanal. Chem.*, vol. 73, no. 1, pp. 123–124, Oct. 1976.

[55] A. J. Bard and L. R. Faulkner, *Electrochemical Methods: Fundamentals and Applications*. New York, NY, USA: Wiley, 2001.

[56] T. Cheung, M. Nuño, M. Hoffman, M. Katz, C. Kilbane, R. Alterman, and M. Tagliati, "Longitudinal impedance variability in patients with chronically implanted DBS devices," *Brain Stimulation*, vol. 6, no. 5, pp. 746–751, Sep. 2013.

[57] K. Chen, Z. Yang, L. Hoang, J. Weiland, M. Humayun, and W. Liu, "An integrated 256-channel epiretinal prosthesis," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1946–1956, Sep. 2010.

[58] D. Jiang, A. Demosthenous, T. Perkins, X. Liu, and N. Donaldson, "A stimulator ASIC featuring versatile management for vestibular prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 2, pp. 147–159, Apr. 2011.

[59] M. N. van Dongen and W. A. Serdijn, "A power-efficient multichannel neural stimulator using high-frequency pulsed excitation from an unfiltered dynamic supply," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 61–71, Feb. 2016.

[60] M. Hasanuzzaman, B. G. Motlagh, F. Mounaim, A. Hassan, R. Raut, and M. Sawan, "Toward an energy-efficient high-voltage compliant visual intracortical multichannel stimulator," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 5, pp. 878–891, May 2018.

[61] M. Haas, P. Vogelmann, and M. Ortmanns, "A neuromodulator frontend with reconfigurable class-B current and voltage controlled stimulator," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 3, pp. 54–57, Mar. 2018.

[62] Y. Wu, D. Jiang, and A. Demosthenous, "A multi-channel stimulator with high-resolution time-to-current conversion for vagal-cardiac neuromodulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 6, pp. 1186–1195, Dec. 2021.

[63] M. Feyerick and W. Dehaene, "An 11 V-tolerant, high-density neurostimulator using time-domain calibration in 65 nm CMOS," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Oct. 2022, pp. 429–433.

[64] T. Yousefi, K. Timonina, G. Zoidl, and H. Kassiri, "An implantable optogenetic neuro-stimulator SoC with extended optical pulse-width enabled by supply-variation-immune cycled light-toggling stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 16, no. 4, pp. 557–569, Aug. 2022.

[65] G. L. K. Moganti, V. N. S. Praneeth, and S. R. K. Vanjari, "A hybrid bipolar active charge balancing technique with adaptive electrode tissue interface (ETI) impedance variations for facial paralysis patients," *Sensors*, vol. 22, no. 5, p. 1756, Feb. 2022.

[66] C.-C. Hsieh and M.-D. Ker, "Monopolar biphasic stimulator with discharge function and negative level shifter for neuromodulation SoC integration in low-voltage CMOS process," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 3, pp. 568–579, Jun. 2021.

[67] X. Liu, "A closed-loop bidirectional brain-machine interface system for freely behaving animals," Ph.D. thesis, Univ. Pennsylvania, Philadelphia, PA, USA, 2017.

[68] N. Butz, U. Kalita, and Y. Manoli, "Active charge balancer with adaptive 3.3 V to 38 V supply compliance for neural stimulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 10, pp. 4013–4024, Oct. 2021.

[69] E. Noorsal, K. Sooksood, H. Xu, R. Hornig, J. Becker, and M. Ortmanns, "A neural stimulator frontend with high-voltage compliance and programmable pulse shape for epiretinal implants," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 244–256, Jan. 2012.

[70] K. Sooksood, E. Noorsal, J. Becker, and M. Ortmanns, "A neural stimulator front-end with arbitrary pulse shape, HV compliance and adaptive supply requiring 0.05 mm^2 in 0.35 μm HVCMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2011, pp. 306–308.

[71] Z. Luo, M.-D. Ker, T.-Y. Yang, and W.-H. Cheng, "A digitally dynamic power supply technique for 16-channel 12 V-tolerant stimulator realized in a 0.18-μm 1.8-V/3.3-V low-voltage CMOS process," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 5, pp. 1087–1096, Oct. 2017.

[72] Z. Luo and M.-D. Ker, "A high-voltage-tolerant and power-efficient stimulator with adaptive power supply realized in low-voltage CMOS process for implantable biomedical applications," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 8, no. 2, pp. 178–186, Jun. 2018.

[73] C. Robillard, J. Coulombe, P. Nadeau, and M. Sawan, "Neural stimulation safety and energy efficiency: Waveform analysis and validation," in *Proc. 11th Annu. Conf. Int. FES Soc.*, Jan. 2006, pp. 94–96.

[74] A. Wongsarnpigoon, J. P. Woock, and W. M. Grill, "Efficiency analysis of waveform shape for electrical excitation of nerve fibers," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 18, no. 3, pp. 319–328, Jun. 2010.

[75] M. Hosseinnejad, M. Katebi, A. Erfanian, and M. A. Karami, "A 2-mA charge-balanced neurostimulator in 0.18-μm/1.8 V standard CMOS process," *Int. J. Circuit Theory Appl.*, vol. 51, no. 3, pp. 1092–1109, Mar. 2023.

[76] M. Feyerick and W. Dehaene, "Dense, 11 V-tolerant, balanced stimulator IC with digital time-domain calibration for <100 nA error," *IEEE Trans. Biomed. Circuits Syst.*, vol. 17, no. 5, pp. 1166–1176, Oct. 2023.

[77] H. Chun, Y. Yang, and T. Lehmann, "Safety ensuring retinal prosthesis with precise charge balance and low power consumption," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 1, pp. 108–118, Feb. 2014.

[78] M.-D. Ker, C.-Y. Lin, and W.-L. Chen, "Stimulus driver for epilepsy seizure suppression with adaptive loading impedance," *J. Neural Eng.*, vol. 8, no. 6, Oct. 2011, Art. no. 066008.

[79] X. Liu, L. Yao, K. A. Ng, P. Li, W. Wang, M. Je, and Y. P. Xu, "A power-efficient current-mode neural/muscular stimulator design for peripheral nerve prosthesis," *Int. J. Circuit Theory Appl.*, vol. 46, no. 4, pp. 692–706, Apr. 2018.

[80] M. Shoaran, M. Shahshahani, M. Farivar, J. Almajano, A. Shahshahani, A. Schmid, A. Bragin, Y. Leblebici, and A. Emami, "A 16-channel 1.1 mm^2 implantable seizure control SoC with sub-μW/channel consumption and closed-loop stimulation in 0.18 μm CMOS," in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 1–2.

[81] W.-M. Chen, H. Chiueh, T.-J. Chen, C.-L. Ho, C. Jeng, M.-D. Ker, C.-Y. Lin, Y.-C. Huang, C.-W. Chou, T.-Y. Fan, M.-S. Cheng, Y.-L. Hsin, S.-F. Liang, Y.-L. Wang, F.-Z. Shaw, Y.-H. Huang, C.-H. Yang, and C.-Y. Wu, "A fully integrated 8-channel closed-loop neural-prosthetic CMOS SoC for real-time epileptic seizure control," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 232–247, Jan. 2014.

[82] J.-Y. Son and H.-K. Cha, "An implantable neural stimulator IC with anodic current pulse modulation based active charge balancing," *IEEE Access*, vol. 8, pp. 136449–136458, 2020.

[83] D. B. McCreery, W. F. Agnew, T. G. H. Yuen, and L. Bullara, "Charge density and charge per phase as cofactors in neural injury induced by electrical stimulation," *IEEE Trans. Biomed. Eng.*, vol. 37, no. 10, pp. 996–1001, Oct. 1990.

[84] R. V. Shannon, "A model of safe levels for electrical stimulation," *IEEE Trans. Biomed. Eng.*, vol. 39, no. 4, pp. 424–426, Apr. 1992.

[85] C. M. Zierhofer, I. J. Hochmair-Desoyer, and E. S. Hochmair, "Electronic design of a cochlear implant for multichannel high-rate pulsatile stimulation strategies," *IEEE Trans. Rehabil. Eng.*, vol. 3, no. 1, pp. 112–116, Mar. 1995.

[86] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated implantable stimulator that is fail-safe without off-chip blocking-capacitors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 3, pp. 231–244, Sep. 2008.

[87] B. K. Thurgood, D. J. Warren, N. M. Ledbetter, G. A. Clark, and R. R. Harrison, "A wireless integrated circuit for 100-channel charge-balanced neural stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 6, pp. 405–414, Dec. 2009.

[88] K. Sooksood, T. Stieglitz, and M. Ortmanns, "An active approach for charge balancing in functional electrical stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 162–170, Jun. 2010.

[89] P. J. Langlois, A. Demosthenous, I. Pachnis, and N. Donaldson, "High-power integrated stimulator output stages with floating discharge over a wide voltage range for nerve stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 1, pp. 39–48, Feb. 2010.

[90] K. Song, H. Lee, S. Hong, H. Cho, U. Ha, and H.-J. Yoo, "A sub-10 nA DC-balanced adaptive stimulator IC with multi-modal sensor for compact electro-acupuncture stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 6, pp. 533–541, Dec. 2012.

[91] E. Greenwald, E. So, Q. Wang, M. Mollazadeh, C. Maier, R. Etienne-Cummings, G. Cauwenberghs, and N. Thakor, "A bidirectional neural interface IC with chopper stabilized BioADC array and charge balanced stimulator," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 5, pp. 990–1002, Oct. 2016.

[92] E. Greenwald, C. Maier, Q. Wang, R. Beaulieu, R. Etienne-Cummings, G. Cauwenberghs, and N. Thakor, "A CMOS current steering neurostimulation array with integrated DAC calibration and charge balancing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 2, pp. 324–335, Apr. 2017.

[93] C. A. Gong, K. Yao, and M. Shiue, "A CMOS multichannel electrical stimulation prototype system," *Int. J. Circuit Theory Appl.*, vol. 41, no. 3, pp. 238–258, Mar. 2013.

[94] M. Ghovanloo and K. Najafi, "A wireless implantable multichannel microstimulating system-on-a-chip with modular architecture," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 15, no. 3, pp. 449–457, Sep. 2007.

[95] A. Rothermel, L. Liu, N. P. Aryan, M. Fischer, J. Wuenschmann, S. Kibbel, and A. Harscher, "A CMOS chip with active pixel array and specific test features for subretinal implantation," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 290–300, Jan. 2009.

[96] H.-M. Lee, H. Park, and M. Ghovanloo, "A power-efficient wireless system with adaptive supply control for deep brain stimulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2203–2216, Sep. 2013.

[97] H. Pu, O. Malekzadeh-Arasteh, A. R. Danesh, Z. Nenadic, A. H. Do, and P. Heydari, "A CMOS dual-mode brain–computer interface chipset with 2-mV precision time-based charge balancing and stimulation-side artifact suppression," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1824–1840, Jun. 2022.

[98] B. Smith, P. H. Peckham, M. W. Keith, and D. D. Roscoe, "An externally powered, multichannel, implantable stimulator for versatile control of paralyzed muscle," *IEEE Trans. Biomed. Eng.*, vol. BME-34, no. 7, pp. 499–508, Jul. 1987.

[99] J.-J. Sit and R. Sarpeshkar, "A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6 nA DC error for 1-mA full-scale stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 172–183, Sep. 2007.

[100] R. Ranjandish, F. Bozorgi, S. Ghanbari, and O. Shoaei, "A precise active charge balancing method for neural stimulators by utilizing polarity changes of the remaining voltage," *Int. J. Appl. Innov. Eng. Manag.*, vol. 3, no. 4, pp. 314–319, 2014.

[101] D. Jiang, D. Cirmirakis, and A. Demosthenous, "A vestibular prosthesis with highly-isolated parallel multichannel stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 1, pp. 124–137, Feb. 2015.

[102] L. Yao, P. Li, and M. Je, "A pulse-width-adaptive active charge balancing circuit with pulse-insertion based residual charge compensation and quantization for electrical stimulation applications," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2015, pp. 1–4.

[103] W.-Y. Hsu and A. Schmid, "Compact, energy-efficient high-frequency switched capacitor neural stimulator with active charge balancing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 4, pp. 878–888, Aug. 2017.

[104] D. Jiang and A. Demosthenous, "A multichannel high-frequency power-isolated neural stimulator with crosstalk reduction," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 4, pp. 940–953, Aug. 2018.

[105] A. Taschwer, N. Butz, M. Köhler, D. Rossbach, and Y. Manoli, "A charge balanced neural stimulator with 3.3 V to 49 V supply compliance and arbitrary programmable current pulse shapes," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Oct. 2018, pp. 1–4.

[106] X. Fu, S. Mai, and Z. Wang, "An energy-efficient implantable-neural-stimulator system with wireless charging and dynamic voltage output," in *Proc. 41st Annu. Int. Conf. IEEE Eng. Med. Biol. Soc. (EMBC)*, Jul. 2019, pp. 3835–3839.

[107] K. Sooksood and E. Noorsal, "A highly compliant current driver for electrical stimulator with compliance monitor and digital controlled offset regulation charge balancing," in *Proc. 8th Int. Electr. Eng. Congr. (iEECON)*, Mar. 2020, pp. 1–4.

[108] T.-Y. Yen and M.-D. Ker, "Design of dual-mode stimulus chip with built-in high voltage generator for biomedical applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 5, pp. 961–970, Oct. 2020.

[109] U. Bihr, T. Ungru, H. Xu, J. Anders, J. Becker, and M. Ortmanns, "A bidirectional neural interface with a HV stimulator and a LV neural amplifier," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2013, pp. 401–404.

[110] E. Noorsal and M. Ortmanns, "An architecture for a universal neural stimulator with almost arbitrary current waveform," in *Proc. Annu. Int. Conf. IEEE Eng. Med. Biol.*, Aug. 2010, pp. 2931–2934.

[111] A. Urso, V. Giagka, M. van Dongen, and W. A. Serdijn, "An ultra high-frequency 8-channel neurostimulator circuit with 68% peak power efficiency," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 5, pp. 882–892, Oct. 2019.

[112] S. Ethier and M. Sawan, "Exponential current pulse generation for efficient very high-impedance multisite stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 1, pp. 30–38, Feb. 2011.

[113] R. Shirafkan and O. Shoaei, "A power efficient, differential multichannel adiabatic electrode stimulator for deep brain stimulation," *Anal. Integr. Circuits Signal Process.*, vol. 95, no. 3, pp. 481–497, Jun. 2018.

[114] K. Arabi and M. A. Sawan, "Electronic design of a multichannel programmable implant for neuromuscular electrical stimulation," *IEEE Trans. Rehabil. Eng.*, vol. 7, no. 2, pp. 204–214, Jun. 1999.

[115] G. J. Suaning and N. H. Lovell, "CMOS neurostimulation ASIC with 100 channels, scaleable output, and bidirectional radio-frequency telemetry," *IEEE Trans. Biomed. Eng.*, vol. 48, no. 2, pp. 248–260, Feb. 2001.

[116] M. Sivaprakasam, W. Liu, M. S. Humayun, and J. D. Weiland, "A variable range bi-phasic current stimulus driver circuitry for an implantable retinal prosthetic device," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 763–771, Mar. 2005.

[117] X. Liu, A. Demosthenous, and N. Donaldson, "A fully integrated fail-safe stimulator output stage dedicated to FES stimulation," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2007, pp. 2076–2079.

[118] J. Lee, H.-G. Rhew, D. R. Kipke, and M. P. Flynn, "A 64 channel programmable closed-loop neurostimulator with 8 channel neural amplifier and logarithmic ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1935–1945, Sep. 2010.

[119] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni, "A battery-powered activity-dependent intracortical microstimulation IC for brain–machine–brain interface," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 731–745, Apr. 2011.

[120] C.-Y. Lin, Y.-J. Li, and M.-D. Ker, "Design of high-voltage-tolerant stimulus driver with adaptive loading consideration to suppress epileptic seizure in a 0.18-μm CMOS process," *Anal. Integr. Circuits Signal Process.*, vol. 79, no. 2, pp. 219–226, May 2014.

[121] R. Erfani, F. Marefat, S. Mandal, and P. Mohseni, "A 1.3 mA biphasic current stimulator IC with active charge balancing for nerve interfacing applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 1090–1093.

[122] A. Abdi and H.-K. Cha, "A bidirectional neural interface CMOS analog front-end IC with embedded isolation switch for implantable devices," *Microelectron. J.*, vol. 58, pp. 70–75, Dec. 2016.

[123] M. H. Maghami, A. M. Sodagar, and M. Sawan, "Versatile stimulation back-end with programmable exponential current pulse shapes for a retinal visual prosthesis," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 24, no. 11, pp. 1243–1253, Nov. 2016.

[124] C.-H. Cheng, P.-Y. Tsai, T.-Y. Yang, W.-H. Cheng, T.-Y. Yen, Z. Luo, X.-H. Qian, Z.-X. Chen, T.-H. Lin, W.-H. Chen, W.-M. Chen, S.-F. Liang, F.-Z. Shaw, C.-S. Chang, F.-Y. Shih, Y.-L. Hsin, C.-Y. Lee, M.-D. Ker, and C.-Y. Wu, "A fully integrated closed-loop neuromodulation SoC with wireless power and bi-directional data telemetry for real-time human epileptic seizure control," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C44–C45.

[125] S. Ha, C. Kim, J. Park, G. Cauwenberghs, and P. P. Mercier, "A fully integrated RF-powered energy-replenishing current-controlled stimulator," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 1, pp. 191–202, Feb. 2019.

[126] F. Eshaghi, E. Najafiaghdam, and H. Kassiri, "A 24-channel neurostimulator IC with one-shot impedance-adaptive channel-specific charge balancing," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2021, pp. 1–2.

[127] F. Eshaghi, E. Najafiaghdam, and H. Kassiri, "A 24-channel neurostimulator IC with channel-specific energy-efficient hybrid preventive-detective dynamic-precision charge balancing," *IEEE Access*, vol. 9, pp. 95884–95895, 2021.

[128] K.-Y. Yeh, H.-W. Chiu, W.-T. Tseng, H.-C. Chen, C.-T. Yen, S.-S. Lu, and M.-L. Lin, "A dual-mode multifunctional pulsed radio-frequency stimulator for trigeminal neuralgia relief and its animal model," *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 4, pp. 719–730, Aug. 2021.

[129] U. Shin, C. Ding, L. Somappa, V. Woods, A. S. Widge, and M. Shoaran, "A 16-channel 60 μW neural synchrony processor for multi-mode phase-locked neurostimulation," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2022, pp. 01–02.

[130] U. Shin, C. Ding, B. Zhu, Y. Vyza, A. Trouillet, E. C. M. Revol, S. P. Lacour, and M. Shoaran, "NeuralTree: A 256-channel 0.227-μJ/class versatile neural activity classification and closed-loop neuromodulation SoC," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3243–3257, Nov. 2022.

[131] M. Sivaprakasam, W. Liu, G. Wang, J. D. Weiland, and M. S. Humayun, "Architecture tradeoffs in high-density microstimulators for retinal prosthesis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2629–2641, Dec. 2005.

[132] J. Coulombe, M. Sawan, and J.-F. Gervais, "A highly flexible system for microstimulation of the visual cortex: Design and implementation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 4, pp. 258–269, Dec. 2007.

[133] W. Liu, K. Vichienchom, M. Clements, S. C. DeMarco, C. Hughes, E. McGucken, M. S. Humayun, E. De Juan, J. D. Weiland, and R. Greenberg, "A neuro-stimulus chip with telemetry unit for retinal prosthetic device," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1487–1497, Oct. 2000.

[134] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated stimulator with DC-isolation and fine current control for implanted nerve tripoles," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1701–1714, Jul. 2011.

[135] R. St-Amand, Y. Savaria, and M. Sawan, "Design optimization of a current source for microstimulator applications," in *Proc. 37th Midwest Symp. Circuits Syst.*, Aug. 1994, pp. 129–132.

[136] K. Sooksood and M. Ortmanns, "Power efficient output stage for high density implantable stimulators," *Electron. Lett.*, vol. 48, no. 10, p. 551, 2012.

[137] F. B. Mooziraji and O. Shoaei, "A high power efficient multi-waveform current stimulator used in implantable neural stimulation," *Anal. Integr. Circuits Signal Process.*, vol. 86, no. 3, pp. 459–469, Mar. 2016.

[138] S. K. Kelly and J. L. Wyatt, "A power-efficient neural tissue stimulator with energy recovery," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 1, pp. 20–29, Feb. 2011.

[139] S. K. Arfin and R. Sarpeshkar, "An energy-efficient, adiabatic electrode stimulator with inductive energy recycling and feedback current regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 1, pp. 1–14, Feb. 2012.

[140] J. H. Park, J. S. Y. Tan, H. Wu, Y. Dong, and J. Yoo, "1225-channel neuromorphic retinal-prosthesis SoC with localized temperature-regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1230–1240, Dec. 2020.

[141] Y. Ding, X. Gu, X. Guo, S. Wu, and H. Lyu, "An 8-channel 9-V-compliant crosstalk-free bipolar biphasic current-controlled neural stimulator in a standard CMOS technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 71, no. 7, pp. 3293–3297, Jul. 2024.

[142] Y. Zhou, K. Wang, S. Yin, W.-Y. Li, F. Meng, Z.-G. Wang, and K. Ma, "A fully integrated stimulator with high stimulation voltage compliance using dynamic bulk biasing technique in a bulk CMOS technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 71, no. 6, pp. 2525–2537, Jun. 2024.

[143] S.-Y. Lee, Z.-X. Liao, I.-T. Feng, H.-Y. Lee, and C.-C. Lin, "Charge-mode neural stimulator with a capacitor-reuse residual charge detector and active charge balancing for epileptic seizure suppression," *IEEE Trans. Biomed. Circuits Syst.*, early access, Mar. 21, 2024, doi: 10.1109/TBCAS.2024.3380055.

[144] K. Cui, Y. Jin, X. Fan, and Y. Ma, "A 3-mV precision dual-mode-controlled fast charge balancing for implantable biphasic neural stimulators," *IEEE Trans. Biomed. Circuits Syst.*, early access, Feb. 23, 2024, doi: 10.1109/TBCAS.2024.3366518.

[145] S. Bourret, M. Sawan, and R. Plamondon, "Programmable high-amplitude balanced stimulus current-source for implantable microstimulators," in *Proc. 19th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc. Magnificent Milestones Emerg. Opportunities Med. Eng.*, Oct. 1997, pp. 1938–1941.

[146] K. W. E. Cheng, Y. Lu, K.-Y. Tong, A. B. Rad, D. H. K. Chow, and D. Sutanto, "Development of a circuit for functional electrical stimulation," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 12, no. 1, pp. 43–47, Mar. 2004.

[147] A. Masdar, B. S. K. K. Ibrahim, and M. M. Abdul Jamil, "Development of wireless-based low-cost current controlled stimulator for patients with spinal cord injuries," in *Proc. IEEE-EMBS Conf. Biomed. Eng. Sci.*, Dec. 2012, pp. 493–498.

[148] H.-C. Wu, S.-T. Young, and T.-S. Kuo, "A versatile multichannel direct-synthesized electrical stimulator for FES applications," *IEEE Trans. Instrum. Meas.*, vol. 51, no. 1, pp. 2–9, Feb. 2002.

[149] M. Yochum, S. Binczak, T. Bakir, S. Jacquir, and R. Lepers, "A mixed FES/EMG system for real time analysis of muscular fatigue," in *Proc. Annu. Int. Conf. IEEE Eng. Med. Biol.*, Aug. 2010, pp. 4882–4885.

[150] H. Qu, T. Wang, M. Hao, P. Shi, W. Zhang, G. Wang, and N. Lan, "Development of a network FES system for stroke rehabilitation," in *Proc. Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, Aug. 2011, pp. 3119–3122.

[151] M. P. Willand and H. de Bruin, "Design and testing of an instrumentation system to reduce stimulus pulse amplitude requirements during FES," in *Proc. 30th Annu. Int. Conf. IEEE Eng. Med. Biol. Soc.*, Aug. 2008, pp. 2764–2767.

[152] S. Khosravani, N. Lahimgarzadeh, and A. Maleki, "Developing a stimulator and an interface for FES-cycling rehabilitation system," in *Proc. 18th Iranian Conf. Biomed. Eng. (ICBME)*, Dec. 2011, pp. 175–180.

[153] F. Brunetti, Á. Garay, J. C. Moreno, and J. L. Pons, "Enhancing functional electrical stimulation for emerging rehabilitation robotics in the framework of hyper project," in *Proc. IEEE Int. Conf. Rehabil. Robot.*, Jun. 2011, pp. 1–6.

[154] M. H. Maghami, A. M. Sodagar, and M. Sawan, "Analysis and design of a high-compliance ultra-high output resistance current mirror employing positive shunt feedback," *Int. J. Circuit Theory Appl.*, vol. 43, no. 12, pp. 1935–1952, Dec. 2015.

[155] K. C. Smith and A. Sedra, "The current conveyor—A new circuit building block," *Proc. IEEE*, vol. 56, no. 8, pp. 1368–1369, Aug. 1968.

[156] A. M. Dymond, L. E. Kaechele, J. M. Jurist, and P. H. Crandall, "Brain tissue reaction to some chronically implanted metals," *J. Neurosurgery*, vol. 33, no. 5, pp. 574–580, Nov. 1970.

[157] R. L. White and T. J. Gross, "An evaluation of the resistance to electrolysis of metals for use in biostimulation microprobes," *IEEE Trans. Biomed. Eng.*, vol. BME-21, no. 6, pp. 487–490, Nov. 1974.

[158] P. F. Johnson and L. L. Hench, "An in vitro analysis of metal electrodes for use in the neural environment," *Brain. Behav. E*, vol. 14, nos. 1–2, pp. 23–45, 1977.

[159] S. B. Brummer and M. J. Turner, "Electrochemical considerations for safe electrical stimulation of the nervous system with platinum electrodes," *IEEE Trans. Biomed. Eng.*, vol. BME-24, no. 1, pp. 59–63, Jan. 1977.

[160] R. C. Black and P. Hannaker, "Dissolution of smooth platinum electrodes in biological fluids," *Stereotactic Funct. Neurosurgery*, vol. 42, no. 6, pp. 366–374, 1979.

[161] J. McHardy, L. S. Robblee, J. M. Marston, and S. B. Brummer, "Electrical stimulation with Pt electrodes. IV. Factors influencing Pt dissolution in inorganic saline," *Biomaterials*, vol. 1, no. 3, pp. 129–134, Jul. 1980.

[162] L. S. Robblee, J. McHardy, J. M. Marston, and S. B. Brummer, "Electrical stimulation with Pt electrodes. V. The effect of protein on pt dissolution," *Biomaterials*, vol. 1, no. 3, pp. 135–139, Jul. 1980.

[163] L. S. Robblee, J. L. Lefko, and S. B. Brummer, "Activated Ir: An electrode suitable for reversible charge injection in saline solution," *J. Electrochemical Soc.*, vol. 130, no. 3, pp. 731–733, Mar. 1983.

[164] S. B. Brummer and M. J. Turner, "Electrical stimulation of the nervous system: The principle of safe charge injection with noble metal electrodes," *Bioelectrochemistry Bioenergetics*, vol. 2, no. 1, pp. 13–25, Jan. 1975.

[165] S. B. Brummer and M. J. Turner, "Electrical stimulation with Pt electrodes: A method for determination of 'real' electrode areas," *IEEE Trans. Biomed. Eng.*, vol. BME-24, no. 5, pp. 436–439, Sep. 1977.

[166] S. B. Brummer and M. J. Turner, "Electrical stimulation with Pt electrodes: II—Estimation of maximum surface redox (theoretical non-gassing) limits," *IEEE Trans. Biomed. Eng.*, vol. BME-24, no. 5, pp. 440–443, Sep. 1977.

[167] L. S. Robblee and T. L. Rose, "Electrochemical guidelines for selection of protocols and electrode materials for neural stimulation," in *Neural Prostheses: Fundamental Studies*. Upper Saddle River, NJ, USA: Prentice-Hall, 1990.

[168] A. B. Majji, M. S. Humayun, J. D. Weiland, S. Suzuki, S. A. D'Anna, and E. de Juan, "Long-term histological and electrophysiological results of an inactive epiretinal electrode array implantation in dogs," *Invest. Ophthalmol. Vis. Sci.*, vol. 40, no. 9, pp. 81–2073, Aug. 1999. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/10440263

[169] C. H. Chouard and P. Pialoux, "[Biocompatibility of cochlear implants]," *Bull. Acad. Nat. Med.*, vol. 179, no. 3, pp. 55–549, Mar. 1995. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/7648301

[170] J. K. Niparko, R. A. Altschuler, J. A. Wiler, X. Xue, and D. J. Anderson, "Surgical implantation and biocompatibility of central nervous system auditory prostheses," *Ann. Otol., Rhinol. Laryngol.*, vol. 98, no. 12, pp. 965–970, Dec. 1989.

[171] J. K. Krauss, N. Lipsman, T. Aziz, A. Boutet, P. Brown, J. W. Chang, B. Davidson, W. M. Grill, M. I. Hariz, A. Horn, M. Schulder, A. Mammis, P. A. Tass, J. Volkmann, and A. M. Lozano, "Technology of deep brain stimulation: Current statusand future directions," *Nature Rev. Neurol.*, vol. 17, pp. 75–87, Nov. 2020.

[172] H.-C. Lin, Y.-H. Wu, C.-W. Huang, and M.-D. Ker, "Verification of the beta oscillations in the subthalamic nucleus of the MPTP-induced parkinsonian minipig model," *Brain Res.*, vol. 1798, Jan. 2023, Art. no. 148165.

[173] J. G. V. Habets, M. Heijmans, M. L. Kuijf, M. L. F. Janssen, Y. Temel, and P. L. Kubben, "An update on adaptive deep brain stimulation in Parkinson'sdisease," *Movement Disorders*, vol. 33, no. 12, pp. 1834–1843, Dec. 2018.

[174] A. C. Meidahl, G. Tinkhauser, D. M. Herz, H. Cagnan, J. Debarros, and P. Brown, "Adaptive deep brain stimulation for movement disorders: The long road to clinical therapy," *Movement Disorders*, vol. 32, no. 6, pp. 810–819, Jun. 2017.

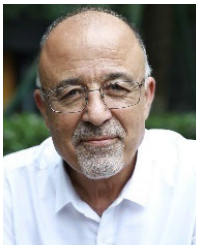
[175] S. Gallégo, E. Truy, A. Morgon, and L. Collet, "EABRs and surface potentials with a transcutaneous multielectrode cochlear implant," *Acta Oto-Laryngologica*, vol. 117, no. 2, pp. 164–168, Jan. 1997.

[176] X.-H. Qian et al., "Design and in vivo verification of a CMOS bone-guided cochlear implant microsystem," *IEEE Trans. Biomed. Eng.*, vol. 66, no. 11, pp. 3156–3167, Nov. 2019.

MOSTAFA KATEBI (Member, IEEE) received the bachelor's and master's degrees from the Department of Electrical Engineering, University of Zanjan, Zanjan, Iran, in 2015 and 2018, respectively. He is currently pursuing the Ph.D. degree with Iran University of Science and Technology. He was a Lecturer (as a Teaching Assistant) with the University of Zanjan, from 2014 to 2018. He joined the CenBRAIN Neurotech Center of Excellence, as a Visiting Ph.D. Student, in 2023. His research interests include implantable electrical neural stimulators, including RF and mixed-mode integrated circuits and microwave power amplifiers. He is focusing on designing an electrical stimulation system that includes a front-end rectifier, a regulator, a charge pump, a control unit, and an output stage forming the main core of the stimulator.

ABBAS ERFANIAN (Member, IEEE) received the B.Sc. degree in computer engineering from Shiraz University, Shiraz, Iran, in 1985, the M.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1989, and the Ph.D. degree in biomedical engineering from Tarbiat Modarres University, Tehran, in 1995. He was a Senior Research Associate with Case Western Reserve University, Cleveland, OH, from 1993 to 1994, and Veterans Affairs Medical Center, Cleveland, where he did research in the area of functional electrical stimulation and neuromuscular control systems. Since 1995, he has been a Faculty Member with the Iran University of Science and Technology, Tehran, serving as Head of the Department of Biomedical Engineering from 2000 to 2008. Currently, he is a Professor of Biomedical Engineering and the Director of Iran Neural Technology Center, Tehran. He is also working on the decoding limb kinematics information from the neural signals recorded from the dorsal horn and dorsal column within the spinal cord as well as from the ECoG signals. His research is in the area of control of intraspinal microstimulation for restoring motor function and restoring bladder function, seizure detection and prediction, seizure suppression as well as treatment of Parkinson's disease using closed-loop control of deep brain stimulation.

MOHAMMAD AZIM KARAMI (Member, IEEE) received the B.Sc. degree from Shahid Beheshti University, Tehran, Iran, the M.Sc. degree from University of Tehran, Iran, and the Ph.D. degree from the Technical University of Delft, Delft, The Netherlands, in 2011. Since 2011, he has been with the School of Electrical Engineering, Iran University of Science and Technology (IUST), Tehran, where he has been the Head since 2021 and is an Associate Professor. His main research focus is on optoelectronic devices and systems.



MOHAMAD SAWAN (Life Fellow, IEEE) received the Ph.D. degree from the University of Sherbrooke, Canada. He is currently a Chair Professor with Westlake University, Hangzhou, China, and an Emeritus Professor with Polytechnique Montréal, Canada. He is the Founder and the Director of the Centre of Excellence in Biomedical Research of Advanced Integrated-on-Chips Neurotechnologies (CenBRAIN Neurotech), Westlake University, and the Polystim Neurotech Laboratory, Polytechnique Montréal. He published more than 1000 peer-reviewed articles, five books, 15 book chapters, 15 awarded, and 25 pending patents. He is a fellow of Canadian Academy of Engineering, a fellow of the Engineering Institutes of Canada, and an Officer of the National Order of Quebec. He was awarded Canada Research Chair in Smart Medical Devices, from 2001 to 2015, and led the Microsystems Strategic Alliance of Quebec, Canada, from 1999 to 2018. He received several awards, including the Queen Elizabeth II Golden Jubilee Medal, Shanghai International Collaboration Award, Zhejiang Westlake Friendship Award, Qianjiang Friendship Ambassador Award, and the Medal of Merit from the President of Lebanon. He was the General Chair of the 2016 IEEE International Symposium on Circuits and Systems and the 2020 IEEE International Medicine, Biology, and Engineering Conference (EMBC). He was the VP of the Publications of IEEE Circuits and Systems Society, from 2019 to 2022. He is the Co-Founder, an Associate Editor, and was the Editor-in-Chief of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, from 2016 to 2019. He is the Co-Founder of the International IEEE-NEWCAS and the International IEEE-BioCAS Conference.