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RESEARCH ARTICLE

Analysis and Design of SiC Three-Phase Four-Wire Five-Level E-Type STATCOM Inverter

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ABSTRACT In power quality applications, the long-term reliability, low maintenance cost, and low volume and weight of a STATCOM converter are of the paramount importance. The use of the series multi-level power converter topology can significantly improve both volumetric and gravimetric density as well as power conversion efficiency of the STATCOM converter. This paper presents a solution that utilizes the Novel 5 Level E Type topology for the 3-phase, 4-wire STATCOM power quality applications. A comprehensive theoretical analysis and step-by-step design process are presented and discussed in the paper. A proof of the concept prototype (12kVA 3 × 400.230V) has been designed, manufactured, and intensively tested and experimentally verified. The experimental results are discussed in detail and compared with state-of-the-art solutions from both academic and industrial sectors. The achieved improvements in volumetric and gravimetric density, along with ultra-high power conversion efficiency and reduced cooling effort, justifies significant benefits of the proposed topology and approach.

INDEX TERMS STATCOM, multi-level, power converter, VSI, dc bus voltage balancer.

I. INTRODUCTION

Today's electrical distribution networks are subject to various power quality issues. Power quality issues are mainly caused by unbalanced and non-linear loads, by the presence of excessive neutral current or currents with DC offset, by voltage imbalance. To mitigate power quality issues, nowadays a power quality conditioner is often used that is capable of correcting or eliminating power quality issues. For low-voltage distribution networks, the most state-of-the-art power quality conditioners are based on 2- or 3-level power converter topologies. However, with the ever-evolving requirements to achieve more efficient and compact power conversion system, the multi-level conversion has become more interesting approach to meet the requirements. The multi-level conversion has been a subject of extensive research over the years for wide range of applications, e.g., high-voltage dc transmission, flexible ac transmission systems, adjustable speed drives, active front-end converters, etc., [1], [2], [3]. The main advantages of the multilevel topologies are as follows. The ability to handle high voltage and higher power levels by reducing stress on components. Furthermore, higher partial load and overall conversion efficiency, resulting in less cooling effort. Then, the smoother output waveforms compared to traditional converters, consequently better harmonic content and reduced AC harmonics related losses in AC magnetics and lower electromagnetic interference (EMI).

With multiple voltage levels distributed the stress on power electronic components more evenly, such as semiconductors devices, AC filter and DC bus capacitors. This can lead to increased reliability and extended lifespan for those components.

In addition, a use of multi-level conversion leads to reduction of the size and volume of the power converter, by reducing size of magnetics, capacitors and heatsink or

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cooling effort in general. Thus, the reduction of the gravimetric and volumetric density or the amount of power that can be handled per unit mass and per unit volume respectively. While multi-level converters offer several advantages, they also come with additional complexity such as increased controls complexity by requiring more sophisticated control algorithms to generate the multiple voltage levels. Furthermore, achieving and maintaining voltage balance across the different levels, especially balancing the voltages across series connected DC bus capacitors. Also driving multiple power semiconductor devices adds complexity to the gate driver design, as well as protection and fault management. Finally increased number of components can lead to higher costs and theoretically increased probability of component failures.

Despite these complexities, advancements in control algorithms, semiconductor technology, and manufacturing processes have been made to address these challenges.

STATCOM, a form of power quality conditioner for power quality applications, can supply or absorb reactive power as needed to maintain desired voltage levels in the power system. Reactive power is essential for voltage support and stability. The STATCOM can dynamically adjust its output reactive current to compensate for changes in grid conditions by quickly responding to voltage fluctuations and providing the necessary reactive power to keep the voltage within acceptable limits. With penetration of renewable energy sources, such as wind and solar, which are integrated into the power grid, the variability of those sources can impact grid stability. Thus, STATCOMs can help smooth out fluctuations caused by renewable generation and maintain the system stability.

Moreover, the STATCOM can improve power factor, and therefore reduce line losses and improve the system overall efficiency. In this way, the STATCOM can be used to increase the grid capacity. For example, more electric vehicle chargers, PV and Wind Energy Systems and other loads can be installed in emerging grids.

In many regions where low-voltage distribution lines are dominated by overhead lines, it is the most economical solution to install STATCOMs next to the actual lines or directly on the poles close to end users [4], FIGURE 1. Since pole mounted STATCOMs must be lifted and installed on the poles, it is highly desirable to minimize the volume and weight of the STATCOMs and other required installation equipment. If possible, to a level that can be handled by a single installer without the need for mounting and handling equipment. Among the benefits of the multi-level conversion, the reduction of the gravimetric and volumetric density and losses is particularly beneficial for the outdoor and pole mounted STATCOM application.

The STATCOMs are based on either current source inverter (CSI) or voltage source inverters (VSI). For the CSI STATCOMs energy is stored in a DC bus inductor, which is inherently more reliable than a DC bus capacitor in the VSI STATCOMs. However, the major drawbacks are lower

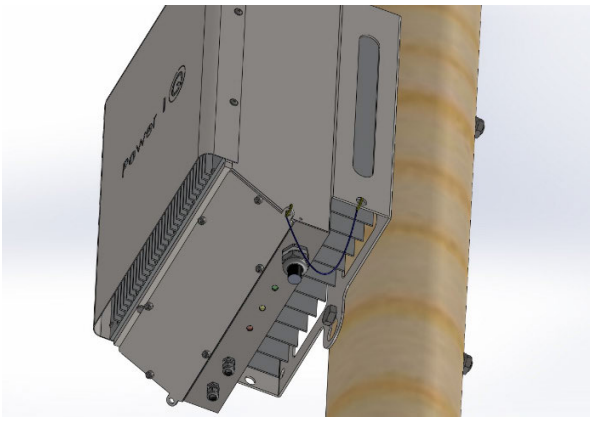

FIGURE 1. Pole mounted STATCOM mockup.

energy density of the DC BUS inductor versus capacitor, greater losses of the DC bus inductor energy storage versus the DC bus capacitor losses. Moreover, CSI STATCOMs topologies require the voltage bi-directional semiconductors which availability is limited at present time. At present, the most STATCOMs are voltage source inverters (VSI) based on either two or three level topologies, while the CSI STATCOMs are available at smaller extent [5]. For VSI STATCOM applications the most prevalent semiconductor technology is Si IGBT, but the most recently SiC MOSFETs are getting utilized due to their perceived benefits in terms of their switching speed and reduces losses.

In this paper a novel 5 Level E Type topology is proposed for the 3-phase 4-wire STATCOM application. The objective of this paper is to provide a detailed analysis and design guideline for the 3-phase 4-wire 5 Level E Type STATCOM.

The paper is organized as follows:

First, the advantages of the proposed solution for STATCOM applications are comprehensively reviewed. Then, the analysis of novel 5 Level E Type topology is carried out and a detailed design procedure is given. Finally, the experimental validation of the SiC three-phase/four-wire 5 Level E Type STATCOM inverter prototype is presented, followed by a discussion of the advantages of the proposed solution.

II. 5 LEVEL E TYPE 3-PHASE 4-WIRE STATCOM

A simplified block diagram of a 3-phase 4-wire STATCOM is depicted in FIGURE 2. The novel 5 Level E Type 3-phase 4-wire STATCOM consists of the common DC BUS, three 5 Level E Type phase legs and an output AC filter.

The AC filter is connected to a grid via interface transformer or line chokes at a point of common coupling (PCC).

The DC bus is made of four serially connected DC capacitors, C_1 to C_4 with interconnection points: upper mid-point (UPM), mid-point (MP) and lower mid-point (LMP), and DC bus terminals: DC+ and DC-.

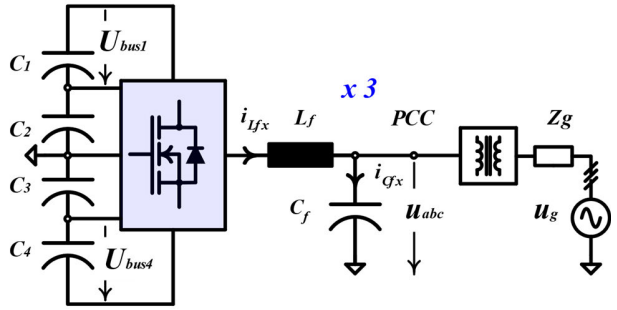

FIGURE 2. 3-phase 4-wire STATCOM: simplified schematic.

A. 5 LEVEL E TYPE 3-PHASE TOPOLOGY

A detailed schematic of the proposed 5 Level E Type topology is shown in FIGURE 3.

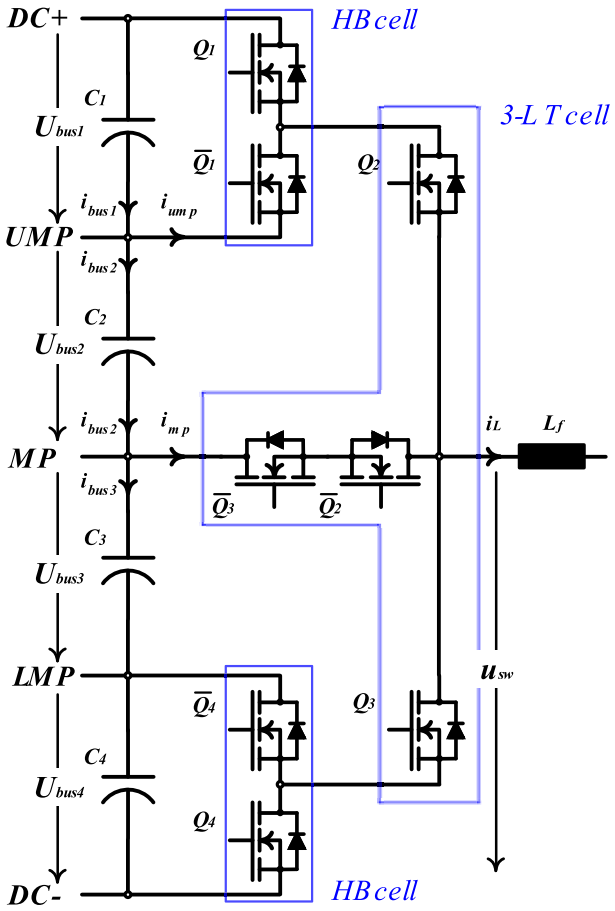

FIGURE 3. The 5 Level E-Type Phase leg.

The 5 Level E-Type phase leg consists of the inner 3-Level T-cell, Q_2, $\bar{Q}_2$, Q_3, $\bar{Q}_3$, the upper, Q_1; $\bar{Q}_1$, and the lower half bridge cells, Q_4; $\bar{Q}_4$, as depicted in FIGURE 3.

The 5 Level E-Type topology was introduced recently, and it was previously studied for the back-to-back AC drives, UPS and in general grid connected applications [6], [7], [8].

Thus, the topology will be briefly introduced in this paper and focus shall be given on application of this topology for a 3-phase 4 wire STATCOM.

1) MODULATION SCHEME

The modulation strategy of the 5 Level E-Type topology is based on the naturally sampled phase disposition pulse with modulation (PWM) method. The normalized sinusoidal reference, $m\,(t)$, as a modulation signal, crosses over the fixed frequency triangular carriers $c_1\,(t)$ to $c_4\,(t)$, FIGURE 4.

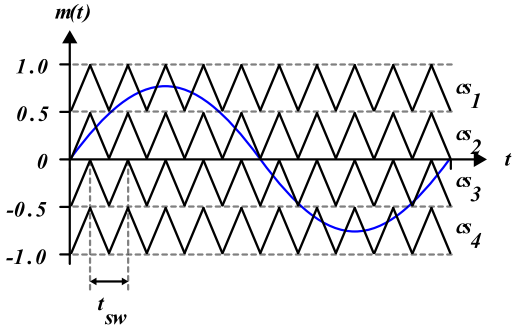

FIGURE 4. Naturally sampled PD sine-triangle modulation for the N5 Level E Type phase leg.

There are four ranges for the normalized modulation signal: $-1 < m\,(t) < -0.5$, $-0.5 < m\,(t) < 0$, $0 < m\,(t) < 0.5$ and $0.5 < m\,(t) < 1$. Depending on the range of the modulation signal, only one switching cell is being switched with the carrier frequency, while the others are in the recessive state.

When the normalized modulation signal is in the range of $-0.5 < m\,(t) < 0.5$, the 3 Level T-cell devices are switched while when $0.5 < m\,(t) < 1$, the upper half bridge cell devices are switched and when $-1 < m\,(t) < 0.5$, the lower half bridge cell devices are being switched respectively. Since the PWM modulation scheme is symmetric for $m\,(t) > 0$ and $m\,(t) < 0$ only the positive normalized modulation signal cases need to be examined.

The One Carrier Cycle switching for $m\,(t) > 0$ of the phase leg N5 Level E Type is shown in FIGURE 5. While, the corresponding gate signals, and corresponding current commutation loops in FIGURE 6 and devices switching states, TABLE 1.

The device currents thought devices for the 3 Level T-cell commutation loop and the upper half-bridge are given in FIGURE 7and FIGURE 8 respectively. While the device duty cycle functions for the upper devices, Q_1, $\bar{Q}_1$, Q_2; $\bar{Q}_2$, are summarized in TABLE 2.

It's important to notice that there are four complementary gates, which makes implementation of the 5 Level E Type PWM modulation feasible in a state-of-the-art DSC/MCU platforms. Furthermore, only one set of gates is switched at the time which allows from uniformly spreading switching losses. As far as voltage rating of the devices, the complementary pairs Q_1, $\bar{Q}_1$, Q_4; $\bar{Q}_4$ are rated to withstand $U_{bus}/4$, the devices Q_2, Q_3 to withstand $3U_{bus}/4$ and the devices $\bar{Q}_2$ $\bar{Q}_3$ to withstand $U_{bus}/2$ respectively. This makes the topology suitable for mixing devices of the different technologies and voltage ratings for the optimal performance.

Where $\theta_1 = arcsin\,(1/2m)$ and $\theta_2 = \pi - \theta_1$

TABLE 1. 5 Level E type inverter output voltages and switching states.

HB cell upper		3-L T cell				HB cell lower		Modulation index	Phase voltages	Switching states
Q_1	$\overline{Q}_1$	Q_2	$\overline{Q}_2$	Q_3	$\overline{Q}_3$	Q_4	$\overline{Q}_4$			
1	0	1	0	0	1	0	1	$0.5 < m(t) < 1$	$U_{dc}/2$	u_{sw1}
0	1	1	0	0	1	0	1	$0.5 < m(t) < 1$	$U_{dc}/4$	u_{sw2}
0	1	1	0	0	1	0	1	$0 < m(t) < 0.5$	$U_{dc}/4$	u_{sw3}
0	1	0	1	0	1	0	1	$0 < m(t) < 0.5$	0	u_{sw4}
0	1	0	1	0	1	0	1	$-0.5 < m(t) < 0$	0	u_{sw5}
0	1	0	1	1	0	0	1	$-0.5 < m(t) < 0$	$-U_{dc}/4$	u_{sw6}
0	1	0	1	1	0	0	1	$-1 < m(t) < -0.5$	$-U_{dc}/4$	u_{sw7}
0	1	0	1	1	0	1	0	$-1 < m(t) < -0.5$	$-U_{dc}/2$	u_{sw8}

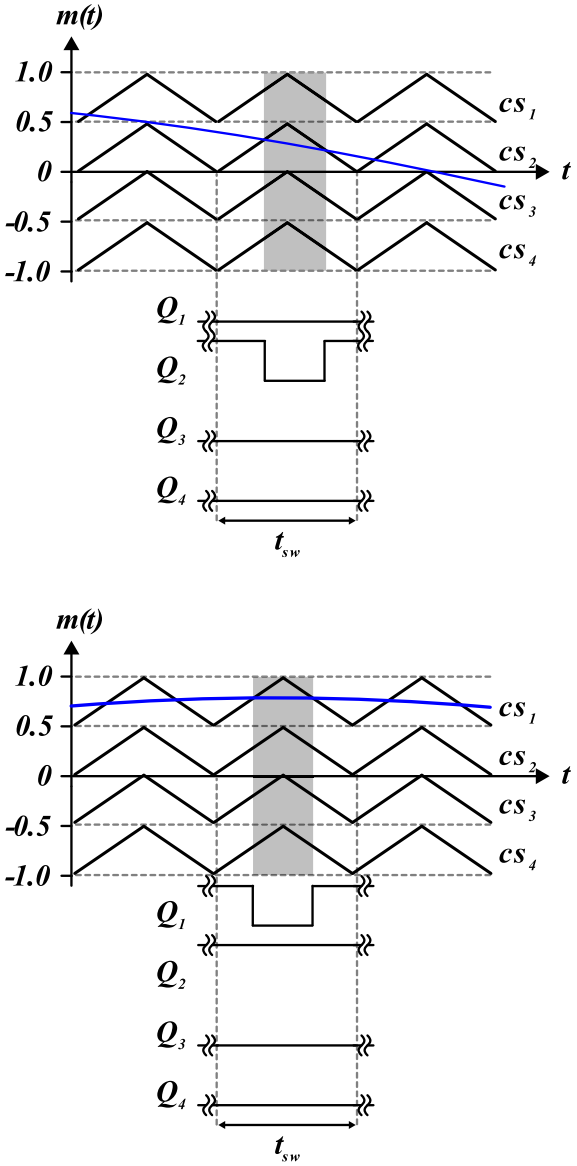

FIGURE 5. 5 Level E Type phase leg: Phase Disposition PWM One Carrier Cycle for $m(t) > 0$.

2) ANALYSIS OF THE 5 LEVEL E TYPE TOPOLOGY

Based on the duty cycle functions, given in TABLE 2, the values of a device instantaneous, average and rms currents

TABLE 2. Duty cycle functions of the 5 Level E type inverter (MOSFETs).

$$d_{Q_1}(t) = \begin{cases} 2msin(\omega t) - 1;\ \theta_1 \le \omega t \le \theta_2 \\ 0;\ 0 \le \omega t \le \theta_1\ \theta_2 \le \omega t \le 2\pi \end{cases}$$

$$d_{\overline{Q_1}}(t) = \begin{cases} 1 - 2msin(\omega t);\ 0 \le \omega t \le \theta_1\ \theta_2 \le \omega t \le \pi - \theta\ \pi - \theta \le \omega t \le \pi \\ 2(1 - msin(\omega t));\ \theta_1 \le \omega t \le \theta_2 \\ 0;\ \pi \le \omega t \le 2\pi \end{cases}$$

$$d_{Q_2}(t) = \begin{cases} 2msin(\omega t);\ 0 \le \omega t \le \theta_1\ \theta_2 \le \omega t \le \pi - \theta\ \pi - \theta \le \omega t \le \pi \\ 1;\ \theta_1 \le \omega t \le \theta_2 \\ 0;\ \pi \le \omega t \le 2\pi \end{cases}$$

$$d_{\overline{Q_2}}(t) = \begin{cases} 1 - 2msin(\omega t);\ 0 \le \omega t \le \theta_1\ \theta_2 \le \omega t \le \pi - \theta\ \pi - \theta \le \omega t \le \pi \\ 0;\ \theta_1 \le \omega t \le \theta_2\ (\pi + \theta_1) \le \omega t \le (\pi + \theta_2) \\ 2msin(\omega t) - 1;\ \pi \le \omega t \le (\pi + \theta_1)\ \&(\pi + \theta_2) \le \omega t \le 2\pi \end{cases}$$

Where $\theta_1 = arcsin(1/2m)$ and $\theta_2 = \pi - \theta_1$

can be written as follows: (1), (2) and (3) respectively

$$i_{Q_x}(t) = d_{Q_x}(t)\sqrt{2}I_{rms}sin(\omega t + \theta) \tag{1}$$

$$I_{Q_x(av)} = \frac{1}{2\pi}\int_0^{2\pi} i_{Q_x} d(\omega t) \tag{2}$$

$$I_{Q_x(rms)} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} {i_{Q_x}}^2 d(\omega t)} \tag{3}$$

where I_{rms} is the RMS value of the output current, θ phase angle between the output phase voltages and currents, $Q_x \in \{Q_1, \bar{Q}_1, Q_2, \bar{Q}_2, Q_3, \bar{Q}_3, Q_4, \bar{Q}_4\}$ and $d_{Q_x}(t) \in \left\{d_{Q_1}, d_{\bar{Q}_1}, d_{Q_2}, d_{\bar{Q}_2}, d_{Q_3}, d_{\bar{Q}_3}, d_{Q_4}, d_{\bar{Q}_4}\right\}$.

As a result, based on (2) and (3) the closed form expressions of the average and rms currents of the devices is given in (38)-(41) and (42)-(45).

It should be noted that for $PF \cong 0$, or for STATCOM application, the value of the average currents of UPM, MP, LMP are equal to zero. This means that the mid-points balancing for the STACOM application requires minor cumulative effort as far as DC current quantities, hence this makes the 5 Level E topology particularly suitable for the STATCOM application.

3) LOSSES ANALYSIS

Device losses can be specified as follows:

$$P_d = P_{cond} + P_{sw} \tag{4}$$

where P_{cond} represents conduction and P_{sw} switching losses. Furthermore, the conduction and switching losses per device

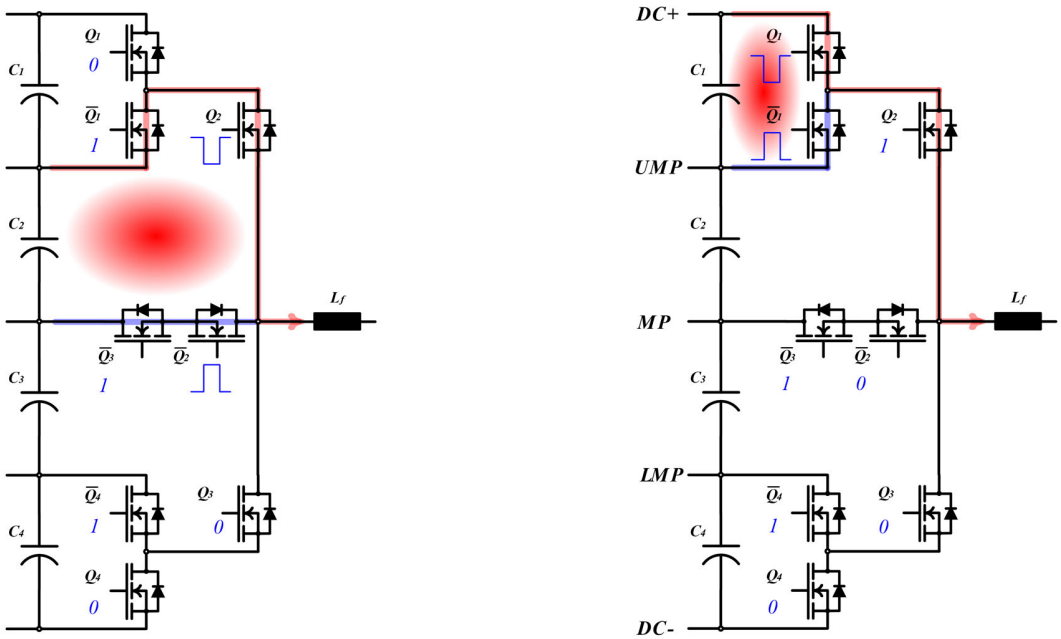

FIGURE 6. The 5 Level E-Type phase leg switching states and commutation loops for $m\,(t) > 0$ and $i_L > 0$:(a) 3-L T cell commutation loop and (b) half-bridge cell commutation loop.

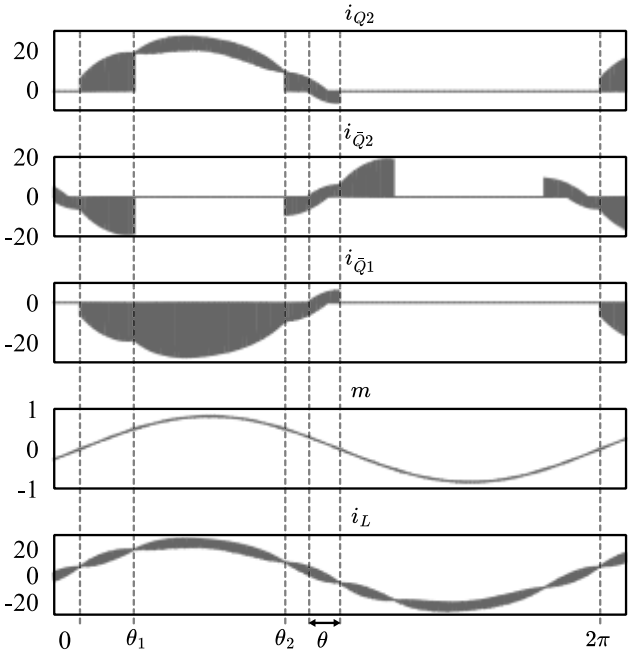

FIGURE 7. Device currents 3 Level T cell commutation loop for $\theta = 15°$.

can be further defined as shown in (5)-(7).

$$P_{cond}\,(Q_x) = I_{Q_x(av)}U_{ds0} + I^2_{Q_x(rms)}R_{ds,on} \tag{5}$$

$$P_{sw}\,(Q_x) = \frac{1}{2\pi}f_{sw}\left(E_{on} + E_{off}\right)\int_{\alpha_1}^{\alpha_2} sin\,(\omega t)\,d\,(\omega t) + \frac{1}{2}f_{sw}C_{oss}U^2_{Q_x} \tag{6}$$

$$P_{sw}\,(D_x) = \frac{1}{2\pi}f_{sw}E_{rec}\int_{\alpha_1}^{\alpha_2} sin\,(\omega t)\,d\,(\omega t) \tag{7}$$

where U_{ds0} represent device voltage knee, $R_{ds,on}$ on-resistance, E_{on}, E_{off}, and E_{rec} represent device turn on and turn off switching energy losses, $\frac{1}{2}f_{sw}C_{oss}U^2_{Q_x}$ dissipation of energy stored in the output capacitance of a device, C_{oss}, and diode recovery energy loss. Where U_{Q_x} is a hold up voltage of a device. These parameters depend on a junction temperature, external gate resistors as well as actual commutation loops layout.

B. AC FILTER ANALYSIS

The instantaneous AC inductor current is defined as in (8), where $I_{rms}$is the RMS value of the output current, φ phase angle between the output phase voltages and inductor currents and Δi_L is high-frequency current ripple.

$$i_{L_f}(t) = \sqrt{2}I_{rms}sin\,(\omega t + \varphi) + \Delta i_{L_f}(t) \tag{8}$$

The inductor maximum peak to peak current ripple is given with the following generalized closed form expression [9].

$$\Delta i_{L_f} = \frac{U_{bus}}{4\,(N-1)\,f_{sw}L_f} \tag{9}$$

where U_{bus} is the DC BUS voltage, L_f is the filter inductance, f_{sw} is the switching frequency and $N = 2, 3, 5, \ldots$ number of the levels. Therefore, for a 5 Level topology, AC filter inductance L_f can be expressed with (10)

$$L_f = \frac{U_{bus}}{16 f_{sw}\Delta i_{L_f}} \tag{10}$$

Furthermore, the inductor RMS current ripple can be expressed as (11)

$$\Delta I_{L_{f(rms)}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\int_t^{t+T_{sw}} \left(\Delta i_{L_f}(\tau)\right)^2 d(\tau)\, d(\omega t)} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(\frac{\Delta i_{L_f}}{2\sqrt{3}}\right)^2 d(\omega t)} \cong 0.9\frac{\Delta i_{L_f}}{2\sqrt{3}} \quad (11)$$

The AC filter capacitor RMS current is composed from the fundamental frequency and the equivalent switching frequency current ripple [7], hence total RMS AC filter capacitor current $I_{C_{f(rms)}}$ can be expressed with (12)

$$I_{C_{f(rms)}} = \sqrt{\left(U_{ln} C_f \omega\right)^2 + \left(0.9\frac{\Delta i_{L_f}}{2\sqrt{3}}\right)^2} \quad (12)$$

While the total RMS AC inductor current with (13)

$$I_{L_{f(rms)}} = \sqrt{\left(U_{ln(rms\omega)} C_f\right)^2 + \left(0.9\frac{\Delta i_{L_f}}{2\sqrt{3}}\right)^2 + I_{rms}^2} \quad (13)$$

At last, the AC filter inductance L_f inductance can be computed from (10).

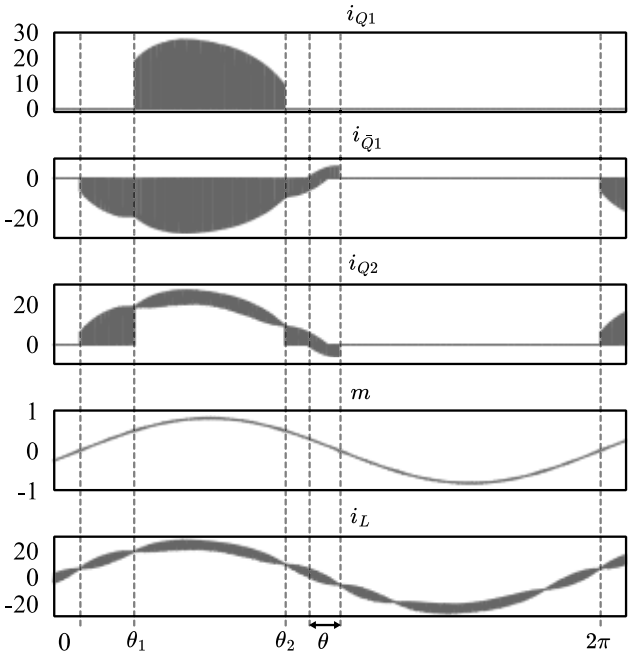

FIGURE 8. Device currents upper Half-Bridge cell commutation loop $\theta = 15°$.

The AC filter inductor losses P_{L_f} consist of the core and the winding losses and can be estimated with

$$P_{L_f} = m_C k_p B_{max}^{\alpha} f_{sw}^{\beta} + R_{L_f,DC} I_{rms}^2 + \sum_{n=1}^{\infty} + R_{L_f,AC}(n) I_{L_f}^2(n) \quad (14)$$

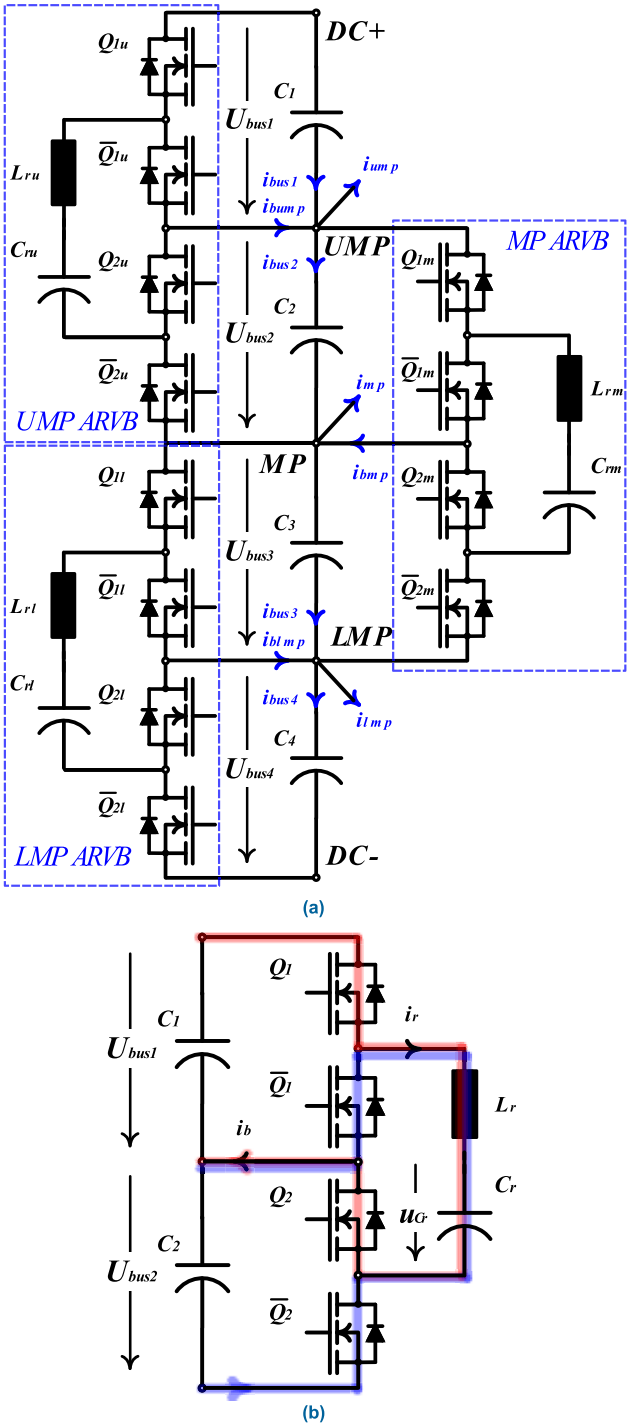

FIGURE 9. Active Resonant Voltage Balancers: (a) UPM, MP and LMP ARVBs, (b) An ARVB: Resonant current for $Q_1 = 1, \bar{Q}_1 = 0$ (red) and for $Q_1 = 0, \bar{Q}_1 = 1$ (blue).

where m_C is core mass, k_p, α and β are the magnetic core coefficients specific for each magnetic material, while $R_{L_f,DC}$ represent the AC inductor winding DC resistance, while $R_{L_f,AC}(n)$ AC resistance at given frequency, I_{rms} the RMS value of the inductor current at the fundamental frequency and $I_{L_f}(n)$ the RMS value of the n^{th} harmonic of the switching frequency inductor current.

C. THE DC BUS MID POINTS VOLTAGE BALANCING

One of the major challenges of the multi-level topologies is balancing of the DC BUS partial voltages.

Unlike 3 Level NPC, 3 Level T Type or 5 Level-ANPC topologies, where the DC BUS mid-point can be balanced either by injecting a DC offset into the modulation index [10], the 5 Level E Type topology requires an active balancing. This is since the upper (UMP) and the lower mid-point (LMP) average current flowing into or from those nodes is non-zero. This is noticeable by observing $i_{\bar{Q}_1}$ waveform, FIGURE 7 and FIGURE 8. Therefore, with the active balancing the value of the DC bus capacitor average current is nulled. The partial DC BUS voltages can be balanced with an Active Resonant Voltage Balancer (ARVB) [11], [12], [13], [14] and FIGURE 9 (a), applied to each mid-point.

Hence, three ARVBs are utilized, UMP ARVB, MP ARVB and LMP ARVB.

An ARVB, FIGURE 9 (b), is controlled by a complementary pair of gate signals, Q_1 and $\bar{Q}_1$ operated with almost 50% duty cycle at a resonant tank L_rC_r resonant frequency $f_r = 1/2\pi\sqrt{L_rCr}$, with a dead band DT, where a balancing current, i_b flows into a mid-point and evens out the partial DC BUS voltages.

In case of a STATCOM application of the 5 Level E Type topology, there is rather very small transfer of the active power only to sustain desired operational DC BUS voltage. Hence, the balancing current demand is reduced, and the balancers can be optimized. Especially, given the fact that the average currents flowing into mid points are zero, as mentioned previously.

1) ANALYSIS OF ARVBS FOR 3-PHASE 5 LEVEL E TYPE INVERTER

Detailed analysis of the ARVB is presented in [11], [12], [13], and [14]. In this paper focus shall be on the analysis of ARVBs for balancing mid-points of the 3-phase 5 Level E Type inverter. The UMP ARVB and the MP ARVB shall be examined as the LMP ARVB is symmetrical and equivalent in operation to the UPM ARVB.

As denoted in FIGURE 3, the instantaneous current following into the upper mid-point i_{ump} and the mid-point i_{mp} can be expressed with (15) and (16), while the average value of the partial DC bus currents as (17). Furthermore, since $i_{ump}(t)$ and $i_{mp}(t)$ are periodic functions with fundamental grid frequency period, by applying frequency decomposition those equations can be expanded into a Fourie series (18) and (19).

$$i_{ump}(t) = \sum_{x=a}^{c} i_{\bar{Q}_{1x}}(t) = i_{b_{ump}}(t) + i_{bus1}(t) - i_{bus2}(t) - i_{q1m}(t) \tag{15}$$

$$i_{mp}(t) = \sum_{x=a}^{c} i_{\bar{Q}_{2x}}(t) = i_{b_{mp}}(t) + i_{bus2}(t) - i_{bus3}(t) - i_{q1l}(t) + i_{\bar{q}2u}(t) \tag{16}$$

$$I_{bus1(av)} \cong I_{bus2(av)} \cong I_{bus3(av)} \cong I_{bus4(av)} \cong 0 \tag{17}$$

$$i_{ump}(t) = \sum_{n=1}^{\infty} \sqrt{2} I_{ump}(n) sin\left(n\omega t + \varphi_{ump}(n)\right) \tag{18}$$

$$i_{mp}(t) = \sum_{n=1}^{\infty} \sqrt{2} I_{mp}(n) sin\left(n\omega t + \varphi_{mp}(n)\right) \tag{19}$$

Consequently, the average mid-point and balancing current can be expressed with (20) and (21).

Applying Parseval's theorem, [15], $I_{ump(rms)}$ and $I_{mp(rms)}$ mid-point RMS currents can be computed from (23) and (22), where $\sqrt{2}I_{(u)mp}(n)$ and $\varphi_{(u)mp}(n)$ represent magnitude and phase angle of the n^{th} harmonic.

It should be noted that in a case of the symmetrical and balanced three-phase output currents, such as for the STATCOM application, only the zero sequence harmonics (3^{rd}, 6^{th}, 9^{th},...) contribute to the mid-point currents, while the positive and negative sequences harmonics sums are equal to zero. Hence, (22), (23) can be rewritten as (24), (25).

$$I_{ump(av)} = \sum_{x=a}^{c} I_{\bar{Q}_{1x}(av)} = 3I_{\bar{Q}_1(av)} \cong I_{b_{ump}(av)} \tag{20}$$

$$I_{mp(av)} = \sum_{x=a}^{c} I_{\bar{Q}_{2x}(av)} = 3I_{\bar{Q}_2(av)} \cong I_{b_{mp}(av)} \tag{21}$$

$$I_{ump(rms)} = \sqrt{\left(\sum_{n=1}^{\infty} I^2_{ump(rms)}(n)\right)} = \sqrt{\sum_{n=1}^{\infty}\left(\sum_{x=a}^{c} I_{\bar{Q}_{1x}(rms)}(n)\right)^2} \cong I_{b_{ump}(rms)} \tag{22}$$

$$I_{mp(rms)} = \sqrt{\left(\sum_{n=1}^{\infty} I^2_{mp(rms)}(n)\right)} = \sqrt{\sum_{n=1}^{\infty}\left(\sum_{x=a}^{c} I_{\bar{Q}_{2x}(rms)}(n)\right)^2} \cong I_{b_{mp}(rms)} \tag{23}$$

$$I_{ump(rms)} = \sqrt{\sum_{n=1}^{\infty}\left(\sum_{x=a}^{c} I_{\bar{Q}_{1x}(rms)}(3n)\right)^2} \cong I_{b_{ump}(rms)} \tag{24}$$

$$I_{mp(rms)} = \sqrt{\sum_{n=1}^{\infty}\left(\sum_{x=a}^{c} I_{\bar{Q}_{2x}(rms)}(3n)\right)^2} \cong I_{b_{mp}(rms)} \tag{25}$$

where $I_{\bar{Q}_1(rms)}$ and $I_{\bar{Q}_2(rms)}$ are given in (43) and (45)

As described in [11] the total RMS and peak resonant current of the ARVB can be computed from (26).

$$I_{r_{(u)mp}(rms)} \cong I_{b_{(u)mp}(av)} \frac{\pi}{2\sqrt{2}}$$
$$I_{r_{(u)mp}(pk)} \cong I_{b_{(u)mp}(av)} \frac{\pi}{2}. \tag{26}$$

2) ARVBS LOSS MODEL

At last, for MOSFTETs the ARVBs device losses can be estimated as per (27), (28) and (29).

$$P_{cond_{(u)mp}} = \frac{1}{2} R_{ds,on} I^2_{r_{(u)mp}(rms)} \tag{27}$$

$$P_{sw} = \frac{1}{2} U^2_{bus(x)} C_{oss} f_r \tag{28}$$

$$P_{d(arvb)} = 12P_{sw} + 8P_{cond_{ump}} + 4P_{cond_{mp}} \tag{29}$$

where $U_{bus(x)}$ is the device hold up voltage, $R_{ds,on}$ and C_{oss} are MOSFET on-resistance and output capacitance respectively, while f_r resonant frequency defined as $f_r = {}^1\!/_{2\pi\sqrt{L_r C_r}}$

D. DC BUS ANALYSIS

For the STATCOM application DC BUS analysis the operating modulation depth M is close to unity. Also, based on the assumption that the ARVBs compensate mid-point average currents (17) FIGURE 1, the instantaneous DC bus current is given with (30). Consequently, the average DC bus current is given with (31), over the fundamental period, and the total RMS bus current stress with (32). In case of the symmetrical and balanced three-phase output currents (33) is applicable., such as the STATCOM application only zero sequency harmonics contribute to the total RMS DC bus current.

$$i_{bus}(t) = \sum_{x=a}^{c} i_{Q_{1x}}(t) \tag{30}$$

$$I_{bus(av)} = \sum_{x=a}^{c} I_{Q_{1x}(av)} = 3I_{Q_1(av)} \tag{31}$$

$$\begin{aligned} I_{bus(rms)} &= \sqrt{\left(\sum_{n=1}^{\infty} I^2_{bus(rms)}(n)\right)} \\ &= \sqrt{\sum_{n=1}^{\infty}\left(\sum_{x=a}^{c} I_{Q_{1x}(rms)}(n)\right)^2} \\ &= \sqrt{\sum_{n=1}^{\infty}\left(\sum_{x=a}^{c} I_{Q_{1x}(rms)}(3n)\right)^2} \end{aligned} \tag{32}$$

$$I_{bus(rms)} = \sqrt{3} I_{Q_{1x}(rms)} \tag{33}$$

where $I_{Q_{1x}(av)}$ is the value of the average Q_{1x} current, and $I_{Q_{1x}(rms)}(n)$ is the RMS value of the n^{th} harmonic, and $I_{Q_{1x}}$ is the RMS value of Q_{1x} current and $x \in \{a, b, c\}$

The DC bus capacitors instantaneous voltage is given by (34), while the ripple with (35),

$$u_{bus(x)}(t) = \frac{U_{bus}}{4} + \frac{1}{\omega C_{bus}} \sum_{n=1}^{\infty} \frac{I_{bus}(n)}{n} sin(n\omega t + \varphi_n) \tag{34}$$

$$\Delta u_{bus(x)}(t) = \frac{1}{\omega C_{bus}} \sum_{n=1}^{\infty} \frac{I_{bus}(n)}{n} sin(n\omega t + \varphi_n) \tag{35}$$

while the average DC bus capacitors losses can be computed from (36).

$$P_{bus} = \sum_{n=1}^{\infty} R_{est0}(n) I^2_{bus(rms)}(n) \tag{36}$$

The $R_{esr0}(n)$ is capacitors equivalent series resistance and it is a frequency dependable resistance.

E. STATCOM CONTROL

The simplified block diagram of the 5 Level-E Type 3-phase 4-wire STATCOM Control is shown in FIGURE 10.

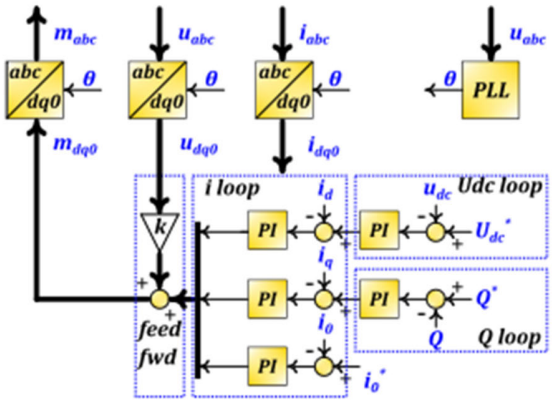

FIGURE 10. 5 Level-E Type 3-phase 4-wire STATCOM Control structure.

The controller [16] is based on the synchronous rotating reference frame ($dq0$) where the SOGI PLL [17] provides grid phase angle θ, and the AC voltage magnitudes vector, U_{dq0}. The reference frame is positioned so that the d-axis is aligned with the active power and the q-axis with the reactive power.

The STATCOM inverter operates as a controlled current source since it is synchronized with the grid. Hence, the inner current loops in $dq0$ frame are provided with scalar values of the active i_d, reactive i_q and zero i_0 sequence currents. The active current reference i_{d*} is fed by the DC bus voltage loop, while the reactive current reference i_{q*}, by the average reactive power loop. Set points for desired DC BUS voltage and average reactive power are U_{dc*} and Q_* respectively. The outputs of current loops are vector summed and vector added to the AC voltage feed-forward term. Furthermore, the sum is decomposed from $dq0$ frame to abc to get modulation index vector m_{abc}. The modulation index vector is fed as the modulation signals, m_a, m_b and m_c to the naturally sampled PD PWM modulator.

III. STATCOM DESIGN

The design parameters for the 3-phase 4-wire 5 Level E Type STATCOM inverter are given in TABLE 3.

The design parameters Δi_L, Q_{C_f} are typical design parameter values for the STATCOM application, while dU/dt was chosen to limit stress on the AC filter inductor isolation, to manage EMI and reduce stress on the AC filter output capacitor.

TABLE 3. STATCOM design parameters.

Symbol	Definition	Values
S	Nominal power	12 kVA
I	Nominal current	17A
U_{bus}	DC BUS voltage	800V
Δi_L	Inductor Current Ripple	15%
Q_{C_f}	Capacitor Reactive Power	1%
f_{sw}	Switching frequency	20kHz
B_{max}	Max allowable Flux density	0.75 of B_{sat}
J	AC current density	<4A/mm^2
du/dt	Rate of change of voltage	<50kV/µs
T_{hs}	Average Heatsink Temperature	90°C
T_{amb}	Max Ambient Temperature	50°C

A. STATCOM SEMICONDUCTOR DEVICES

Based on previous discussion outlined in the ANALYSIS OF THE 5 LEVEL E TYPE TOPOLOGY and devices stress equations (38) to (43), the following SiC MOSFETs have been selected, Table 4. and the actual 5 Level E Type power leg has been designed accordingly, FIGURE 11.

TABLE 4. STATCOM semiconductor devices.

Ref Designator	Mnf Part Number	Type/Value
Q_1, $\overline{Q}_1$, Q_4, $\overline{Q}_4$	IPF190S40N1	400V SiC
$\overline{Q}_2$, $\overline{Q}_3$	IMBG65R022M1	650V SiC
Q_2, Q_3	IMBG120R030M1	1200V SiC

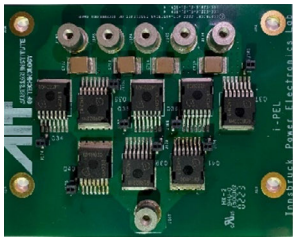

FIGURE 11. Actual 5 Level-E Type phase leg.

B. HEATSINK

To estimate a volume and size of the heatsink, for given design parameters as per TABLE 3, the semiconductor losses according to (5) to (7) are estimated first.

Based on the estimated semiconductor losses, for given ambient and average heatsink temperature as per TABLE 3, the heatsink thermal resistance, R_{th} is calculated as per (37).

$$R_{th} \cong \frac{T_{hs} - T_{amb}}{P_d} \tag{37}$$

Assuming uniform spread of heat, for the calculated thermal resistance an appropriate heatsink is selected, TABLE 5.

C. AC FILTER

According to (10) as well as design parameters, U_{dc}, Δi_L, f_{sw} as per TABLE 3, the values of the AC filter inductance and capacitance can be calculated. Furthermore, to choose the value of the AC filter capacitance C_f, two criteria are to be met: the AC filter corner frequency is to be chosen at least 1/2 of the switching frequency and specified AC capacitor reactive power, Q_{C_f}, TABLE 3. Metglas AMCC Series Cut Cores [18] was chosen for the design of the AC filter inductor. This core material exhibits high saturation AC flux density and moderate losses for desired switching frequency f_{sw}. Taking into consideration design parameters max AC flux density B_{max} and AC current density J and previously calculated L_f and by applying the Kg method [19] for magnetic design calculations, the AC filter inductor is designed. The AC inductors 3D model illustration is shown in FIGURE 12 while analytically derived values accordingly in TABLE 6.

TABLE 5. Heatsink design: analytically derived values and heatsink selection.

Symbol	Definition	Values
P_d	Semiconductor Losses @PF=1	43 W
R_{th}	Heatsink Thermal Resistance	1.16 K/W
Symbol	Mnf Part Number	Type/Value
	SK 555 100 AL	0.6 K/W

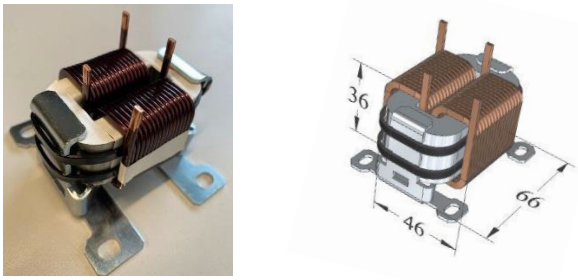

FIGURE 12. AC filter inductor: Actual (left) and 3D model illustration (right).

TABLE 6. AC Filter design: analytically derived values.

Symbol	Definition	Values
Δi_{Lpk-pk}	Inductor Current Ripple	7.21 A
L_f	AC Filter Inductance	340µH
V_e	Effective Volume	0.11 cm^3
W_e	Effective Weight	388 g
C_f	AC Filter Capacitance	2.2 µF
P_{L_f}	Total AC Filter Inductors losses (*14*)[1]	18.38W

[1] $R_{L_f,AC}(n)$ inductor AC resistance losses due to proximity effect were not considered, due to moderate switching frequency.

D. DC BUS

Based on the DC bus current stress and voltage ripple outlined in the DC BUS analysis, the following DC capacitors are

selected, TABLE 7. Each partial DC bus contains 2 capacitors in parallel, hence 8 capacitors per phase.

The DC Bus losses are being evaluated from and the selected capacitor data sheet ESR data, R_{esr0} (n) and (36), while the useful life with the web tool [20].

TABLE 7. DC bus losses and capacitors selection.

Symbol	Definition	Type/Value
P_{bus}	Total DC bus capacitors power losses (36) @PF=0 and T_{dc} = 60 ℃	1.31W
Symbol	Mnf Part Number	Type/Value
C_{busx}	B43630E2277M000	6x270µF/250V

IV. ARVBS DESIGN

A. ARVBS SEMICONDUCTOR DEVICES

As depicted in FIGURE 9 (a), ARVBs are balancing partial bus voltages with the value of the average voltage $\frac{U_{dc}}{4}$, (34), furthermore considering (20) to (26) selected semiconductors are listed in TABLE 8.

B. ARVBS HEATSINK

Taking into consideration ARVBs power loss (27) to (29) and selected ARVB semiconductors required heatsink thermal resistance was calculated and the heatsink selected, TABLE 8.

C. ARVB RESONANT TANK

In the end, taking into consideration (26) the resonant inductor has been selected and the value of the resonant tank capacitance calculated from $f_r = {}^1\!/_{2\pi\sqrt{L_r C_r}}$ and the bank of ceramic capacitors have been selected accordingly TABLE 8.

TABLE 8. ARVBS Design: analytically derived values.

Symbol	Definition	Type/Value
$I_{r_{ump(rms)}}$	Upper/Lower mid-point ARVB resonant RMS current @PF=0	3.47A
$I_{r_{mp(rms)}}$	Mid-point ARVB resonant RMS current @PF=0	10.76A
$P_{d(arvb)}$	Total ARVBs devices power dissipation @PF=0	11.03W
R_{th}	Heatsink Thermal Resistance	3.63 K/W
Symbol	Mnf Part Number	Type/Value
$Q_1, \overline{Q}_1$	IPP410N30NAKSA1	44A/300V
L_r	SRP1770TA-1R5M	1.5µH/47A
C_r	C5750X7T2W105M250KA	24x1µF
	SK 489 75 SA	3.5 K/W

V. STATCOM PROTOTYPE

As per above outlined design parameters, TABLE 3, and design procedure, the 5 Level E Type 3-phase 4-wire STATCOM inverter prototype has been developed and the major parts of the prototype are indicated in FIGURE 14 accordingly.

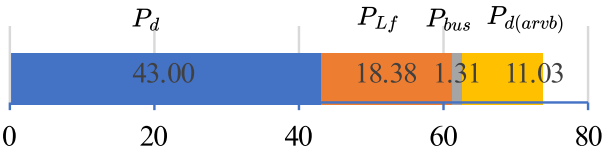

FIGURE 13. 5 Level E Type 3-phase 4-wire STACOM losses estimate.

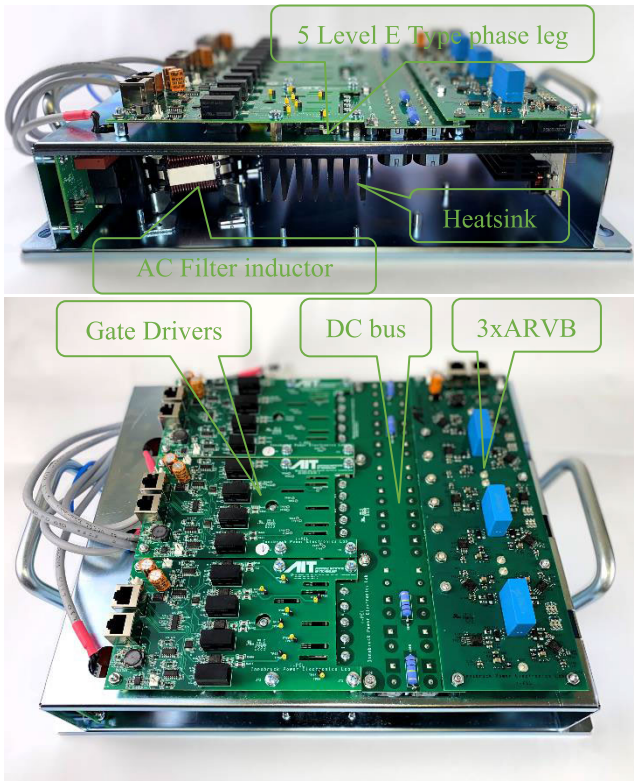

FIGURE 14. 5 Level E Type 3-phase 4-wire STACOM Inverter prototype.

The breakdown of the STATCOM inverter losses estimation is shown in FIGURE 13, where P_d represents semiconductor losses TABLE 5, P_{L_f} total AC filter inductor losses TABLE 6, P_{bus} total DC bus capacitor losses TABLE 7 and $P_{d(arvb)}$ total ARVBs devices losses.

The losses estimation does not include SiC MOSFET dead-band conduction losses, AC inductor proximity losses, AC filter capacitor losses, pre-charge relay losses, auxiliary power supply losses such as the gate drivers and the control system power losses.

The total size and volume or volumetric and gravimetric density are given in TABLE 9.

VI. EXPERIMENTAL RESULTS

The 5 Level E Type 3-phase 4-wire STACOM experimental setup is shown In FIGURE 15. Where the Regatron ACS grid simulator is used as the grid source, while the experimental data is taken with the DeweSoft acquisition system [21].

TABLE 9. 5 Level E type 3-Phase 4-Wire STATCOM mechanical properties.

Symbol	Definition	Values
	Dimensions	30x28x6.65cm
V_e	Effective Total Volume	5.58 dm^3
W_e	Effective Total Weight	4.63 kg
δ_{V_e}	Effective Volumetric density	2.15 kVA/dm^3
δ_{W_e}	Effective Gravimetric density	2.59 kVA/kg

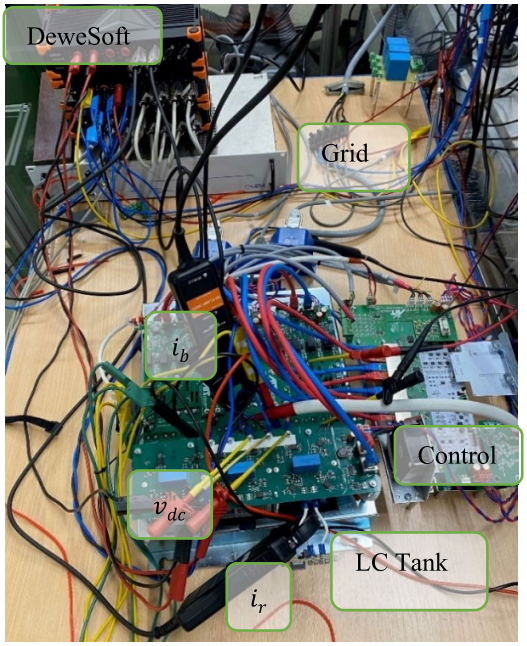

FIGURE 15. 5 Level E Type 3-phase 4-wire STACOM experimental setup.

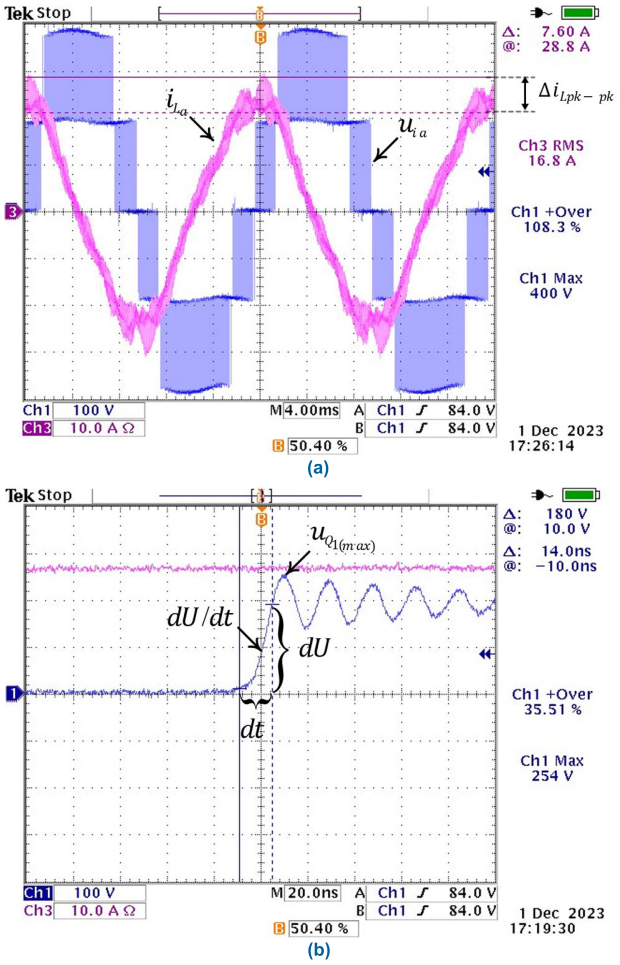

FIGURE 16. 5 Level E Type STATCOM switching waveforms: (a) Ch1 u_{ia} inverter input voltage phase A, Ch3 i_{L_a} input current phase A (b) Ch1 device voltage Q_1 turn off at the peak current i_{L_a}.

The control system is based on the TI MCU TMS320F283 79D. The 3-phase 5 Level E Type STATCOM inverter driven with 16 PWM signals. The signals Q_{1x}, Q_{2x}, Q_{3x} and Q_{4x} per phase are generated at the control board while their complementary pairs $\bar{Q}_{1x}$, $\bar{Q}_{2x}$, $\bar{Q}_{3x}$ and $\bar{Q}_{4x}$ as well as the respective dead-time is generated on the gate driver boards.

Additional 2 PWMs signals are used to drive the ARVBs. The ARVBs are operated with the fixed 50% duty cycle at the resonant frequency. The resonant frequency is determined by a resonance of the LC tank. In this case the resonant and switching frequency are 28kHz. The ARVBs dead time is set to DT $= 0.8\mu$s.

The experimental data are presented hereafter.

The FIGURE 16 shows the 5 Level phase A inverter voltage and the AC inductor current. In The FIGURE 16 (a) inverter voltage distinct 5 voltage levels can be observed, as well as the AC inductor peak-to-peak ripple current Δi_{Lpk-pk}, which corresponds to the analytically derived value in TABLE 6. The phase displacement of the AC inductor current i_{L_a} by $\pi/2$ toward the inverter input voltage u_{i_a} is noticeable too.

The FIGURE 16 (b) shows the device Q_1 voltage turn off at the peak current. As shows that the commutation overshoot is approx 65V while the max voltage $u_{Q_{1(max)}}$ is 254V. This is well within the Safe Operating Area of the selected 400V SiC MOSFET Table 4.

The STATCOM inverter operation steady state input voltage and AC input current waveforms at the nominal reactive power are shown in FIGURE 17 (a) and (b).

The FIGURE 18 depicts the apparent conversion efficiency and active power for the whole reactive power range.

The TABLE 10 presents the DC and AC quantities at the nominal reactive power.

The experimentally obtained active power P includes the total STATCOM inverter losses, and a tiny fraction of the active power required to maintain the DC bus voltage at the desired level. TABLE 10.

The FIGURE 19 (a) shows partial DC bus voltages which are well balanced and exhibit the 3rd harmonic voltage ripple, while the FIGURE 19 (b) upper ARVB resonant current $i_{r_{ump}}$ and the FIGURE 19 (c) upper ARVB balancing current $i_{b_{ump}}$.

As shown in FIGURE 19 (c) and TABLE 11, the RMS value of the respective balancing current is somewhat

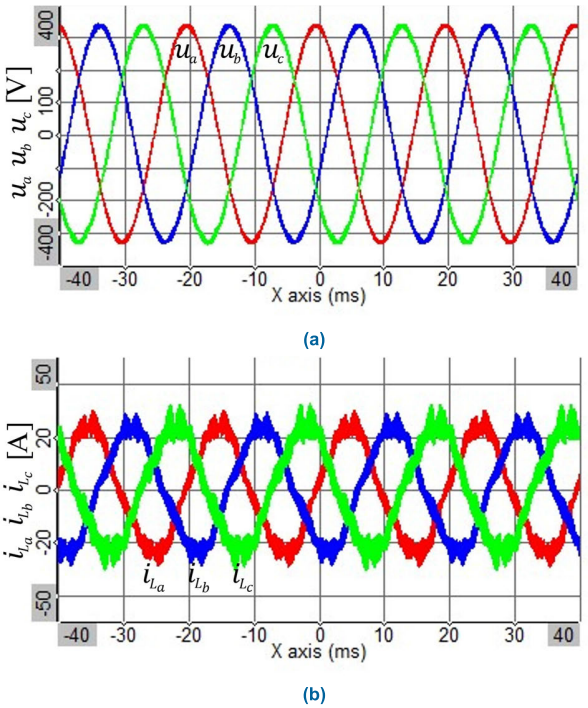

FIGURE 17. 5 Level E Type STATCOM steady state waveforms: (a)u_a, u_b, u_c input voltages, (b) i_{L_a}, i_{L_b}, i_{L_c} input AC inductor currents (b).

TABLE 10. 5 Level E type STATCOM experimental data: DC and AC quantities at the nominal reactive power.

Symbol	Quantity	Value
U_{bus}	DC BUS Voltage	765.17V
$U_{a(rms)}$	AC Voltage phase A	232.4 V
$U_{b(rms)}$	AC Voltage phase B	232.4 V
$U_{c(rms)}$	AC Voltage phase C	232.4 V
$I_{a(rms)}$	AC Current phase A	17.13 A
$I_{b(rms)}$	AC Current phase B	16.81 A
$I_{c(rms)}$	AC Current phase C	17.13 Arms
P	Active Power	150 W
Q	Reactive Power	11796 VAr
PF	Power Factor	-0.0143
Δi_L	Inductor Current Ripple	3.80 A
dU/dt	Rate of voltage change	≅11.2kV/μs

contradictory to the discussion on the balancing current requirements at PF = 0 outlined in Section II-C. This is because the ARVBs with this type of control are non-selective in terms of the voltage ripple compensation. In fact, the ARVBs compensate the 3rd harmonic voltage ripple, FIGURE 19 (a), resulting from the 3-phase operation. As the consequence, the resulting RMS value of the balancing current is increased. If the capacitance of the DC bus had been increased, the 3rd harmonic voltage ripple would have been reduced and the resulting value of the balancing currents would have been lower.

VII. DISCUSSION

The proposed solution exhibits remarkably high apparent conversion efficiency or exceptionally low losses. Thus, the required cooling effort is minimal. This is evident when

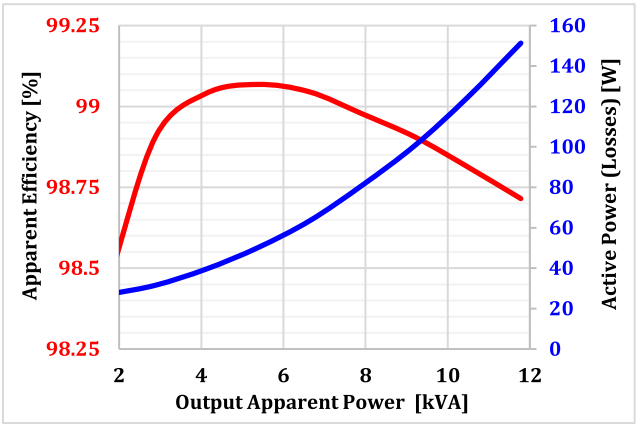

FIGURE 18. STATCOM Apparent efficiency & active power (losses).

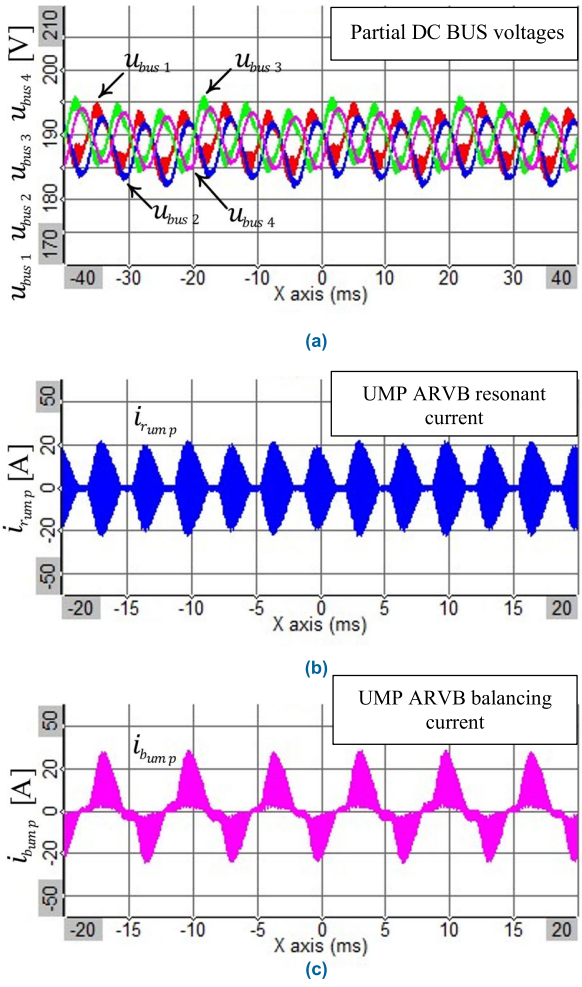

FIGURE 19. 5 Level E Type STATCOM steady state waveforms:(a) u_{bus1}, u_{bus2}, u_{bus3}, u_{bus4} partial DC BUS voltages, (b) $i_{r_{ump}}$ upper ARVB resonant current, (c) $i_{b_{ump}}$ upper ARVB balancing current.

considering the analytical losses estimation, FIGURE 13, and the experimental losses, TABLE 10 and FIGURE 18. If the STATCOM is mounted upright, no additional forced air cooling is required, hence passive cooling can be obtained. The passive cooling is the primary market requirement for the pole-mounted STATCOM application.

$$\bar{I}_{Q_1(av)} = \frac{\hat{I}}{2\pi}\left[-cos\left(\theta+\theta_1\right)+cos\left(\theta+\theta_2\right)+\left(\theta_2-\theta_1\right)mcos\left(\theta\right)+msin\left(\theta_1-\theta_2\right)cos\left(\theta+\theta_1+\theta_2\right)\right] \tag{38}$$

$$\begin{aligned}\bar{I}_{\overline{Q}_1(av)} = \frac{\hat{I}}{2\pi}&\left[cos(\theta)+\theta_1(-m)cos(\theta)+cos(\theta_1+\theta)(msin(\theta_1)-1)+2(cos(\theta_1+\theta)-cos(\theta_2+\theta))\right.\\&\left.-1/2m(sin(2\theta_1+\theta)-sin(2\theta_2+\theta)-2\theta_1cos(\theta)+\theta_2mcos(\theta)+cos(\theta_2+\theta)(1-msin(\theta_2))+(1-\pi m)cos(\theta)\right]\end{aligned} \tag{39}$$

$$\bar{I}_{Q_2(av)} = \frac{\hat{I}}{2\pi}\left[m\left(\theta_1\cos\left(\theta\right)-\sin\left(\theta_1\right)\cos\left(\theta+\theta_1\right)\right)+m\left(\left(\pi-\theta_2\right)\cos\left(\theta\right)+\sin\left(\theta_2\right)\cos\left(\theta+\theta_2\right)\right)+2m\left(cos\left(\theta_2\right)+1\right)\right] \tag{40}$$

$$\bar{I}_{\overline{Q}_2(av)} = 0 \tag{41}$$

$$\begin{aligned}I_{Q_1(rms)} = \frac{\hat{I}}{\sqrt{2\pi}}&\left[\frac{1}{24}\left(6\sin\left(2\left(\theta_1+\theta\right)\right)-6\sin\left(2\left(\theta_2+\theta\right)\right)-3m^2\left(-4\sin\left(2\left(\theta_1+\theta\right)\right)+\sin\left(2\left(2\theta_1+\theta\right)\right)+4\theta_1\cos\left(2\theta\right)\right)\right.\\&+3m^2\left(-4\sin\left(2\left(\theta_2+\theta\right)\right)+\sin\left(2\left(2\theta_2+\theta\right)\right)+4\theta_2\cos\left(2\theta\right)\right)-12\theta_1\left(2m^2+1\right)+12\theta_2\left(2m^2+1\right)\\&+8m\left(\cos\left(3\theta_1+2\theta\right)-3\cos\left(\theta_1+2\theta\right)\right)-8m\left(\cos\left(3\theta_2+2\theta\right)-3\cos\left(\theta_2+2\theta\right)\right)-24m\cos\left(\theta_2\right)\\&\left.\times\ \left(m\sin\left(\theta_2\right)-2\right)+24m\cos\left(\theta_1\right)\left(m\sin\left(\theta_1\right)-2\right)\right]^{(1/2)}\end{aligned} \tag{42}$$

$$\begin{aligned}I_{\overline{Q}_1(rms)} = \frac{\hat{I}}{\sqrt{2\pi}}&\left[\frac{1}{24}\left(-6\sin\left(2\left(\theta_1+\theta\right)\right)+6\sin\left(2\theta\right)+12\theta_1\left(2m^2+1\right)\right.\right.\\&+m\left(3m\left(-4\sin\left(2\left(\theta_1+\theta\right)\right)+\sin\left(2\left(2\theta_1+\theta\right)\right)+4\theta_1\cos\left(2\theta\right)\right)-8\left(\cos\left(3\theta_1+2\theta\right)-3\cos\left(\theta_1+2\theta\right)\right)\right)\\&-24m\cos\left(\theta_1\right)\left(m\sin\left(\theta_1\right)-2\right)+m\left(9m\sin\left(2\theta\right)-16\cos\left(2\theta\right)\right)-48m\Big)+\frac{1}{24}\left(6\sin\left(2\left(\theta_2+\theta\right)\right)-6\sin\left(2\theta\right)\right.\\&+12m^2\sin\left(2\left(\theta_2+\theta\right)\right)-3m^2\sin\left(2\left(2\theta_2+\theta\right)\right)-12\theta_2\left(m^2\cos\left(2\theta\right)+2m^2+1\right)+12m^2\sin\left(2\theta_2\right)\\&-9m^2\sin\left(2\theta\right)+24\pi m^2-24m\cos\left(\theta_2+2\theta\right)+8m\cos\left(3\theta_2+2\theta\right)-48m\cos\left(\theta_2\right)+4\left(3\pi m-4\right)m\cos\left(2\theta\right)\\&-48m+12\pi\Big)+\sin\left(2\left(\theta_1+\theta\right)\right)-\sin\left(2\left(\theta_2+\theta\right)\right)+\frac{1}{2}m^2\sin\left(2\left(\theta_1+\theta\right)\right)-\frac{1}{8}m^2\sin\left(2\left(2\theta_1+\theta\right)\right)\\&-\frac{1}{2}m^2\sin\left(2\left(\theta_2+\theta\right)\right)+\frac{1}{8}m^2\sin\left(2\left(2\theta_2+\theta\right)\right)\\&-\frac{1}{2}\theta_1\left(m^2\cos\left(2\theta\right)+2m^2+4\right)+\theta_2\left(\frac{1}{2}m^2\cos\left(2\theta\right)+m^2+2\right)-\frac{1}{2}m^2\sin\left(2\theta_2\right)\\&+m^2\sin\left(\theta_1\right)\cos\left(\theta_1\right)-2m\cos\left(\theta_1+2\theta\right)+\frac{2}{3}m\cos\left(3\theta_1+2\theta\right)\\&\left.+2m\cos\left(\theta_2+2\theta\right)-\frac{2}{3}m\cos\left(3\theta_2+2\theta\right)-4m\cos\left(\theta_1\right)+4m\cos\left(\theta_2\right)\right]^{(1/2)}\end{aligned} \tag{43}$$

$$\begin{aligned}I_{Q_2(rms)} = \frac{\hat{I}}{\sqrt{2\pi}}&\left[\frac{1}{4}m^2\left(2\theta_1\left(\cos\left(2\theta\right)+2\right)+\sin\left(\theta_1\right)\left(-3\cos\left(\theta_1+2\theta\right)+\cos\left(3\theta_1+2\theta\right)-4\cos\left(\theta_1\right)\right)\right)\right.\\&+\frac{1}{8}m^2\left(4\sin\left(2\left(\theta_2+\theta\right)\right)-\sin\left(2\left(2\theta_2+\theta\right)\right)-4\theta_2\left(\cos\left(2\theta\right)+2\right)+4\sin\left(2\theta_2\right)-3\sin\left(2\theta\right)+4\pi\cos\left(2\theta\right)+8\pi\right)\\&\left.+\frac{1}{4}\left(\sin\left(2\left(\theta_1+\theta\right)\right)-\sin\left(2\left(\theta_2+\theta\right)\right)-2\theta_1+2\theta_2\right)\right]^{(1/2)}\end{aligned} \tag{44}$$

$$\begin{aligned}I_{\overline{Q}_2(rms)} = \frac{\hat{I}}{\sqrt{\pi}}&\left[\frac{1}{24}\left(-6\sin\left(2\left(\theta_1+\theta\right)\right)+6\sin\left(2\theta\right)+12\theta_1\left(2m^2+1\right)+m\left(3m\left(-4\sin\left(2\left(\theta_1+\theta\right)\right)+\sin\left(2\left(2\theta_1+\theta\right)\right)\right)\right.\right.\\&+4\theta_1\cos\left(2\theta\right)\Big)-8\left(\cos\left(3\theta_1+2\theta\right)-3\cos\left(\theta_1+2\theta\right)\right)\Big)-24m\cos\left(\theta_1\right)\left(m\sin\left(\theta_1\right)-2\right)\\&+m\left(9m\sin\left(2\theta\right)-16\cos\left(2\theta\right)\right)-48m\Big)\\&+\frac{1}{24}\left(6\sin\left(2\left(\theta_2+\theta\right)\right)-6\sin\left(2\theta\right)+12m^2\sin\left(2\left(\theta_2+\theta\right)\right)-3m^2\sin\left(2\left(2\theta_2+\theta\right)\right)\right.\\&-12\theta_2\left(m^2\cos\left(2\theta\right)+2m^2+1\right)+12m^2\sin\left(2\theta_2\right)-9m^2\sin\left(2\theta\right)+24\pi m^2-24m\cos\left(\theta_2+2\theta\right)\\&\left.+8m\cos\left(3\theta_2+2\theta\right)-48m\cos\left(\theta_2\right)+4\left(3\pi m-4\right)m\cos\left(2\theta\right)-48m+12\pi\right)]^{(1/2)}\end{aligned} \tag{45}$$

TABLE 11. 5 Level E type STATCOM experimental data: DC bus and ARVB quantities.

Symbol	Quantity	Value
U_{bus1}, U_{bus2}, U_{bus3}, U_{bus4}	Partial DC BUS voltages	189.26 V, 187.70 V, 189.78 V, 189.29 V
$\Delta U_{bus1pk-pk}$, $\Delta U_{bus2pk-pk}$, $\Delta U_{bus3pk-pk}$, $\Delta U_{bus4pk-pk}$	Peak to peak partial DC BUS voltages	12.05 V, 10.97 V, 12.15V, 10.05 V
$I_{r(rms)}$	Upper ARVB resonant current	8.45 A
$I_{b(rms)}$	Upper ARVB balancing current	9.94 A

Regarding the gravimetric and volumetric density TABLE 9, the presented experimental prototype proves to be at par with the similar state-of-art academic research prototype [22], which is presented as new benchmark for ultra-high efficient and power dense converter. But when comparing to the state-of-the art industrial STATCOM [23], it shows significant improvements in terms of the efficiency, weight, and volume. The comparison of the proposed solution versus the benchmark academic research prototype and the industrial STATCOM is summarized in TABLE 12.

TABLE 12. STATCOM solutions comparison: volume, weight, efficiency.

Symbol	Definition	5 Level E Type STATCOM	7 Level HANPC [22]	Pole mounted STATCOM [23]
	Dimensions	30x28x6.65cm	25.6x26.9x53cm	80x45x27.5 cm
δ_{V_e}	Effective Volumetric density	2.15 kVA/dm^3	3.4 kW/dm^3	0.1 kVA/dm^3
δ_{W_e}	Effective Gravimetric density	2.59 kVA/kg	3.2 kW/kg	0.25 kVA/kg
	Peak electrical efficiency	99.1%	99.4 %	98.5%

It should be noted that the slightly better efficiency and power density of the 7 Level HANPC prototype [22] is to be expected given the number of voltage levels, 7 versus 5 voltage levels.

The total weight includes enclosure, mechanical support, control system and auxiliary power supply, i.e., FIGURE 15, it must not exceed the maximum allowable manual lifting weight, i.e., 23kg according to OSHA U.S. Furthermore, no special lifting or handling tools would be required to mount the 5 Level E Type STATCOM.

Although the complexity of the control system of the 5 Level E Type 3-phase 4-wire STATCOM has increased, the control and PWM modulator have been implemented on the standard cost-effective MCU platform. Thus, this challenge is managed without the need to use more complex and expensive control hardware such as FPGA-based.

VIII. CONCLUSION

This paper presents the analysis and design of the SiC three-phase/four-wire 5 Level E Type STATCOM. Accordingly, the experimental 5 Level E Type STATCOM prototype was constructed, and experimental validation was carried out. The experimental results validate the design and clearly demonstrates the benefits of multi-level conversion in terms of reduction of conversation losses, cooling effort, size, volume, weight, and finally a manageable increase in control complexity.

One of the key challenges remains the mid-point voltage balancing. Further research on this topic may bring more optimized partial bus voltage balancing solution, which could be based on an advanced control strategy of the ARVBs or having ARVBs to balance only the DC content of the mid-point currents.

APPENDIX

In this appendix, the closed form expressions for the values of the devices average and RMS currents are derived from (2) and (3) taking into consideration TABLE 2 and given in (38) to (41), as shown at the bottom of the previous page, for the average values and (42) to (45), as shown at the bottom of the previous page, for the RMS values.

where $\theta_1 = arcsin\,(1/2m)$ and $\theta_2 = \pi - \theta_1$

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